Product Bulletin

April 2023 **#PB230301 Rev 1.1**

Diamond Support for ECP5 Low Skew Clock Nets

Product Affected: Diamond SW release 3.12 SP1 and earlier releases that support the ECP5, ECP5U, ECP5UM and ECP5UM5G families are covered by this Product Bulletin.

Customers Affected: Only designs that have Clock Enable or Reset signals that wake up from configuration in logic state high and are implemented on the Low Skew Clock Network (PCLK tree).

Background: The Lattice Semiconductor FPGA devices in the ECP5, ECP5U, ECP5UM and ECP5UM5G families contain Low Skew Clock nets. The low skew clock nets have a Dynamic Clock Control circuit that ensures that if a clock is multiplexed onto the low skew clock net, its operation will be free from glitches. The Diamond software may route high fanout nets, such as clock enables and resets, onto unused low skew clock nets.

Observation: Lattice found that the Diamond Software may generate ECP5 designs that are 100% logically correct but do not work properly in silicon. This may occur if Clock Enable or Reset signals that wake up from configuration in logic state high are implemented on the Low Skew Clock Network.

Detailed Workaround Description: There are three separate methods that can be used to avoid this issue.

1. Ensure that all high fanout clock enables and reset signals wake up from configuration in logic state low.
2. Use the PROHIBIT PRIMARY NET setting on any high fanout signals that initialize high, to prevent these signals from being routed on the low skew nets.
3. Apply Diamond patch number 131107. The patch inserts additional logic to resolve the issue.

Diamond Patch Details: The patch inserts circuitry to every CE/LSR net that is assigned to a low skew clock net. This circuitry pulls the CE/LSR signal low during wake up from configuration.
The point of insertion is shown in figure 1.

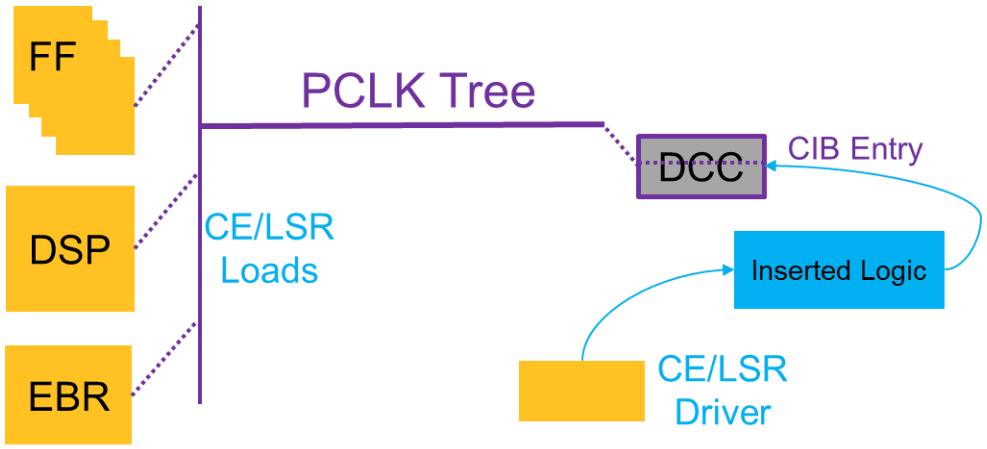

Figure 1: Insertion of logic from patch

The logic that the patch inserts consist of an AND gate, two registers and a ring oscillator, as shown in figure 2.

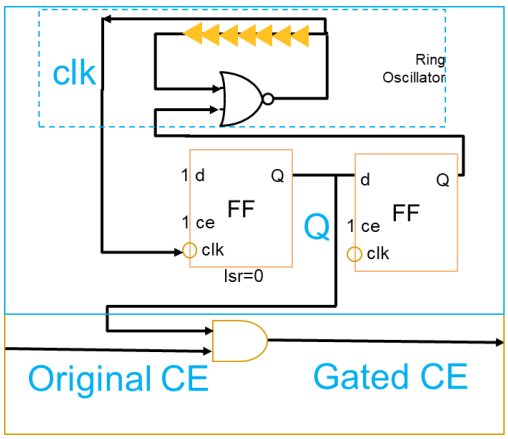

Figure 2: Logic Circuit details.

The circuitry uses the hardware global GSR to force the Clock Enable to a logic ‘0.’ It then automatically releases the clock enable during wake up and automatically shuts off the ring oscillator. The circuit operation is shown in figure 3.

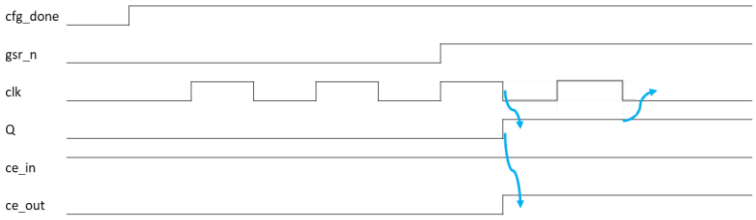

Figure 3: Waveform of Logic Circuit Operation

The use of the patch will impact the Diamond timing report. The Diamond trace report will report a logic loop. This is due to the insertion of the ring oscillator logic.
The Trace report shall also detail an additional clock domain based upon the ring oscillator generated clock. This will result in reduced constraint coverage below 100%.
The area consumed by the inserted logic will be 4 SLICEs + 1 SLICE per Clock Enable/Reset. There will be minimal impact on DC power and zero impact on AC power.

Revision History:

Date	Version	Description of Revisions
March 17, 2023	1.0	Initial Document Release
April 23, 2023	1.1	Added patch version