MachXO5T-NX-Development Board

Evaluation Board User Guide

FPGA-EB-02052-1.0

April 2023

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CMOS	Complementary Metal-Oxide Semiconductor
DNI	Do Not Install
FTDI	Future Technology Devices International
FPC	Flexible Printed Circuit
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
LDO	Low Dropout
LVDS	Low Voltage Differential Signaling
PCIe	Peripheral Component Interconnect Express
SLVS	Scalable Low Voltage Signaling
SPI	Serial Peripheral Interface
TPI	Twisted Pair Interface

1. Introduction

The Lattice Semiconductor MahXO5T™-NX Development Board allows you to investigate and experiment with the features of the LFMXO5-100T device. The features of the MachXO5T-NX Development Board can assist you with the rapid prototyping and testing of your specific designs.

The MachXO5T-NX Development Board is part of the MachXO5T-NX Development Kit, which includes the following:

- MachXO5T-NX Development Board pre-loaded with the demo design
- 12 V AC/DC Power adapter
- Mini USB cable
- Quick Start Guide

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the onboard headers, diodes and switches, and a complete set of schematics.

1.1. MachXO5T-NX Development Board

Along with the LFMXO5-100T device, the MachXO5T-NX Development Board also includes features to expand the LFMXO5-100T usability with Arduino, Raspberry, PCIe, RJ45, Versa, and Aardvark headers.

Figure 1.1 shows the top view of the MachXO5T-NX Development Board.

Figure 1.2 shows the bottom view of this board.

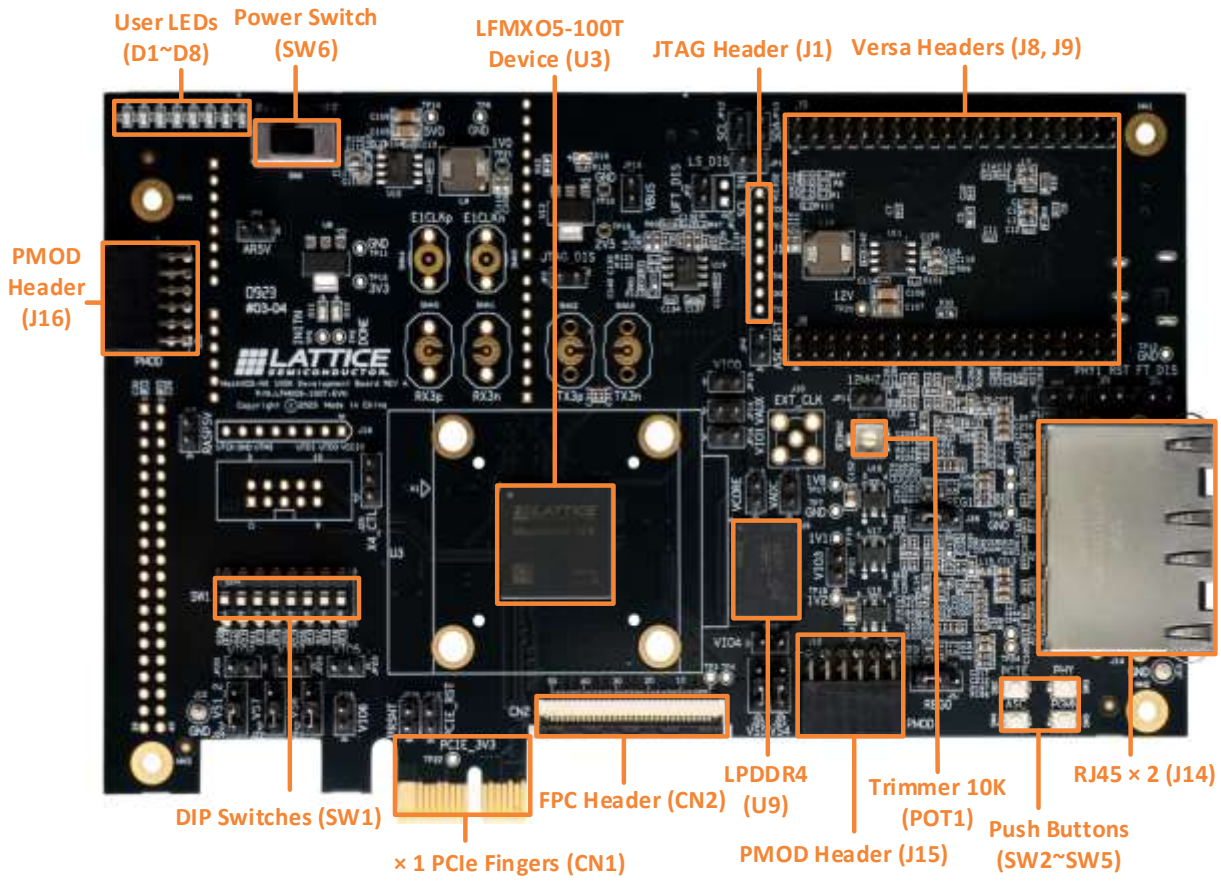

Figure 1.1. Top View of MachXO5T-NX Development Board

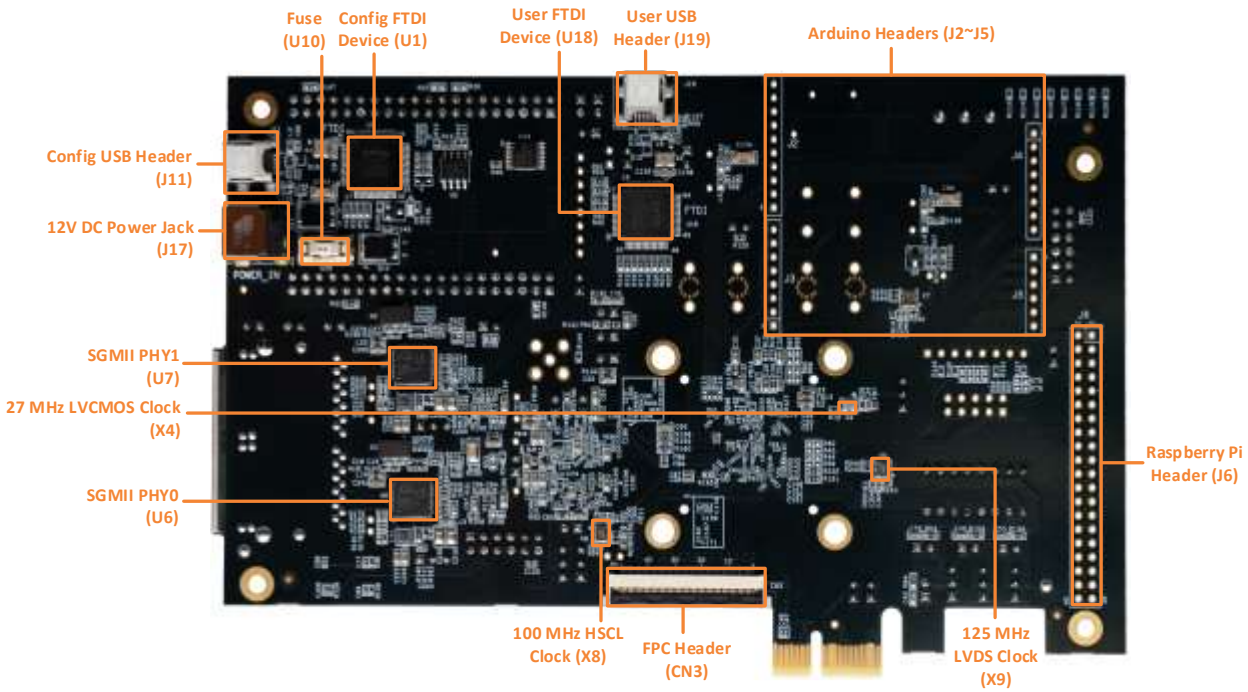

Figure 1.2. Bottom View of MachXO5T-NX Development Board

1.2. Features

- On board LFMXO5-100T Device
- Two Gbe PHY RJ45 connectors, with SGMII PHY support
- LPDDR4 up to 1066 Mbps, ×16 bits
- PCIe Gen2 x1 Edge Connector
- Optional SMA to support ×1 PCIe
- Versa Headers bridge with Lattice ASC Demo Board to support L-ASC10
- General Purpose Input/Output (GPIO) interface with PMOD, Arduino and Raspberry Pi boards
- USB-B connection for device programming with JTAG and Inter-Integrated Circuit (I^2C) utility
- Additional USB-B connection for user with Soft JTAG and UART utility
- Eight-position DIP Switches, four push buttons, and eight red LEDs for demo purposes
- ADC interface with 10K POT
- Two 50-pin FPC headers
- Multiple reference clock sources
- Optional Aardvark header
- Support FPGA Power Evaluation
- Lattice Radiant® programming support

Note: DNI stands for *Do Not Install* parts and DI stands for *Do Install* parts for assembly.

Caution: The MachXO5T-NX Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

1.3. LFMXO5-100T Device

The MachXO5T-NX Development Board features the LFMXO5-100T device in a 400-ball caBGA package. This device offers a variety of features and programmability that enhances Secure Control PLD functionality with Multiple Boot capabilities. Its cryptographic engine supports user-mode security features. Along with the cryptographic engine, numerous system functions are included such as four PLLs and 3,744 kbits of embedded RAM plus hardened implementations of I^2C and SPI, MachXO5T-NX FPGAs feature one hard PCIe link layer IP block which supports PCIe Gen1, Gen2 with one or two ×1 configuration, with flexible, high performance I/O support numerous single-ended and differential standards including LPDDR4 controller and SLVS. For more information on the capabilities of LFMXO5-100T device, see MachXO5-NX Family Data Sheet (FPGA-DS-02102).

2. Applying Power to the Board

The MachXO5T-NX Development Board comes ready to power up with onboard DC/DC switching regulators and Low Dropout (LDO) generators powered by an external 12 V DC power source. The external power supply can be connected with the DC power input jack J17 or the PCIe edge connector CN1, which is fused with a surface mounted fuse U10. The 5A fuse prevents the crashed current from flowing into the internal circuits and cause serious damage, as shown in Figure 2.1.

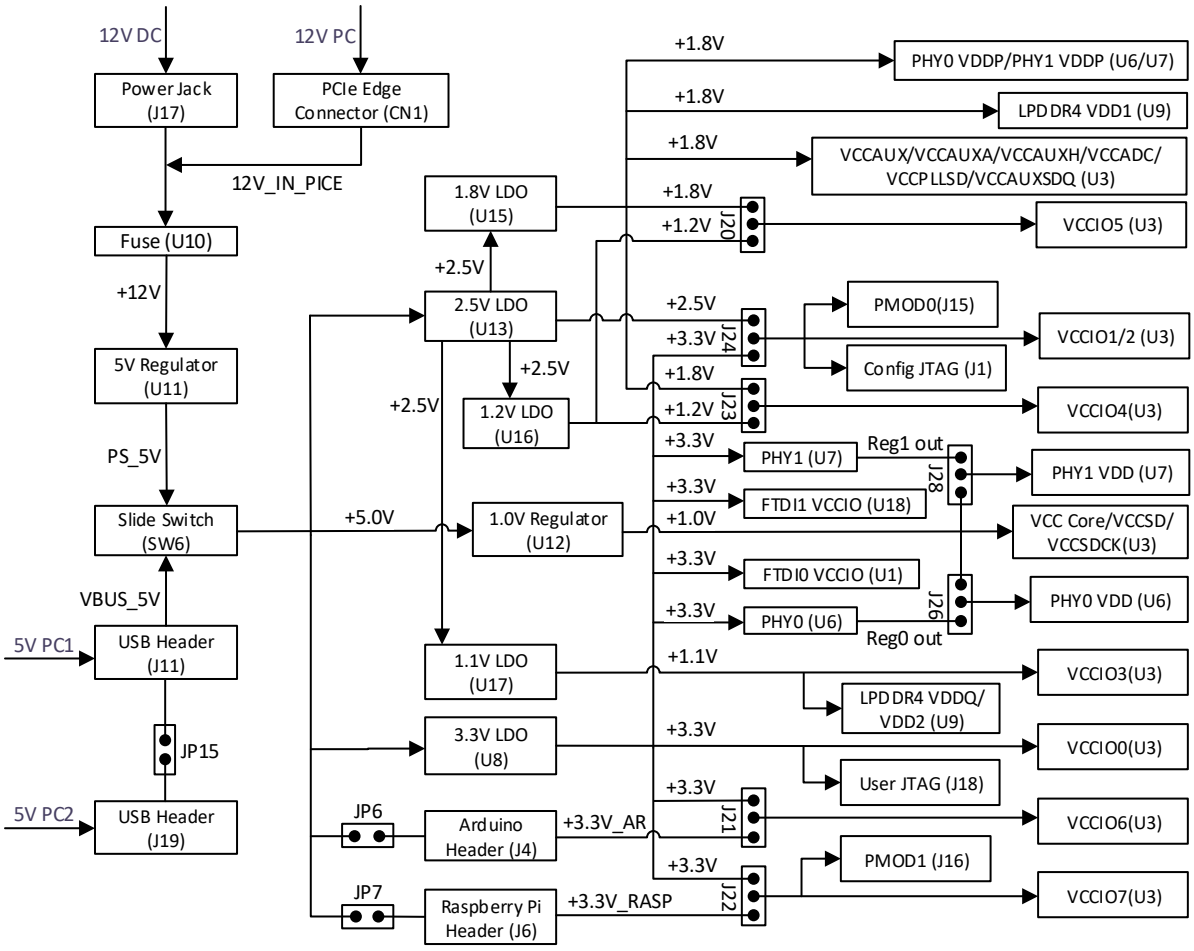

Figure 2.1. Board Power Supply

The onboard 5 V power regulator U11 provides 90% power convert efficiency from 12 V DC when output current between 50 mA and 3 A. It is distributed to 3.3 V, 2.5 V LDOs and 1.0 V regulator through one side of slide switch SW6 to support onboard devices. Through another side of SW6, this board can take the 5 V DC power from USB header J11 as well to supply those LDOs. For some low power applications, JP15 can be used to double the power supplier capability, if J19 is also plugged into the same PC that is connected to J11. You need to ensure 5 V DC power consume less than maximum capability from each USB port of PC when taking power from J11 and J19.

For the board extension, 5 V DC power can also supply Raspberry Pi and Arduino boards through the jumpers and onboard headers, to consolidate AC/DC adapters for stack boards system. Conversely, 5 V DC power for MachXO5T-NX Development Board can be supplied either from mated Raspberry Pi or Arduino Boards, if they are powered up by external AC/DC adapters already. You need to ensure 5 V power from a single source when adding JP6 or JP7 jumpers. However, maintain 5 V DC supplier is the basic requirement to power on the board, by checking the power good blue LED D18.

The onboard 1.1 V, 1.2 V, and 1.8 V LDOs take the power from 2.5 V LDO output.

Table 2.1 summarizes onboard major power rails and their test points.

Table 2.1. Onboard Major Power Rails

Power Net Name	Primary Source	Test Point
+12V	DC Power Jack (J17) or PCIE Edge Connecter (CN1)	TP20
PS_5V	DC/DC Regulator (U11)	—
VBUS_5V	Mini-USB Headers (J11 or J19)	JP15
+5.0V	Selected by Slide switch (SW6)	TP14
+3.3V	LDO (U8)	TP15
+2.5V	LDO (U13)	TP16
+1.8V	LDO (U15)	TP17
+1.2V	LDO (U16)	TP18
+1.1V	LDO (U17)	TP19
+1.0V	DC/DC Regulator (U12)	TP21
+3.3V_RASP	Raspberry Pi Header (J6)	—
+3.3V_AR	Arduino Header (J4)	—

As shown in Figure 2.1, this board provides multiple power options for I/O bank voltage flexibility. Table 2.2 summarizes the V_{CCIO} support matrix on this board. For an example, V_{CCIO1} and V_{CCIO2} share the same three positions jumper J24 and short its Pin 1 and Pin 2 can bring the 3.3 V LDO output to both I/O bank 1 and bank 2. For power consumption evaluation, this board facilitate some two-position jumpers with 1 Ω sense resistors to measure the voltage drop on each power rail, then the supply current can be calculated.

Table 2.2. LFMXO5-100T IO Bank Power Rails Stuff

LFMXO5-100T Power (U3)	Jumpers	3.3 V	2.5 V	1.8 V	1.2 V	1.1 V	Ext 3.3 V	Power Test Point	Sense Resistor of 1 Ω
V_{CCIO0}	—	Fixed	—	—	—	—	—	JP19	R132
V_{CCIO1}	J24	Pin 1-2	Pin 2-3	—	—	—	—	JP16	R133
V_{CCIO2}	J24	Pin 1-2	Pin 2-3	—	—	—	—	JP20	R134
V_{CCIO3}	—	—	—	—	—	Fixed	—	JP21	R61
V_{CCIO4}	J23	—	—	Pin 1-2	Pin 2-3	—	—	JP22	R62
V_{CCIO5}	J20	—	—	Pin 1-2	Pin 2-3	—	—	JP23	R63
V_{CCIO6}	J21	Pin 1-2	—	—	—	—	Pin 2-3	JP24	R64
V_{CCIO7}	J22	Pin 1-2	—	—	—	—	Pin 2-3	JP25	R153

Other than power rail for each I/O Bank, this board also provides some test points to evaluate the major power consumptions for LFMXO5-100T device as listed in Table 2.3.

Table 2.3. LFMXO5-100T Major Power Rails Stuff

LFMXO5-100T Power (U3)	Power Test Point	Voltage Drop Resistor	Resistance
V_{CC_CORE}	JP18	R112	0.01 Ω
V_{CC_AUX}/V_{CC_AUXH}/V_{CCAUXA}	JP14	R131	1 Ω
V_{CC_ADC}	JP17	R137	1 Ω

3. Hard JTAG/I²C Programming

The hardened JTAG/I²C programming architecture of the MachXO5T-NX Development Board is shown in Figure 3.1. The board has a built-in download controller for programming the LFMXO5-100T device. It uses an FT2232H Future Technology Devices International (FTDI) part U1 to convert USB to JTAG from port A, or convert USB to I²C from port B. Using Detect Cable function with Radiant programming software installed, you can detect dual ports after power up the board and connect the mini USB to USB-A cable from J11 to your PC, ensuring FTDI reset control jumper JP9 is not populated as default. The software select option FTUSB-0 is dedicate for hard JTAG and FTUSB-1 is dedicated for hard I²C which is mapping with port A and port B from hardware perspective, as shown in Figure 3.2.

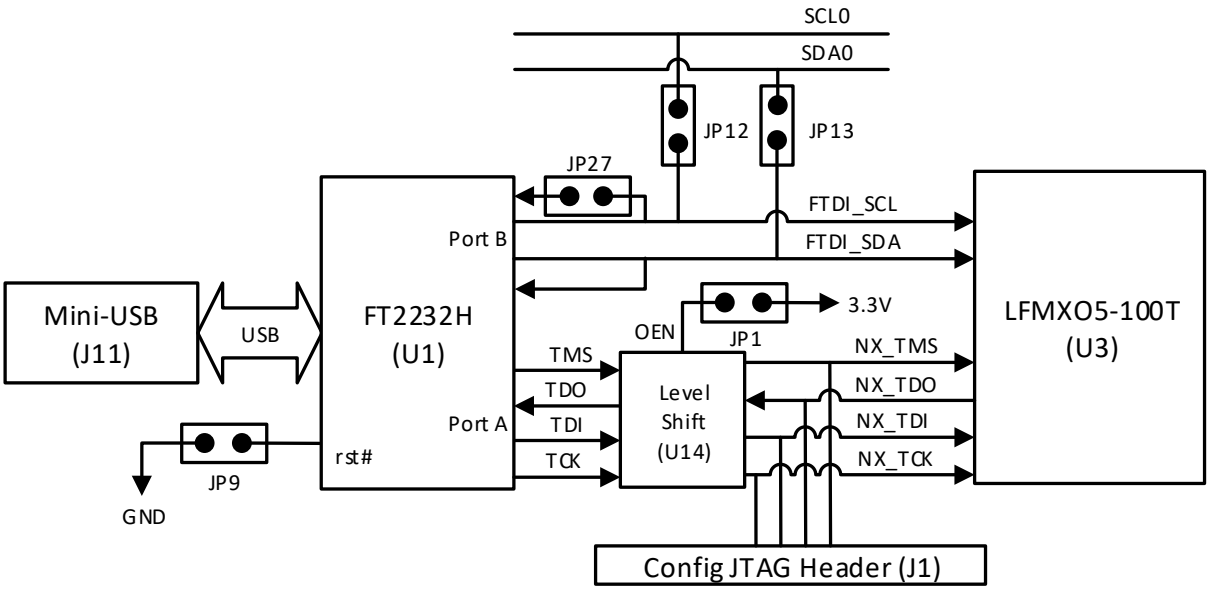

Figure 3.1. JTAG/I²C Programming Architecture

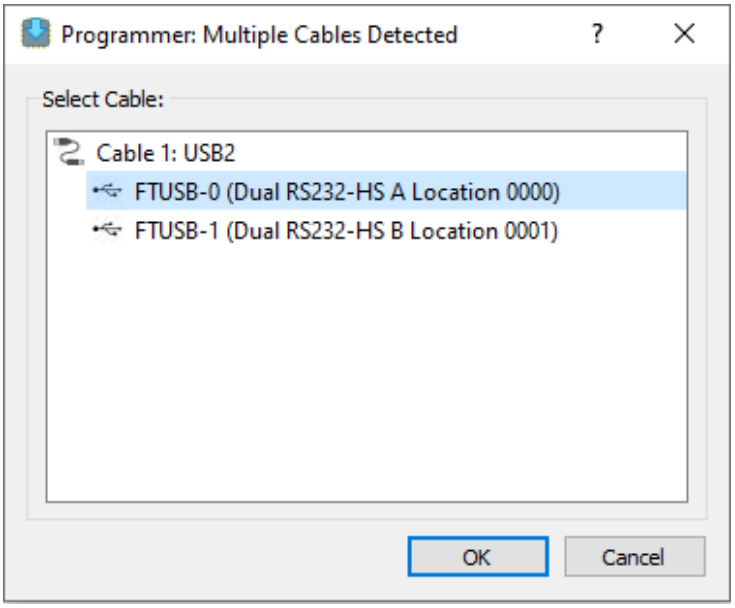

Figure 3.2. Radiant Programmer Detect Dual Ports

3.1. JTAG Download Interface

A level shifter SN74AVC4T774 U14 from TI is inserted between Config FTDI Port A and LFMXO5-100T JTAG port to make sure the FTDI fixed I/O voltage can adapt with flexible voltage selection of bank 2 of the FPGA, as shown in Figure 3.3. An eight-pin header J1 (Figure 3.4) allowing you to probe the JTAG signals to access LFMXO5-100T JTAG port from the external JTAG host, such as external Lattice HW-USBN-2B Programming Cable (available separately), or to access SSPI port from the external SPI host. In those cases, jumper JP1 must be added to pull OEN high and ensure U14 to output tri-state mode so as to avoid multi-drivers on those shared signals. The JTAG connections between J1 and LFMXO5-100T are listed in Table 3.1.

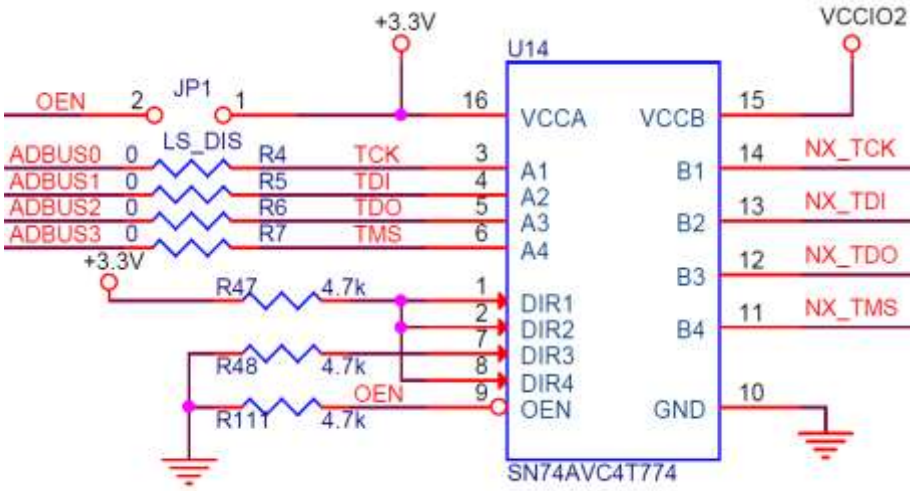

Figure 3.3. Level Shift for JTAG Download Interface

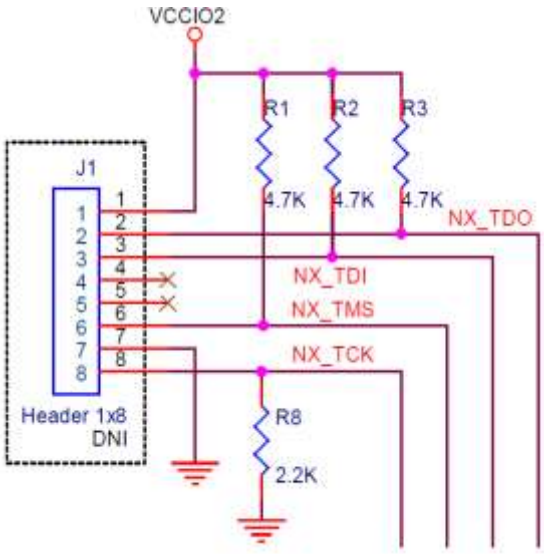

Figure 3.4. JTAG Test Header

Table 3.1. Config JTAG Connections

J1 Pin Number	JTAG Net Name	LFMXO5-100T Ball Location for JTAG	Optional SSPI Function
1	VCCIO2	—	—
2	NX_TDO	E16	SSI
3	NX_TDI	C16	SSO
4	—	—	—
5	—	—	—
6	NX_TMS	B16	SCSN
7	GND	—	—
8	NX_TCK	B19	SCLK

The MachXO5T-NX Development Board also provides test points for other dedicated JTAG configuration pins as shown in Table 3.2.

Table 3.2. Other Config JTAG Control Signals

Net Name	LFMXO5-100T Ball Location	LED Indicator	Test Point
JTAGEN	A14	—	Pin 2 of JP2
PROGRAMN	G10	—	—
INITN	H10	D11	TP5
DONE	H11	D10	TP6

JP2 for JTAGEN is used to pull down the JTAGEN to disable JTAG port. Using SW5 push button with PROGRAMN reloads the bitstream from internal Flash when PROGRAMN_PORT function is enabled by software.

3.2. I²C Download Interface

The USB hub on the PC can also detect the addition of the USB function on Config FTDI Port B. You can select the port FTUSB-1 on the programmer interface for the accessing from Config FTDI Port B to the LFMXO5-100T dedicated I²C download port (Figure 3.2) that is named as FTDI_SDA/FTDI_SCL with 2.2 kΩ pull up resistor each. The Diode D21 is inserted to support I²C clock stretching mode with JP27 added to drive FTDI_SCL from FTDI, but JP27 cannot be added when using I²C config mode. Figure 3.5 details the design of Config FTDI Port B for dedicated I²C download interface. Table 3.3 summarizes the interconnection with LFMXO5-100T and its supported circuits. JP12 and JP13 are used to connect the dedicated I²C download port of LFMXO5-100T with the bridge I²C bus SDA0/SCL0 cross the whole board, in case you need access I²C download port from other on board headers other than Config FTDI part. For the detail connection from other headers to bridge I²C bus SDA0/SCL0, refer to the User I2C Interface section.

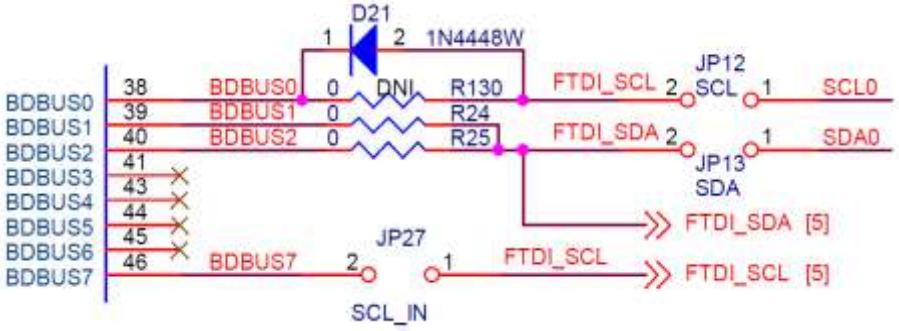

Figure 3.5. I²C Programming Mode

Table 3.3. Download I²C Connections

Download I²C Net Name	LFMXO5-100T Ball Location for JTAG	2.2 kΩ Pull up Resistor	Bridge I²C Net Name	Bridge Jumper
FTDI_SCL	A19	R33	SCL0	JP12
FTDI_SDA	A18	R34	SDA0	JP13

For more information on LFMXO5-100T JTAG/ I²C programming, refer to MachXO5-NX Programming and Configuration User Guide (FPGA-TN-02271).

4. Soft JTAG/UART User Interface

The soft JTAG/UART user interface for the MachXO5T-NX Development Board is shown in Figure 4.1. Supposedly it also uses an FT2232H FTDI part U18 to convert USB to user JTAG from port A, or convert USB to UART from port B. Using Detect Cable function with Radiant programming software installed and ensuring FTDI reset control jumper JP8 is not populated in default, as shown in Figure 3.2, you can detect other dual ports after power up the board. You can then connect the mini USB to USB-A cable from J19 to your PC. The software select option FTUSB-0 is targeted for user JTAG, and FTUSB-1 is targeted for UART that is mapped with port A and port B from hardware perspective.

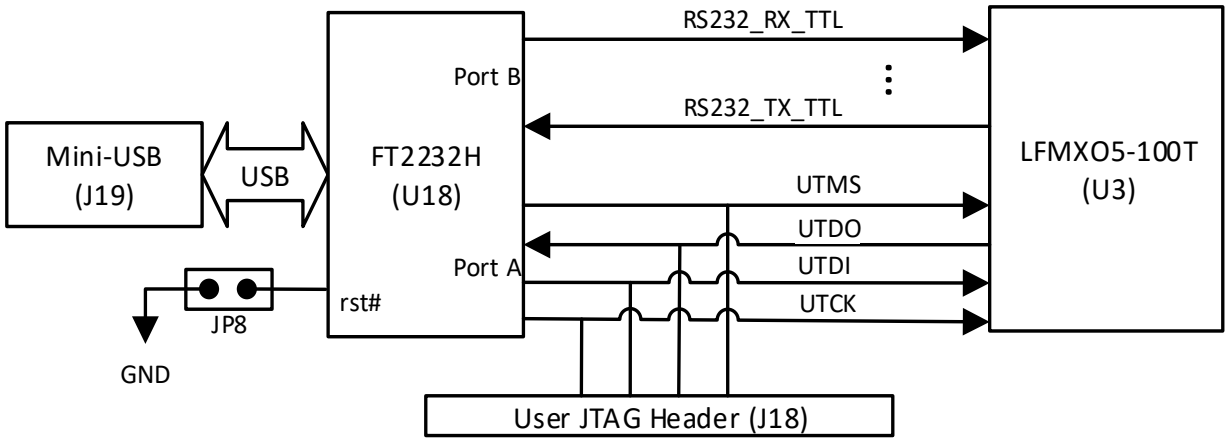

Figure 4.1. JTAG/UART User Interfacing

4.1. Soft JTAG User Interface

User FTDI Port A is connected with GPIOs in Bank 1 directly. You need allocate GPIOs for adaption with JTAG signals by programmable logic, which is defined by FTDI Port A when converting USB to JTAG through FTUSB-0. J18 is an eight-pin standalone JTAG header that is used with an external Lattice download cable (available separately) when the FTDI part is disabled from the JTAG chain after setting JP8. J18 can also be used as test point when USB to JTAG is working.

Table 4.1. Soft JTAG Connections

J18 Pin Number	FTDI Signal	JTAG Net Name	LFMXO5-100T Ball Location
1	—	VCCIO1	—
2	UADBUS2	UTDO	F12
3	UADBUS1	UTDI	F13
4	—	—	—
5	—	—	—
6	UADBUS3	UTMS	G13
7	—	GND	—
8	UADBUS0	UTCK	G14

4.2. Soft UART User Interface

User FTDI Port B is also connected with GPIOs in Bank 0 directly. You need allocate GPIOs for adaption with UART signals by programmable logic, which is defined by FTDI Port B when converting USB to UART through FTUSB-1.

Table 4.2. Soft UART Connections

FTDI Signal	UART Net Name	LFMXO5-100T Ball Location for Port A
UBDBUS0	RS232_RX_TTL	C15
UBDBUS1	RS232_TX_TTL	D15
UBDBUS2	RTSn	B15
UBDBUS3	CTSn	A15
UBDBUS4	DTRn	E13
UBDBUS5	DSRn	E12
UBDBUS6	DCDn	D14
UBDBUS7	RI	E15

5. LFMXO5-100T Clock Sources

The MachXO5T-NX Development Board has multiple external clock options for the LFMXO5-100T applications as shown in Figure 5.1.

- 12 MHz from U1 (FTDI)
- 27 MHz from ×4 (OSC MEM)
- External clock source from J10 (SMA)
- Differential 100 MHz from ×7
- Differential 100 MHz from ×8
- Differential 125 MHz from ×9
- Differential external clock source from SMA4 and SMA5 (SMA pair)

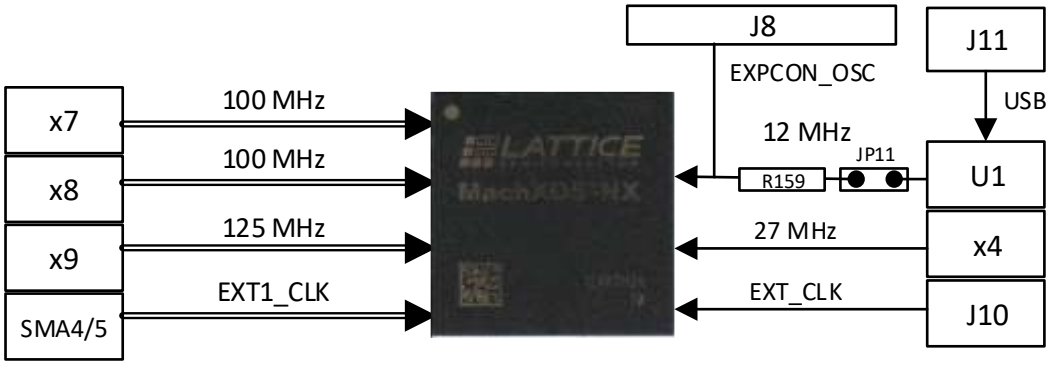

Figure 5.1. Onboard Clock Resources

You need take care 12 MHz clocks from the FT2232H FTDI U1 device are not always on without some hardware configuration. SMA clocks need source from external boards. Refer to Table 5.1 for those clock utilization and enable conditions.

Table 5.1. Input Clock Options

Clock Frequency	Net Name	LFMXO5-100T Ball Location	Clock Source	IO Type	Enable Conditions
12 MHz	EXPCON_OSC	J16	U1	LVCMOS33	Need add R159 and JP11. USB header J11 connected with power on.
27 MHz	27M_OSC_IN	C2	X4	LVCMOS33	Always on. Use J25 to disable or control clock output.
EXT_CLK	OSC_IN	A17	J10	LVCMOS33 or LVCOMS25	Need add J10 SMA. Connect to external clock generator through SMA cable.
100 MHz	EXT0_CLKp/ EXT0_CLKn	C11/C12	X7	LVDS	Always on. Dedicated reference clock for PCS. Refer to the SerDes/PCS User Guide FPGA-TN-02245 for details.
100 MHz	LVSTLD_100MHzp/ LVSTLD_100MHzn	U19/U20	X8	LVSTLD	Always on. Generated by the HSCL clock and AC coupled to the 1.1 V I/O bank for LPDDR4.
125 MHz	LVDS_125MHzp/ LVDS_125MHzn	R3/P3	X9	LVDS	Always on. Dedicated reference clock for PCS. Refer to the CertusPro-NX SerDes/PCS User Guide (FPGA-TN-02245) for details.
SMA_CLK	EXT1_CLKp/EXT1_ CLKn	B13/C13	SMA4/ SMA5	LVDS	Need add SMA4 and SMA5. Connect to external differential clock generator through SMA cables.

6. SGMII Ethernet Connections

This section describes the MachXO5T-NX Development Board SGMII application for Ethernet connections. This board can support two independent Ethernet connections through on-board SGMII PHY devices PHY0 and PHY1, which is GPY115C0VI from Maxlinear, as shown in Figure 6.1. Table 6.1 listed the signals from the FPGA interfacing with SGMII PHY devices.

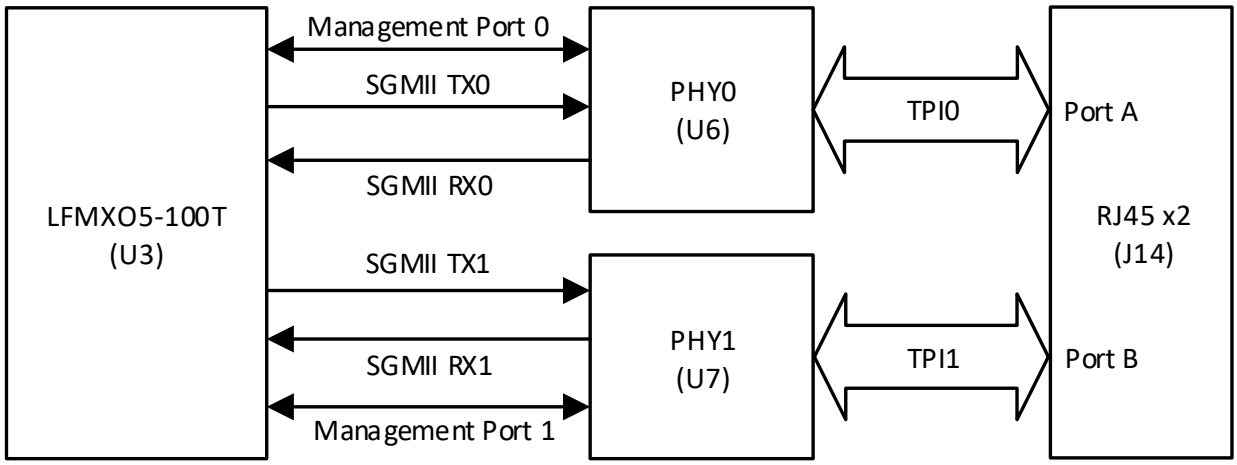

Figure 6.1. SGMII ×2 Interfacing

Table 6.1. SGMII Ethernet PHY Interfacing

PHY Interface	LFMXO5-100T Ball Location	Net Name	Pin Number of PHY Device
PHY0 (U6)	P6	PHY0_MDIO	10
	U2	PHY0_MDC	11
	R4	PHY0_MDINT	12
	T5	PHY0_EXINT0	13
	P2	SGMII_FPGA_RX0P	25
	R2	SGMII_FPGA_RX0N	24
	T1	SGMII_FPGA_TX0P	27
	U1	SGMII_FPGA_TX0N	28
PHY1 (U7)	P7	PHY1_MDIO	10
	T2	PHY1_MDC	11
	P4	PHY1_MDINT	12
	U5	PHY1_EXINT0	13
	R5	SGMII_FPGA_RX1P	25
	P5	SGMII_FPGA_RX1N	24
	P1	SGMII_FPGA_TX1P	27
	R1	SGMII_FPGA_TX1N	28

The pin strapping configuration for both SGMII PHY devices have been implemented on board, as shown in Table 6.2 and Table 6.3.

Table 6.2. SGMII Ethernet PHY0 Strapping Configuration

U6 Pin Number	Configuration Item Description	Logic Value in Default	1K Pull up Resistor	1K Pull down Resistor
37	PS_PHY_MADDR(0)	0	R182 (DNI)	R172
35	PS_PHY_MADDR(1)	0	R178 (DNI)	R173
34	PS_PHY_MADDR(2)	0	R179 (DNI)	R174
3	PS_PHY_MADDR(3)	0	R180 (DNI)	R175
2	PS_PHY_MADDR(4)	0	R181 (DNI)	R176
12	PS_MINT_POL	0	R183 (DNI)	R171
18	PS_RJ45_TAP	0	R184 (DNI)	R170
19	PS_MDIO_VOLTAGE	0	NA	R177

Table 6.3. SGMII Ethernet PHY1 Strapping Configuration

U7 Pin Number	Configuration Item Description	Logic Value in Default	1K Pull up Resistor	1K Pull down Resistor
37	PS_PHY_MADDR(0)	0	R224(DNI)	R215
35	PS_PHY_MADDR(1)	0	R220(DNI)	R216
34	PS_PHY_MADDR(2)	0	R221(DNI)	R217
3	PS_PHY_MADDR(3)	0	R222(DNI)	R218
2	PS_PHY_MADDR(4)	0	R223(DNI)	R219
12	PS_MINT_POL	0	R225(DNI)	R214
18	PS_RJ45_TAP	0	R226(DNI)	R213
19	PS_MDIO_VOLTAGE	0	—	R202

MachXO5T-NX Development Board provides two options to supply the VDD power of PHY devices, as shown in Table 6.4. One option is to supply the VDD with on-board 1.0 V regulator. The other option needs additional power from the on-board 3.3 V LDO and converts to 1.0 V output by the internal regulator of PHY devices. It is recommended to use the first option to improve the power efficiency and off load the 3.3V LDO on this board.

Table 6.4. PHY device VDD Power Supply Options

PHY VDD	Jumper	Supply from On-board Regulator	Supply from in-chip Regulator
U6	J26	Pin 2-3 (U12)	Pin 1-2 (U6)
U7	J28	Pin 2-3 (U12)	Pin 1-2 (U7)

7. PCIe Gold Finger

MachXO5T-NX Development Board supports ×1 PCIe Gen2, as shown in Figure 7.1. The signal connections are listed in Table 7.1.

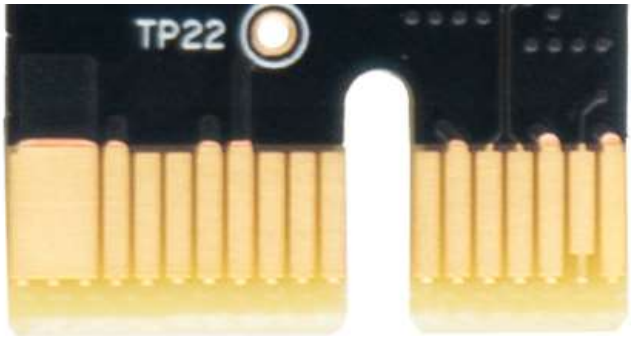

Figure 7.1. Top Side of PCIe Edge Connector

Table 7.1. Gold Finger Pin Connections

CN1 Pin Number	Net Name	LFMXO5-100T Ball Location
A1	PRSNT1n	—
A2,A3,B1,B2,B3	12_IN_PCIE	—
A4,A12,A15,A18,B4,B7,B13,B16,B18	GND	—
A9,A10,B8	PCIE_3V3	—
A11	PCIE_PERSTn	K6[1]
A13	PCIE_CLKP	C7
A14	PCIE_CLKN	B7
A16	x1_PERp0	A5
A17	x1_PERn0	A6
B14	x1_PETp0	A2
B15	x1_PETn0	A3
B17	PRSNT2n	—
—	R0_ext	C4
—	RET0_ref	B4

Note:

1. Need add JP10 to bridge with FPGA control I/O.

8. Optional SMA Headers

MachXO5T-NX Development Board provides two pairs of high speed SMA footprints to support flexible Serdes Protocol validation, with x1 RX and TX signal pairs, as shown in Figure 8.1. Their SMA footprint is compatible with SF2921-61345-2S from Amphenol. The signal mapping was shown as Table 8.1.

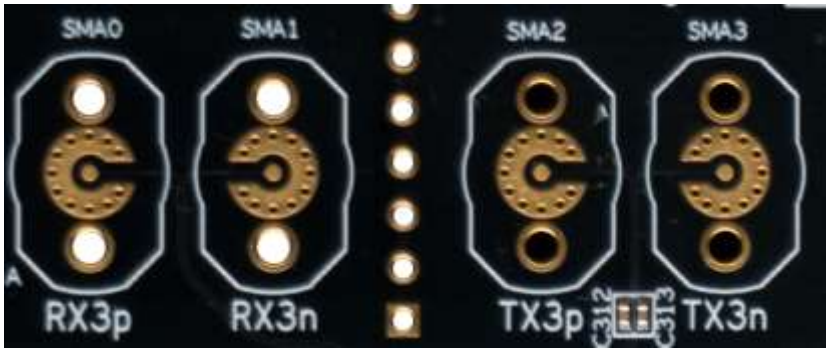

Figure 8.1. SMA Interfacing for x1 Serdes RX and TX

Table 8.1. Connections for SMA Serdes signal pair

Reference	Net Name	LFMXO5-100T Ball Location
SMA0	SD3_RXp	A8
SMA1	SD3_RXn	A9
SMA2	SD3_TXp	A11
SMA3	SD3_TXn	A12

Note: LFMXO5-100T engineering samples cannot support additional PCIe lane via the SMA.

MachXO5T-NX Development Board also provides a pair of high-speed SMA footprints to support SerDes extension reference clock input as shown in Figure 8.2. Their SMA footprint is compatible with SF2921-61356-2S from Amphenol and the LVDS clock is recommended to be connected. The signal mapping is shown in Table 8.2.

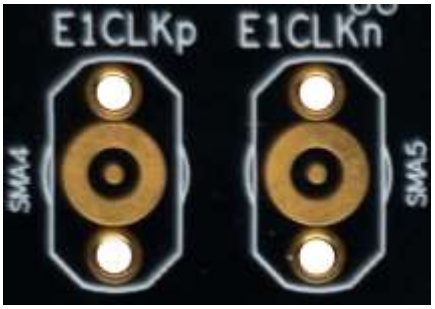

Figure 8.2. SMA Interfacing for x1 SerDes Rx and Tx

Table 8.2. Connections for External SMA Reference Clock

SMA	Net Name	LFMXO5-100T Ball Location
SMA4	EXT1_CLKp	B13
SMA5	EXT1_CLKn	C13

MachXO5T-NX Development Board is also designed with a single-end SMA clock header J10, as shown in Figure 8.3. This is low-cost standard type SMA footprint, such as 5-1814832-2 from TE Connectivity. You need solder it on the board. Table 8.3 details its connection to the FPGA.

Figure 8.3. SMA Clock Input

Table 8.3. Single-end External SMA Clock

SMA	Net Name	LFMXO5-100T Ball Location
J10	EXT_CLK	A17

9. LPDDR4 Memory Controller Interface

Table 9.1 lists all LPDDR4 memory controller Interface signals. The LFMXO5-100T device Memory Controller is used to interface with the onboard 16-bit parallel data and 8 Gb capacity LPDDR4 memory device (Micron MT53E512M16D1), which is supported with 512 Meg ×16 configurations. This board is designed to use on-die termination in default and reserved on-board termination options.

Table 9.1. LPDDR4 Memory Controller Interconnections

LPDDR4 Net Name (U9)	LFMXO5-100T Ball Location
DQ0_A	N18
DQ1_A	N20
DQ2_A	P18
DQ3_A	P17
DQ4_A	P16
DQ5_A	N19
DQ6_A	M17
DQ7_A	M16
DMI0_A	N17
DQS0_T_A	P19
DQS0_C_A	P20
DQ8_A	R15
DQ9_A	T14
DQ10_A	R14
DQ11_A	T15
DQ12_A	V14
DQ13_A	W14
DQ14_A	V15
DQ15_A	U14
DMI1_A	U15
DQS1_T_A	Y15
DQS1_C_A	Y14
CA0_A	W19
CA1_A	V18
CA2_A	T19
CA3_A	V19
CA4_A	V20
CA5_A	T20
CK_T_A	R19
CK_C_A	R20
CKE0_A	W20
CS0_A	W18
ODT_CA_A	R16
RESET_N	N16
ZQ0[1]	—

Note:

1. ZQ0 is pull up VDDQ through a 240 Ω resistor.

Caution: The MachXO5T-NX Development Board is designed to support ×16 bits with default population but reserved to support x24 bits configuration if change to x32 LPDDR4 device.

10. Generating the Programming File

The demo project on the MachXO5T-NX Development Board Rev A board can be downloaded from the Lattice website (https://www.latticesemi.com/products/developmentboardsandkits/machxo5-nx-development-board).

To generate the JEDEC (.jed) file:

1. Open the Lattice Radiant software.
2. From the **File** menu, choose **Open > Project**.
3. In the **Open Project** dialog box, select the *test.rdf* file and click **Open**, as shown in Figure 10.1. This opens the demo project.

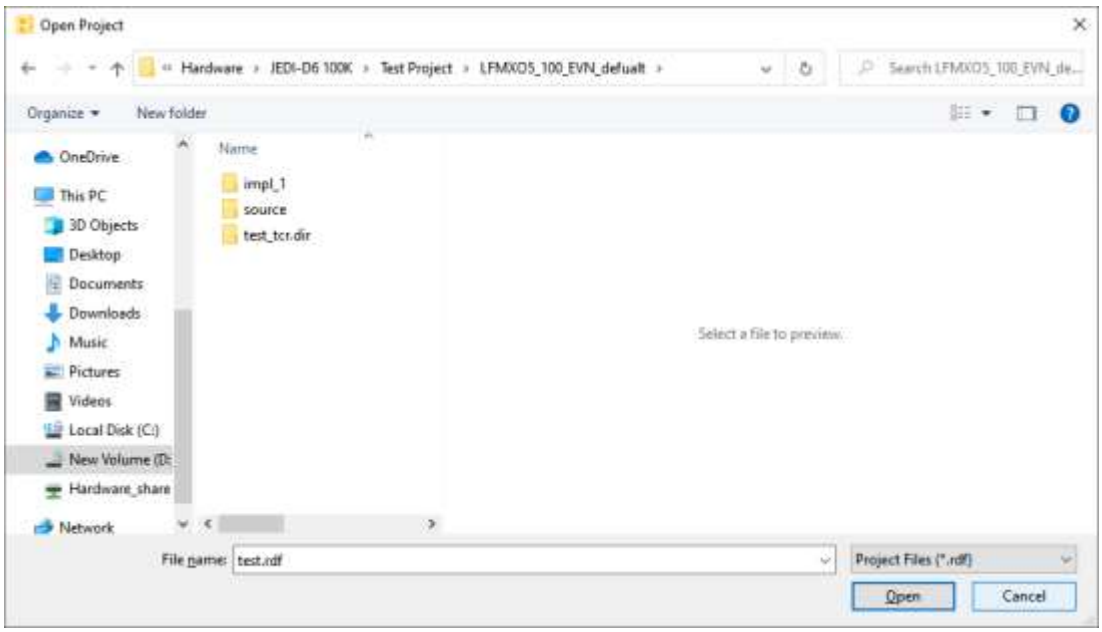

Figure 10.1. Radiant Software – Open Project Dialog Box

4. In the **Process Toolbar**, click **Run All** , as shown in Figure 10.2.

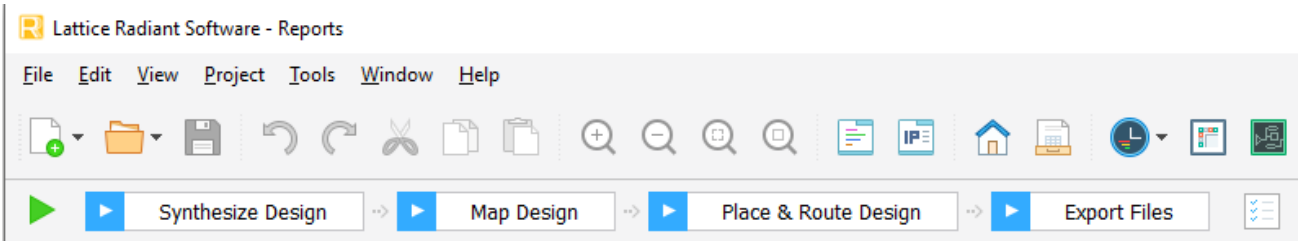

Figure 10.2. Radiant Software – Process Toolbar Initial State

Green checkmarks appear on each successfully-completed step, including the generation of the JEDEC file, as shown in Figure 10.3.

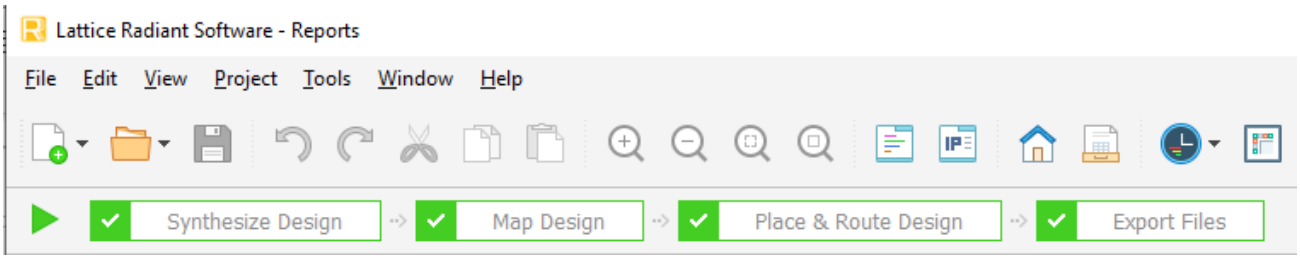

Figure 10.3. Radiant Software – State of the Processes Toolbar Completion

The generated .mcs and *.jed* file are located in the *impl_1* folder.

11. Programming the MachXO5-NX Device

Lattice Radiant Programmer can be used to program the JEDEC file to the MachXO5-NX embedded flash after the JEDEC data file is generated, as shown in the Generating the Programming File section. Radiant Programmer is integrated into the Radiant software and is also available as a standalone version.

To program the MachXO5-NX embedded flash:

1. Connect the PC and MachXO5T-NX Development Board (J11) using the USB cable.
2. In Radiant Software, click **Tools** > **Programmer**, as shown in Figure 11.1.

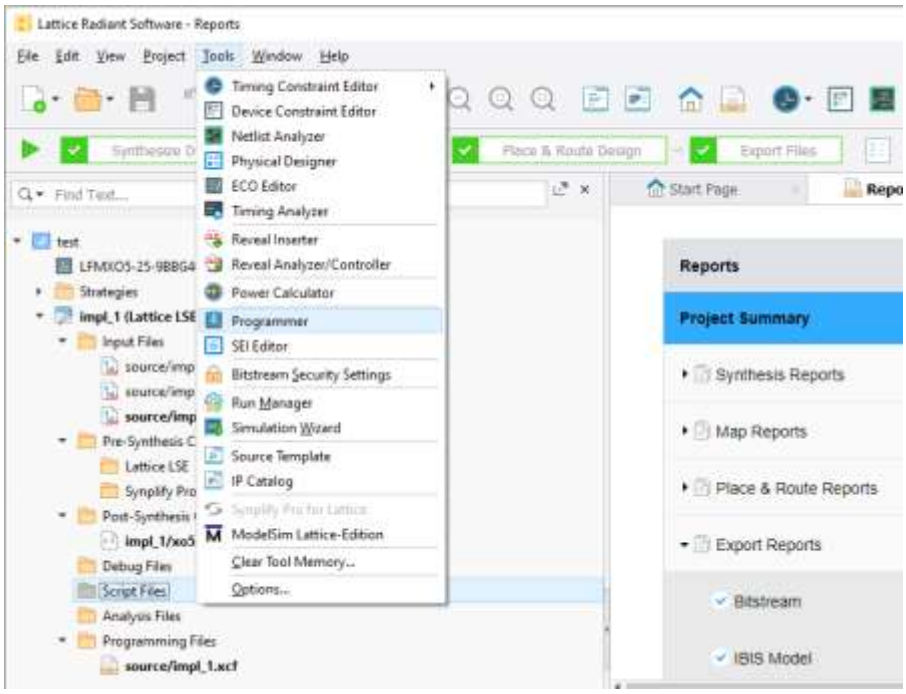

Figure 11.1. Radiant Software – Radiant Programmer

3. After the Radiant Programmer interface opens (Figure 11.2), power up MachXO5T-NX Development Board by correctly positioning the power switch **SW6**.

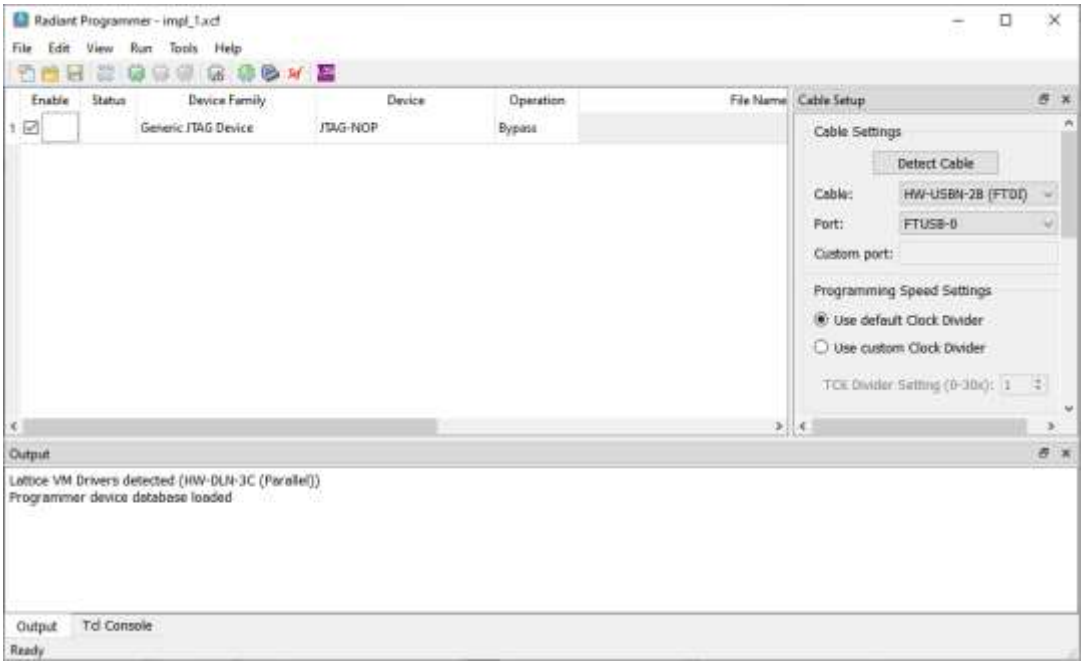

Figure 11.2. Radiant Programmer – Initial Opened

4. Click **Run** > **Scan Device** to check the board through FTUSB-0 Port of embedded HW-USBN-2B(FTDI) cable, as shown in Figure 11.3. The MachXO5-NX device named as LFMXO5-100T should be detected on the JTAG chain as shown in Figure 11.4.

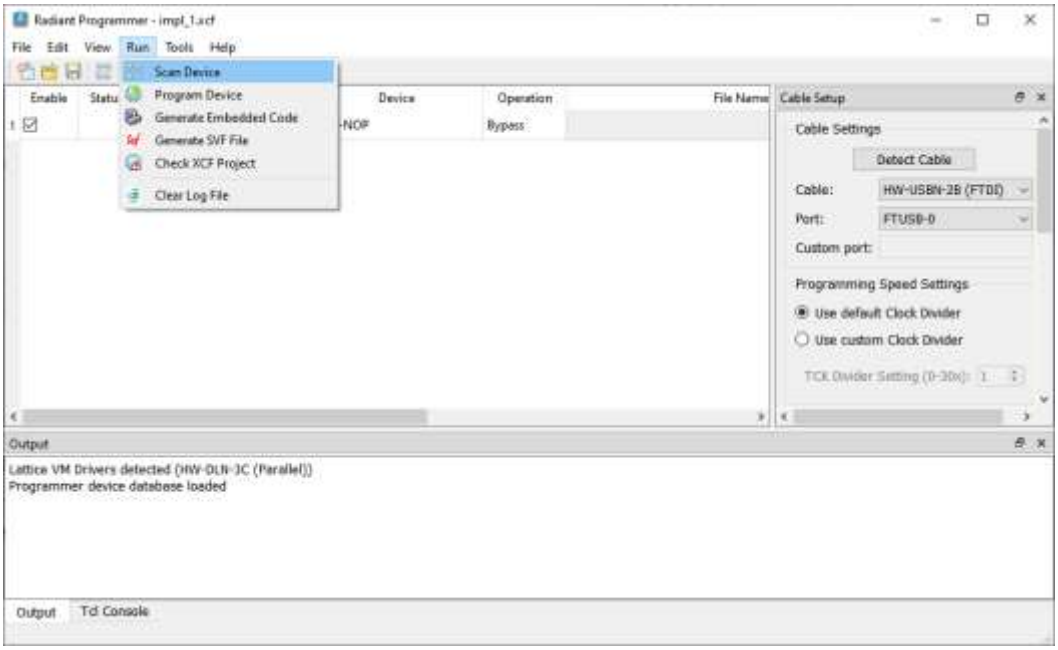

Figure 11.3. Radiant Programmer – Scan Device

5. Change the **Programming Speed Settings** in the **Cable Setup** pane on the right. Check the **Use custom Clock Divider** option to increase the **TCK Divider Setting** to 3 or above, as shown in Figure 11.4.

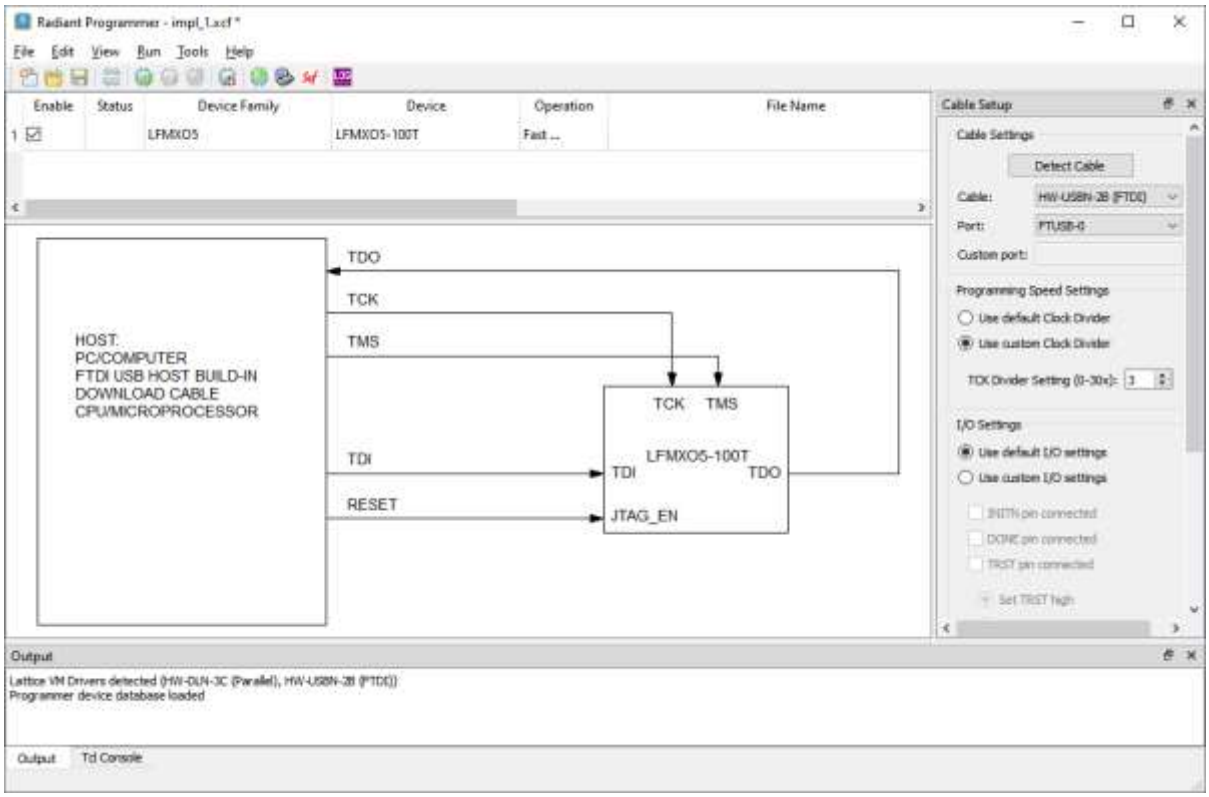

Figure 11.4. Radiant Programmer – Device Detected

6. Open the **Device Properties** dialog box by double click **Operation** column. Select **FLASH Configuration Memory** from **Target Memory** drop-down list in the **Device Operation** area, as shown in Figure 11.5. You can then see the **Device Properties** dialog showing FLASH Configuration Memory details (Figure 11.6).

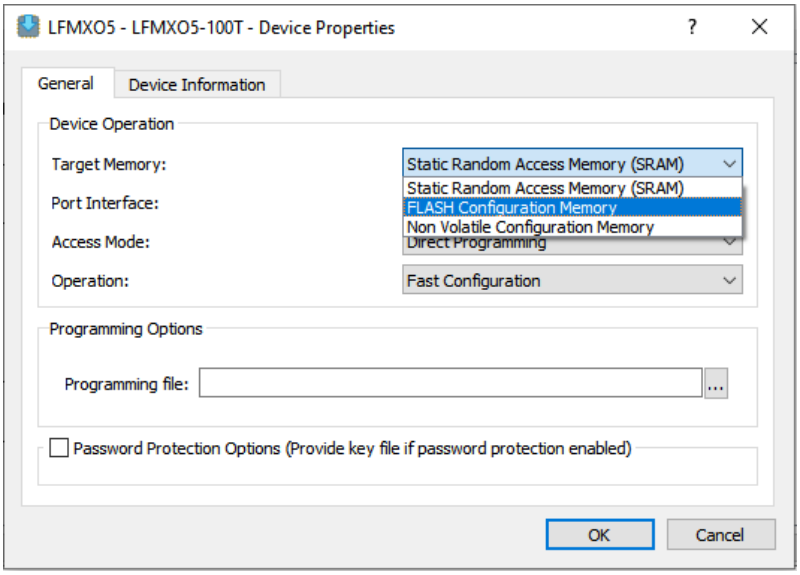

Figure 11.5. Radiant Programmer – Select Target Memory for Device Properties

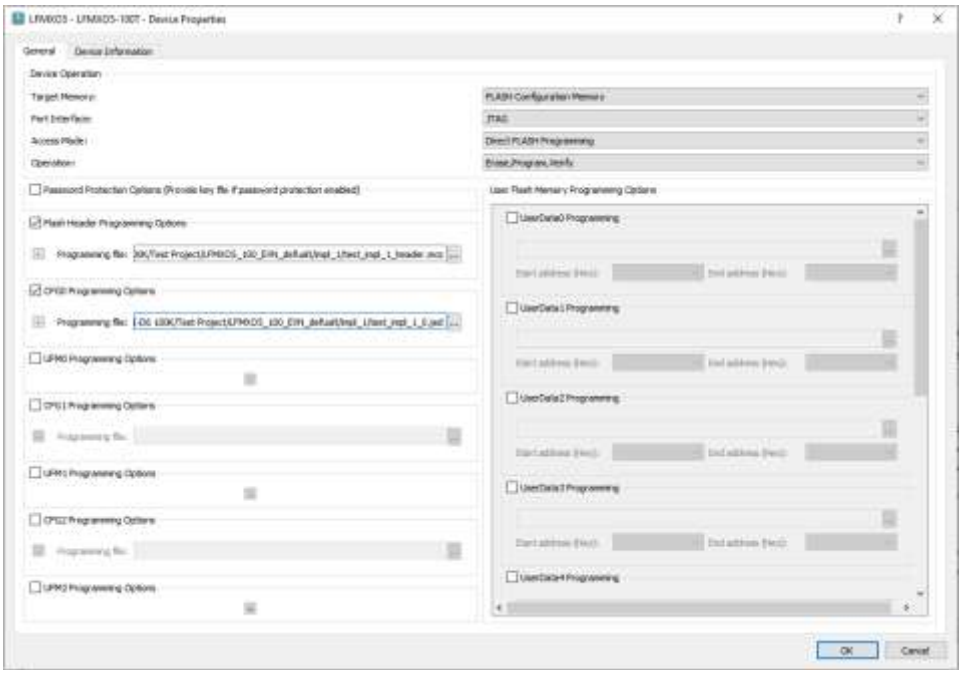

Figure 11.6. Radiant Programmer – Device Properties for FLASH Configuration Memory

7. Confirm the **Device Operation** options as follows:
   - **Target Memory** is *FLASH Configuration Memory*;
   - **Port Interface** is *JTAG*;
   - **Access Mode** is *Direct FLASH Programming*;
   - **Operation** is *Erase, Program, Verify*;

   and select target **User Flash Memory Programming Options** according to Figure 11.6.
8. Check the **Flash Header Programming Options** and click **…** to select the .mcs file.
9. Check the **CFG0 Programming Options** and click **…** to select the .jed file.
10. Click **OK** to program the embedded Flash.
11. Click the **Program Device** button in Radiant Programmer as shown in Figure 11.7.

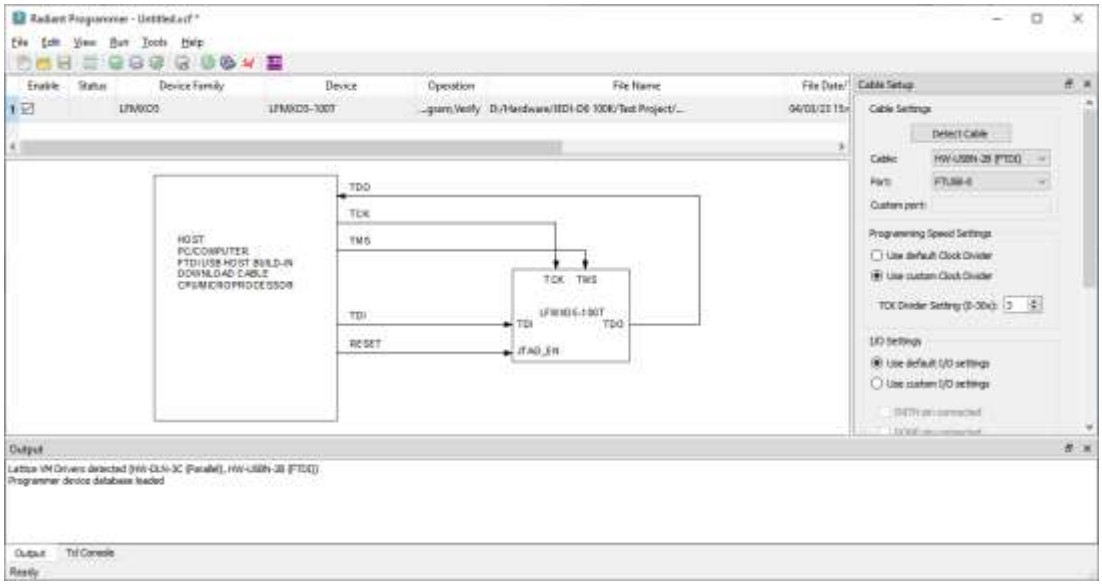

Figure 11.7. Radiant Programmer – Ready for Flash Programming

12. Wait for about 2 minutes. If programming successful, the **Status** column shows **PASS** with the Output pane also shows INFO – Operation: successful.

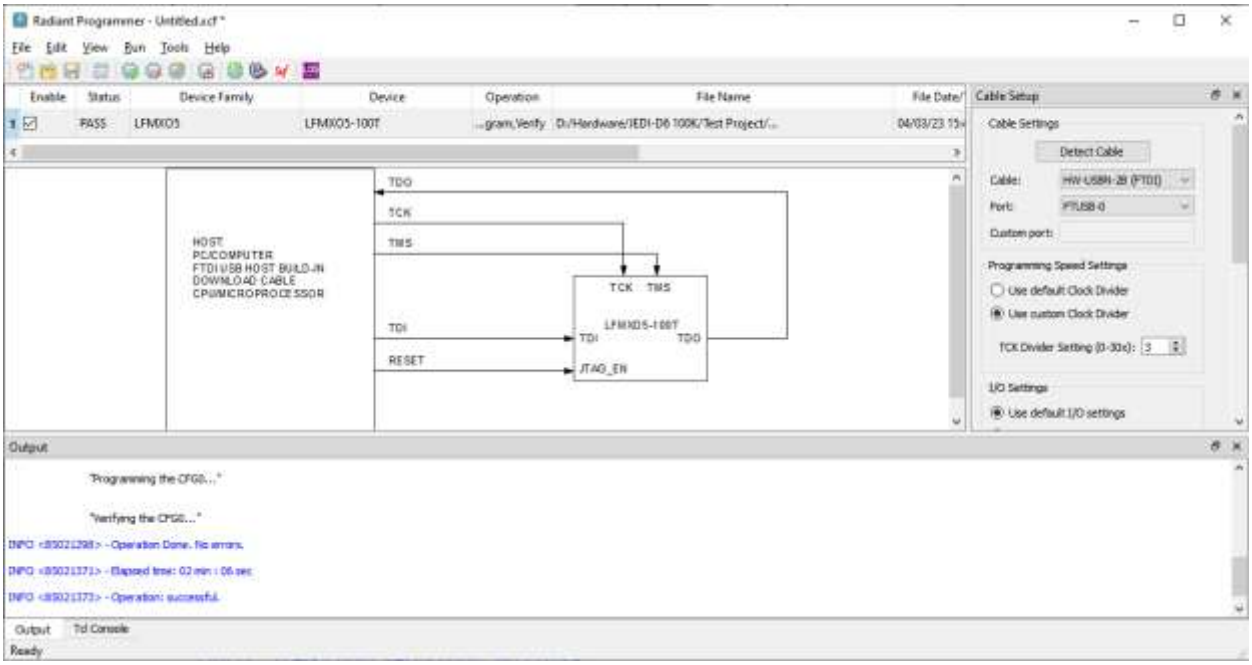

Figure 11.8. Radiant Programmer – Flash Programming Successful

12. Headers and Test Connections

This section describes the MachXO5T-NX Development Board headers and test connections.

12.1. Versa Headers

The board provides two headers, J8 and J9, for expansion purpose.

Table 12.1. Versa J8 Header Pin Connections

J8 Pin Number	Net Name	LFMXO5-100T Ball Location
1	GND	—
2	NC	—
3	EXPCON_2V5*	—
4	EXPCON_IO29	J10
5	EXPCON_IO30	J11
6	EXPCON_IO31	K10
7	EXPCON_IO32	J17
8	EXPCON_IO33	J12
9	EXPCON_IO34	H20
10	EXPCON_IO35	H19
11	EXPCON_IO36	K11
12	EXPCON_IO37	J19
13	EXPCON_IO38	J14
14	EXPCON_IO39	J13
15	EXPCON_IO40	K16
16	EXPCON_IO41	J15
17	EXPCON_IO42	K14
18	EXPCON_IO43	K15
19	EXPCON_IO44	K12
20	EXPCON_IO45	K13
21	5VIN*	—
22	GND	—
23	EXPCON_2V5*	—
24	GND	—
25	+3.3V	—
26	GND	—
27	+3.3V	—
28	GND	—
29	EXPCON_OSC	J16
30	GND	—
31	EXPCON_CLKIN	J18
32	GND	—
33	EXPCON_CLKOUT	J20
34	GND	—
35	EXPCON_3V3**	—
36	GND	—
37	EXPCON_3V3**	—
38	GND	—
39	EXPCON_3V3**	—
40	GND	—

Notes:

* Net is optionally connected to power source through resistor DNI.

** Net is optionally connected to power source through resistor DI.

Table 12.2. Versa J9 Header Pin Connections

J9 Pin Number	Net Name	LFMXO5-100T Ball Location
1	HPE_RESOUT#	H14
2	GND	—
3	EXPCON_IO0	H15
4	EXPCON_IO1	H13
5	EXPCON_IO2	F15
6	EXPCON_IO3	H16
7	EXPCON_IO4	D16
8	EXPCON_IO5	F16
9	EXPCON_IO6	C17
10	EXPCON_IO7	A16
11	EXPCON_IO8	B18
12	EXPCON_IO9	B17
13	EXPCON_IO10	F17
14	EXPCON_IO11	E17
15	EXPCON_IO12	E18
16	EXPCON_IO13	B20
17	EXPCON_IO14	F18
18	EXPCON_IO15	G16
19	GND	—
20	EXPCON_3V3**	—
21	EXPCON_IO16	G17
22	GND	—
23	EXPCON_IO17	C19
24	GND	—
25	EXPCON_IO18	C20
26	GND	—
27	EXPCON_IO19	D20
28	EXPCON_IO20	D19
29	EXPCON_IO21	E19
30	GND	—
31	EXPCON_IO22	F19
32	EXPCON_IO23	E20
33	EXPCON_IO24	F20
34	GND	—
35	EXPCON_IO25	G20
36	EXPCON_IO26	G19
37	EXPCON_IO27	H17
38	CARDSEL#*	—
39	EXPCON_IO28	H18
40	GND	—

Notes:

* Net is optionally connected to power source through resistor DNI.

** Net is optionally connected to power source through resistor DI.

12.2. Arduino Board GPIO Headers

The board provides four headers, J2, J3, J4, and J5, for Arduino Zero board adaption.

Table 12.3. Arduino J2 Pin Connections

J2 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-100T Ball Location	Comments
1	AR_IO8	~D8/PA06	K3	—
2	AR_IO9	~D9/PA07	K2	—
3	AR_SS_IO10	~D10/PA18/SS	K1	Defaults to SS function on Arduino ZERO Board.
4	AR_MOSI_IO11	~D11/PA16/COPI	L3	Defaults to COPI function on Arduino ZERO Board.
5	AR_MISO_IO12	~D12/PA19/CIPO	L1	Defaults to CIPO function on Arduino ZERO Board.
6	AR_SCK_IO13	~D13/PA17/SCK	L2	Defaults to SCK function on Arduino ZERO Board.
7	GND	GND	—	—
8	AR_AREF	AREF/PA03	L6	AR_AREF connection to AREF through R43.
9	AR_SDA	D20/PA22/SDA	N5	Defaults to SDA function on Arduino ZERO Board. It is optionally connected to SDA0 through R44 (DNI).
10	AR_SCL	D21/PA23/SCL	N6	Defaults to SCL function on Arduino ZERO Board. It is optionally connected to SCL0 through R45 (DNI).

Table 12.4. Arduino J3 Pin Connections

J3 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-100T Ball Location	Comments
1	AR_IO0	D0/RX/PA11	K4	—
2	AR_IO1	D1//TX/PA10	K5	—
3	AR_IO2	D2/PA14	J6	—
4	AR_IO3	~D3/PA09	K7	—
5	AR_IO4	~D4/PA08	J7	—
6	AR_IO5	~D5/PA15	J8	—
7	AR_IO6	~D6/PA20	H9	—
8	AR_IO7	D7/PA21	K8	—

Table 12.5. Arduino J4 Pin Connections

J4 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-100T Ball Location	Comments
1	AR_IO14	ATN	L7	—
2	NC	IOREF	—	—
3	AR_RESET	RESET	K2	Pin K2 should be set high by default. Avoid Arduino ZERO board in Reset status when connected.
4	+3.3V_AR	+3V3	—	3.3 V power supply from Arduino ZERO board.
5	AR_5V	+5V	—	Jump to 5 V onboard power rail through JP6.
6	GND	GND	—	—
7	GND	GND	—	—
8	+12V	VIN	—	Share with +12 V onboard power rail.

Note:
If JP6 is installed, 5 V power can be supplied from either the Arduino board or the MachXO5T-NX Development Board. With JP6 removed, both boards need their own 5 V power.

Table 12.6. Arduino J5 Pin Connections

J5 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-100T Ball Location	Comments
1	AR_AD0	D14/ADC0/PA02	M1	Defaults to ADC0 on Arduino ZERO Board.
2	AR_AD1	D15/ADC1/PB08	M2	Defaults to ADC1 on Arduino ZERO Board.
3	AR_AD2	D16/ADC2/PB09	M3	Defaults to ADC2 on Arduino ZERO Board.
4	AR_AD3	D17/ADC3/PA04	M4	Defaults to ADC3 on Arduino ZERO Board.
5	AR_AD4	D18/ADC4/PA05	M5	Defaults to ADC4 on Arduino ZERO Board.
6	AR_AD5	D19/ADC5/PB02	M6	Defaults to ADC5 on Arduino ZERO Board.

12.3. FPC Headers

The board provides two 50-Pin FPC headers, CN2 and CN3, for board signal extension. Each header got 14 pairs of LVDS or SLVS signals for high-speed data transmitter or receiver. CN2 and CN3 are designed to support loopback test with a standard 50-pin FPC cable.

Table 12.7. FPC Header Pin Connections

CN2 at the Top Side			CN3 at the Bottom Side		
Pin Number	Net Name	CertusPro-NX Ball Location	Pin Number	Net Name	CertusPro-NX Ball Location
1	NC	—	50	NC	—
2	TP3	—	49	TP4	—
3	TP3	—	48	TP4	—
4	TP3	—	47	TP4	—
5	TP3	—	46	TP4	—
6	NC	—	45	NC	—
7	SLVS_TP1	V6	44	SLVS_TP2	W6
8	GND	—	43	GND	—
9	SLVS_DP26	W4	42	SLVS_DP24	Y2
10	SLVS_DN26	Y4	41	SLVS_DN24	Y3
11	GND	—	40	GND	—
12	SLVS_DP27	W5	39	SLVS_DP25	V1
13	SLVS_DN27	Y5	38	SLVS_DN25	W1
14	GND	—	37	GND	—
15	SLVS_DP0	W13	36	SLVS_DP12	U13
16	SLVS_DN0	W12	35	SLVS_DN12	V13
17	GND	—	34	GND	—
18	SLVS_DP1	V11	33	SLVS_DP13	R13
19	SLVS_DN1	U12	32	SLVS_DN13	T13
20	GND	—	31	GND	—
21	SLVS_DP2	Y12	30	SLVS_DP14	P12
22	SLVS_DN2	Y13	29	SLVS_DN14	R12
23	GND	—	28	GND	—
24	SLVS_DP3	W9	27	SLVS_DP15	U10
25	SLVS_DN3	W10	26	SLVS_DN15	V10
26	GND	—	25	GND	—
27	SLVS_DP4	V12	24	SLVS_DP16	U9
28	SLVS_DN4	W11	23	SLVS_DN16	V9
29	GND	—	22	GND	—

CN2 at the Top Side			CN3 at the Bottom Side		
Pin Number	Net Name	CertusPro-NX Ball Location	Pin Number	Net Name	CertusPro-NX Ball Location
30	SLVS_DP5	P13	21	SLVS_DP17	R9
31	SLVS_DN5	P14	20	SLVS_DN17	T9
32	GND	—	19	GND	—
33	SLVS_DP6	Y10	18	SLVS_DP18	W7
34	SLVS_DN6	Y11	17	SLVS_DN18	W8
35	GND	—	16	GND	—
36	SLVS_DP7	Y8	15	SLVS_DP19	N9
37	SLVS_DN7	Y9	14	SLVS_DN19	P9
38	GND	—	13	GND	—
39	SLVS_DP8	Y6	12	SLVS_DP20	N7
40	SLVS_DN8	Y7	11	SLVS_DN20	N8
41	GND	—	10	GND	—
42	SLVS_DP9	U7	9	SLVS_DP21	M12
43	SLVS_DN9	V7	8	SLVS_DN21	N12
44	GND	—	7	GND	—
45	SLVS_DP10	T7	6	SLVS_DP22	R11
46	SLVS_DN10	R7	5	SLVS_DN22	R10
47	GND	—	4	GND	—
48	SLVS_DP11	R8	3	SLVS_DP23	P10
49	SLVS_DN11	P8	2	SLVS_DN23	P11
50	GND	—	1	GND	—

12.4. Aardvark Header (DNI)

The Aardvark I^2C /SPI Host Adapter is a fast and powerful I^2C bus and SPI bus host adapter through USB. It allows you to interface a Windows, Linux, or Mac OS X PC through USB to a downstream embedded system environment and transfer serial messages using the I^2C and SPI protocols.

The MachXO5T-NX Development Board provides an Aardvark compatible header for customer applications. The I^2C bus is optional connecting to a global I^2C bus on the board.

Table 12.8. Aardvark J7 Header Pin Connections

J7 Pin Number	Net Name	LFMXO5-100T Ball Location
1	AK_SCL	M7
2	GND	—
3	AK_SDA	M8
4	+5V_I2C	—
5	AK_MISO	N1
6	+5V_SPI	—
7	AK_SCLK	N2
8	AK_MOSI	N4
9	AK_SS	N3
10	GND	—

12.5. Raspberry Pi Board GPIO Header

The MachXO5T-NX Development Board provides a 40-pin receptacle that is compatible with the GPIO header of Raspberry Pi 2/3 serial models.

Table 12.9. Raspberry Pi J6 Header Pin Connections

J6 Pin Number	Net Name	LFMXO5-100T Ball Location	J6 Pin Number	Net Name	LFMXO5-100T Ball Location
1	3.3V_RASP*	—	2	RASP_5V**	—
3	RASP_IO02	E8	4	RASP_5V**	—
5	RASP_IO03	F6	6	GND	—
7	RASP_IO04	G9	8	RASP_IO14	G8
9	GND	—	10	RASP_IO15	F8
11	RASP_IO17	E7	12	RASP_IO18	G7
13	RASP_IO27	E6	14	GND	—
15	RASP_IO22	E5	16	RASP_IO23	E4
17	3.3V_RASP*	—	18	RASP_IO24	E3
19	RASP_IO10	F7	20	GND	—
21	RASP_IO09	E2	22	RASP_IO25	F3
23	RASP_IO11	F2	24	RASP_IO08	F1
25	GND	—	26	RASP_IO07	G3
27	RASP_ID_SD	D1	28	RASP_ID_SC	E1
29	RASP_IO05	G1	30	GND	—
31	RASP_IO06	G2	32	RASP_IO12	F5
33	RASP_IO13	G6	34	GND	—
35	RASP_IO19	H4	36	RASP_IO16	H5
37	RASP_IO26	H6	38	RASP_IO20	H7
39	GND	—	40	RASP_IO21	H8

Notes:

* 3.3 V power is supplied from Raspberry Pi board.

** 5 V power can come from either the Raspberry Pi board or the MachXO5T-NX Development Board when jumper JP7 is installed. When jumper JP7 is not installed, both boards need their own 5 V power.

12.6. PMOD Headers

The MachXO5T-NX Development Board provides two 12-pin receptacle headers that is compatible with the Digilent PMOD™ interface spec.

Table 12.10. J15 Header Pin Connections

J15 Pin Number	Net Name	LFMXO5-100T Ball Location	J15 Pin Number	Net Name	LFMXO5-100T Ball Location
1	PMOD0_1	K20	7	PMOD0_5	K19
2	PMOD0_2	L16	8	PMOD0_6	L17
3	PMOD0_3	L18	9	PMOD0_7	L20
4	PMOD0_4	L19	10	PMOD0_8	M18
5	GND	—	11	GND	—
6	VCCIO2	—	12	VCCIO2	—

Table 12.11. J16 Header Pin Connections

J16 Pin Number	Net Name	LFMXO5-100T Ball Location	J16 Pin Number	Net Name	LFMXO5-100T Ball Location
1	PMOD1_1	J4	7	PMOD1_5	J5
2	PMOD1_2	J1	8	PMOD1_6	J3
3	PMOD1_3	H1	9	PMOD1_7	J2
4	PMOD1_4	H3	10	PMOD1_8	H2
5	GND	—	11	GND	—
6	VCCIO7	—	12	VCCIO7	—

12.7. User I²C Interface

This board provides more options for user I²C access from different LFMXO5-100T Wide Range I/O to multiple onboard headers. They are solid connected for target applications, but those connections to bridge SCL0/SDA0 are not populated in default. User need to customize interconnection for I²C applications across the board. For example, if you want to use an Ardvark I²C host to access ARDUINO board, you can use internal fabric logic of LFMXO5-100T to bridge AK_SCL/AK_SDA with AR_SCL/AR_SDA, or add bridge resistors according to Table 12.12 to connect all of them to SCL0/SDA0 for bridge interconnections on board without involvement of FPGA. You also need to setup the design with tri-state mode for output high with pull up resistors. If there is no pull up setup on the counterpart boards or internal GPIOs of FPGA, you can add JP12 and JP13 to leverage FTDI's I2C pull up R33 and R34 for SCL0/SDA0. Note that the multi-drives should be disabled for FTDI_SCL/FTDI_SDA in this case. You can add JP9 to disable FTDI output and force FPGA output High-Z from ball location A19/A18.

By adding JP12 and JP13, you can also access FPGA I²C configure interface from those extension boards with I²C host through SCL0/SDA0, which provides the flexibility to update the bitstream from an extension board in some applications.

Table 12.12. I²C Connections

Extend header	LFMXO5-100T Bank	LFMXO5-100T Ball Location for JTAG	Net Name	Bridge Resistor to SCL0/SDA0
Versa Header (J9)	1	B20	EXPCON_IO13	R35 (DNI)
		G16	EXPCON_IO15	R37 (DNI)
Aardvark Header (J7)	6	M7	AK_SCL	R60 (DNI)
		M9	AK_SDA	R59 (DNI)
Arduino Header (J2)	6	N5	AR_SCL	R45 (DNI)
		N6	AR_SDA	R44 (DNI)
Raspberry Pi Header (J6)	7	E1	RASP_ID_SC	R85 (DNI)
		D1	RASP_ID_SD	R87 (DNI)
Raspberry Pi Header (J6)	7	F6	RASP_IO03	R96 (DNI)
		E8	RASP_IO02	R84 (DNI)

12.8. ADC and Potentiometer

There are two dedicate ADC input pairs for LFMXO5-100T. This board provides multiple application options. For default population, one pair of ADC0 is used to measure the core VCC voltage drop through a 10 mΩ resistor R112. Therefore, the core VCC current is calculable, as shown in Figure 12.1. Positive input of another pair ADC1 is connected to a 10 kΩ Trimmer Potentiometers (POT1) which provides voltage variation from 0 V to selectable VCCIO4, as shown in Figure 12.2. The negative input of ADC1 is grounded through 1 kΩ resistor.

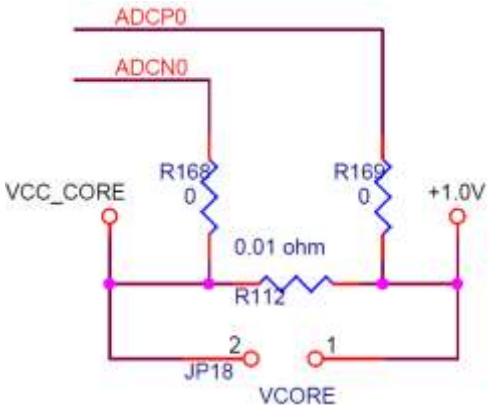

Figure 12.1. Circuit Design for ADC0

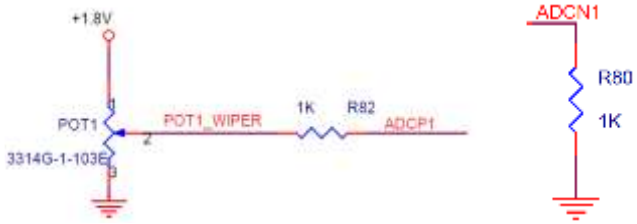

Figure 12.2. Circuit Design for ADC1

Rotate the Trimmer clockwise to decrease the voltage, as shown in Figure 12.3. To increase the voltage to ADCP1, rotate the POT counter-clockwise.

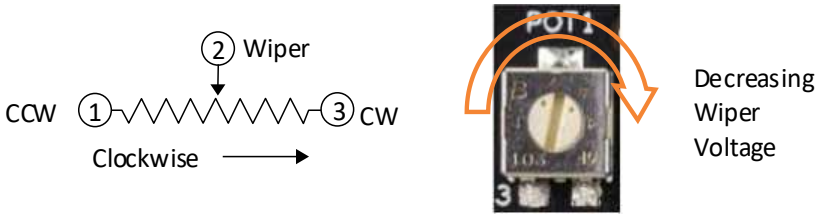

Figure 12.3. Trimmer Wiper Description

13. LEDs and Switches

LEDs and switches of the MachXO5T-NX Development Board that can be used in demo and customer designs are described in this section.

13.1. 8-Position DIP Switch

Four LFMXO5-100T pins are connected to the four switches of SW1, as shown in the circuit design in Figure 13.1. The DIP switches are connected to logic level 0 when in the ON position, as shown in Figure 13.2.

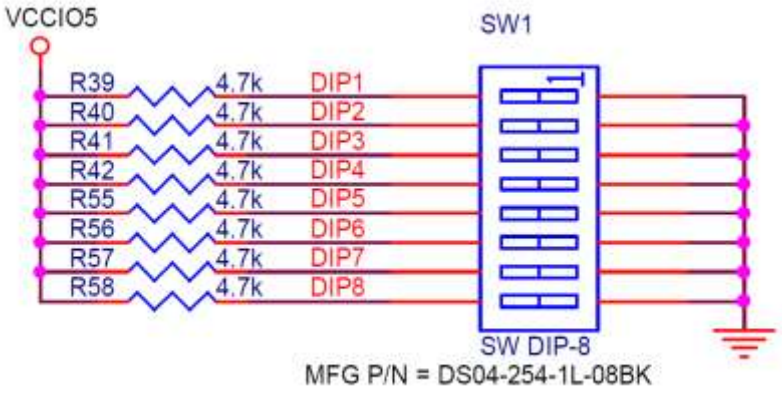

Figure 13.1. Eight-Position DIP Switch Circuits

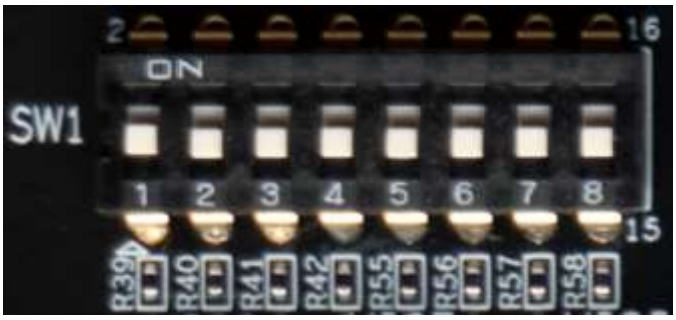

Figure 13.2. Eight-position DIP Switch

One side of each switch is connected to GPIOs within the VCCIO5 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected, as shown in Table 13.1.

Table 13.1. Four-Position DIP Switch Signals

Net Name	LFMXO5-100T Ball Location	SW1 DIP Switch Position	4.7 kΩ Pull up Resistor	Logic Input Level at ON Position
DIP1	V2	1	R39	0
DIP2	V3	2	R40	0
DIP3	W2	3	R41	0
DIP4	W3	4	R42	0
DIP5	U4	5	R55	0
DIP6	V4	6	R56	0
DIP7	T4	7	R57	0
DIP8	V5	8	R58	0

13.2. General Purpose Push Buttons

The MachXO5T-NX Development Board provides four push button switches, SW2, SW3, SW4 and SW5, for demos and user applications. Pressing these buttons drives a logic level *0* to the corresponding I/O pins.

Table 13.2. Push Button Switch Signals

Push Button Number	Reference name	LFMXO5-100T Ball Location	Shared function	Check Conditions
PB1	SW2	K6	PCIE Reset	JP10
PB2	SW3	—	PHY devices Reset	JP3, JP5
PB3	SW4	D19	ASC Reset	JP4
PB4	SW5	G10	PROGRAMN	—

SW2 is designed for general-purpose applications. At the same time, SW2 can be used to trigger PCIE reset by adding JP10 jumper. SW3 can be used to trigger the reset sequency of SGMII PHY devices after adding JP3 and JP5 jumpers. SW4 can be used as ASC global reset push button when JP4 is set to connect with EXPCON_IO20, which is connected to MANDATORY_RESET signal when mated with Lattice ASC Bridge Board. Refer to ASC Bridge Board Evaluation Board User Guide (FPGA-EB-02025) for detailed information with ASC application. SW5 can be used as PROGRAMN push button to trigger the configuration process without power cycle. For detailed information on PROGRAMN, refer to MachXO5 Programming and Configuration User Guide (FPGA-TN-02271).

13.3. General Purpose LEDs

The MachXO5T-NX Development Board provides eight red LEDs that are connected to general purpose I/O. The LEDs are lighted when the output is driven LOW. Table 13.3 lists the red LEDs and their associated pins.

Table 13.3. LED Signals

Red LEDs Ref Name	Net Name	LFMXO5-100T Ball Location
D1	XLED0	G11
D2	XLED1	G15
D3	XLED2	G12
D4	XLED3	H12
D5	XLED4	L14
D6	XLED5	L15
D7	XLED6	M20
D8	XLED7	M19

14. Software Requirements

The following software are required to develop designs for the MachXO5T-NX Development Board:

- Radiant 2022.1.1 (or later version)
- Radiant Programmer 2022.1.1 (or later version)

15. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the MachXO5T-NX Development Board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

16. Ordering Information

Table 16.1 Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO5T-NX Development Board	LFMXO5-100T-EVN	

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Appendix A. MachXO5T-NX Development Board Schematics

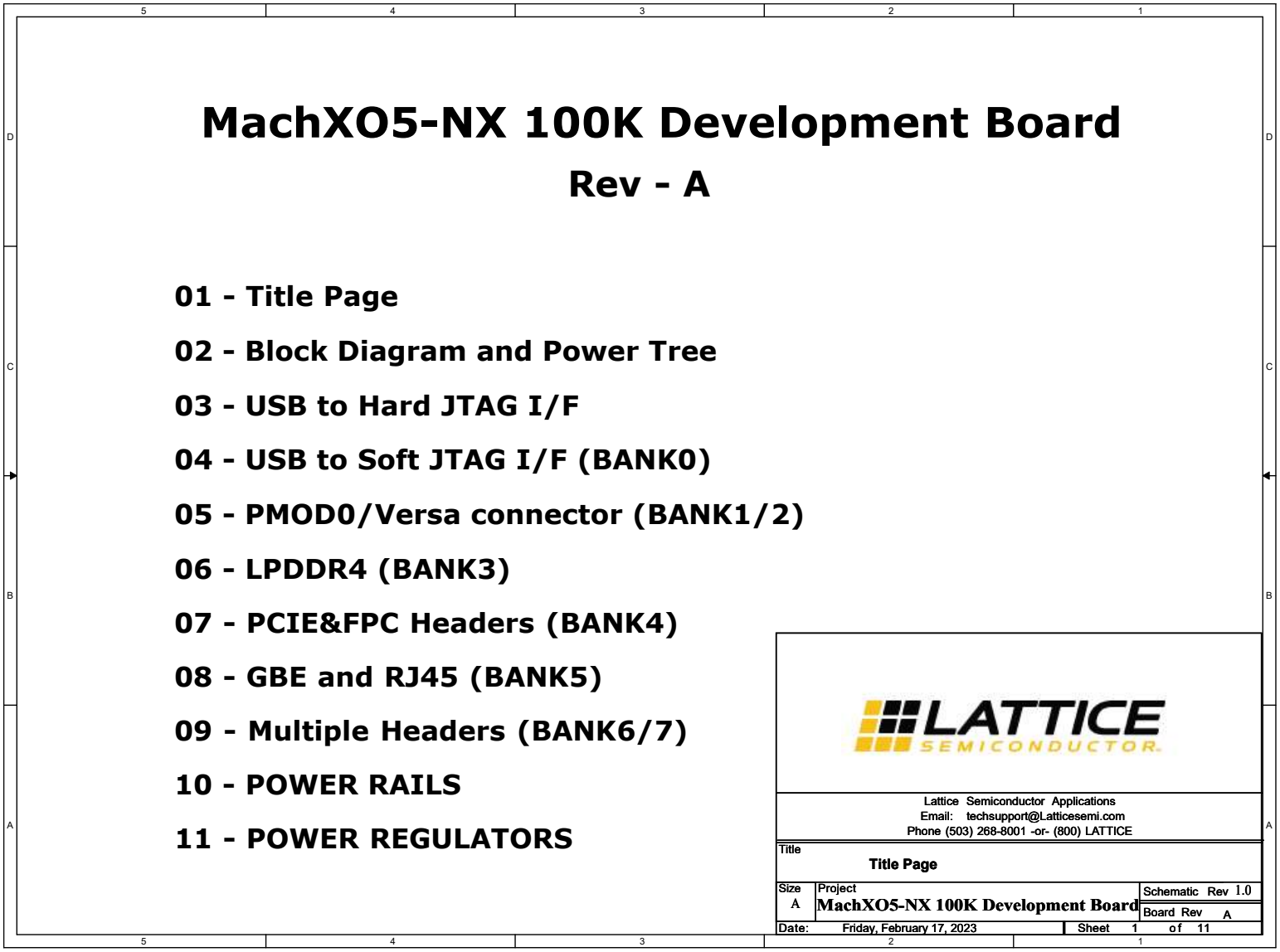

Figure A. 1. Title Page

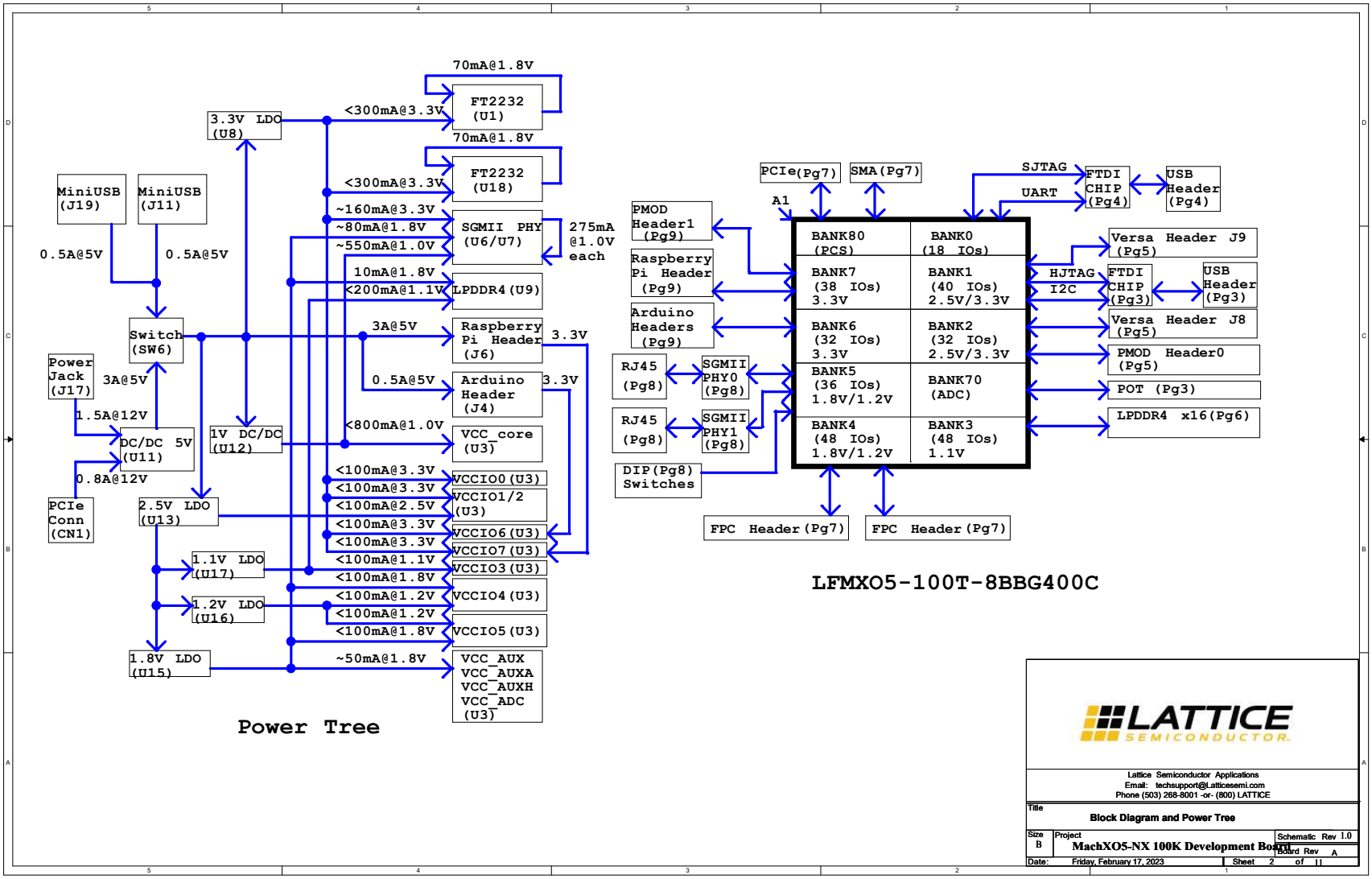

Figure A. 2. Block Diagram and Power Tree

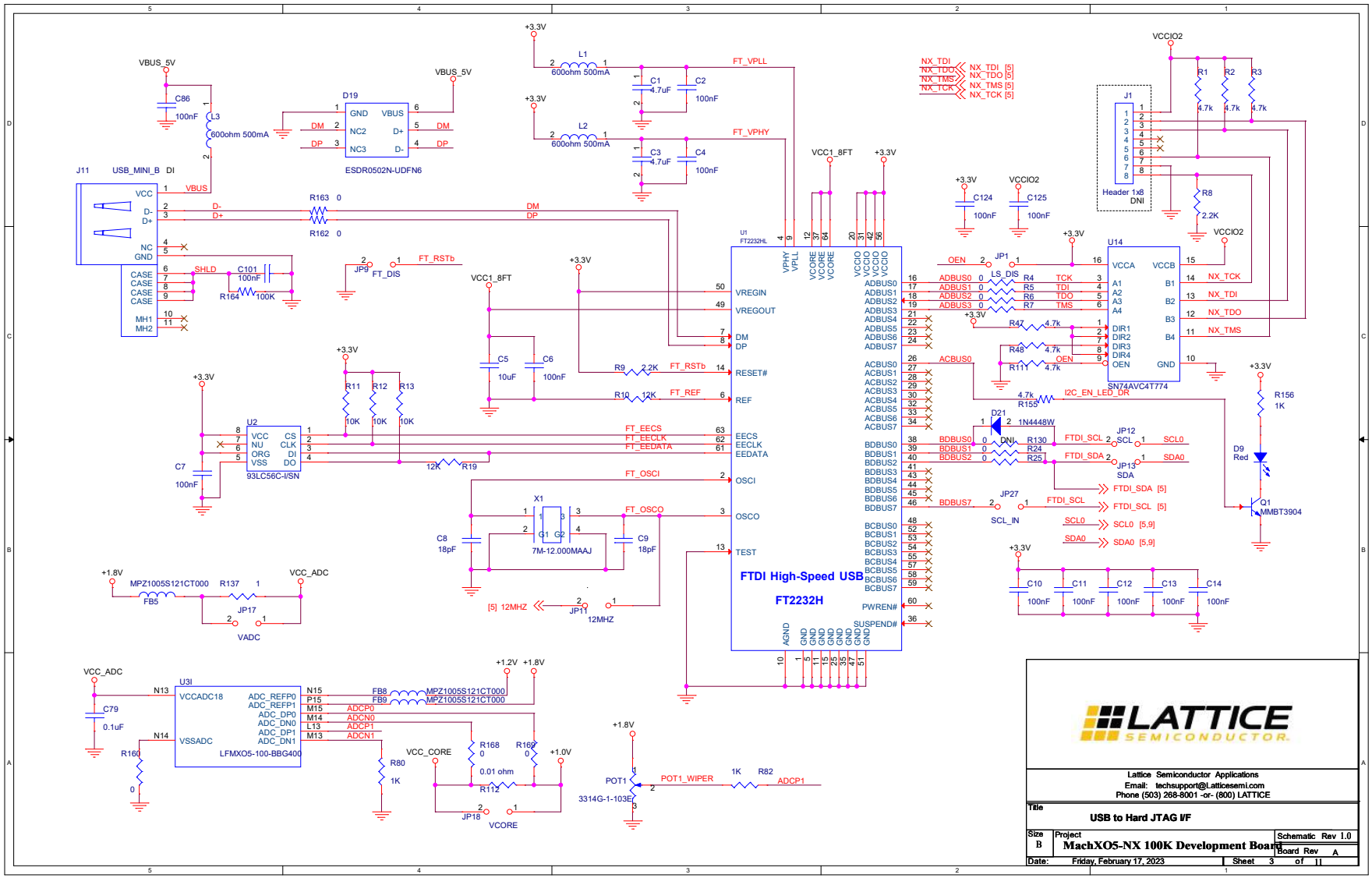

Figure A. 3. USB to Hard JTAG I/F

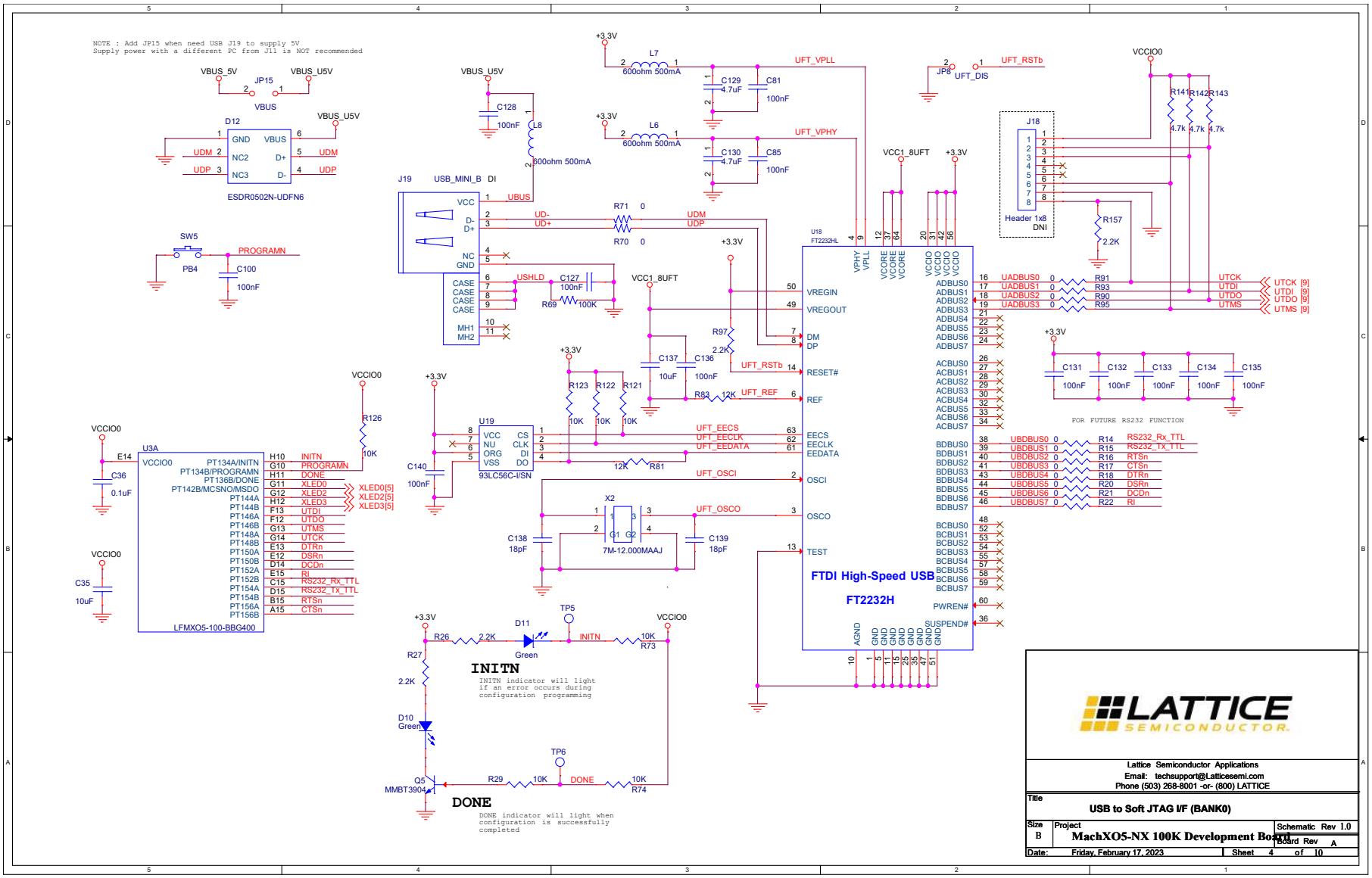

Figure A. 4. USB to Soft JTAG I/F (BANK0)

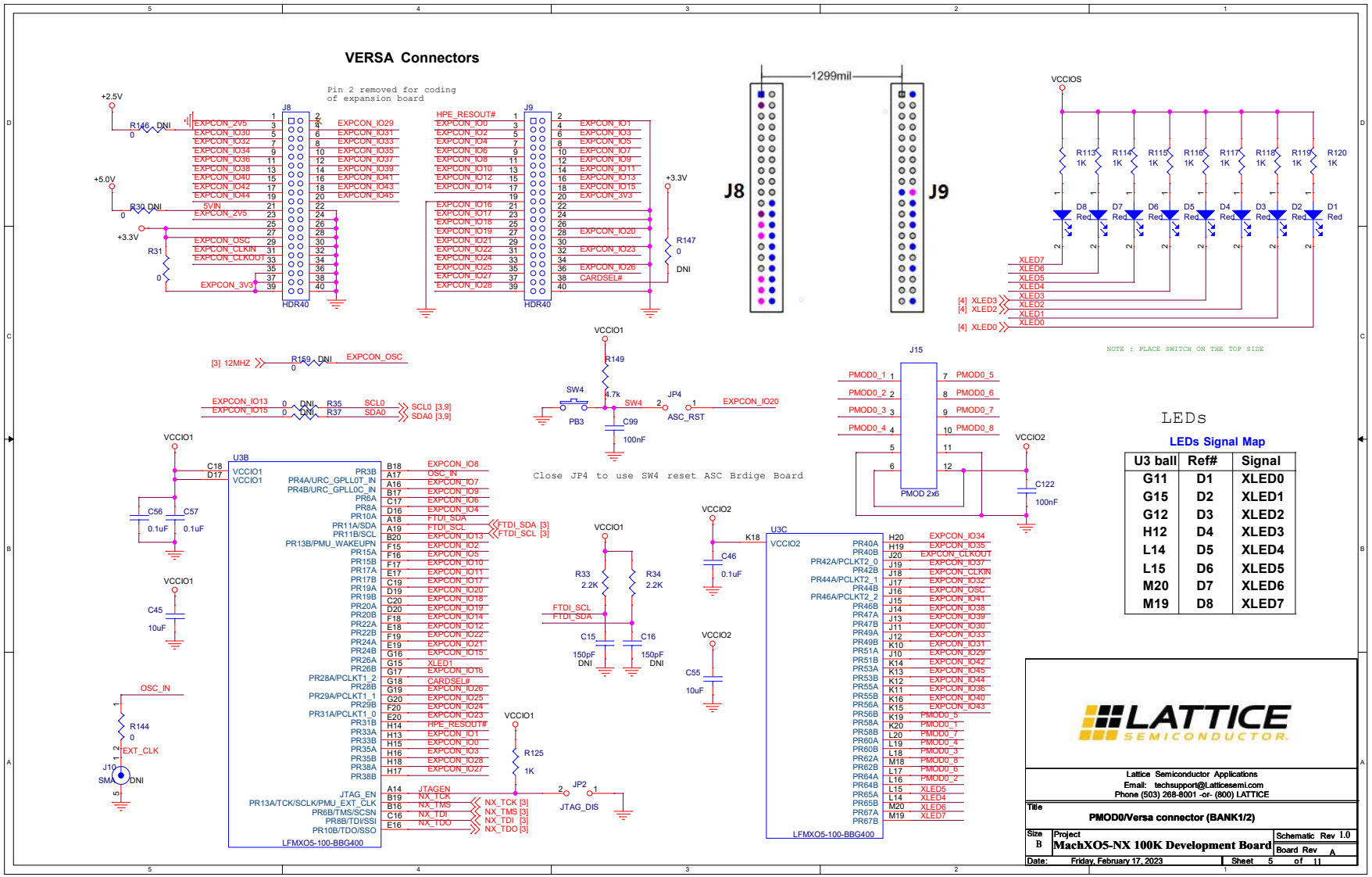

Figure A. 5. PMOD0/Versa Connector (BANK1/2)

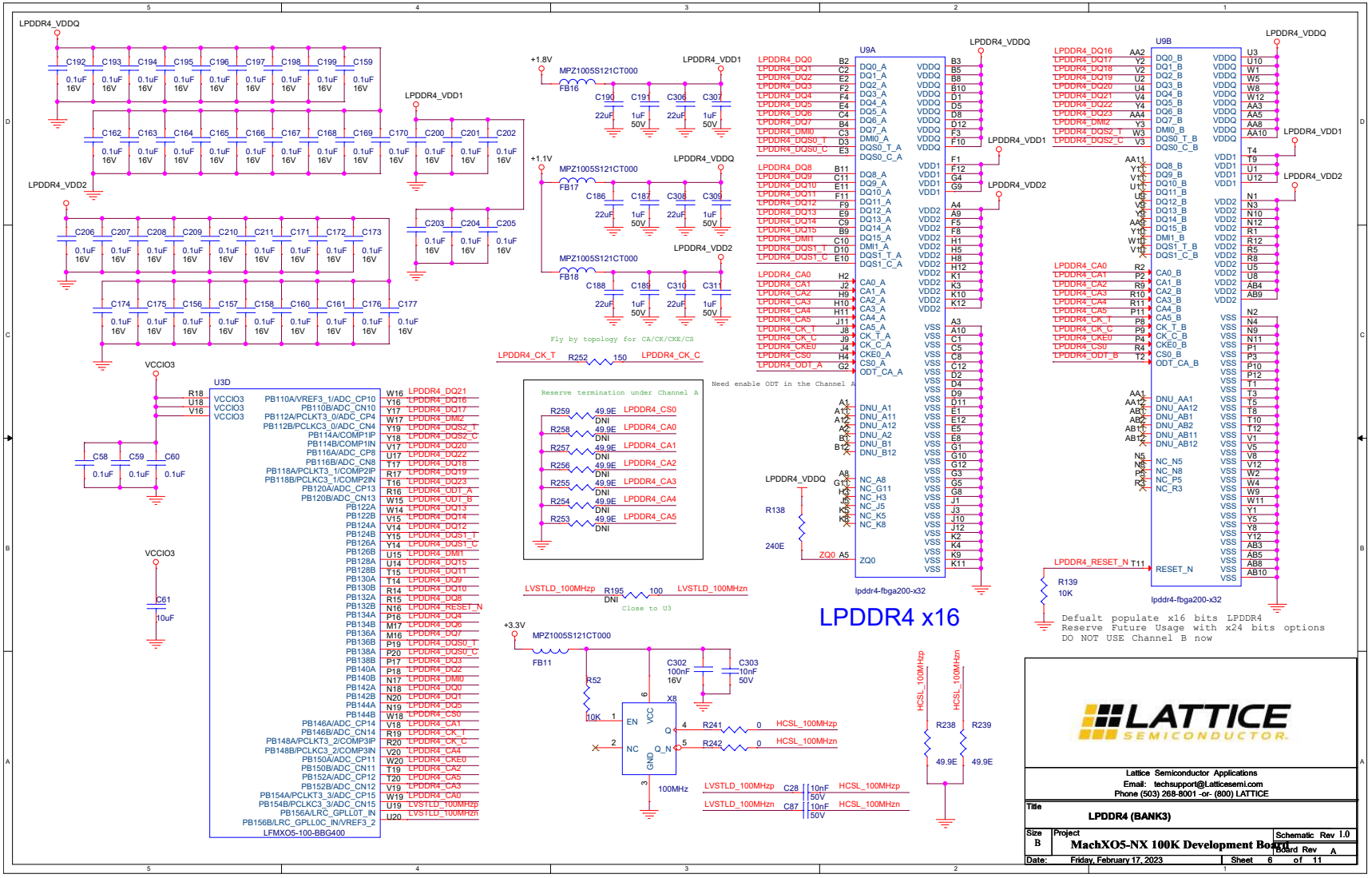

Figure A. 6. LPDDR4 (BANK3)

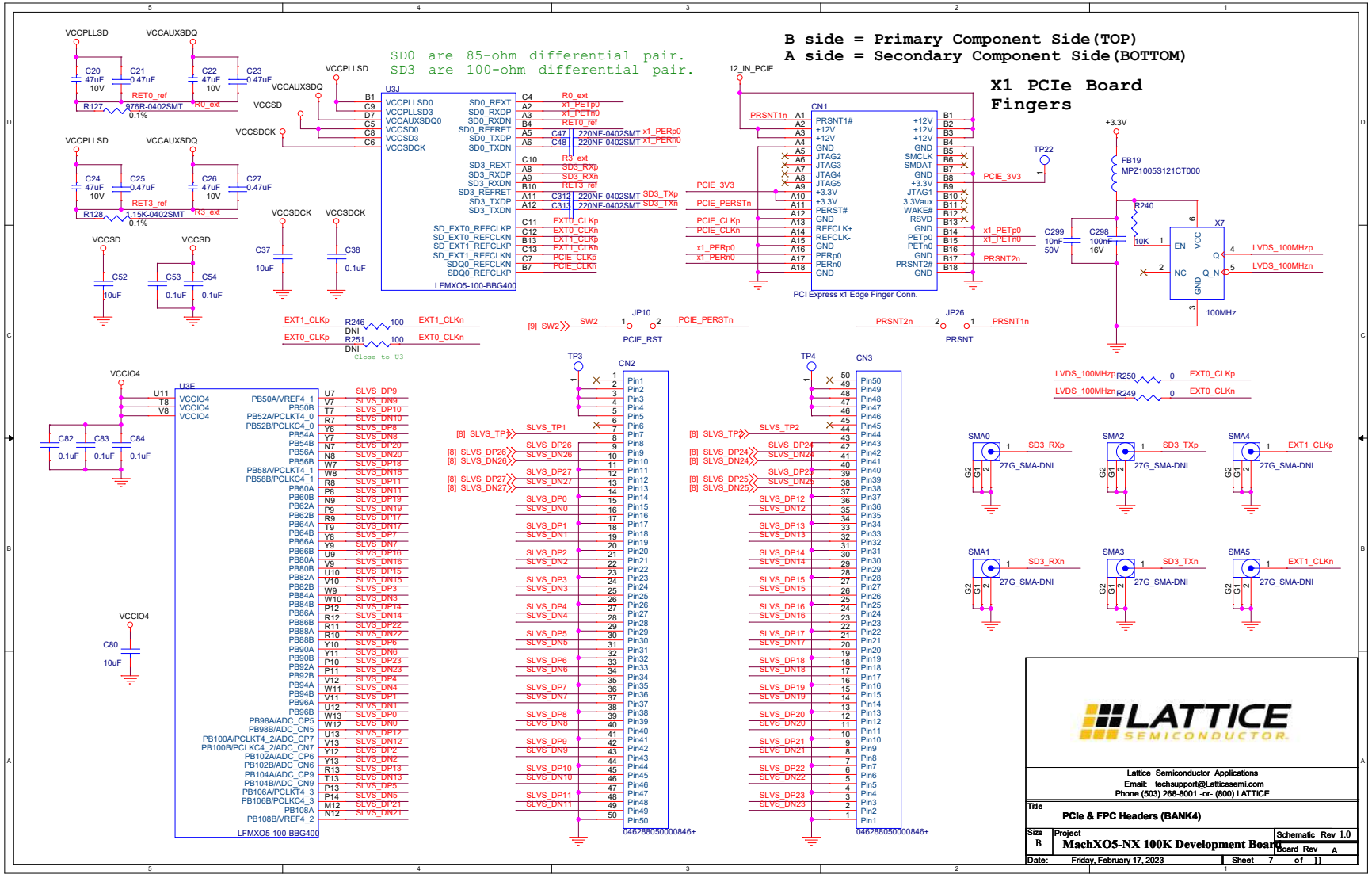

Figure A. 7. PCIE&FPC Headers (BANK4)

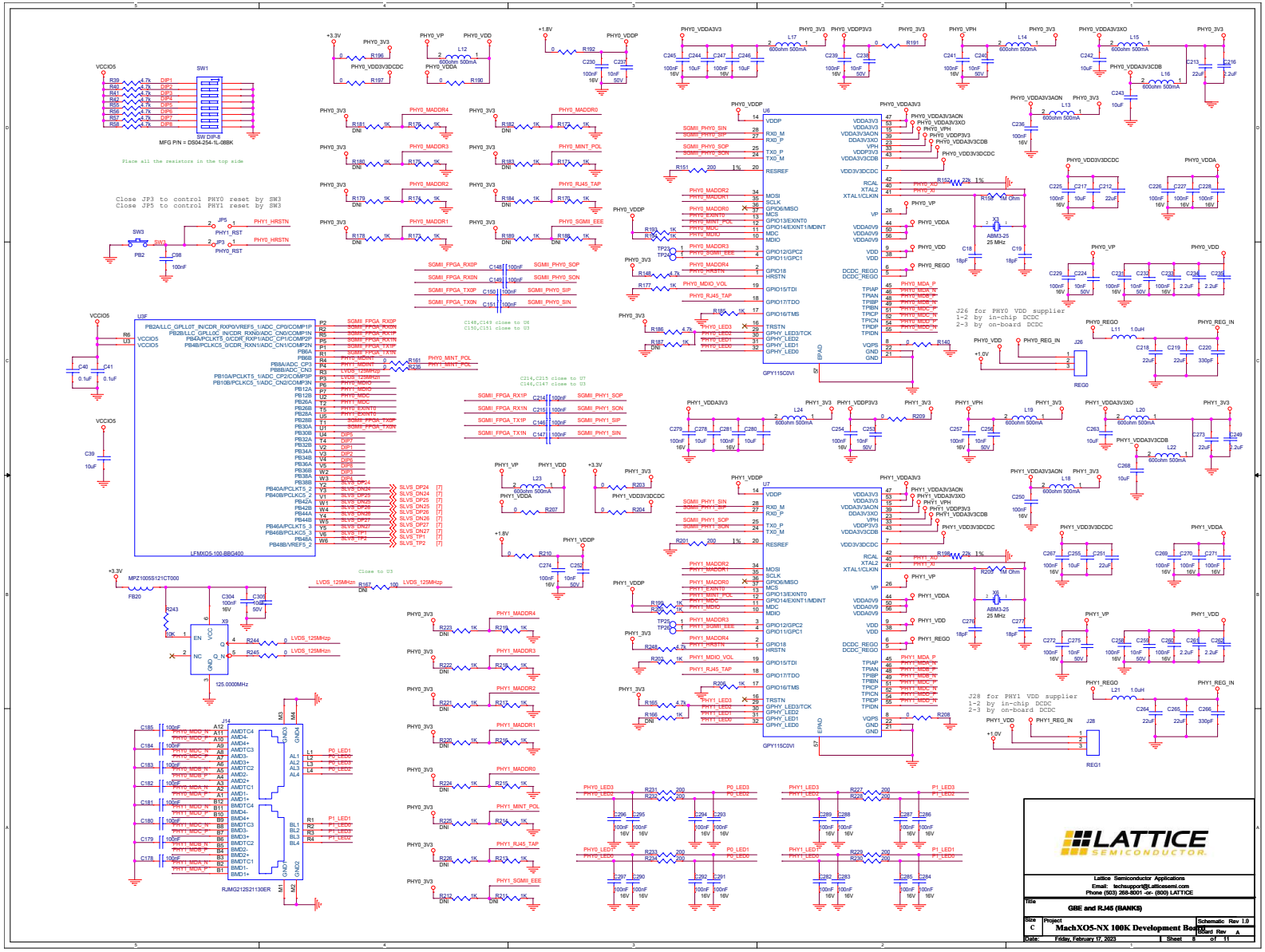

Figure A. 8. GBE and RJ45 (BANK5)

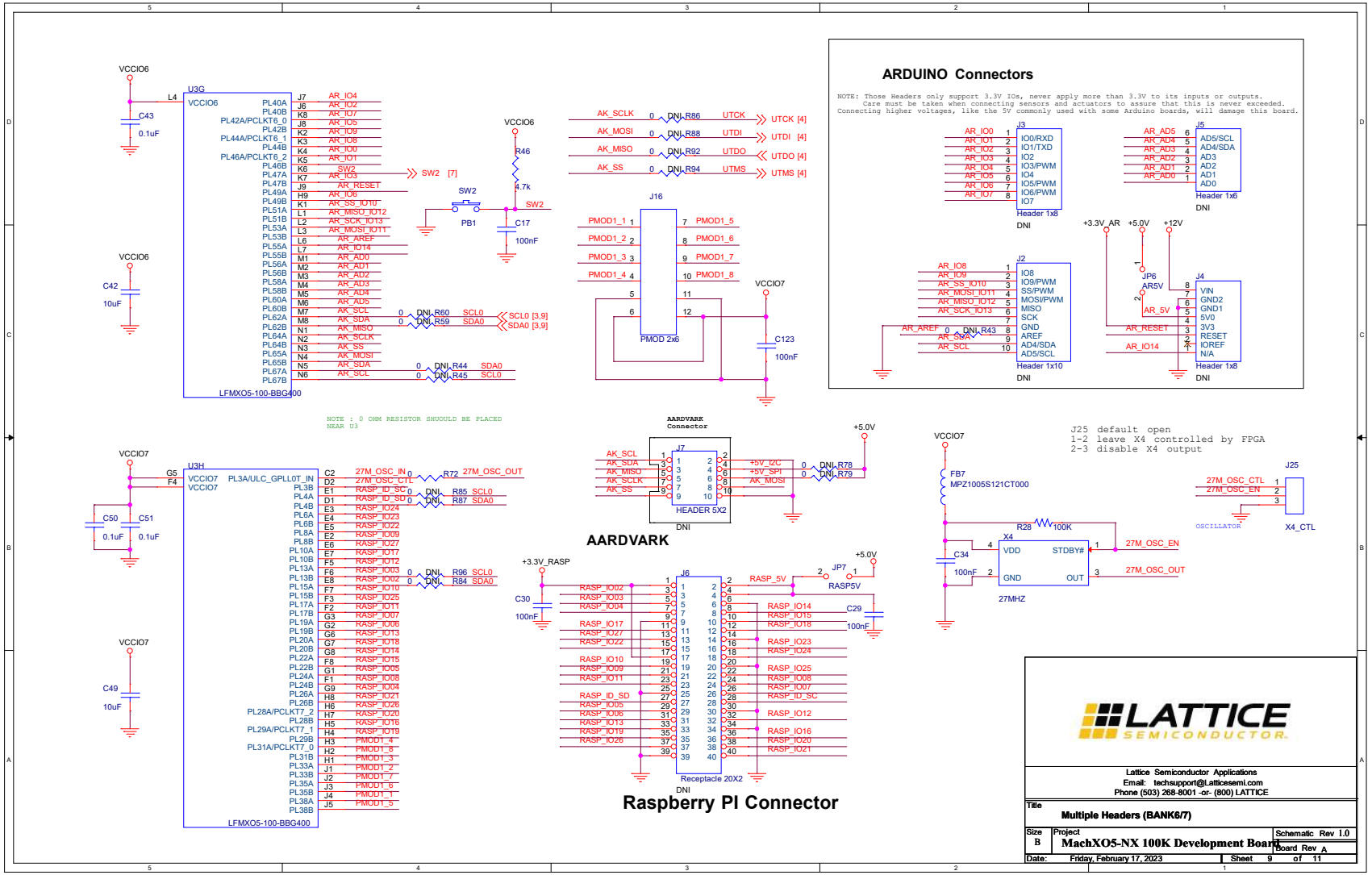

Figure A. 9. Multiple Headers (BANK6/7)

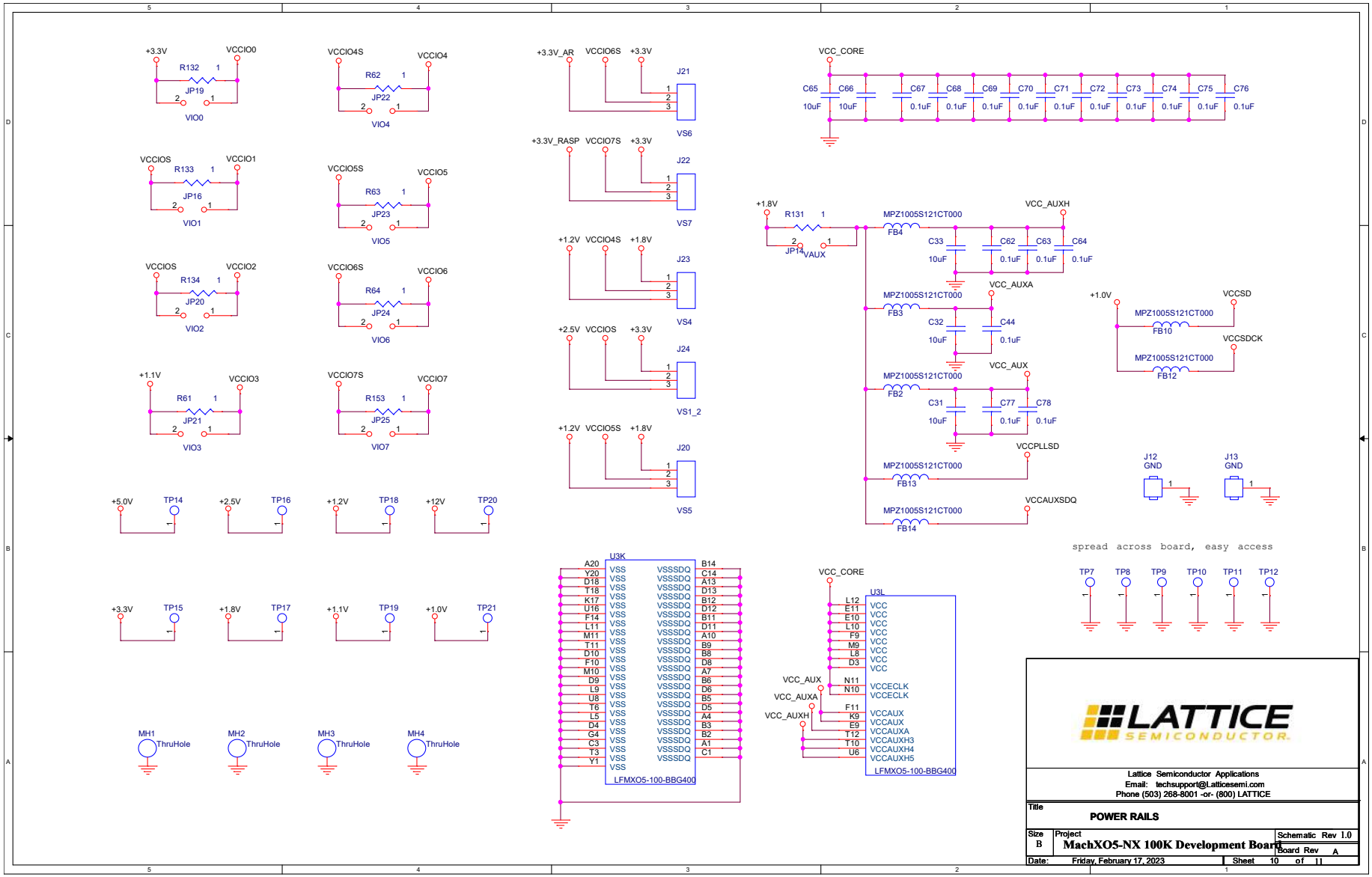

Figure A. 10. Power Rails

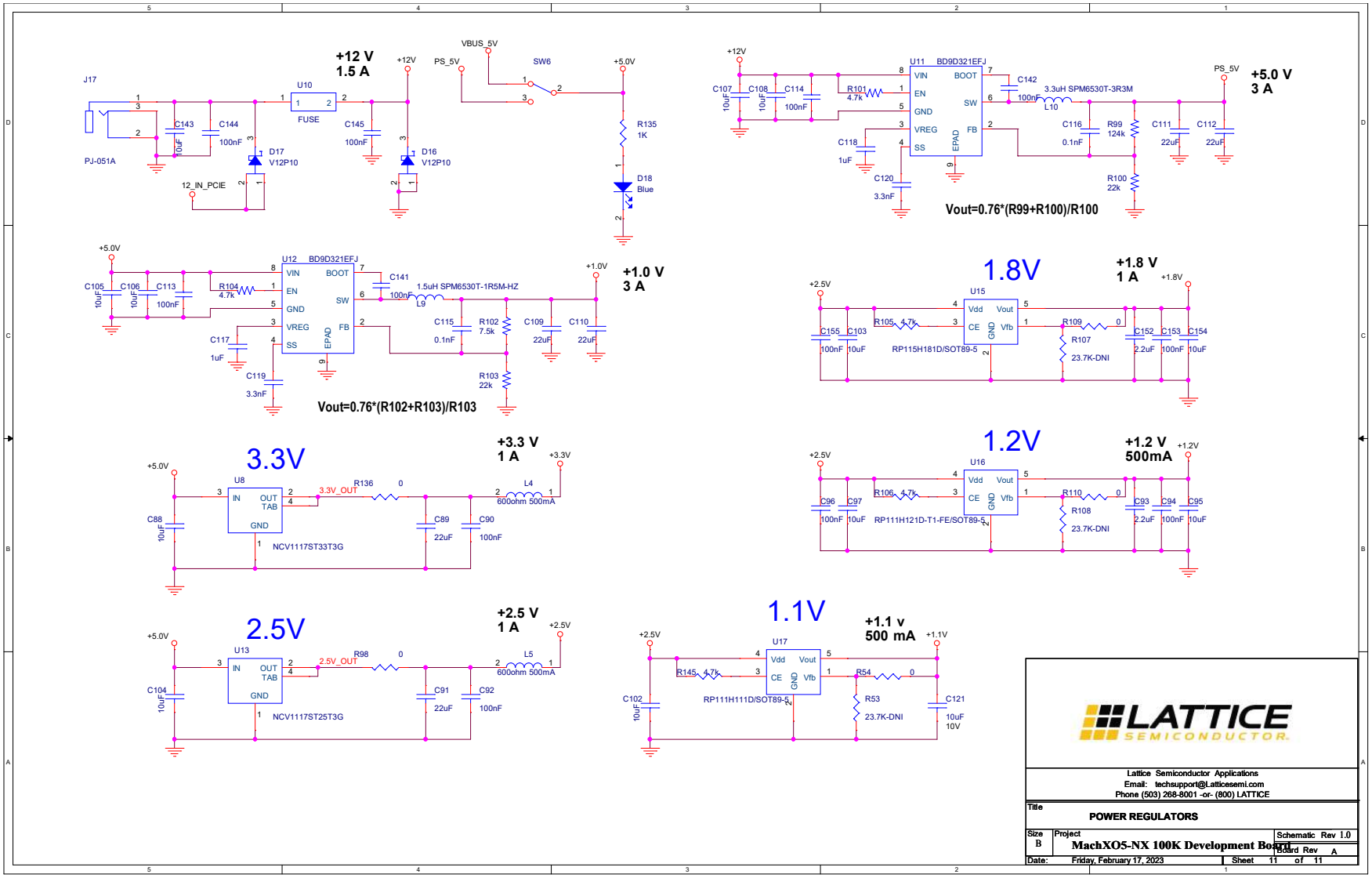

Figure A. 11. Power Regulators

Appendix B. MachXO5T-NX Development Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
1	CN1	1	—	PCIE-X1	—	—	PCIE edge connector	—
2	CN2,CN3	2	046288050000846+	04628805000084 6plus	046288050000846+	KYOCERA AVX	CONN FFC BOTTOM 50POS 0.50MM R/A	—
3	C1,C3,C129,C130	4	4.7uF	C0603	885012106005	Wurth	CAP CER 4.7UF 6.3V X5R 0603	—
4	C2,C4,C6,C7,C10,C11,C12, C13,C14,C17,C29,C30,C34, C81,C85,C86,C90,C92,C94, C96,C98,C99,C100,C101, C113,C114,C122,C123,C124, C125,C127,C128,C131,C132, C133,C134,C135,C136,C140, C141,C142,C144,C145,C146, C147,C148,C149,C150,C151, C153,C155,C178,C179,C180, C181,C182,C183,C184,C185, C214,C215,C225,C226,C227, C228,C229,C230,C231,C233, C236,C239,C241,C245,C247, C250,C254,C257,C258,C260, C267,C269,C270,C271,C272, C274,C279,C281,C282,C283, C284,C285,C286,C287,C288, C289,C290,C291,C292,C293, C294,C295,C296,C297,C298, C302,C304	106	100nF	C0402	GRM155R71H104KE14D	Murata	CAP CER 0.1UF 50V X7R 0402	—
5	C5,C31,C32,C33,C35,C37, C39,C42,C45,C49,C52,C55, C61,C65,C66,C80,C95,C97, C103,C121,C137,C154,C217, C242,C243,C244,C246,C255, C263,C268,C278,C280	32	10uF	C0603	0603ZD106KAT2A	KYOCERA AVX	CAP CER 10UF 10V X5R 0603	—
6	C8,C9,C18,C19,C138,C139, C276,C277	8	18pF	C0402	C0402C180K3GACTU	KEMET	CAP CER 18PF 25V NP0 0402	—
7	C15,C16	2	150pF	C0402	—	—	—	DNI
8	C20,C22,C24,C26	4	47uF	C0603	GRM188R60J476ME15D	Murata	CAP CER 47UF 6.3V X5R 0603	—
9	C21,C23,C25,C27	4	0.47uF	C0402	EMK105ABJ474KVHF	Taiyo Yuden	CAP CER 0.47UF 25V 10% X5R 0402	—
10	C28,C87,C224,C232,C237, C238,C240,C252,C253,C256, C259,C275,C299,C303,C305	15	10nF	C0402	GRT155R71E103KE01J	Murata	CAP CER 10000PF 25V X7R 0402	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
11	C36,C38,C40,C41,C43,C44, C46,C50,C51,C53,C54,C56, C57,C58,C59,C60,C62,C63, C64,C67,C68,C69,C70,C71, C72,C73,C74,C75,C76,C77, C78,C79,C82,C83,C84,C156, C157,C158,C159,C160,C161, C162,C163,C164,C165,C166, C167,C168,C169,C170,C171, C172,C173,C174,C175,C176, C177,C192,C193,C194,C195, C196,C197,C198,C199,C200, C201,C202,C203,C204,C205, C206,C207,C208,C209,C210, C211	77	0.1uF	C0201	CC0201KRX5R8BB104	YAGEO	CAP CER 0.1UF 25V X5R 0201	—
12	C47,C48,C312,C313	4	220NF-0402SMT	C0402	GCM155R71C224KE02D	Murata	CAP CER 0.22UF 16V X7R 0402	—
13	C88,C102,C104,C105,C106, C107,C108,C143	8	10uF	C1206	CL31B106KBHNNNE	Samsung	CAP CER 10UF 50V X7R 1206	—
14	C89,C91,C109,C110,C111, C112,C186,C188,C190,C212, C213,C218,C219,C251,C264, C265,C273,C306,C308,C310	20	22uF	C0603	CL10A226MO7JZNC	Samsung	CAP CER 22UF 16V X5R 0603	—
15	C93,C152,C216,C234,C235, C249,C261,C262	8	2.2uF	C0805	CL21B225KPFNNNE	Samsung	CAP CER 2.2UF 10V X7R 0805	—
16	C115,C116	2	0.1nF	C0603	CC0603JRNPO9BN101	YAGEO	CAP CER 100PF 50V C0G/NPO 0603	—
17	C117,C118,C187,C189,C191, C307,C309,C311	8	1uF	C0603	CL10A105KO8NNNC	Samsung	CAP CER 1UF 16V X5R 0603	—
18	C119,C120	2	3.3nF	C0201	GRM033R71A332JA01D	Murata	CAP CER 3300PF 10V X7R 0201	—
19	C220,C266	2	330pF	C0402	GCM155R71H331KA37D	Murata	CAP CER 330PF 50V X7R 0402	—
20	D1,D2,D3,D4,D5,D6,D7,D8, D9	9	Red	led_0603	LTST-C190KRKT	LITE-On INC	LED RED CLEAR 0603 SMD	—
21	D10,D11	2	Green	led_0603	LTST-C190KGKT	LITE-On INC	LED GREEN CLEAR CHIP SMD	—
22	D12,D19	2	ESDR0502N-UDFN6	UDFN6_040	ESDR0502NMUTBG	ON semi	TVS DIODE 5.5VWM 6UDFN	—
23	D16,D17	2	V12P10	V12P10	V12P10-M3/87A	Vishay	DIODE SCHOTTKY 12A 100V SMPC TO-277A	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
24	D18	1	Blue	led_0603	LTST-C190TBKT	LITE-On INC	LED 468NM BLUE CLEAR 0603 SMD	—
25	D21	1	1N4448W	1N4448W	1N4448WT	Onsemi	DIODE GEN PURP 75V 200MA SOD523F	—
26	FB2,FB3,FB4,FB5,FB7,FB8,FB9,FB10,FB11,FB12,FB13,FB14,FB16,FB17,FB18,FB19,FB20	17	MPZ1005S121CT000	MPZ1005S121CT000	MPZ1005S121CT000	TDK	FERRITE BEAD 120 OHM 0402 1LN	—
27	JP1,JP2,JP3,JP4,JP5,JP6,JP7,JP8,JP9,JP10,JP11,JP12,JP13,JP14,JP15,JP16,JP17,JP18,JP19,JP20,JP21,JP22,JP23,JP24,JP25,JP26,JP27	27	JUMPER	Header_1x2	861400021YO2LF	Amphenol	CONN HEADER VERT 2POS 2.54MM	—
28	J1,J18	2	Header 1x8	hdr_amp_87220_8_1x8_100	22284081	Molex	CONN HEADER 8POS .100 VERT TIN	DNI
29	J2	1	Header 1x10	CONF1X10-254P_2612X240X850H_TH	10129378-910002BLF	Amphenol	CONN HEADER VERT 10POS 2.54MM	DNI
30	J3,J4	2	Header 1x8	CONF1X8-254P_2104X240X850H_TH	10129378-908002BLF	Amphenol	CONN HEADER VERT 8POS 2.54MM	DNI
31	J5	1	Header 1x6	CONF1X6-254P_1596X240X850H_TH	10129378-906002BLF	Amphenol	CONN HEADER VERT 6POS 2.54MM	DNI
32	J6	1	Receptacle 20X2	HDR254-2X20_socket	PPTC202LFBN-RC	Sullins	CONN HEADER FEM 40POS .1" DL TIN	DNI
33	J7	1	HEADER 5X2	HDR254-2X5_SHROUDED	30310-6002HB	3M	CONN HEADER 10POS DL STR GOLD	DNI
34	J8,J9	2	HDR40	HDR-20x2	PRPC020DFBN-RC	Sullins	CONN HEADER VERT 40POS 2.54MM	—
35	J10	1	SMA	bnc5-100-280t	5-1814832-1	TE Connectivity	CONN SMA JACK STR 50 OHM PCB	DNI
36	J11,J19	1	USB_MINI_B	usb2-0-rec-240-0001-9	UX60-MB-5ST	Hirose	CONN RECEPT MINI USB2.0 5POS	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
37	J12,J13	2	GND	TUR_TH	1573-2	Keystone Electronics	TERMINAL TURRET DBL .082"L	—
38	J14	1	RJMG212S21130ER	"RJMG212S2XX30XR	"	RJMG212S21130ER	Amphenol	—
39	J15,J16	2	PMOD 2x6	PPPC062LJBN-RC	PPPC062LJBN-RC	Sullins	CONN HDR 12POS 0.1 GOLD PCB R/A	—
40	J17	1	PJ-051A	PJ_051A	PJ-051A	CUI Device	CONN PWR JACK 2X5.5MM SOLDER	—
41	J20,J21,J22,J23,J24,J25,J26, J28	8	HDR1X3	HDR1X3	PRPC003SAAN-RC	Sullins	CONN HEADER VERT 3POS 2.54MM	—
42	L1,L2,L3,L4,L5,L6,L7,L8,L12, L13,L14,L15,L16,L17,L18,L19, L20,L22,L23,L24	20	600ohm 500mA	fb0603	BLM18KG601SN1D	Murata	FERRITE BEAD 600 OHM 0603 1LN	—
43	L9	1	SPM6530T-1R5M	SPM6530T-2R2M	SPM6530T-1R5M	TDK	FIXED IND 1.5UH 11A 10.67MOHM SM	—
44	L10	1	SPM6530T-3R3M	SPM6530T-2R2M	SPM6530T-3R3M	TDK	FIXED IND 3.3UH 6.8A 29.7MOHM SM	—
45	L11,L21	2	1.0uH	SRP3020TA	SRP3020TA-1R0M	Bourns Inc.	FIXED IND 1UH 4A 38 MOHM SMD	—
46	POT1	1	3314G-1-103E	sot23-3314G-1	3314G-1-103E	Bourns Inc.	TRIMMER 10K OHM 0.25W SMD	—
47	Q1,Q5	2	2N3904	MMBT3904	MMBT3904-7-F	Diodes	TRANS NPN 40V 0.2A SOT-23	—
48	R1,R2,R3,R39,R40,R41,R42, R46,R47,R48,R55,R56,R57, R58,R101,R104,R105,R106, R111,R141,R142,R143,R145, R148,R149,R155,R165,R186, R248	29	4.7k	R0402	RT0402FRE074K7L	yageo	RES SMD 4.7K OHM 1% 1/16W 0402	—
49	R4,R5,R6,R7,R14,R15,R16,R17,R18,R20,R21,R22,R24,R25, R31,R90,R91,R93,R95,R98, R136,R140,R160,R161,R168, R169,R190,R191,R192,R196, R197,R203,R204,R207,R208, R209,R210,R235	38	0	R0603	RC0603FR-070RL	yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
50	R8,R9,R26,R27,R33,R34,R97, R157	8	2.2k	R0402	RC0402FR -072K2L	yageo	RES 2.2K OHM 1% 1/16W 0402	—
51	R10,R19,R81,R83	4	12K	R0603	RC0603FR -0712KL	yageo	RES 12K OHM 1/10W 1% 0603 SMD	—
52	R11,R12,R13,R29,R52,R73, R74,R121,R122,R123,R126, R139,R240,R243	14	10K	R0402	RT0402FR E0710KL	yageo	RES SMD 10K OHM 1% 1/16W 0402	—
53	R28,R69,R164	3	100K	R0402	AC0402FR -7W100KL	yageo	RES 100 KOHM 1% 1/8W 0402	—
54	R30,R35,R37,R43,R44,R45, R59,R60,R78,R79,R84,R85, R86,R87,R88,R92,R94,R96, R130,R146,R147,R159	22	0	R0603	—	—	—	DNI
55	R53,R107,R108	3	23.7K-DNI	R0603	—	—	—	DNI
56	R54,R70,R71,R72,R109,R110 ,R144,R162,R163,R241,R242 ,R244,R245,R249,R250	15	0	R0402	AC0402JR -070RL	yageo	RES SMD 0 OHM JUMPER 1/16W 0402	—
57	R61,R62,R63,R64,R131,R132 ,R133,R134,R137,R153	10	1	R0603	RT0603DR E071RL	yageo	RES 1 OHM 0.5% 1/10W 0603	—
58	R80,R82,R113,R114,R115, R116,R117,R118,R119,R120, R125,R135,R156,R170,R171, R172,R173,R174,R175,R176, R177,R185,R193,R194,R199, R200,R202,R206,R213,R214, R215,R216,R217,R218,R219	35	1k	R0402	AF0402FR -071KL	yageo	RES SMD 1K OHM 1% 1/16W 0402	—
59	R99	1	124K	R0603	RT0603DR D07124KL	yageo	RES SMD 124K OHM 0.5% 1/10W 0603	—
60	R100,R103,R152,R198	4	22K	R0402	AC0402FR -0722KL	yageo	RES SMD 22K OHM 1% 1/16W 0402	—
61	R102	1	7.5k	R0603	RT0603DR D077K5L	yageo	RES SMD 7.5K OHM 0.5% 1/10W 0603	—
62	R112	1	10mOhms	R0603	WSL0603 R0100FEA	Vishay	RES 0.01 OHM 1% 1/10W 0603	—
63	R127	1	976R-0402SMT	R0402	RT0402BR D07976RL	Yageo	RES SMD 976 OHM 0.1% 1/16W 0402	—
64	R128	1	1.15K-0402SMT	R0402	RT0402BR D071K15L	Yageo	RES SMD 1.15K OHM 0.1% 1/16W 0402	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
65	R138	1	240E	R0402	RC0402FR-07240RL	Yageo	RES SMD 240 OHM 1% 1/16W 0402	—
66	R151,R201,R227,R228,R229,R230,R231,R232,R233,R234	10	200	R0603	RC0603FR-13200RL	Yageo	RES 200 OHM 1% 1/10W 0603	—
67	R158,R205	2	1M Ohm	R0402	AC0402FR-071ML	Yageo	RES SMD 1M OHM 1% 1/16W 0402	—
68	R166,R178,R179,R180,R181,R182,R183,R184,R187,R188,R189,R211,R212,R220,R221,R222,R223,R224,R225,R226	20	1k	R0402	—	—	—	DNI
69	R167,R195,R246,R251	4	100	R0402	—	—	—	DNI
70	R238,R239	2	49.9E	R0402	RC0402FR-0749R9L	Yageo	RES SMD 49.9 OHM 1% 1/16W 0402	—
71	R252	1	150	R0201	RC0201FR-07150RL	Yageo	RES 150 OHM 1% 1/20W 0201	—
72	R253,R254,R255,R256,R257,R258,R259	7	49.9E	R0201	—	—	—	DNI
73	SMA0,SMA1,SMA2,SMA3	4	27G_SMA-DNI	SV_SF2921-61345-2S	SF2921-61345-2S	Amphenol	CONN SMA JACK STR 50 OHM SMD	DNI
74	SMA4,SMA5	2	27G_SMA-DNI	SV_SF2921-61356-2S	SF2921-61356-2S	Amphenol	CONN SMA JACK STR 50 OHM SMD	DNI
75	SW1	1	SW DIP-8	DIP_254-8	DS04-254-1L-08BK	CUI device	DIP SWITCH, SPST, 2.54 PITCH, RA	—
76	SW2,SW3,SW4,SW5	4	SYS_RST	sw_sp_st_eswitch_tl1015	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V	—
77	SW6	1	1101M2S2CQE2	SWITCH_3P-6A	1101M2S2CQE2	C&K	Slide Switches	—
78	TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26	23	T POINT R	TP	TP	—	—	DNI
79	U1,U18	2	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	FT2232HL-TRAY	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP	—
80	U2,U19	2	93LC56C-I/SN	so8_50_244	93LC56C-I/SN	Microchip	IC EEPROM 2KBIT 3MHZ 8SOIC	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
81	U3	1	JEDI_D6_Final	BGA400-080-17X17-SOCKET	LFMXO5-100-BBG400	Lattice	Target Device	—
82	U6,U7	2	GPY115C0VI	56VQFN_GPY115	GPY115C0VI	Maxlinear	IC TRANSVR IC GPY115C0VI VQFN56	—
83	U8	1	NCP1117	sot223_4p	NCP1117ST33T3G	ON semi	IC REG LDO 3.3V 1A SOT223	—
84	U9	1	lpddr4-fbga200-x16	TFBGA200	MT53E512M16D1	Micron	LPDDR4 8G 512MX16 FBGA	—
85	U10	1	FUSE	0154004DRT	0154005.DRT	Littelfuse	FUSE BRD MNT 5A 125VAC/VDC 2SMD	—
86	U11,U12	2	BD9D321EFJ	HTSOP_8_BD9D321	BD9D321EFJ-E2	Rohm	IC REG BUCK ADJ 3A 8HTSOP-J	—
87	U13	1	NCV1117ST25T3G	sot223_4p	NCV1117ST25T3G	ON semi	IC REG LINEAR 2.5V 1A SOT223-4	—
88	U14	1	SN74AVC4T774	tssop16-0p65mm	SN74AVC4T774PWR	TI	IC TRNSLTR BIDIRECTIONAL 16TSSOP	—
89	U15	1	RP115H181D/SOT89-5	SOT89-5	RP115H181D-T1-FE	Nisshinbo	IC REG LINEAR 1.8V 1A SOT89-5	—
90	U16	1	RP111H121D/SOT89-5	SOT89-5	RP111H121D-T1-FE	Nisshinbo	IC REG LINEAR 1.2V 1A SOT89-5	—
91	U17	1	RP111H111D/SOT89-5	SOT89-5	RP111H111D-T1-FE	Nisshinbo	IC REG LINEAR 1.1V 1A SOT89-5	—
92	X1,X2	2	7M-12.000MAAJ	xtal_4p_7m	7M-12.000MAAJ-T	TXC	CRYSTAL 12MHZ 18PF SMD	—
93	X3,X6	2	ABM3-25	XTAL_ABM3	ABM7-25.000MHZ-D2Y-T	Abracon LLC	CRYSTAL 25.0000MHZ 18PF SMD	—
94	X4	1	DSC1001DE2-027.0000	x4-2520	ASDAIG-27.000MHZ-C-S-T	Abracon LLC	MEMS OSC XO 27.0000MHZ CMOS SMD	—
95	X7	1	NX33A0006Z	3225-6PIN	NX33A0006Z	Diodes	XTAL OSC XO 100MHZ 3.3V LVDS	—
96	X8	1	NX34A0005Z	3225-6PIN	NX34A0005Z	Diodes	XTAL OSC XO 100MHZ 3.3V HCSL	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description	Assembly
97	X9	1	NX33C5013Z	3225-6PIN	NX33C5013Z	Diodes	XTAL OSC XO 125MHZ 3.3V LVDS	—

Appendix C. User Defined Preference File

```
// These names follow the MachXO5T-NX Development Board schematic but,
// they may be defined by the user.  Thus, they can be copied into the
// preference file and edited to match a different naming convention if
// needed or used to fill in the Spreadsheet view.

// LFMXO5-100T LED Connections
// Note: The following order matches the LED locations on the board
// from top D1 to bottom D8
ldc_set_location -site {G11} [get_ports {LED[0]}]
ldc_set_location -site {G15} [get_ports {LED[1]}]
ldc_set_location -site {G12} [get_ports {LED[2]}]
ldc_set_location -site {H12} [get_ports {LED[3]}]
ldc_set_location -site {L14} [get_ports {LED[4]}]
ldc_set_location -site {L15} [get_ports {LED[5]}]
ldc_set_location -site {M20} [get_ports {LED[6]}]
ldc_set_location -site {M19} [get_ports {LED[7]}]

//DIP Switch Connections
ldc_set_location -site {V2} [get_ports {DIPSW[0]}]
ldc_set_location -site {V3} [get_ports {DIPSW[1]}]
ldc_set_location -site {W2} [get_ports {DIPSW[2]}]
ldc_set_location -site {W3} [get_ports {DIPSW[3]}]
ldc_set_location -site {U4} [get_ports {DIPSW[4]}]
ldc_set_location -site {V4} [get_ports {DIPSW[5]}]
ldc_set_location -site {T4} [get_ports {DIPSW[6]}]
ldc_set_location -site {V5} [get_ports {DIPSW[7]}]


//Push Button Connections
ldc_set_location -site {K6} [get_ports PB1]

//add JP4 to enable PB2 control
ldc_set_location -site {B7}  [get_ports PB3]

//ldc_set_sysconfig {PROGRAMN_PORT=DISABLE}
//ldc_set_location -site {G10} [get_ports PB4]

//Clock inputs

ldc_set_location -site {C2} [get_ports clk_x4]
ldc_set_port -iobuf {IO_TYPE=LVCMOS33} [get_ports clk_x4]

ldc_set_location -site {U19} [get_ports clk_x8]
ldc_set_port -iobuf {IO_TYPE= LVSTLD_I} [get_ports clk_x8]

ldc_set_location -site {R3} [get_ports clk_x9]
ldc_set_port -iobuf {IO_TYPE=LVDS} [get_ports clk_x9]

//SLVS
ldc_set_location -site {W13} [get_ports {slvs_data[0]}]
ldc_set_location -site {V11} [get_ports {slvs_data[1]}]
ldc_set_location -site {Y12} [get_ports {slvs_data[2]}]
ldc_set_location -site {W9} [get_ports {slvs_data[3]}]
ldc_set_location -site {V12} [get_ports {slvs_data[4]}]
ldc_set_location -site {P13} [get_ports {slvs_data[5]}]
ldc_set_location -site {Y10} [get_ports {slvs_data[6]}]
```

```
ldc_set_location -site {Y8} [get_ports {slvs_data[7]}]
ldc_set_location -site {Y6} [get_ports {slvs_data[8]}]
ldc_set_location -site {U7} [get_ports {slvs_data[9]}]
ldc_set_location -site {T7} [get_ports {slvs_data[10]}]
ldc_set_location -site {R8} [get_ports {slvs_data[11]}]
ldc_set_location -site {U13} [get_ports {slvs_data[12]}]
ldc_set_location -site {R13} [get_ports {slvs_data[13]}]
ldc_set_location -site {P12} [get_ports {slvs_data[14]}]
ldc_set_location -site {U10} [get_ports {slvs_data[15]}]
ldc_set_location -site {U9} [get_ports {slvs_data[16]}]
ldc_set_location -site {R9} [get_ports {slvs_data[17]}]
ldc_set_location -site {W7} [get_ports {slvs_data[18]}]
ldc_set_location -site {N9} [get_ports {slvs_data[19]}]
ldc_set_location -site {N7} [get_ports {slvs_data[20]}]
ldc_set_location -site {M12} [get_ports {slvs_data[21]}]
ldc_set_location -site {R11} [get_ports {slvs_data[22]}]
ldc_set_location -site {P10} [get_ports {slvs_data[23]}]
ldc_set_location -site {Y2} [get_ports {slvs_data[24]}]
ldc_set_location -site {V1} [get_ports {slvs_data[25]}]
ldc_set_location -site {W4} [get_ports {slvs_data[26]}]
ldc_set_location -site {W5} [get_ports {slvs_data[27]}]

//LPDDR4

# DQS GROUP 0
ldc_set_location -site {N18} [get_ports {ddr_dq_io[0]}]
ldc_set_location -site {N20} [get_ports {ddr_dq_io[1]}]
ldc_set_location -site {P18} [get_ports {ddr_dq_io[2]}]
ldc_set_location -site {P17} [get_ports {ddr_dq_io[3]}]
ldc_set_location -site {P16} [get_ports {ddr_dq_io[4]}]
ldc_set_location -site {N19} [get_ports {ddr_dq_io[5]}]
ldc_set_location -site {M17} [get_ports {ddr_dq_io[6]}]
ldc_set_location -site {M16} [get_ports {ddr_dq_io[7]}]
ldc_set_location -site {P19} [get_ports {ddr_dqs_io[0]}]
ldc_set_location -site {N17} [get_ports {ddr_dmi_io[0]}]
# DQS GROUP 1
ldc_set_location -site {R15} [get_ports {ddr_dq_io[8]}]
ldc_set_location -site {T14} [get_ports {ddr_dq_io[9]}]
ldc_set_location -site {R14} [get_ports {ddr_dq_io[10]}]
ldc_set_location -site {T15} [get_ports {ddr_dq_io[11]}]
ldc_set_location -site {V14} [get_ports {ddr_dq_io[12]}]
ldc_set_location -site {W14} [get_ports {ddr_dq_io[13]}]
ldc_set_location -site {V15} [get_ports {ddr_dq_io[14]}]
ldc_set_location -site {U14} [get_ports {ddr_dq_io[15]}]
ldc_set_location -site {Y15} [get_ports {ddr_dqs_io[1]}]
ldc_set_location -site {U15} [get_ports {ddr_dmi_io[1]}]

ldc_set_port -iobuf {IO_TYPE=LVSTL_I TERMINATION=40} [get_ports {ddr_dmi_io[*]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I TERMINATION=40} [get_ports {ddr_dq_io[*]}]
ldc_set_port -iobuf {IO_TYPE=LVSTLD_I TERMINATION=40} [get_ports
{ddr_dqs_io[*]}]

# CK, CKE, CS, CA
ldc_set_location -site {R19} [get_ports {ddr_ck_o[0]}]
ldc_set_location -site {W20} [get_ports {ddr_cke_o[0]}]
ldc_set_location -site {W18} [get_ports {ddr_cs_o[0]}]
ldc_set_location -site {W19} [get_ports {ddr_ca_o[0]}]
ldc_set_location -site {V18} [get_ports {ddr_ca_o[1]}]
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ldc_set_location -site {T19} [get_ports {ddr_ca_o[2]}]
ldc_set_location -site {V19} [get_ports {ddr_ca_o[3]}]
ldc_set_location -site {V20} [get_ports {ddr_ca_o[4]}]
ldc_set_location -site {T20} [get_ports {ddr_ca_o[5]}]
ldc_set_location -site {R16} [get_ports ddr_odt_ca_o]
ldc_set_location -site {N16} [get_ports ddr_reset_n_o]

ldc_set_port -iobuf {IO_TYPE=LVSTLD_I} [get_ports {ddr_ck_o[0]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports {ddr_cke_o[0]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports {ddr_cs_o[0]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports {ddr_ca_o[*]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports ddr_odt_ca_o]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports ddr_reset_n_o]

//PMOD0 Connections
ldc_set_location -site {K20} [get_ports PMOD0_1]
ldc_set_location -site {L16} [get_ports PMOD0_2]
ldc_set_location -site {L18} [get_ports PMOD0_3]
ldc_set_location -site {L19} [get_ports PMOD0_4]
ldc_set_location -site {K19} [get_ports PMOD0_5]
ldc_set_location -site {L17} [get_ports PMOD0_6]
ldc_set_location -site {L20} [get_ports PMOD0_7]
ldc_set_location -site {M18} [get_ports PMOD0_8]

//PMOD1 Connections
ldc_set_location -site {J4} [get_ports PMOD1_1]
ldc_set_location -site {J1} [get_ports PMOD1_2]
ldc_set_location -site {H1} [get_ports PMOD1_3]
ldc_set_location -site {H3} [get_ports PMOD1_4]
ldc_set_location -site {J5} [get_ports PMOD1_5]
ldc_set_location -site {J3} [get_ports PMOD1_6]
ldc_set_location -site {J2} [get_ports PMOD1_7]
ldc_set_location -site {H2} [get_ports PMOD1_8]

//USER JTAG Connections
ldc_set_location -site {F13} [get_ports UTDI]
ldc_set_location -site {F12} [get_ports UTDO]
ldc_set_location -site {G13} [get_ports UTMS]
ldc_set_location -site {G14} [get_ports UTCK]


//USER RS232 Connections
ldc_set_location -site {C15} [get_ports RS232_Rx_TTL]
ldc_set_location -site {D15} [get_ports RS232_Tx_TTL]
ldc_set_location -site {B15} [get_ports RTSn]
ldc_set_location -site {A15} [get_ports CTSn]
ldc_set_location -site {E13} [get_ports DTRn]
ldc_set_location -site {E12} [get_ports DSRn]
ldc_set_location -site {D14} [get_ports DCDn]
ldc_set_location -site {E15} [get_ports RI]

//RASPBERRY PI Connections
ldc_set_location -site {E8} [get_ports RASP_IO02]
ldc_set_location -site {F6} [get_ports RASP_IO03]
ldc_set_location -site {G9} [get_ports RASP_IO04]
ldc_set_location -site {G1} [get_ports RASP_IO05]
ldc_set_location -site {G2} [get_ports RASP_IO06]
ldc_set_location -site {G3} [get_ports RASP_IO07]
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ldc_set_location -site {F1} [get_ports RASP_IO08]
ldc_set_location -site {E2} [get_ports RASP_IO09]
ldc_set_location -site {F7} [get_ports RASP_IO10]
ldc_set_location -site {F2} [get_ports RASP_IO11]
ldc_set_location -site {F5} [get_ports RASP_IO12]
ldc_set_location -site {G6} [get_ports RASP_IO13]
ldc_set_location -site {G8} [get_ports RASP_IO14]
ldc_set_location -site {F8} [get_ports RASP_IO15]
ldc_set_location -site {H5} [get_ports RASP_IO16]
ldc_set_location -site {E7} [get_ports RASP_IO17]
ldc_set_location -site {G7} [get_ports RASP_IO18]
ldc_set_location -site {H4} [get_ports RASP_IO19]
ldc_set_location -site {H7} [get_ports RASP_IO20]
ldc_set_location -site {H8} [get_ports RASP_IO21]
ldc_set_location -site {E5} [get_ports RASP_IO22]
ldc_set_location -site {E4} [get_ports RASP_IO23]
ldc_set_location -site {E3} [get_ports RASP_IO24]
ldc_set_location -site {F3} [get_ports RASP_IO25]
ldc_set_location -site {H6} [get_ports RASP_IO26]
ldc_set_location -site {E6} [get_ports RASP_IO27]
ldc_set_location -site {E1} [get_ports RASP_ID_SC]
ldc_set_location -site {D1} [get_ports RASP_ID_SD]

//VERSA HEADER Connections
ldc_set_location -site {H15} [get_ports EXPCON_IO0]
ldc_set_location -site {H13} [get_ports EXPCON_IO1]
ldc_set_location -site {F15} [get_ports EXPCON_IO2]
ldc_set_location -site {H16} [get_ports EXPCON_IO3]
ldc_set_location -site {D16} [get_ports EXPCON_IO4]
ldc_set_location -site {F16} [get_ports EXPCON_IO5]
ldc_set_location -site {C17} [get_ports EXPCON_IO6]
ldc_set_location -site {A16} [get_ports EXPCON_IO7]
ldc_set_location -site {B18} [get_ports EXPCON_IO8]
ldc_set_location -site {B17} [get_ports EXPCON_IO9]
ldc_set_location -site {F17} [get_ports EXPCON_IO10]
ldc_set_location -site {E17} [get_ports EXPCON_IO11]
ldc_set_location -site {E18} [get_ports EXPCON_IO12]
ldc_set_location -site {B20} [get_ports EXPCON_IO13]
ldc_set_location -site {F18} [get_ports EXPCON_IO14]
ldc_set_location -site {G16} [get_ports EXPCON_IO15]
ldc_set_location -site {G17} [get_ports EXPCON_IO16]
ldc_set_location -site {C19} [get_ports EXPCON_IO17]
ldc_set_location -site {C20} [get_ports EXPCON_IO18]
ldc_set_location -site {D20} [get_ports EXPCON_IO19]
ldc_set_location -site {D19} [get_ports EXPCON_IO20]
ldc_set_location -site {E19} [get_ports EXPCON_IO21]
ldc_set_location -site {F19} [get_ports EXPCON_IO22]
ldc_set_location -site {E20} [get_ports EXPCON_IO23]
ldc_set_location -site {F20} [get_ports EXPCON_IO24]
ldc_set_location -site {G20} [get_ports EXPCON_IO25]
ldc_set_location -site {G19} [get_ports EXPCON_IO26]
ldc_set_location -site {H17} [get_ports EXPCON_IO27]
ldc_set_location -site {H18} [get_ports EXPCON_IO28]
ldc_set_location -site {J10} [get_ports EXPCON_IO29]
ldc_set_location -site {J11} [get_ports EXPCON_IO30]
ldc_set_location -site {K10} [get_ports EXPCON_IO31]
ldc_set_location -site {J17} [get_ports EXPCON_IO32]
ldc_set_location -site {J12} [get_ports EXPCON_IO33]
```

```
ldc_set_location -site {H20} [get_ports EXPCON_IO34]
ldc_set_location -site {H19} [get_ports EXPCON_IO35]
ldc_set_location -site {K11} [get_ports EXPCON_IO36]
ldc_set_location -site {J19} [get_ports EXPCON_IO37]
ldc_set_location -site {J14} [get_ports EXPCON_IO38]
ldc_set_location -site {J13} [get_ports EXPCON_IO39]
ldc_set_location -site {K16} [get_ports EXPCON_IO40]
ldc_set_location -site {J15} [get_ports EXPCON_IO41]
ldc_set_location -site {K14} [get_ports EXPCON_IO42]
ldc_set_location -site {K15} [get_ports EXPCON_IO43]
ldc_set_location -site {K12} [get_ports EXPCON_IO44]
ldc_set_location -site {K13} [get_ports EXPCON_IO45]
ldc_set_location -site {J16} [get_ports EXPCON_OSC]
ldc_set_location -site {J18} [get_ports EXPCON_CLKIN]
ldc_set_location -site {J20} [get_ports EXPCON_CLKOUT]
ldc_set_location -site {H14} [get_ports HPE_RESOUT#]
ldc_set_location -site {G18} [get_ports HPE_CARDSEL#]

//Aardvark Header Connections
ldc_set_location -site {M7} [get_ports AK_SCL]
ldc_set_location -site {M8} [get_ports AK_SDA]
ldc_set_location -site {N1} [get_ports AK_MISO]
ldc_set_location -site {N2} [get_ports AK_SCLK]
ldc_set_location -site {N3} [get_ports AK_SS]
ldc_set_location -site {N4} [get_ports AK_MOSI]


//Arduino Header Connections
ldc_set_location -site {K4} [get_ports AR_IO0]
ldc_set_location -site {K5} [get_ports AR_IO1]
ldc_set_location -site {J6} [get_ports AR_IO2]
ldc_set_location -site {K7} [get_ports AR_IO3]
ldc_set_location -site {J7} [get_ports AR_IO4]
ldc_set_location -site {J8} [get_ports AR_IO5]
ldc_set_location -site {H9} [get_ports AR_IO6]
ldc_set_location -site {K8} [get_ports AR_IO7]
ldc_set_location -site {K3} [get_ports AR_IO8]
ldc_set_location -site {K2} [get_ports AR_IO9]
ldc_set_location -site {K1} [get_ports AR_SS_IO10]
ldc_set_location -site {L3} [get_ports AR_MOSI_IO11]
ldc_set_location -site {L1} [get_ports AR_MISO_IO12]
ldc_set_location -site {L2} [get_ports AR_SCK_IO13]
ldc_set_location -site {L7} [get_ports AR_IO14]
ldc_set_location -site {N5} [get_ports AR_SDA]
ldc_set_location -site {N6} [get_ports AR_SCL]
ldc_set_location -site {J9} [get_ports AR_RESET]
ldc_set_location -site {M1} [get_ports AR_AD0]
ldc_set_location -site {M2} [get_ports AR_AD1]
ldc_set_location -site {M3} [get_ports AR_AD2]
ldc_set_location -site {M4} [get_ports AR_AD3]
ldc_set_location -site {M5} [get_ports AR_AD4]
ldc_set_location -site {M6} [get_ports AR_AD5]
```

Appendix D. MachXO5T-NX Development Board Errata

As shown in Appendix A. MachXO5T-NX Development Board Schematics:

- Page3 of the Schematics, USB to Hard JTAG I/F
  Pin 1 of J1 and Pin 15 of U14 are connected with VCCIO2. It is recommended to connect them with VCCIO1 to ensure JTAG pins pull up to VCCIO1.
- Page 7 of the Schematics, PCIE&FPC Headers (BANK4)
  PCIE_CLKp and PCIE_CLKn assignments are mismatched with the U3 ball locations. It is recommended to swap them with the correct assignment. PCIE_CLKp should be connected to B7 of U3. PCIE_CLKn should be connected to C7 of U3.

References

For more information, refer to the following documents:

- MachXO5 Programming and Configuration User Guide (FPGA-TN-02271)
- Programming Cable User Guide (FPGA-UG-02042)

Revision History

Revision 1.0, April 2023

Section	Change Summary
All	Production release.

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