Always ON IP - Lattice Radiant Software

User Guide

FPGA-IPUG-02216-1.0

September 2023

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AON	Always ON
FPGA	Field Programmable Gate Array
HPD	High Performance Detection
IP	Intellectual Property

1. Introduction

The Always ON (AON) IP is used to power down the entire FPGA except for the AON block itself to minimize power when the FPGA is not needed to run High Performance Detection (HPD) AI. When AON is powered up, the output of AON drives the FPGA power to switch on. The FPGA AI can detect when the FPGA user leaves and would ask AON to power down the FPGA if it has been confirmed. The timer inside AON starts to count down during this power-save mode. When the timer limit is reached, AON can power up the FPGA. HPD AI runs to determine if the FPGA user is back. If the AI is confident that the owner is not back yet, the FPGA goes back to sleep or power-save mode—the FPGA is power down and AON is running. If the owner is back, the AI notifies the CPU to power up the entire FPGA. If the AI is not sure yet, it checks a few times to be sure and to decide whether to remain in power-save mode or to power up the FPGA.

1.1. Quick Facts

Table 1.1 presents a summary of the Always ON IP.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Families	CrossLink™-NX
Resource Utilization	Targeted Devices	LIFCL-33U
	Resources	See Table A.1 and Table A.2.
Design Tool Support	Lattice Implementation	IP v1.x.x – Lattice Radiant® Software 2022.1 or later
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

The AON IP has the following features:

- Sends an output to wake up the FPGA.
  - Two wake up modes: automatically wake up when the timer runs out or through an external wake up pin.
- This is only supported in LIFCL-33U devices.

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- *_i* are input signals
- *_o* are output signals
- *_n* are active low

1.3.3. Attribute

The names of attributes in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The AON soft IP is controlled by a 16-bit counter value and a ready-to-sleep signal from HPD AI. The counter value is calculated based on the desired FPGA power saving duration. When AON receives these signals, the FPGA moves to sleep mode and stays on this state until the internal 16-bit counter reaches 0. Once AON has finished counting, it sends an output signal to wake up the FPGA and waits until HPD AI decides to turn off the FPGA again.

Figure 2.1 shows the interface of the AON soft IP. The input signals may or may not directly connect to AON primitive ports. This depends on the mode setting while all output signals are connected directly from the AON primitive.

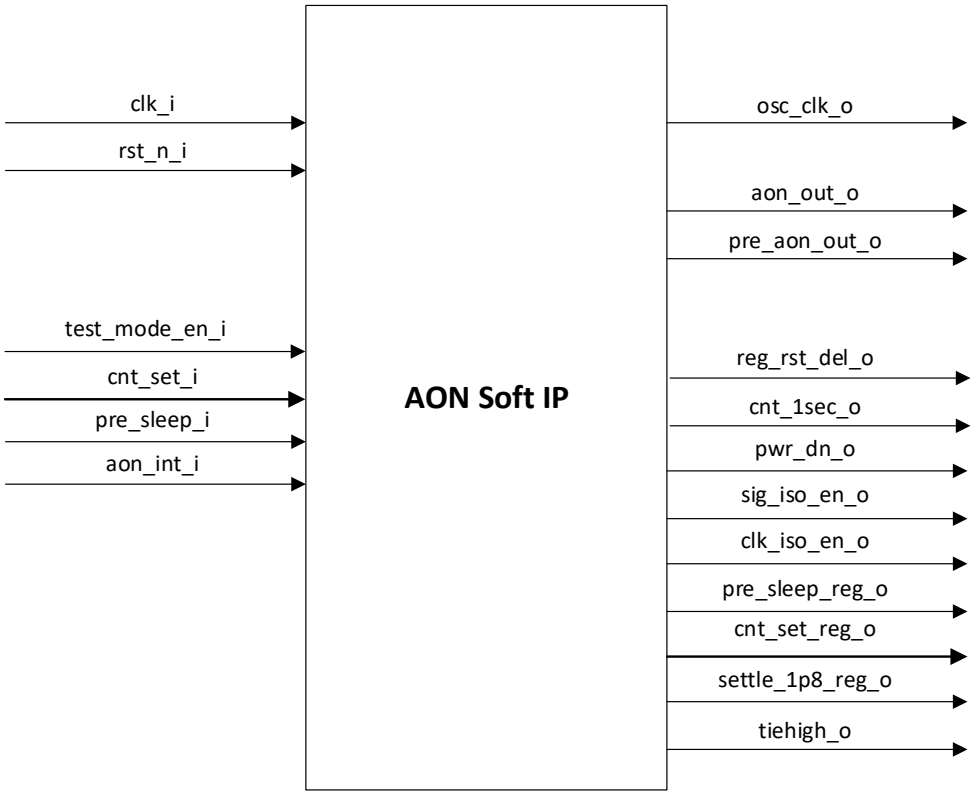

Figure 2.1. AON Soft IP Interface Diagram

The AON soft IP can be used in two modes, which are normal mode and test mode. In normal mode, the pre-calculated counter value and the pre-sleep signal can be transmitted during FPGA power up. In test mode, after every timer calibration, the AON internal state is set to 0 so the counter value and pre-sleep signal need to be re-transmitted to the FPGA. Also, when in test mode, AON state signals are available for timing sequence test.

AON has a built-in oscillator which can generate a 16 kHz clock that can be used to generate the counter set code.

2.2. Signal Description

Table 2.1 lists the ports of the AON soft IP.

Table 2.1. AON Module Signal Description

Port	Type	Width	Description
Clocks and Reset			
clk_i	IN	1	Input clock to synchronize AON control signals (recommended clock frequency to use is 16 kHz).
rst_n_i	IN	1	Active low reset input.
osc_clk_o	OUT	1	16 kHz AON domain built-in oscillator clock used by the AON state machine. This port is available only in the enabled test mode.
Control Signals			
test_mode_en_i	IN	1	AON mode control signal in the enabled test mode only. 1'b1 : AON is in test mode. 1'b0 : AON is in normal mode.
cnt_set_i	IN	16	16-bit binary counter set code for the AON timer in enabled test mode only. This timer is pre-calculated during normal mode.
pre_sleep_i	IN	1	Indicates HPD AI is done. The FPGA is power down except for the AON block. 1'b1 : FPGA presleep. 1'b0 : FPGA wake up.
aon_int_i	IN	1	External wake-up signal that comes from a pin on the FPGA chip. When this interrupt is set to '1', AON output signal is forced to output '1'.
Normal Mode Output Signal			
aon_out_o	OUT	1	Drives an external regulator that acts as the ON/OFF switch of FPGA supply during AON normal mode. 1'b1: Turn on the FPGA supply. 1'b0: Switch off the FPGA.
Test Mode Output Signal			
pre_aon_out_o	OUT	1	The AON block output that goes to the FPGA common interface block for test mode. When this signal asserts, all control signals such as test_mode_en_i, cnt_set_i and pre_sleep_i should be sent to AON sequence again. By default, this signal is high, and de-asserts only when clock and signal isolation are already enabled after pre_sleep_i assertion. After that, the timer starts to count down. When the counter value reaches 0, pre_aon_out toggles from '0' to '1'. When pre-sleep signal asserts again, pre_aon_out toggles back from '1' to '0'.
AON State Signals Available During Enabled Test Mode Only			
reg_rst_del_o	OUT	1	AON reset state. When FPGA re-power up, all AON internal input registers are reset to 0, and AON FSM cycle is restarted.
cnt_1sec_o	OUT	1	Asserts when the AON timer finished counting a certain amount of duration, typically one second.
pwr_dn_o	OUT	1	Indicates that FPGA starts to power down except for the AON block.
sig_iso_en_o	OUT	1	Enables or disables signal isolation. When the FPGA is already powered on, signal isolation is disabled. This is only enabled during pre_sleep_i assertion.
clk_iso_en_o	OUT	1	Enables or disables clock isolation. When FPGA is already powered on, clock isolation is disabled. This is only enabled during pre_sleep_i assertion.
pre_sleep_reg_o	OUT	1	Ready to sleep signal.
cnt_set_reg_o	OUT	16	Starts with counter value and counts down every osc_clk_o cycle after pre-sleep assertion.
settle_1p8_reg_o	OUT	1	Indicates that AON internal power sources are stable thus FPGA is ready and already in user mode.
tiehigh_o	OUT	1	Stays high when the AON power is successfully powered on.

2.3. Attributes Summary

The configurable attributes of the AON soft IP are shown in Table 2.2 and described in Table 2.3. The attributes can be configured through the IP Catalog Module/IP Block Wizard of the Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
Enable Test Mode	Checked, Unchecked	Unchecked	—
Timer Value (in seconds)	1-10	1	Available only when *Enable Test Mode == Unchecked*

Table 2.3. Attributes Descriptions

Attribute	Description
Enable Test Mode	When this is unchecked, the AON IP can be used in normal mode only. Enabling this allows the AON IP to enter either normal mode or test mode at the start of AON operation through dynamic switching of test_mode_en_i.
Timer Value (in seconds)	The timer/counter value to be used during normal mode.

2.4. Operation Details

FPGA powers on and enters user mode when it is power ready after internal power sources are already settled. Timer calibration usually takes 0.625 ms (samples 10 cycles of the AON internal oscillator clock). After timer calibration, the counter set code can already be set. Then pre_sleep_i toggles from '0' to '1' from AI detection indicating the FPGA is ready to sleep. AON processes these control signals, and then, drives the AON output to go high to wake up the FPGA. AON interrupt is the other way to reset the AON state machine.

2.4.1. AON on Normal Mode

Figure 2.2 shows how to control input signals when AON is in normal mode. From the waveform, calc_cnt_set_i holds a fixed binary counter set value. This is evaluated ~4 osc_clk_o after aon_out_o assertion due to internal AON flow state. The pre_sleep_i signal assertion from AI detection indicates that the FPGA is ready to sleep. The minimum pulse requirement of pre_sleep_i is 3 osc_clk_o cycles which is about 0.1875 ms to make sure pre_sleep internal register holds high during FPGA sleep period. The calc_cnt_set_i and pre_sleep_i safest hold time is till when FPGA is still on power down state, aon_out_o is still low. These signals should be retransmitted in case of AON interrupt or when aon_out_o asserts. The interrupt, aon_int_i, needs to be larger than the regular response time. Calibration time is about 0.625 ms.

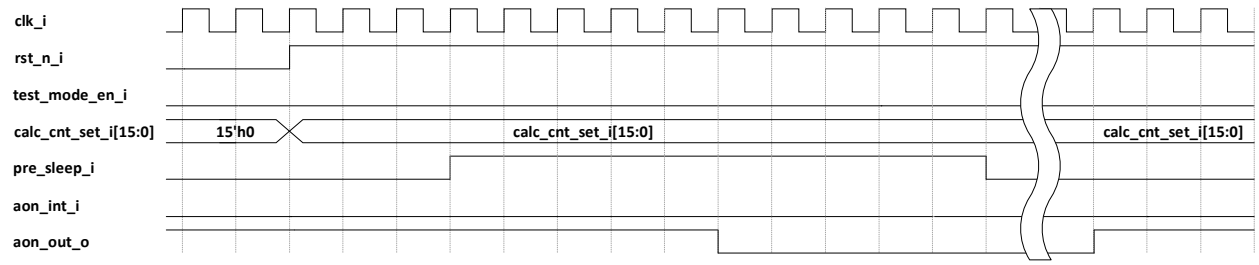

Figure 2.2. AON Normal Mode Sample Waveform

2.4.2. AON in Test Mode

Figure 2.3 shows AON in test mode. During test_mode_en_i = 1'h1, AON automatically goes to power on state. In test mode, the test_mode_en_i rising edge should not be later than pre_sleep_i assertion and hold high for a minimum of four osc_clk_o cycles. Otherwise, it cannot be captured by the AON block. The soft IP implementation includes

retransmission of test_mode_en_i, cnt_set_i, and pre_sleep_i each time an assertion of pre_aon_out_o is detected in the succeeding cycles of AON operation. Default values of these signals are all '0'.

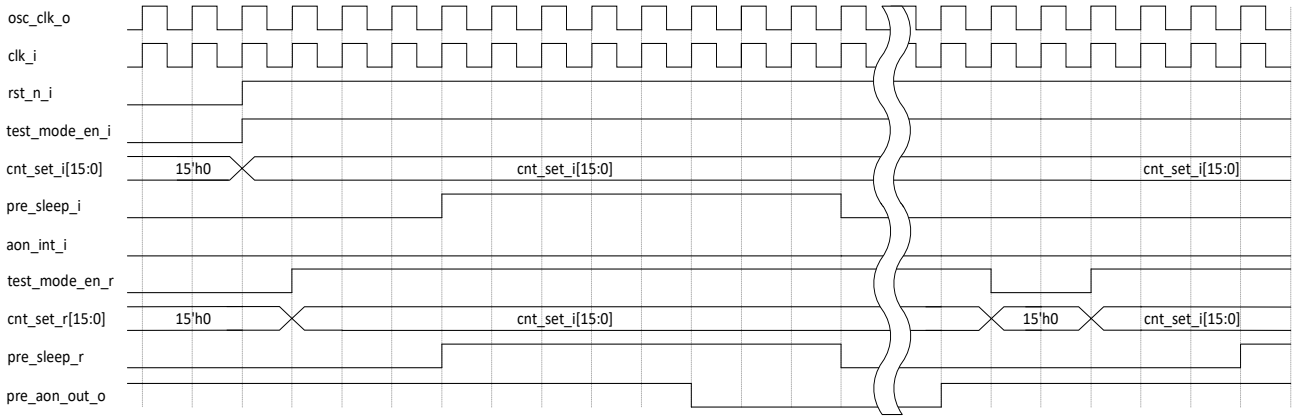

Figure 2.3. AON Test Mode Sample Waveform

2.4.2.1. AON States

AON states can be decoded based on concatenated values of the AON state signal listed in Table 2.4. There are 17 used current states. Other states are considered invalid states. Table 2.5 lists all valid and invalid states and their description.

Table 2.4. AON Current State from State Signals

AON State Signal	Width	Field
reg_rst_del_o	1	aon_cur_state[23]
cnt_1sec_o	1	aon_cur_state[22]
pwr_dn_o	1	aon_cur_state[21]
sig_iso_en_o	1	aon_cur_state[20]
clk_iso_en_o	1	aon_cur_state[19]
pre_sleep_reg_o	1	aon_cur_state[18]
cnt_set_reg_o	16	aon_cur_state[17:2]
settle_1p8_reg_o	1	aon_cur_state[1]
tiehigh_o	1	aon_cur_state[0]

Table 2.5. AON Current State Description

AON Current State Value	Description
Valid/Used States	
000000000	AON power down. Default state, AON output is '0'.
000110001	AON first power on. AON output is set to '1'. Clock and signal isolation are enabled.
000110011	First FPGA power ready. AON internal power signals are sensed by voltage detectors. Internal power signals reached 1.8 V.
000100011	First clock isolation disable.
000000011	First signal isolation disable.
000000n11	First 16-bit binary code is set as the AON timer value. AON stays on this state until pre-sleep signal assertion is detected.
000001n11	The FPGA is ready to sleep.
000011n11	Enabled clock isolation.
000111n11	Enabled signal isolation.

AON Current State Value	Description
001111n11	FPGA power down. AON out toggles from '1' to '0'.
011111n11	The AON counter/timer starts to count down. When the AON counter/timer finished counting, AON output toggles from '0' to '1'.
100110001	After the FPGA re-power up, all internal registers are reset. Internal voltage detector de-asserts.
010110001	AON initialization. Starts next FSM recycle.
010110011	The FPGA is power ready again.
010100011	Clock isolation disable after FPGA wake-up.
010000011	Signal isolation disable after FPGA wake-up.
010000n11	The count set value is set to another value.
Invalid States	
xxxxxxxx0	AON black out. AON loses its power. Re-powering up AON can reset all internal registers and make the AON back to power on state.
xxxxxxxx1	AON is in non-deterministic state. You can use the input signal aon_int to reset all input registers and make AON back to power on state.

2.4.3. Mode Transition of AON

During enabled test mode, AON is allowed to enter either normal mode or test mode at the start of its operation if the desired test_mode_en_i is set before pre_sleep_i assertion. Once pre_sleep_i assertion is detected, AON runs based on the evaluated test_mode_en_i value. After that, the AON internal FSM begins to run disregarding any test_mode_en_i toggling. Current AON mode operation is not affected by the test_mode_en_i toggling.

3. IP Generation, Simulation, and Validation

This section provides information on how to generate the AON module using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

3.1. Generating the IP

The Lattice Radiant software allows you to customize and generate modules and IPs and integrate them into the device architecture. The procedure for generating the AON module in the Lattice Radiant software is described below.

To generate the AON Module:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **Always ON** under **Architecture Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

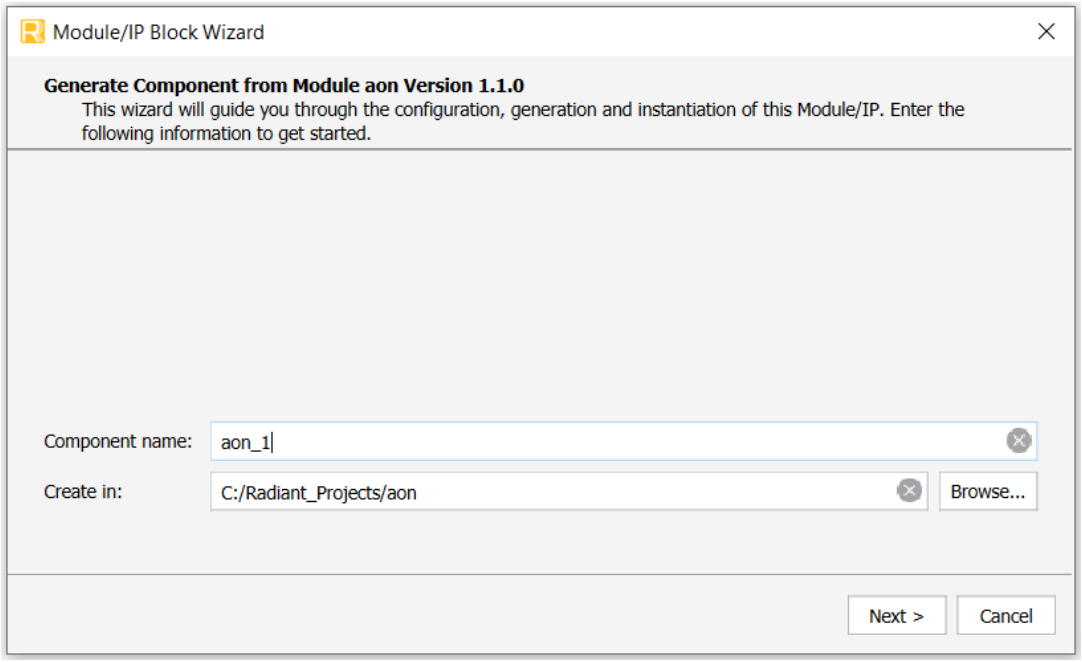

Figure 3.1. Module/IP Block Wizard

3. In the module dialog box of the **Module/IP Block Wizard** window, customize the selected AON Module using drop-down menus and check boxes. For a sample configuration, see Figure 3.2. For configuration options, see the Attributes Summary section.

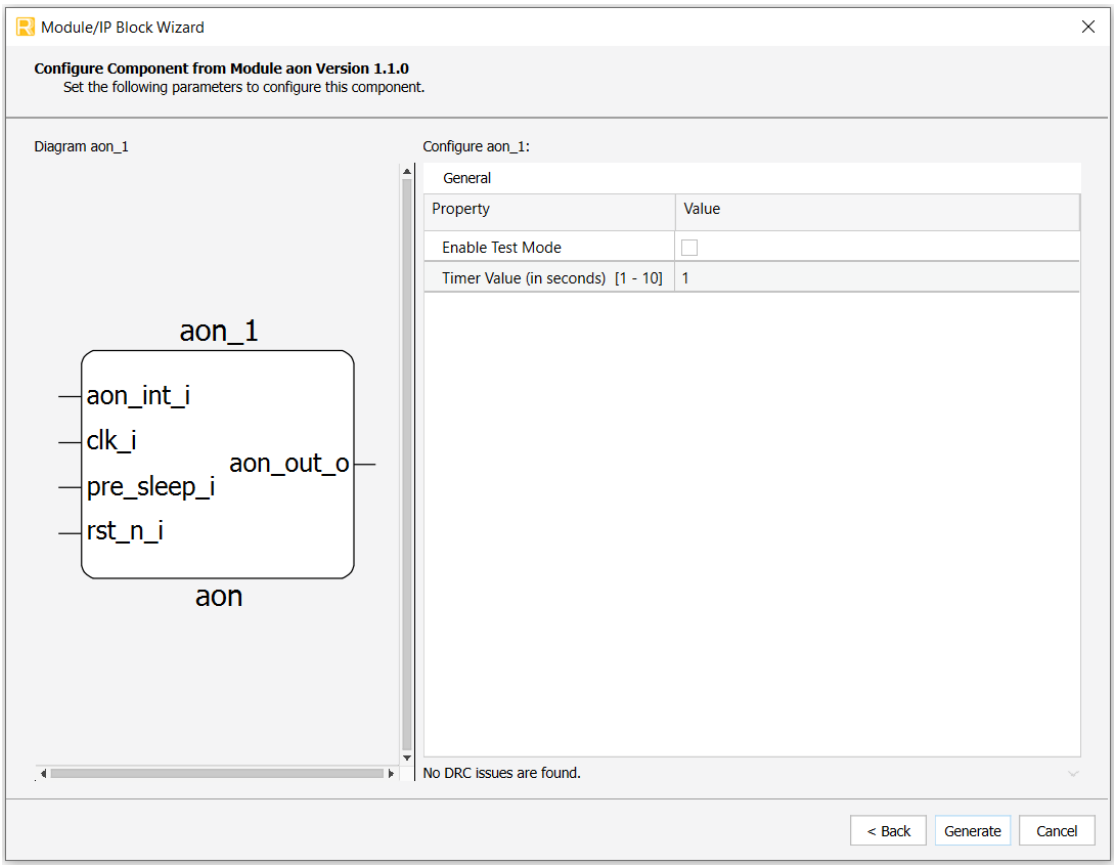

Figure 3.2. Configure User Interface of AON Module

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results, as shown in Figure 3.3.

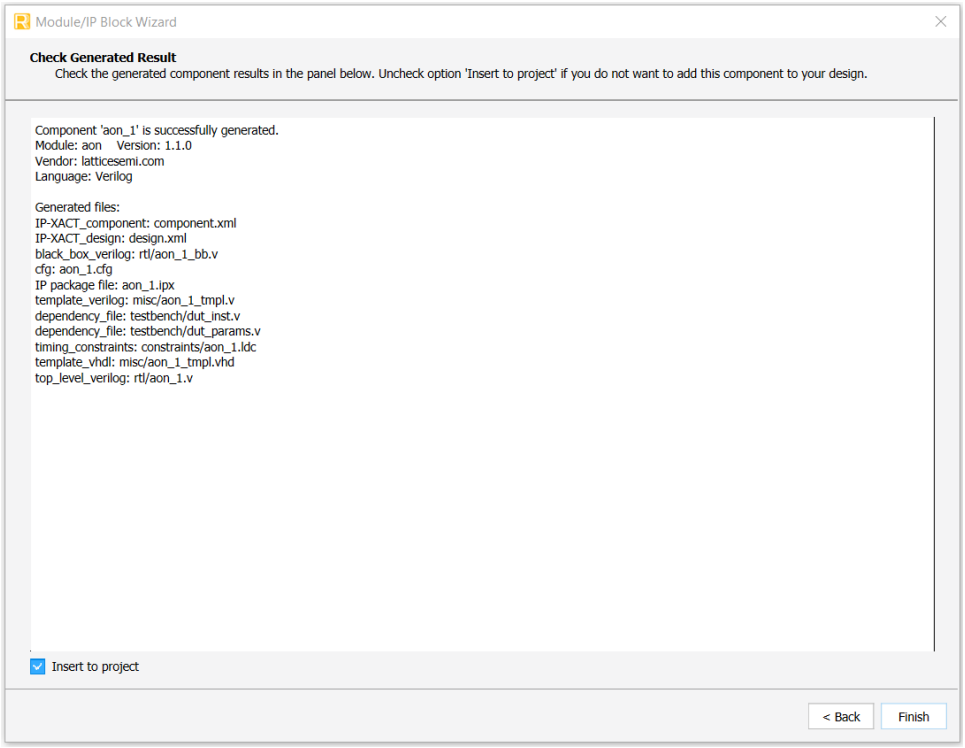

Figure 3.3. Check Generated Result

5. Click the **Finish** button.

All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated AON module package includes the black box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level of the complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis black box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

3.2. Running Functional Simulation

To run functional simulation:

1. Click the  icon located on the **Toolbar** to initiate the **Simulation Wizard** (Figure 3.4).

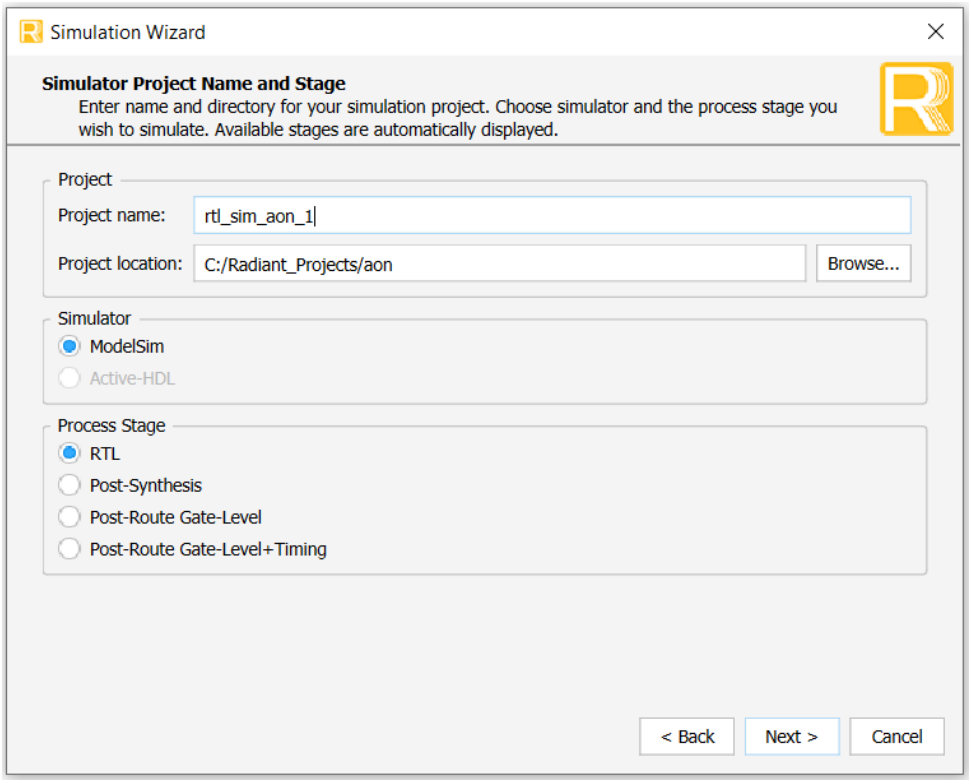

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window, as shown in Figure 3.5.

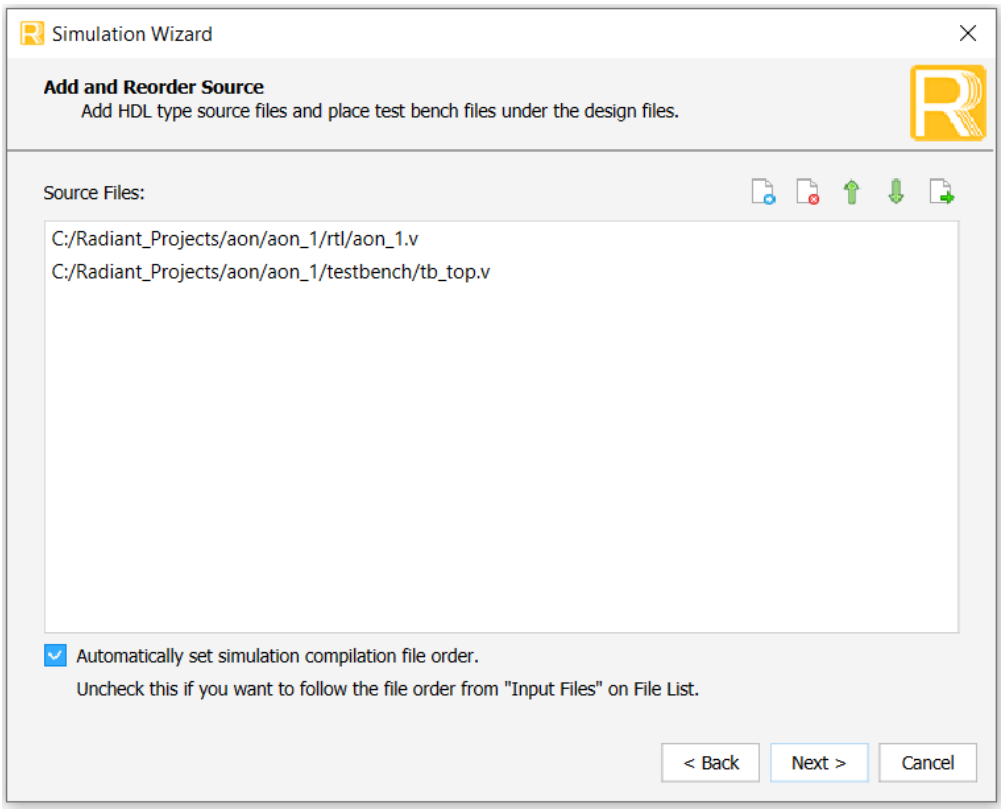

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software suite. The results of the simulation in our example are provided in Figure 3.6.

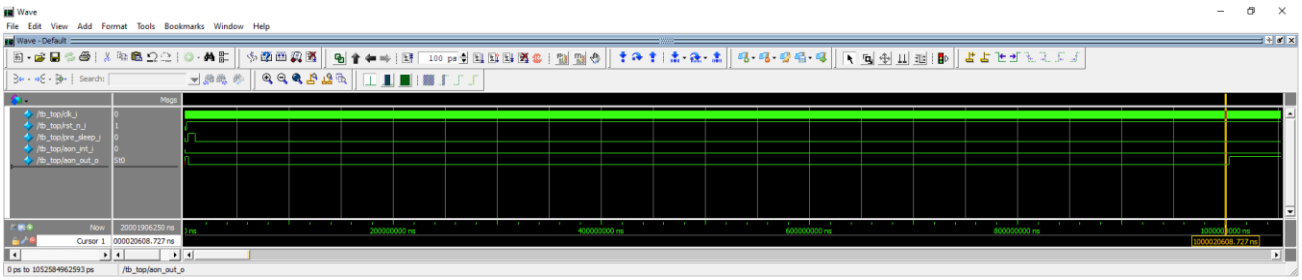

Figure 3.6. Simulation Waveform

3.3. IP Evaluation

There is no restriction on the IP evaluation of this module.

References

- CrossLink-NX Family Devices Web Page
- Lattice Radiant Software Web Page
- Lattice Insights for Training Series and Learning Plans

Appendix A. Resource Utilization

Table A.1 shows the resource utilization of the AON IP for the LIFCL-33U-9USG84C device using Synplify Pro of Lattice Radiant software 2022.1. Default configuration is used, and some attributes are changed from the default values to show the effect on the resource utilization.

Table A.1. LIFCL-33U-9USG84C Resource Utilization

Configuration	Clk Fmax (M Hz)*	Registers	LUTs	EBRs	DSPs
Default	n/a	0	1	0	0
Enable Test Mode: True	200	41	54	0	0

***Note:** Fmax is generated when the FPGA design only contains the AON IP, and the target Frequency is 16 kHz. These values may be reduced when user logic is added to the FPGA design.

Table A.2 shows the resource utilization of the AON IP for the LIFCL-33U-7USG84C device using Synplify Pro of Lattice Radiant software 2022.1. Default configuration is used, and some attributes are changed from the default values to show the effect on the resource utilization.

Table A.2. LIFCL-33U-7USG84C Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs	DSPs
Default	n/a	0	1	0	0
Enable Test Mode: True	191	41	54	0	0

***Note:** Fmax is generated when the FPGA design only contains the AON IP, and the target Frequency is 16 kHz. These values may be reduced when user logic is added to the FPGA design.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Document Revision 1.0, September 2023

Section	Change Summary
All	Removed the original Section 3 Implementation Details.
Introduction	Removed the original sub-section 1.3.3 Host.

Functional Description	• Updated Figure 2.1. AON Soft IP Interface Diagram.
	• Operation Details:
	  • changed the section name to *Operation Details*;
	  • removed the original Figure 2.2. AON Block Usage Flow Chart and related description;
	  • removed *internal POR test signal stays high* in the AON in Test Mode section.

IP Generation, Simulation, and Validation	• Removed the original sub-section 4.1 Licensing the IP.
	• Generating the IP:
	  • changed the section name to *Generating the IP*;
	  • updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure User Interface of AON Module, Figure 3.3. Check Generated Result, Figure 3.4. Simulation Wizard, and Figure 3.5. Adding and Reordering Source.
	• IP Evaluation:
	  • changed the section name to *IP Evaluation*;
	  • updated the content to reflect the section name change.

References	Newly added links to Lattice Radiant Software Web Page and Lattice Insights for Training Series and Learning Plans.
Technical Support Assistance	Newly added the link to the Lattice Answer Database.

Document Revision 0.80, October 2022

Section	Change Summary
All	Preliminary release.

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