Multi-Corner Timing Analysis for Lattice Nexus Devices

Application Note

FPGA-AN-02063-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronyms	Definition
FPGA	Field Programmable Gate Array
PVT	Process Voltage Temperature

1. Introduction

The Lattice Radiant™ software can perform timing analysis on Lattice FPGA devices.

This document provides step-by-step instructions to manually run timing analysis at various corners for Lattice Nexus™ devices. For more information, select **Help** from the Lattice Radiant software menu and refer to the Reading Timing Analysis Reports section.

The default setup and hold timing analysis on Nexus devices is as follows:

- Setup Analysis is performed at user speed grade and temperature based on the device type:
  - Commercial devices: 85 °C
  - Industrial devices: 100 °C
  - Automotive devices: 125 °C
- Hold Analysis is performed at *m* speed grade (where *m* speed grade is a virtual device speed grade which applies the process worst-case condition) based on the device type:
  - Commercial devices: 0 °C
  - Industrial devices: –40 °C
  - Automotive devices: –40 °C

For certain PVT variations, the user may need to run timing analysis at various corners to ensure they are meeting timing at all possible corners. For Nexus devices, if the user needs to perform multi-corner timing analysis, the user may perform timing analysis at various corners by manually changing the speed grade (between *m* and user speed grade for setup/hold analysis) and temperature values.

1.1. Audience

The intended audience for this document includes FPGA design engineers using the Lattice Radiant design software. The technical guidelines assume that the reader has some basic knowledge on Lattice Radiant timing analysis.

2. Running Multi-Corner Timing Analysis

To run multi-corner timing analysis:

1. Generate a .udb file by running the design until **Place & Route Design**. Perform sign-off timing analysis on the generated .udb file.

Figure 2.1. Run Place & Route Design

The generated .udb file is in the project implementation directory. Setup and hold analyses are performed using the default parameters in this .udb file unless the parameters are changed.

2. Vary the temperature and speed grade and use the **Standalone Timing Analyzer** tool to perform timing analysis at different temperature corners.

   To run timing analysis at different corners:

   a. Create a separate .pdc file for each temperature corner along with the original timing constraints and use the file for timing analysis. The constraint to set temperature is ldc_set_attribute {TEMPERATURE=<temp_value_in_Celcius>}. This constraint can be added to the .pdc file (that is: ldc_set_attribute {TEMPERATURE=0C}).

   b. Change the speed grade for timing analysis using the **Standalone Timing Analyzer** tool by selecting **Edit > Timing Option Setting.**

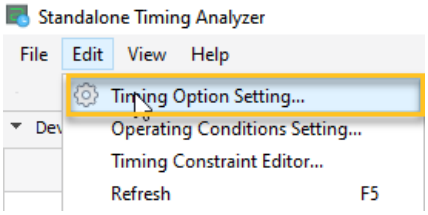

Figure 2.2. Open Timing Option Setting

   c. In the **Timing Option Setting** dialog box, set the **Speed for setup** and **Speed for hold** as needed.

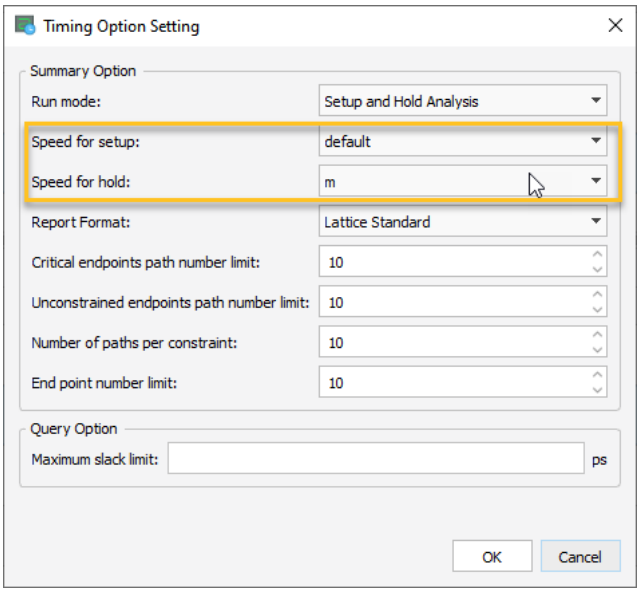

Figure 2.3. Change Timing Option Setting

d. After making the speed grade changes, load the new .pdc file with temperature and original timing constraints added for timing analysis. To load the new .pdc file, select **File > Load Timing Constraint File**.

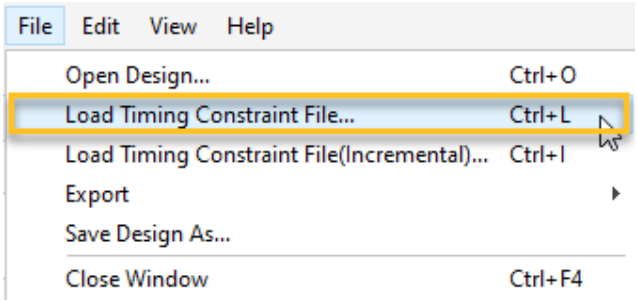

Figure 2.4. Load Timing Constraint File

After loading the constraint file, the tool automatically runs timing analysis on the database using the new constraint file.

e. Generate separate .twr files for different temperatures and speed grades (default *m* and user speed grade for setup/hold analysis) for easy analysis. To export timing reports, select **File > Export**.

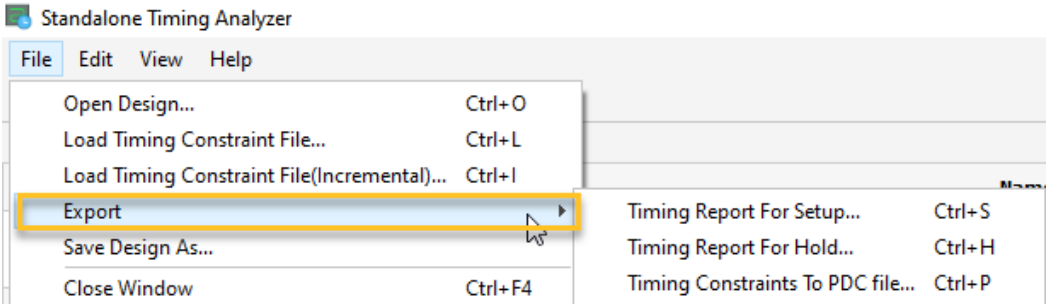

Figure 2.5. Export Timing Reports

Notes:

- If a –9 speed grade is used to perform place & route of the design, changing the speed grade to a lower speed grade is not recommended as moving to a slower speed grade may cause timing failures. If a –7 or a –8 speed grade is used, the user may change the speed grade to –9 to perform multi-corner setup timing analysis.
- For setup/hold analysis, the user may change the speed grade between *m* and user speed grade for multi-corner timing analysis.

f. After generating the timing report, review it and check if there are any timing violations at the specified temperature or speed grades.

g. If there are timing violations at a given speed grade, re-run **Place & Route** at that temperature and speed grade. Temperature constraints can be added to the original .pdc file to generate a new .udb file. The speed grade settings can be changed using the **Place & Route Design Strategy** dialog box. Note that place & route optimizations for setup analysis cannot be performed using the *m* speed grade.

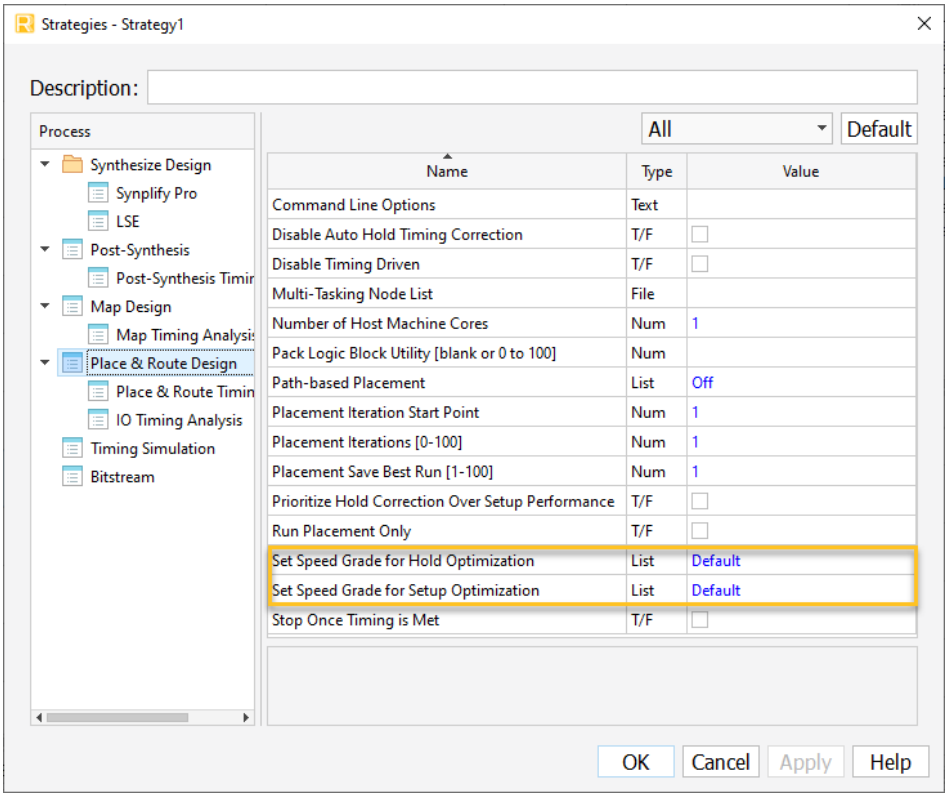

Figure 2.6. Place & Route Strategies

h. After re-running **Place & Route** at the failing temperatures and speed grades, if there are timing violations, over constrain the failing clocks using the set_clock_uncertainty constraint and re-run **Place & Route** so that it can put in extra effort to meet timing.

   However, the timing should be re-run on this new .udb by removing the set_clock_uncertainty constraint. The syntax for set_clock_uncertainty constraint is set_clock_uncertainty [-setup] [-hold] [-from <clock>] [-to <clock>] <uncertainty> [{clock list}].

   Notes:

   - If there are setup violations, use the set_clock_uncertainty constraint on the failing clock with the -setup option.
   - If there are hold violations, use the set_clock_uncertainty constraint on the failing clock with the -hold option.
   - If the failing path is from the input side, use the set_clock_uncertainty constraint with the -to <clock> option.
   - If the failing path is at the output side, use the set_clock_uncertainty constraint with the -from <clock> option.

   Follow steps 2b, 2c, and 2d to perform timing analysis at the speed grade and temperature used for place & route by removing the set_clock_uncertainty constraint.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 1.0, March 2023

Section	Change Summary
All	Initial release.

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