I2C-to-APB Bridge Reference Design User Guide

Reference Design

FPGA-RD-02263-1.1

June 2025

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
FPGA	Field Programmable Gate Array
I2C	Inter-Integrated Circuit
IP	Intellectual Property
LUT	Lookup Table
RTL	Register Transfer Level

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1. Introduction

The I2C-to-APB Bridge Reference Design provides an interface between the low speed I2C Bus and the AMBA 3 APB Bus. The design is implemented in Verilog HDL and comes in .ipk format that is installed within Lattice Propel™ Builder software as an IP. Implementation is done within the Lattice Diamond® software as shown in Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
MachXO2™	Lattice Propel Builder version 2.2 and above	Lattice Diamond version 3.12 and above
MachXO3™	Lattice Propel Builder version 2.2 and above	Lattice Diamond version 3.12 and above
MachXO3D™	Lattice Propel Builder version 2.2 and above	Lattice Diamond version 3.12 and above

1.1. Features

The key features of the I2C to APB Bridge Reference Design include:

- Compliance with AMBA 3 APB Protocol v1.0
- APB Data Bus width of 32 bits.
- APB Address width of 32-bits.
- Registered output

1.2. Limitations

- Reference design is not verified in UVM (Universal Verification Methodology).
- Specifically designed to access the System Memory Module from Lattice Propel Builder. Refer to System Memory Module - Lattice Propel Builder (FPGA-IPUG-02073).

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2. Functional Description

2.1. Overview

The I2C-to-APB Bridge Reference Design is used for interfacing one I2C Controller and one APB Completer. This bridge has two sections: the I2C Target section, and the APB Requester section. An external I2C Controller is required to use this bridge, while the APB Completer can be implemented within the FPGA fabric. When interfacing to multiple APB Completers, the user can use either an APB interconnect IP or multiple instantiations of this I2C to APB Bridge with different Target addresses. Follow the I2C framing described in this document to allow proper conversion of I2C to APB transactions.

2.2. Interface Description

Figure 2.1 shows the interface diagram of the I2C-to-APB Bridge Reference Design. This is in .ipk format and installed within Lattice Propel Builder as an IP. The diagram shows all the available ports for the IP core. The I2C ports (SCL and SDA) act as I2C-Targets requiring separate I2C-Controller to control it. The APB ports act as APB-Requesters that can control an APB-Completer device.

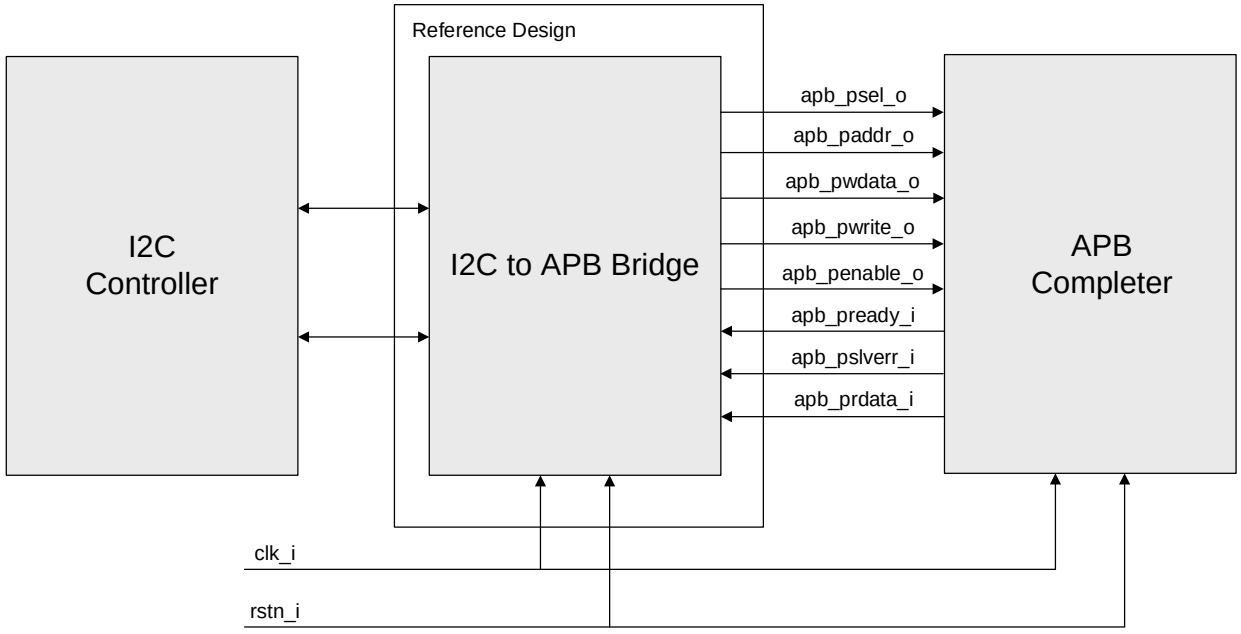

Figure 2.1. Functional Block Diagram

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Table 2.1. APB to AHB-Lite Bridge Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
clk_i	In	1	12 MHz system clock or higher
rstn_i	In	1	Asynchronous active LOW reset input.
I2C Target Interface			
SCL	Bidirectional	1	Serial Clock Line of the I2C Target core.
SDA	Bidirectional	1	Serial Data Line of the I2C Target core.
APB Requester Interface (APB_M0)			
apb_psel_o	Out	1	Select signal. This indicates that the Completer device is selected and that a data transfer is required.
apb_paddr_o	Out	32	Address signal
apb_pwdata_o	Out	32	Write data signal. This is transmitted to the APB Completer during a write transaction.
apb_pwrite_o	Out	1	Direction signal. Write = 1, Read = 0
apb_penable_o	Out	1	Enable signal. This indicates that the second and subsequent cycles of an APB transfer.
apb_pready_i	In	1	Ready signal. This indicates transfer completion. The Completer uses this signal to extend an APB transfer.
apb_pslverr_i	In	1	Error signal. This indicates a transfer failure. If APB Completer does not have this signal, it is tied to 1'b0.
apb_prdata_i	In	32	Read data signal. This comes from the APB Completer during a read transaction.

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2.3. Attributes

Table 2.2 provides the list of user-configurable attributes for the I2C to APB Bridge. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.2.

Table 2.2. Attributes Table

Attributes	Selectable Values	Default	Dependency on Other Attributes
7-Bit Target Address	7'b0000001 – 7'b1111111	7'b1000001	—

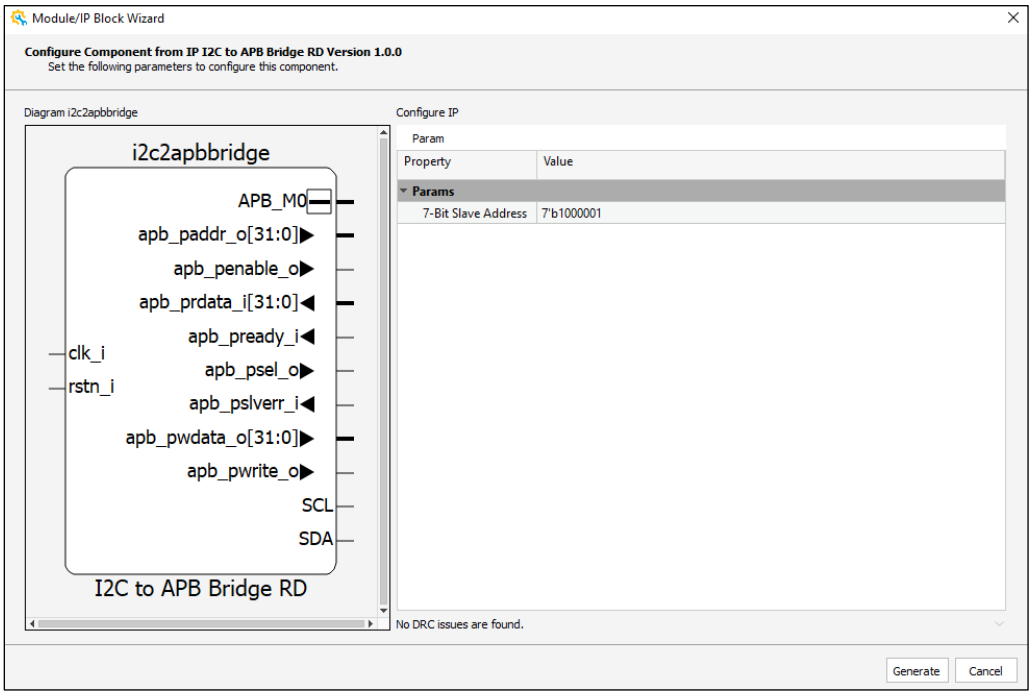

Figure 2.2. I2C to APB Bridge Configuration User Interface

Table 2.3. Attributes Description

Attributes	Description
7-Bit Target Address	User configurable 7-bit Target address.

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3. Operation Sequence

This reference design converts I2C transactions from an external I2C Controller into APB Requester transactions. This can be done by following the proper I2C framing mentioned below.

3.1. Write Operation

Figure 3.1 shows the I2C framing for a single APB Write transaction. The first four bytes of serial data named in the figure as *APB Address[31:0]* are converted into the parallel apb_paddr_o signal mentioned in Table 2.1. The next four bytes of serial data named *APB Write Data[31:0]* are converted into the parallel apb_pwrite_o signal mentioned in Table 2.1. For multiple writes, this framing needs to be repeated by the I2C Controller for every APB address location.

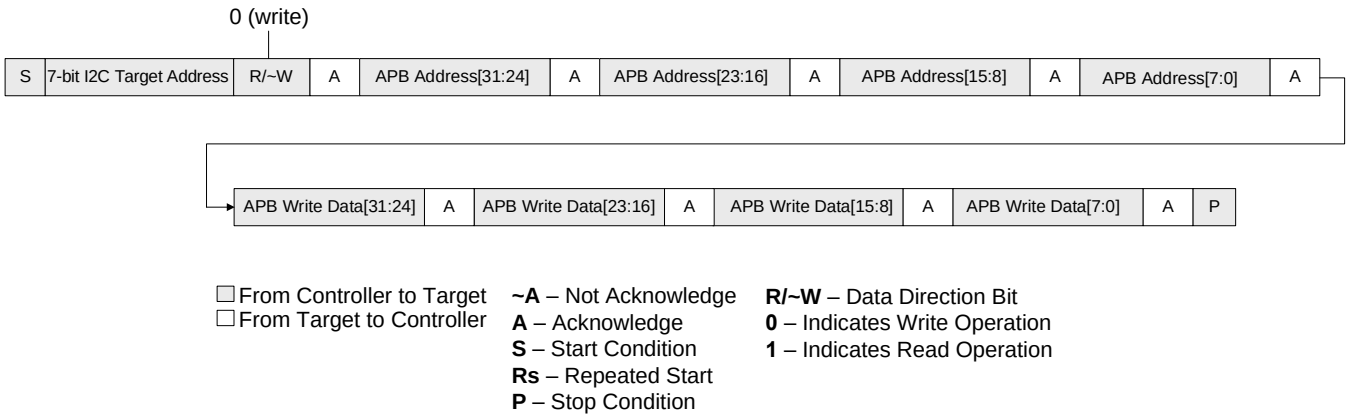

Figure 3.1. Write Operation Data Format for I2C to APB Conversion

3.2. Read Operation

Figure 3.2 shows the I2C framing for a single APB Read transaction. The first four bytes of serial data named in the figure as *APB Address[31:0]* are converted into the apb_paddr_o signal mentioned in Table 2.1. The next four bytes of serial data named *APB Read Data[31:0]* is the serial conversion of the parallel data coming from the apb_prdata_i data line mentioned in Table 2.1. For multiple reads, this framing needs to be repeated by the I2C Controller for every APB address location.

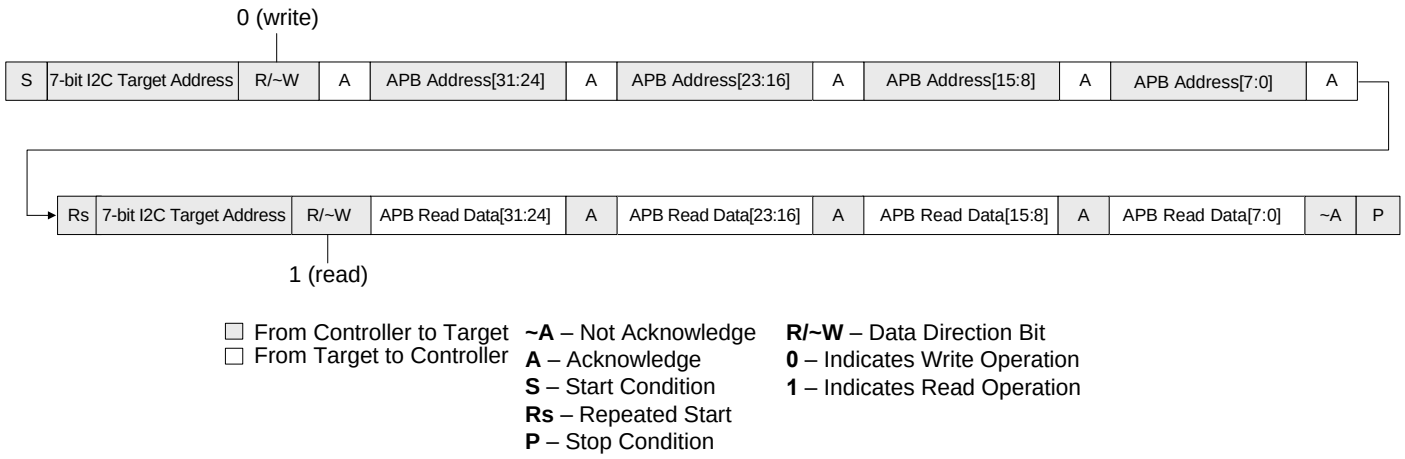

Figure 3.2. Read Operation Data Format for I2C to APB Conversion

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4. Timing Diagram

4.1. Write Transactions

The following steps describe the APB Requester transaction generated after following the correct I2C frame during Write operation. Connect a user APB Completer to this design to allow proper transactions. For simplicity, I2C signals are not included in Figure 4.1 due to the large difference in clock speeds (SCL versus clk_i). Refer to Figure 7.4 to see both I2C and APB waveforms in the same context.

1. The APB Bus is in idle state. During this period, the external I2C Controller starts the write operation shown in Figure 3.1.
2. After receiving the stop condition of the I2C write operation, the APB Requester section of this reference design asserts the apb_pwrite_o and apb_psel_o signals to HIGH. The user APB Completer latches the data presented on the apb_paddr_o and apb_wdata_o data lines.
3. The APB Requester asserts the apb_penable_o signal to HIGH. Wait states can be inserted by the APB Completer during this step by holding apb_ready_i to LOW.
4. The APB Completer asserts the apb_pready_i signal to HIGH signifying that a write transaction has completed.
5. The APB bus returns to an idle state. The apb_psel_o and apb_penable_o signals are deasserted to LOW. Due to the large difference in clock speed of I2C and APB protocols, time periods between multiple writes are much larger than what is shown in Figure 4.1.
6. Similar to steps 2, 3, and 4.
7. Similar to step 1.

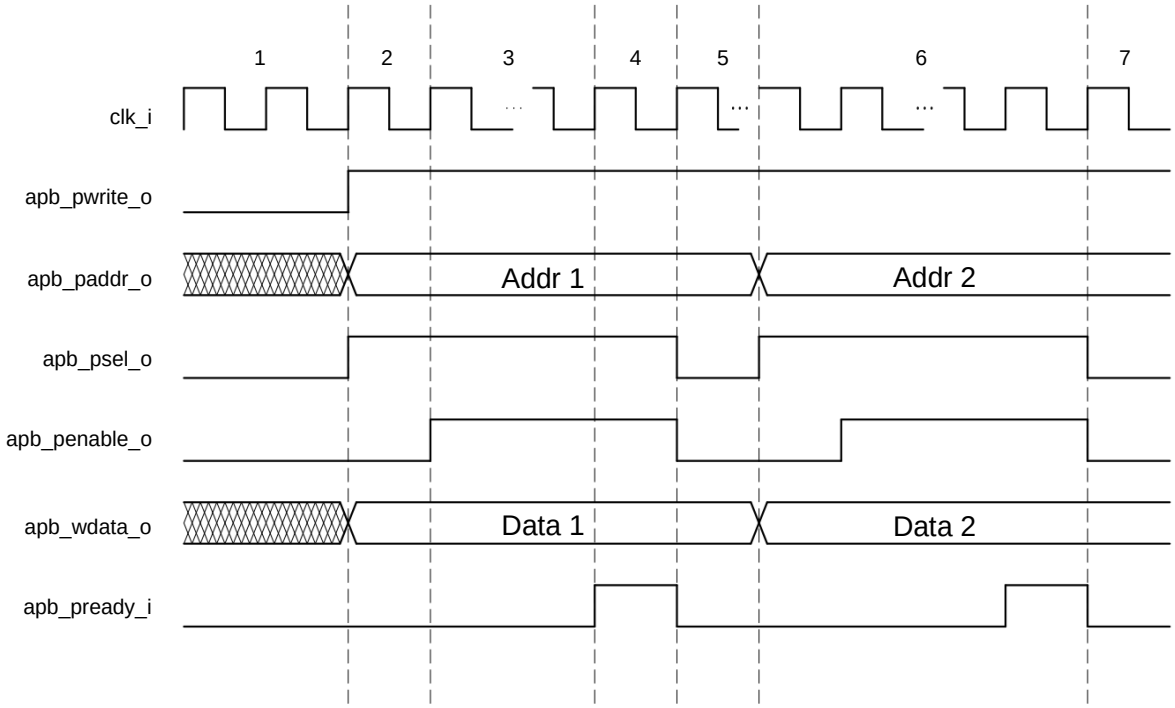

Figure 4.1. I2C-to-APB Bridge Write Transactions

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4.2. Read Transactions

The following steps describe the APB Requester transaction generated after following the correct I2C frame during Read operation. Connect a user APB Completer to this design to allow proper transactions. For simplicity, I2C signals are not included in Figure 4.2 due to the large difference in clock speeds (SCL versus clk_i). Refer to Figure 7.5 to see both I2C and APB waveforms in the same context.

1. The APB Bus is in idle state. During this period, the external I2C Controller starts the read operation shown in Figure 3.2.
2. After receiving the 32-bit APB Address during the I2C read operation, the APB Requester section of this reference design asserts the apb_psel_o signals to HIGH while apb_pwrite_o is deasserted to LOW. The user APB Completer latches the data presented on the apb_paddr_o data line.
3. The APB Requester asserts the apb_penable_o signal to HIGH. Wait states can be inserted by the APB Completer during this step by holding apb_ready_i to LOW.
4. The APB Completer asserts the apb_pready_i signal to HIGH signifying that a read transaction has completed and that the data is already available on the apb_prdata_i data line.
5. The APB bus returns to an idle state. The apb_psel_o and apb_penable_o signals are deasserted to LOW. Due to the large difference in clock speed of I2C and APB protocols, time periods between multiple writes are much larger than what is shown in Figure 4.2.
6. Similar to steps 2, 3, and 4.
7. Similar to step 1

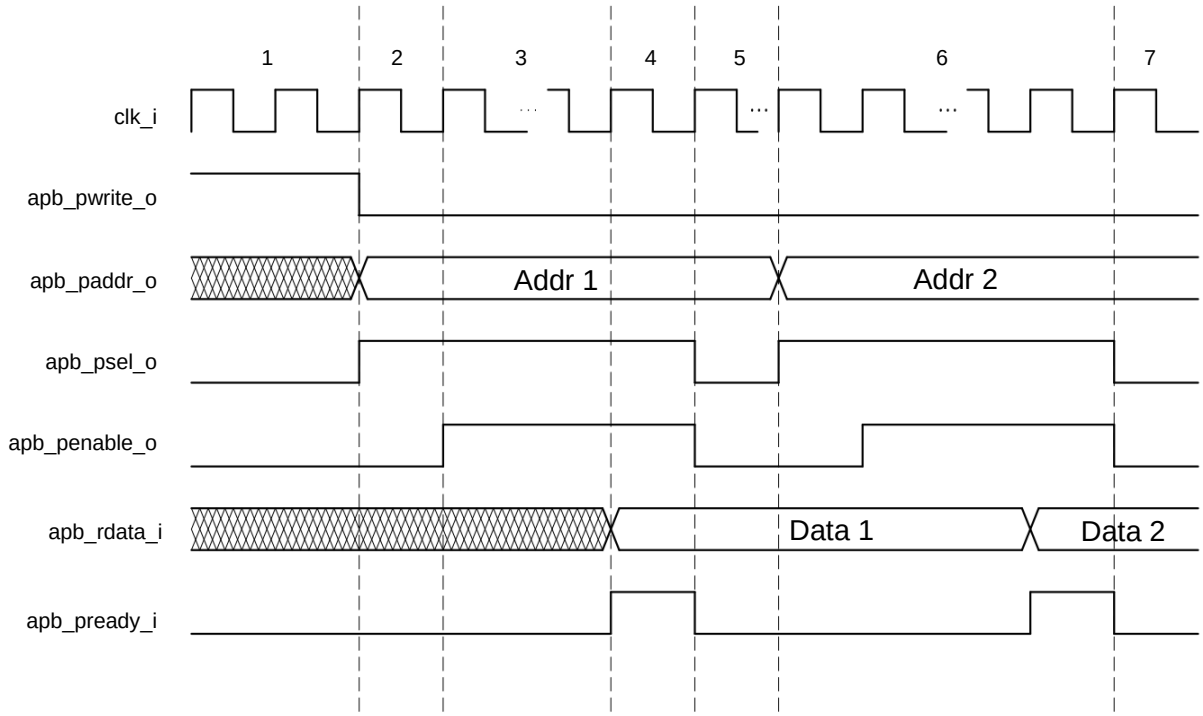

Figure 4.2. I2C-to-APB Bridge Read Transactions

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5. Design Package

The reference design folder (I2C_to_APB_Bridge) contains two subfolders: IP and Simulation:

- IP – Contains the IPK file that can be installed in Lattice Propel Builder.
- Simulation – Contains the simulation script file (.DO) and the pregenerated RTL and Testbench files.

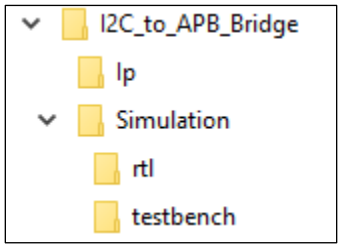

Figure 5.1. Directory Structure

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6. Installing the .ipk Design File

This reference design is in *.ipk* file format and installed within Lattice Propel Builder.

To install the design:

1. Choose **File > New Design** from the Lattice Propel Builder menu bar. The **Create System Design** wizard opens in the **Design Information** page, as shown in Figure 6.1.

   The default Project Type is displayed in the **Type** field.
2. Enter the project name in the **Name** field.
3. The default location is shown in the **Location** field. Use the **Browse…** option to change the project workspace location.
4. Click **Next**.

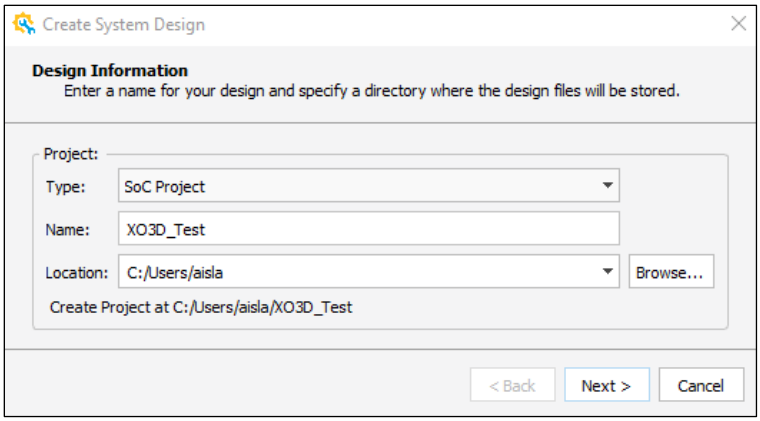

Figure 6.1. Design Information Page

5. In the **Configure Propel Project** page, select a device for the project. Refer to Table 1.1.

   Use the drop-down menu to select device information (**Family**, **Device**, **Package**, and **Speed**).

   Select **Empty Project** in the **Templates** field.
6. Click **Next**.

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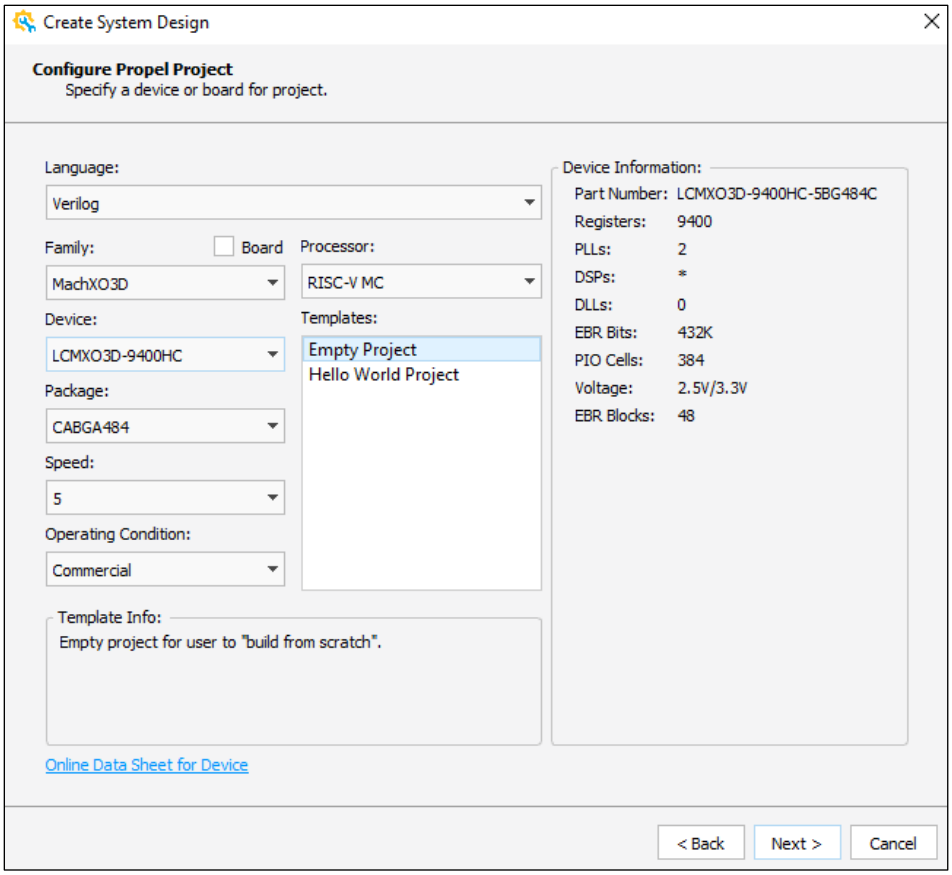

Figure 6.2. Configure Propel Project Page

7. In the **Project Information** page, review the details of the project.
8. Click **Finish**.

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9. In the **IP Catalog** area of the main user interface, click the **Install** button.

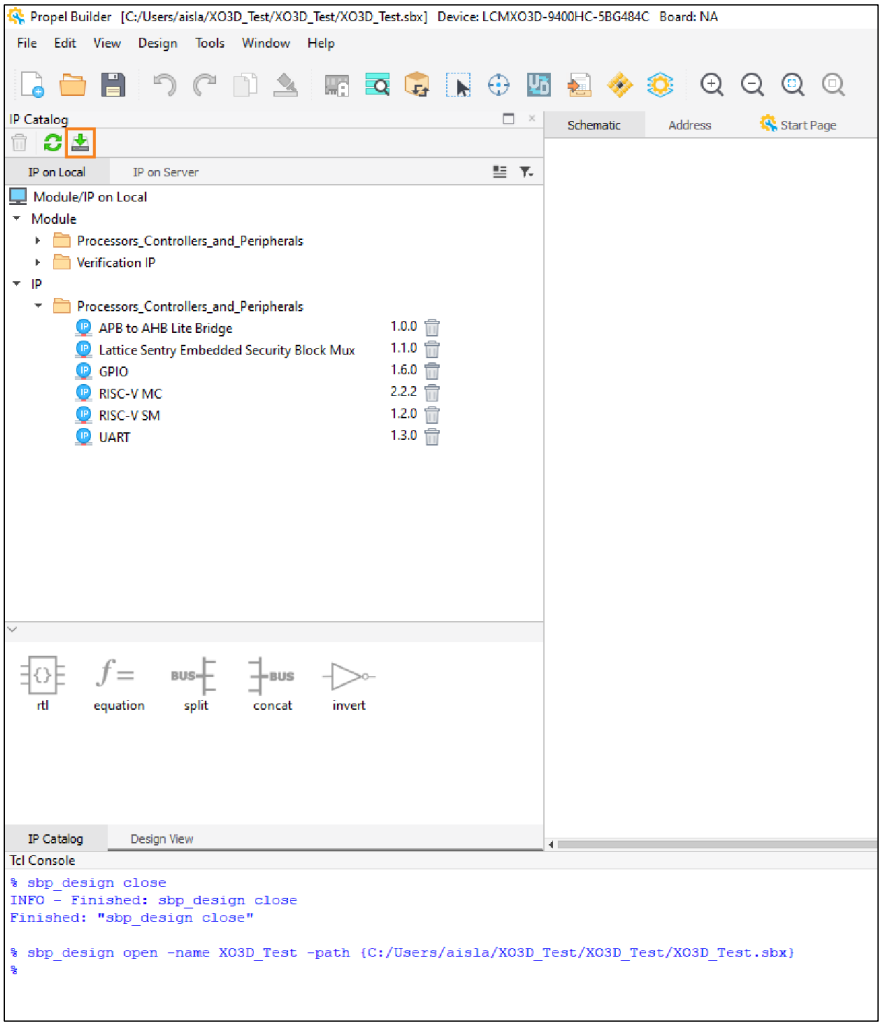

Figure 6.3. IP Catalog View

10. In the **Select User IP Package File to Install** dialog box, select the *.ipk* file and click **Open**.

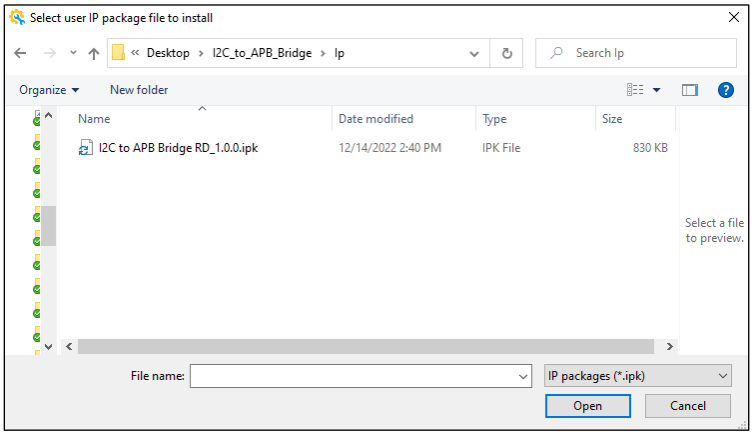

Figure 6.4. Select User IP Package File to Install Dialog Box

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11. After installation, **I2C to APB Bridge RD** is listed under **IP > Processors_Controllers_and_Peripherals**. Double-click the item and follow the **Module/IP Block Wizard** to add the IP to the design.

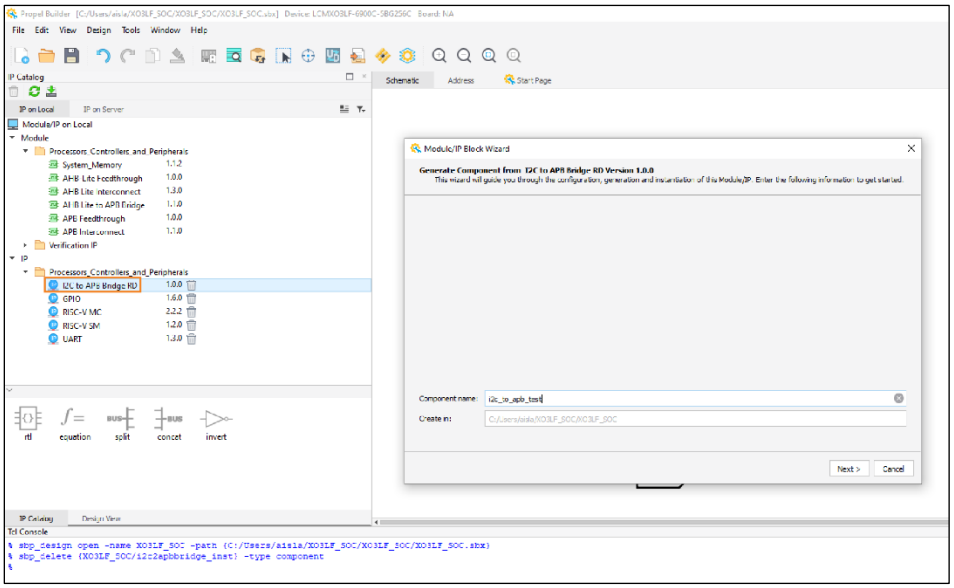

Figure 6.5. Module/IP Block Wizard

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7. Using the .do Simulation Script File

This reference design includes pre-generated RTL files that can be directly simulated within ModelSim or QuestaSim. QuestaSim is supported starting from Lattice Diamond software version 3.14 and later.

To use the simulation script file:

1. Open the *.do* file on a text editor and replace the text SET THE SIMULATION PATH HERE from Line 1 with the directory path of the simulation file. As an example, see Line 4 in Figure 7.1.

```
1  set SIM_DIR "SET THE SIMULATION PATH HERE "
2
3  # Example:
4  # set SIM_DIR "D:/I2C_to_APB_Bridge_/Simulation"
```

Figure 7.1. Changing the Simulation Directory

2. Open ModelSim Lattice FPGA Edition.
3. Click **Tools > Tcl > Execute Macro**.

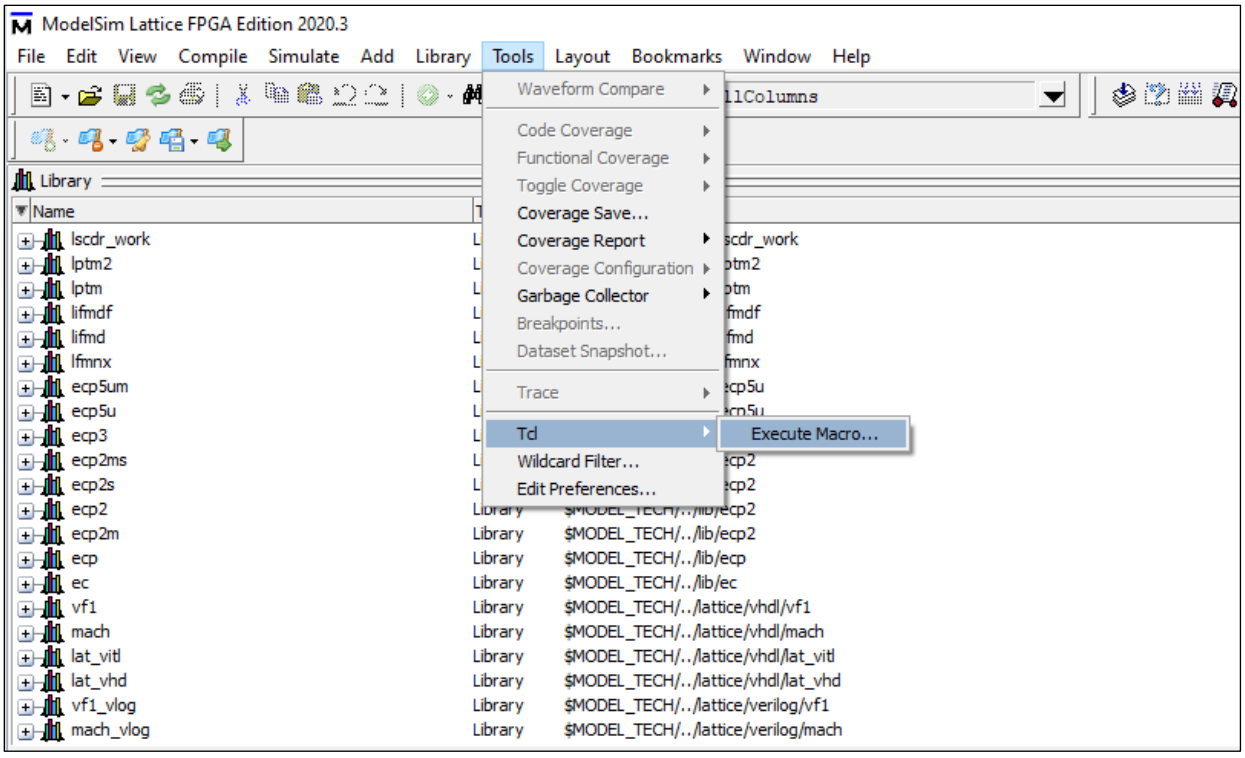

Figure 7.2. Running the Simulation Script File

4. The simulation waveform is generated.

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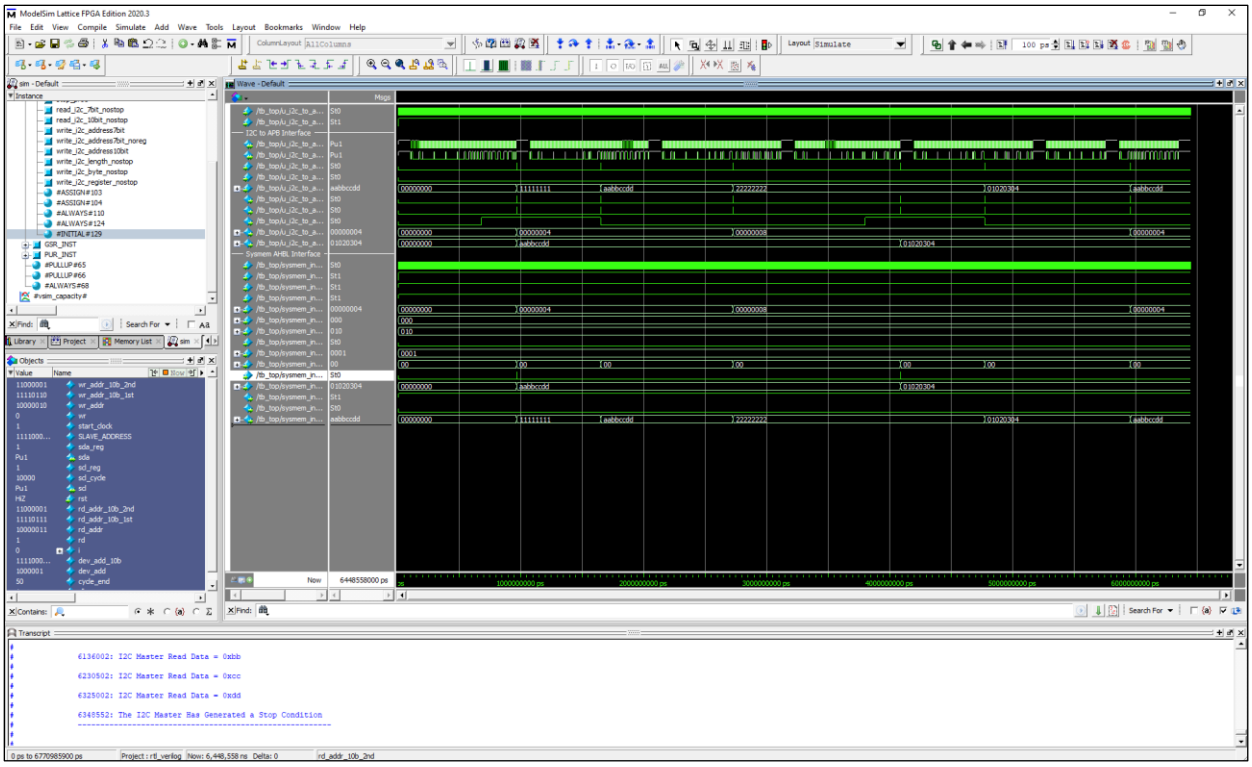

Figure 7.3. Simulation Waveform

Figure 7.4 shows a detailed view of the first I2C transaction following the Write Operation Data Format mentioned in the Write Operation section.

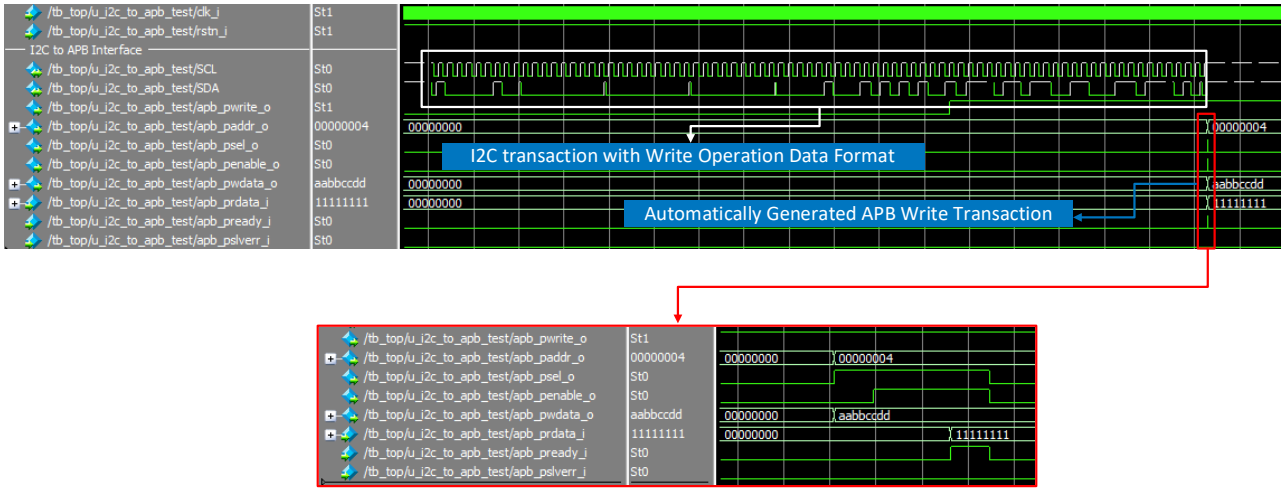

Figure 7.4. I2C to APB (Write) Conversion

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Figure 7.5 shows a detailed view of the second I2C transaction following the Read Operation Data Format mentioned in the Read Operation section.

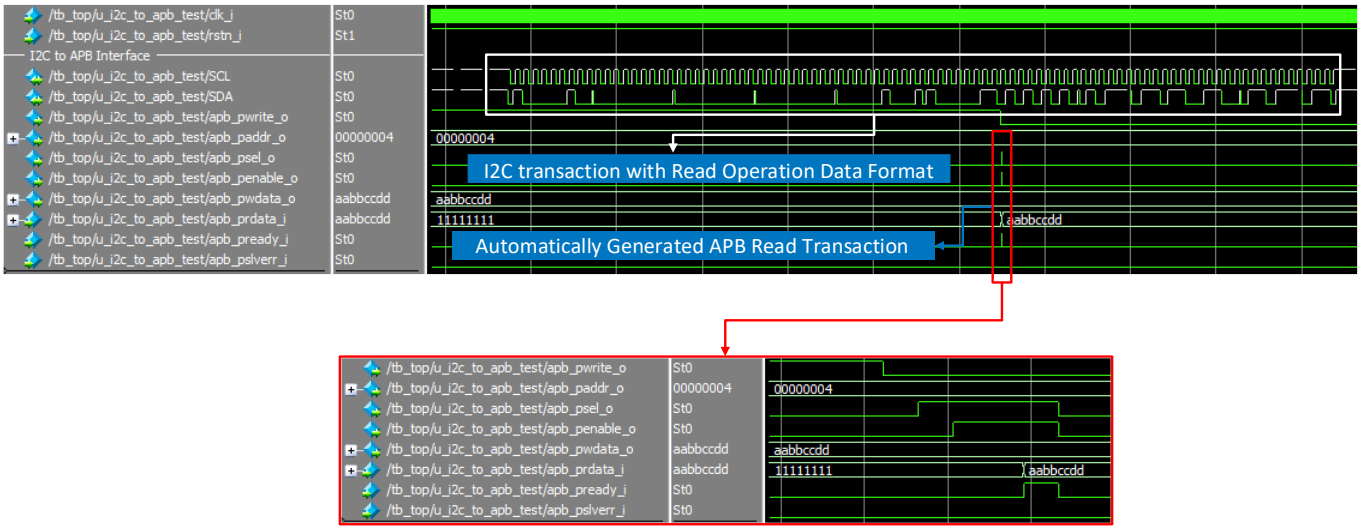

Figure 7.5. I2C to APB (Read) Conversion

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8. Resource Utilization

Table 8.1. Resource Utilization

Device Family	Language	LUTs	Registers	Fmax (MHz)
MachXO2[1]	Verilog	212	205	>50
MachXO3[2]	Verilog	212	205	>50
MachXO3D[3]	Verilog	212	205	>50

Notes:

1. Performance and utilization characteristics are generated using LCMXO2-7000HE-4TG144C with Lattice Diamond 3.12 design software with either LSE (Lattice Synthesis Engine) or Synplify Pro®.
2. Performance and utilization characteristics are generated using LCMXO3LF-6900C-5BG256C with Lattice Diamond 3.12 design software with either LSE (Lattice Synthesis Engine) or Synplify Pro.
3. Performance and utilization characteristics are generated using LCMXO3D-9400HC-5BG256C with Lattice Diamond 3.12 design software with either LSE (Lattice Synthesis Engine) or Synplify Pro.

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References

- MachXO2 web page
- MachXO3 web page
- MachXO3D web page
- Lattice Solutions Reference Designs web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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Revision History

Revision 1.1, June 2025

Section	Change Summary
All	• Added *Reference Design User Guide* to the document title. • Minor adjustments to ensure that the document is consistent with Lattice Semiconductor's inclusive language policy. • Updated *I²C* to *I2C*. • Made editorial fixes.
Disclaimers	Updated boilerplate.
Inclusive Language	Added boilerplate.
Using the .do Simulation Script File	Updated the introductory paragraph in this section.
References	Updated this section.

Revision 1.0, January 2023

Section	Change Summary
All	Initial release.

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