MachXO5-NX Hardware Checklist

Technical Note

FPGA-TN-02274-1.8

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
BGA	Ball Grid Array
CIB	Configuration Interface Block
DC	Direct Current
DLL	Delay-Locked Loop
DM	Data Mask
DQ	Data Queue
DQS	Data Strobe
DRR3	Double Data Rate 3
ECDSA	Elliptic Curve Digital Signature Algorithm
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
GPLL	General Purpose Phase-Locked Loop
HCSL	High-Speed Current Steering Logic
HPIO	High Performance I/O
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IBIS	I/O Buffer Information Specification
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
NDA	Non-Disclosure Agreement
OSC	Oscillator
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POR	Power-On Reset
RST	Reset
SCL/SDA	Serial Clock/Serial Data
SERDES	Serializer/Deserializer
SI	Signal Integrity
SLVS	Scalable Low-Voltage Signaling
SSPI	Slave Serial Peripheral Interface
SSTL	Stub Series-Terminated Logic
USB	Universal Serial Bus
WRIO	Wide Range I/O

1. Introduction

When designing complex hardware using the MachXO5™-NX device, you must pay close attention to critical hardware configuration requirements. This technical note outlines these critical hardware implementation items specific to the MachXO5-NX device. It does not provide detailed step-by-step instructions but offers a high-level checklist to support the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that you are familiar with the MachXO5-NX device features as described in the MachXO5-NX Family Data Sheet (FPGA-DS-02102). The data sheet includes the functional specifications for the device. Topics covered in the data sheet include, but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions.
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to the MachXO5-NX Family Data Sheet (FPGA-DS-02102) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the MachXO5-NX power supply rails and how to connect them to the PCB and the associated system.
- Configuration mode selection for proper power-up behavior.
- Device I/O interface and critical signals.

Important: Refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- Thermal Management (FPGA-TN-02044)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- MachXO5-NX-related pinout information can be found on the MachXO5-NX webpage.
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)

2. Power Supplies

At power up, LFMXO5-25/35/65/35T/65T devices monitor the V_{CC}, V_{CCAUXA}, V_{CCIO1}, and V_{CCIO2} power supplies to determine when MachXO5-NX should de-assert its internal Power-On Reset state and enter the Power Good condition, initiating device initialization and configuration. LFMXO5-55T/100T devices monitor the V_{CC}, V_{CCAUXA}, V_{CCIO0}, and V_{CCIO1} power supplies. These supplies must rise monotonically. Although the device does not monitor other supplies during power-up, they must reach valid and stable levels before the device configuration completes.

Several other supplies are used in conjunction with onboard ADCs and the SERDES blocks which are available in part numbers containing a *T* for *Transceiver*.

Table 2.1 describes the LFMXO5 power supplies and the appropriate voltage levels for each supply.

Table 2.1. LFMXO5 Power Supplies

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCECLK}	1.0 V	FPGA core clock power supply.
V_{CCAUX}	1.8 V	Auxiliary power supply pin for WRIO Banks. Used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	1.8 V	Auxiliary power supply pin for HPIO Banks. Used for generating stable drive current for the I/O and stable current for the differential input comparators.
V_{CCAUXA}	1.8 V	Auxiliary supply voltage for internal analog circuitry. Required for Power Good condition.
$V_{CCIO[11, 9:0]}$ LFMXO5-25/35/65/35T/65T	Wide-Range Banks: Bank 1: 3.3 V Only Banks 0, 2, 3, 4, 7, 8, 9, 11: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V High-Speed Banks: Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V	Bank I/O driver supply voltage. Each bank has its own V_{CCIO} supply. V_{CCIO1} and V_{CCIO2} have pins used for device configuration and are required for Power Good condition.
$V_{CCIO[7 0]}$ LFMXO5-55T/100T	Wide-Range Banks: Bank 0: 3.3 V Only Banks 1, 2, 6, 7: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V High-Speed Banks: Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V	Bank I/O driver supply voltage. Each bank has its own V_{CCIO} supply. V_{CCIO0} and V_{CCIO1} have pins used for device configuration and are required for Power Good condition.
$V_{CCADC18}$	1.8 V	ADC block power supply. Should be isolated from excessive noise.
ADC_REFP[1:0]	1.0 V to 1.8 V Typical	ADC external reference. Should be isolated from excessive noise and have high accuracy (< 0.1%).
V_{CCSDx} *T Parts Only*	1.0 V	SERDES block core power supply voltage. Should be isolated from excessive noise.
V_{CCSDCK} *T Parts Only*	1.0 V	SERDES block clock buffer supply voltage. Should be isolated from excessive noise.
$V_{CCPLLSDx}$ *T Parts Only*	1.8 V	SERDES Block PLL power supply voltage. Should be isolated from excessive noise.
$V_{CCAUXSDQx}$ *T Parts Only*	1.8 V	SERDES block auxiliary power supply voltage. Should be isolated from excessive noise.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage
- Expected voltage drops due to power filtering the ferrite bead's ESR x expected current draw
- Expected voltage drops due to the current measuring resistor's ESR x expected current draw

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is particularly sensitive to noise, as every 10 mV represents 1% of the rail voltage. For SERDES power rails, it is recommended to target a maximum 1% peak noise. For PLLs, they target less than 0.5% peak noise to minimize jitter.

3. Power Supply Filtering

Providing a quiet, filtered supply is important for all rails and critical for analog rails. Supplies should be decoupled with adequate power filters. Place bypass capacitors as close as possible to the device package pins, using short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB-related crosstalk with sensitive blocks are related to FPGA outputs found in close proximity to the sensitive power supplies. These supplies require a cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

It is critical to have very low-noise, highly filtered supplies for the MachXO5-NX SERDES and ADCs. These supplies are also paired with dedicated ground pins.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCECLK}	10 µF x 2 + 100 nF per pin	Core and clock logic. Tie V_{CC} and V_{CCECLK} pins together. 1.0 V
V_{CCAUX}, $V_{CCAUXHx}$	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pins. Tie V_{CCAUX} and $V_{CCAUXHx}$ pins together. 1.8 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for internal sensitive analog circuitry. 1.8 V
$V_{CCIO[11, 9:0]}$	10 µF + 100 nF per pin for each V_{CCIOx}	Bank I/O. Unused banks can use a single 1.0 µF. For banks with many outputs or large capacitive loads, replace the 10 µF capacitor with a 22 µF capacitor or use two 10 µF capacitors. LFMXO5-25/35/65/35T/65T Bank 1: 3.3 V only Banks 0, 2, 3, 4, 7, 8, 9, 11: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V LFMXO5-55T/100T Bank 0: 3.3 V only Banks 1, 2, 6, 7: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V
$V_{CCADC18}$	220 Ω or 120 Ω FB + 10 µF + 100 nF per pin	ADC Blocks. Powering $V_{CCADC18}$ enables the device to read the internal temperature and voltage rails. If both ADC blocks are not used, and reading the internal temperature and voltage rails are not required then, leave $V_{CCADC18}$ open. 1.8 V
ADC_REFP[1:0]	220 Ω or 120 Ω FB + 1.0 µF + 100 nF per pin	ADC Block External Reference. Must have very low noise and high accuracy reference (≤ 0.1% Tolerance). Voltage source/regulator should be filtered by 220 Ω or 120 Ω FB + 1 µF. If ADC Block is not used, connect ADC_REFPx to ground through 0 Ω resistor. 1.0 V to 1.8 V Typical

Power Input	Recommended Filter	Notes
V_{CCSDx} *T Parts Only*	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Core. If SERDES block is not used, leave open. 1.0 V
V_{CCSDCK} *T Parts Only*	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Clock buffer. If both SERDES blocks are not used, leave open. 1.0 V
$V_{CCPLLSDx}$ *T Parts Only*	220 Ω FB + 47 µF + 470 nF per pin IMPORTANT: Connect capacitor grounds only to FPGA pin SDx_REFRET	SERDES Block PLL. If SERDES block is not used, leave open. Route bypass capacitor grounds only to SDx_REFRET. 1.8 V
$V_{CCAUXSDQx}$ *T Parts Only*	120 Ω FB + (10 µF and 100 nF to each channel's SDx_REFRET)	SERDES Block Auxiliary. If SERDES block is not used, leave open. Route bypass capacitor grounds only to SDx_REFRET. 1.8 V

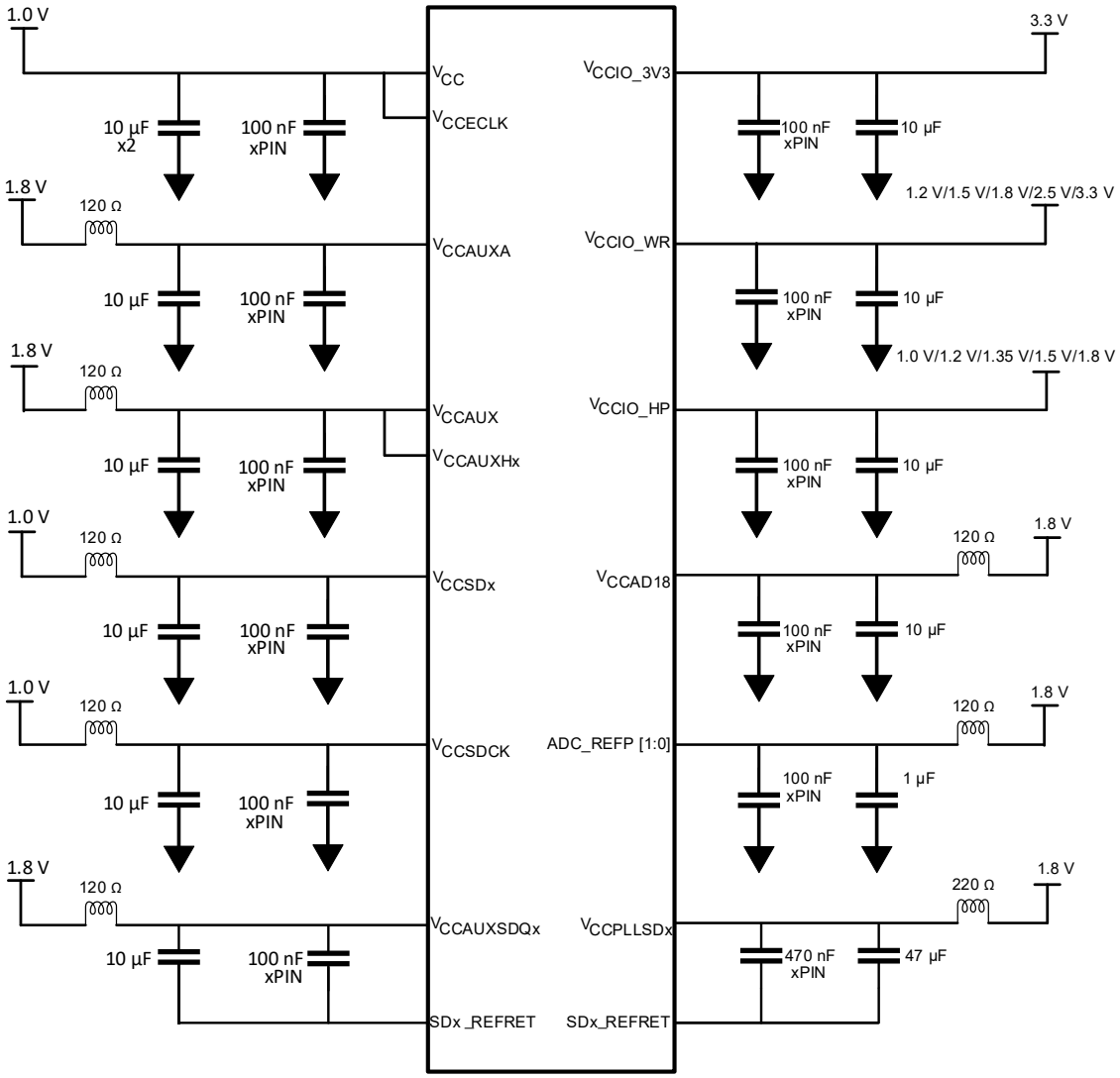

Figure 3.1. Recommended Power Filter

3.2. Ground Pins

- Connect all ground pins to the board's ground plane.
- V_{SSSDx} and V_{SSADC} pins are sensitive to noise and must be isolated from fast-switching, high-current path on the ground plane. Use ground plane islands to isolate sensitive grounds from noisy ground areas. Connect each ground plane island to the main ground plane at only one location, and ensure the connection is at least 2 mm wide. Only signals that belong to the same domain as the ground plane island should reference that island.
- SDx_REFRET — SERDES Reference Return Input. AC coupled (bypass) this pin to the $V_{CCPLLSDx}$ supply.

3.3. Unused Bank V_{CCIOX}

- Connect unused V_{CCIOX} pins to a power rail. Do not leave them open.

3.4. Unused ADC Blocks

- Powering $V_{CCADC18}$ enables the device to read internal temperature and voltage rails.
  If both ADC blocks are not used, and reading internal temperature and voltage rails are not required then, leave $V_{CCADC18}$ open.
- For unused ADC blocks, connect ADC_REFPx, ADC_DPx, and ADC_DNx to board ground.
- Connect V_{SSADC} pins to the board's ground plane, even if the ADC blocks are unused.

3.5. Unused Both SERDES Quads

- Connect V_{SSSDQ} pins, SDx_RXDP/N [x=0 and 3], SDx_REXT [x=0 and 3], SDx_REFRET [x=0 and 3], and SDQ0_REFCLKP/N to board ground.
- Leave the following open: V_{CCSDx} [x=0 and 3], $V_{CCPLLSDx}$ [x=0 and 3], SDx_TXDP/N [x=0 and 3], $V_{CCAUXSDQ0}$, and V_{CCSDCK}.

3.6. Single Unused SERDES Channels

- Connect V_{SSSDQ} pins to board ground, along with the unused channel's SDx_RXDP/N [x=0 or 3], SDx_REXT [x=0 or 3], and SDx_REFRET [x=0 or 3].
- Leave the following open on the unused channel: V_{CCSDx} [x=0 or 3], $V_{CCPLLSDx}$ [x=0 or 3], SDx_TXDP/N [x=0 or 3].

3.7. Clock Oscillator Supply Filtering

When supplying an external reference clock to the FPGA—such as from a single-ended or differential clock oscillator, ensure proper power supply isolation and decoupling of the oscillator.

When selecting components, choose *good-quality* ceramic capacitors in small packages, and place them close to the oscillator's power supply pins. In most cases, *good-quality* bypass capacitors meet the requirement.

3.8. Ferrite Bead Selection

- Most designs perform well with ferrite beads rated between 120 Ω and 240 Ω at 100 MHz.
- The noise voltage induced by a ferrite bead calculated as ESR × CURRENT, should be less than 1% of rail voltage for non-analog rails and less than < 0.25% for sensitive rails.
- For non-PLL rails, use ferrite beads with an ESR between 0.025 Ω and 0.10 Ω, depending on the current load.
- PLL rails, which draw low current, can use ferrite beads with an ESR ≤ 0.3 Ω.
- Smaller package-size ferrite beads have higher ESR than larger ones of the same impedance.
- Higher impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

3.9. Capacitor Selection

When selecting components, choose good-quality ceramic capacitors in small packages, and place them close to the oscillator's power supply pins using short, low inductance connections. In most cases, good quality bypass capacitors meet the requirements discussed in the following sections.

3.9.1. Capacitor Dielectric

Use dielectrics such as X5R, X7R, and similar types that maintain good capacitance tolerance (≤ ±20%) across the operating temperature range. Avoid Y5V, Z5U, and other similarly poor capacitance-controlled dielectrics.

3.9.2. Voltage Rating

Capacitor working capacitance decreases non-linearly under higher voltage bias. To maintain effective capacitance, select capacitors with a voltage rating at least 80% higher than the maximum voltage rail of the rail. Example: For a 3.3 V rail, use bypass capacitors rated at 6.3 V or higher.

3.9.3. Size

Smaller body capacitors offer lower inductance, operate at higher frequencies, and enhance the board layout. At the same voltage rating, smaller body capacitors typically cost more than larger ones. To balance market pricing and size-related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF, 1.0 µF, 2.2 µF	0201	0402
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0603	0805

4. Power

There is no power-up sequence required for the MachXO5-NX device.

5. Power Estimation

Once you finalize the MachXO5-NX device density, package, and logic implementation, power estimation for the system environment should be determined using the Power Calculator included in the Lattice Radiant™ design tool. When performing power estimating, you should keep two goals in mind:

- Power supply budgeting must be based on the maximum power-up in-rush current, configuration current, and maximum DC and AC current under the system's environmental conditions.
- Thermal considerations are also important. Ensure the system environment and the MachXO5-NX device can operate at the maximum operating junction temperature.

Consider both criteria early in the design phase to ensure reliable system performance.

6. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024). For application-specific assembly guidance, consult the design guidelines of the assembly service provider.

The MachXO5-NX device supports FPGA configuration either through the JTAG interface or through various modes using the sysCONFIG port. The JTAG interface consists of four pins and requires the following PCB considerations.

Table 6.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI/SI	4.7 kΩ to 10 kΩ pull-up to V_{CCIO}[1]
TMS/SCSN	4.7 kΩ to 10 kΩ pull-up to V_{CCIO}[1]
TDO/SO	4.7 kΩ to 10 kΩ pull-up to V_{CCIO1}[1]
TCK/SCLK	2.2 kΩ pull-down to GND
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO}[1] (JTAG port enabled)

Note:

1. Use V_{CCIO1} for LFMXO5-55T/100T and use V_{CCIO2} for LFMXO5-25/35/65/35T/65T.

It is recommended that every PCB provides easy access to the FPGA's JTAG pins, even if the JTAG is not the primary configuration interface. This JTAG port is useful for debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header, along with the corresponding V_{CCIO} and ground.

External resistors are required on configuration signals when they are used for handshaking with other devices. However, external pull-resistors are not needed on individual configuration pins if the signal is not held active.

Pull-up resistors to the appropriate bank V_{CCIO} and pull-down resistors to board ground are recommended for the pins listed in Table 6.2.

Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ to 10 kΩ pull-up to V_{CCIO}[2]
INITN	4.7 kΩ to 10 kΩ pull-up to V_{CCIO}[2]
DONE	4.7 kΩ to 10 kΩ pull-up to V_{CCIO}[2]
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO}[3] (JTAG port enabled)
TMS/SCSN	4.7 kΩ to 10 kΩ pull-up to V_{CCIO}[3]
SCL/SDA[1]	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO}[3]

Notes:

1. Pull-up resistors are not required in target I3C configuration mode.
2. Use V_{CCIO0} for LFMXO5-55T/100T and use V_{CCIO1} for LFMXO5-25/35/65/35T/65T.
3. Use V_{CCIO1} for LFMXO5-55T/100T and use V_{CCIO2} for LFMXO5-25/35/65/35T/65T.

Table 6.3. Configuration Pins Needed per Programming Mode[1]

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
JTAG	1	JTAG_EN pin[2]	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key[2]	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

Notes:

1. Leave unused configuration ports open.
2. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

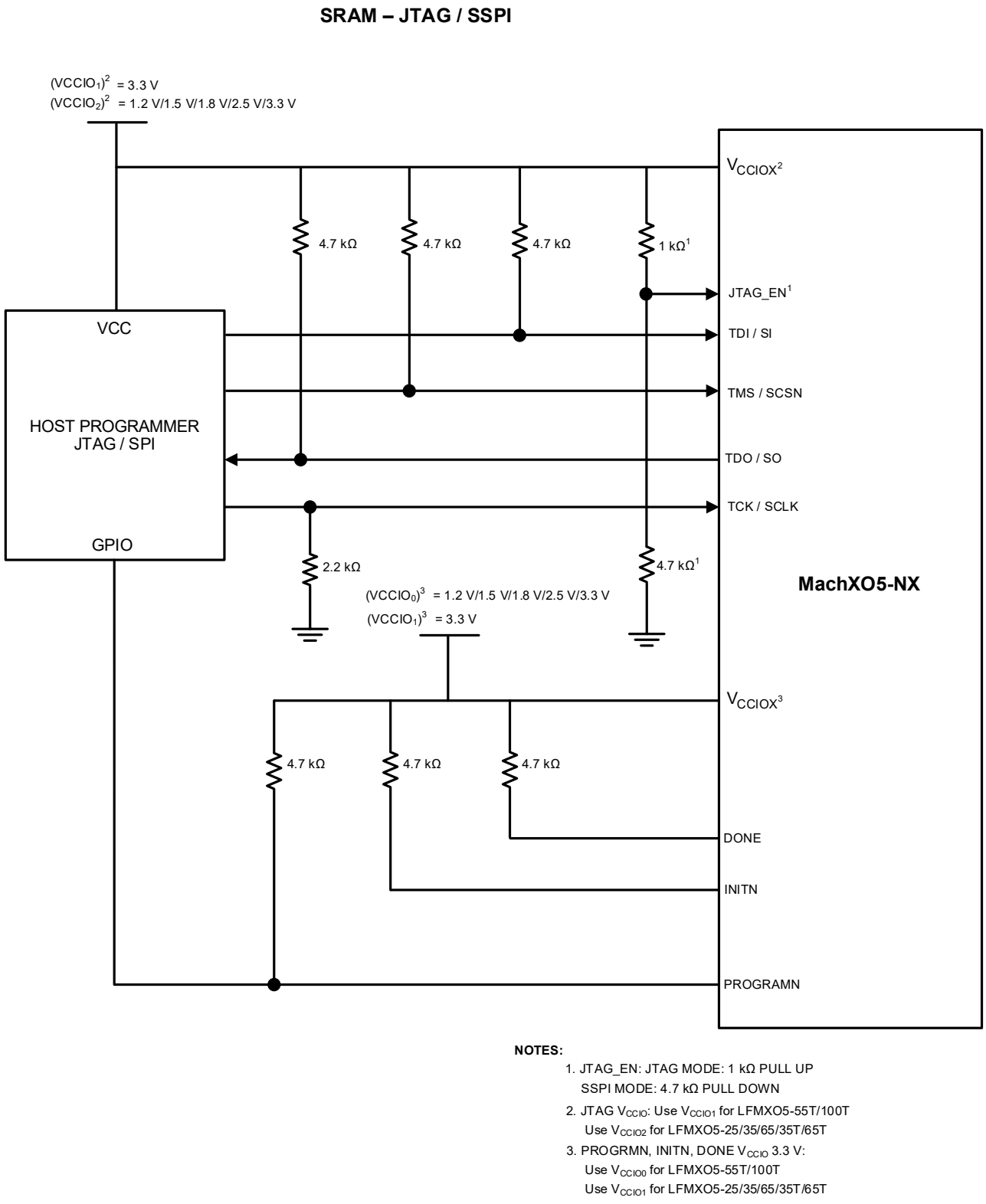

Figure 6.1. Typical Connections for Programming SRAM / FLASH via JTAG / SSPI

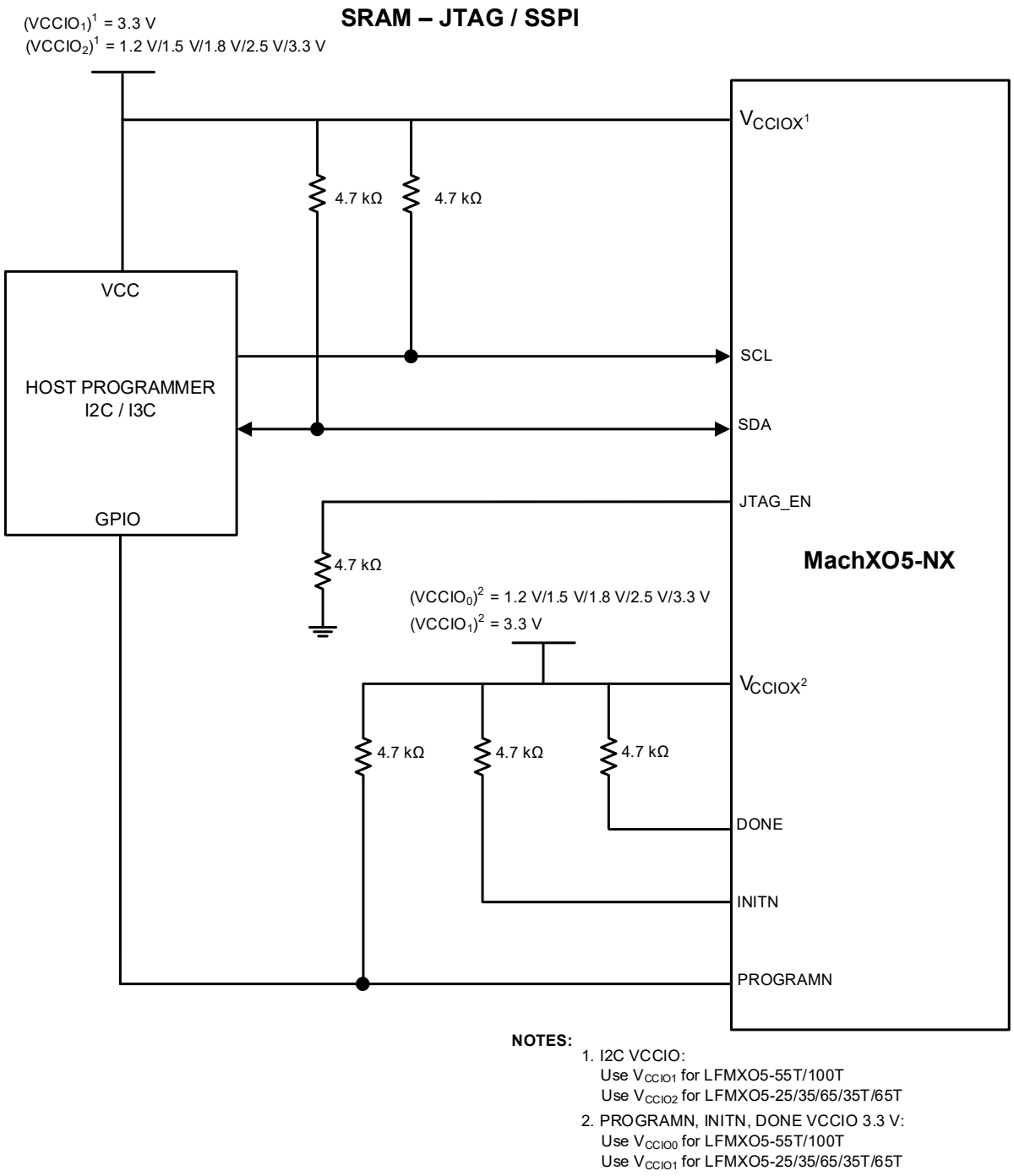

Figure 6.2. Typical Connections for Programming SRAM / FLASH via I2C / I3C

7. I/O Pin Assignments

The V_{CCSDCK}, $V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ provide low-noise power supplies for the SERDES blocks. To achieve optimal jitter performance, assign pins carefully to avoid placing noisy I/O signals near sensitive pins. A primary cause of PCB-induced SERDES crosstalk is the close placement of FPGA output pins near SERDES power supplies. These supplies require meticulous PCB layout to maintain noise immunity against switching noise from FPGA outputs. While guidelines are available for designing quiet, filtered power supplies, a robust PCB layout is essential to prevent noise from coupling into these sensitive analog supplies.

Although the MachXO5-NX devices packages help reduce crosstalk-induced coupling, the PCB layout can still introduce significant noise from I/O pins located near SERDES data, reference clock, power pins, or other critical I/O signals such as clocks. The Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing the hardware design to minimize crosstalk into analog supplies. PCB traces that run in parallel over long distances require careful analysis. Use a PCB crosstalk simulation tool to evaluate any potentially problematic traces and determine their impact.

It is common practice for system designers to define pinouts early in the design cycle. For the FPGA designers, this step requires a thorough understanding of the target FPGA device. Designers often begin by capturing the I/O list in a spreadsheet application. To support this process, Lattice Semiconductor provides detailed pinout data in downloadable .csv format from the Lattice website. By accessing the pinout.csv file, you can obtain comprehensive pinout information for all package variants within a device family. This includes I/O bank assignments, differential pairing, dual function of the pins, and input and output characteristics.

7.1. Early I/O Release

The MachXO5-NX device supports the Early I/O release feature, which enables I/O pins located in the left and right I/O banks to assume user-defined drive states early in the bitstream processing sequence. Specifically, this applies to LFMXO5-25/35/65/35T/65T devices (Banks 2, 3, 4, 7, 8, 9) and LFMXO5-55T/100T devices (Banks 1, 2, 6, 7). The feature activates after the I/O configuration data for these banks—located near the beginning of the bitstream—is processed. Once the left/right Memory Interface Block (MIB) is programmed, the corresponding I/O pins are released to their predefined states. To enable this feature, set the EARLY_IO_RELEASE preferences to ON in the Lattice Radiant Device Constraint Editor.

In addition, using the Early I/O Release feature requires instantiating an output buffer register with an asynchronous set or reset function to define the desired drive behavior—logic high (1) or logic low (0), respectively—during the early release period. Unregistered outputs in Early-Release banks will remain in High-Z (high impedance) state until the full device configuration is complete. Note that certain dual-purpose sysCONFIG I/O pins cannot be used for Early I/O Release. Refer to the device pinlist .csv file to identify which pins supports this feature. Additionally, if ECDSA bitstream authentication is enabled on the MachXO5-NX device, the Early I/O Release feature is not supported.

8. sysI/O

MachXO5-NX provides the flexibility to configure each I/O according to the user's requirements. These pins can be configured as input, output, and tri-state. Additionally, attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can also be set up.

For PULLMODE, pull-up and pull-down resistors can be set. The implementation of these resistors is by using a constant current that has the following values:

Table 8.1. Weak pull-up/down current specifications

Configuration	Parameter	Condition	Min	Max	Unit
Pull-up	I/O Weak pull-up resistor current	$0 \le VIN \le 0.7 \times V_{CCIO}$	–30	–150	µA
Pull-down	I/O Weak pull-down resistor current	$VIL\ (max) \le VIN \le V_{CCIO}$	30	150	µA

The MachXO5-NX also features specialized I/O types, such as HPIO and WRIO which support high-speed communication applications.

Figure 8.1 shows the block diagram for HPIO and Figure 8.2 shows the block diagram for WRIO.

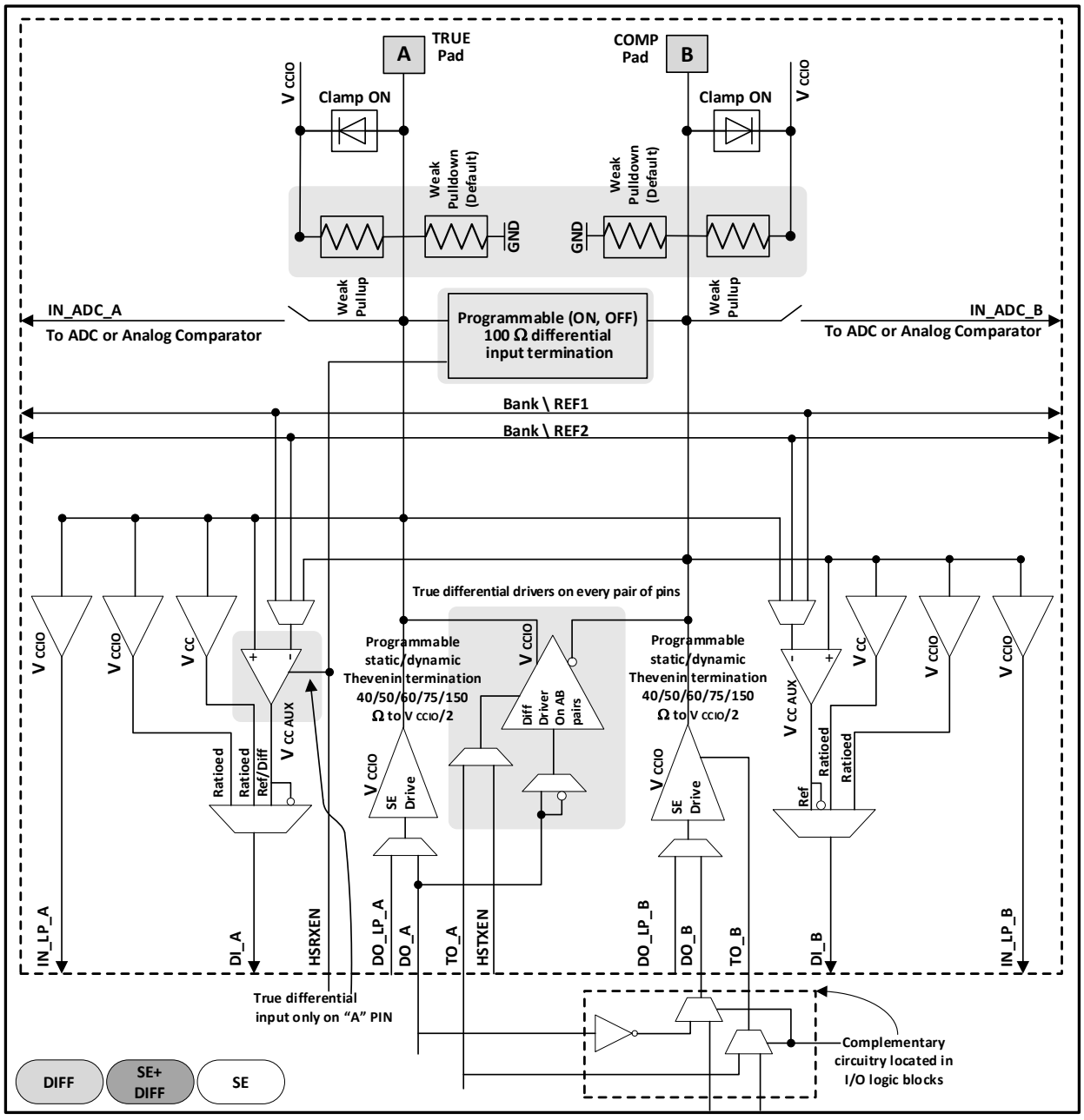

Figure 8.1. High-Performance sysI/O Buffer Pair for Bottom Side

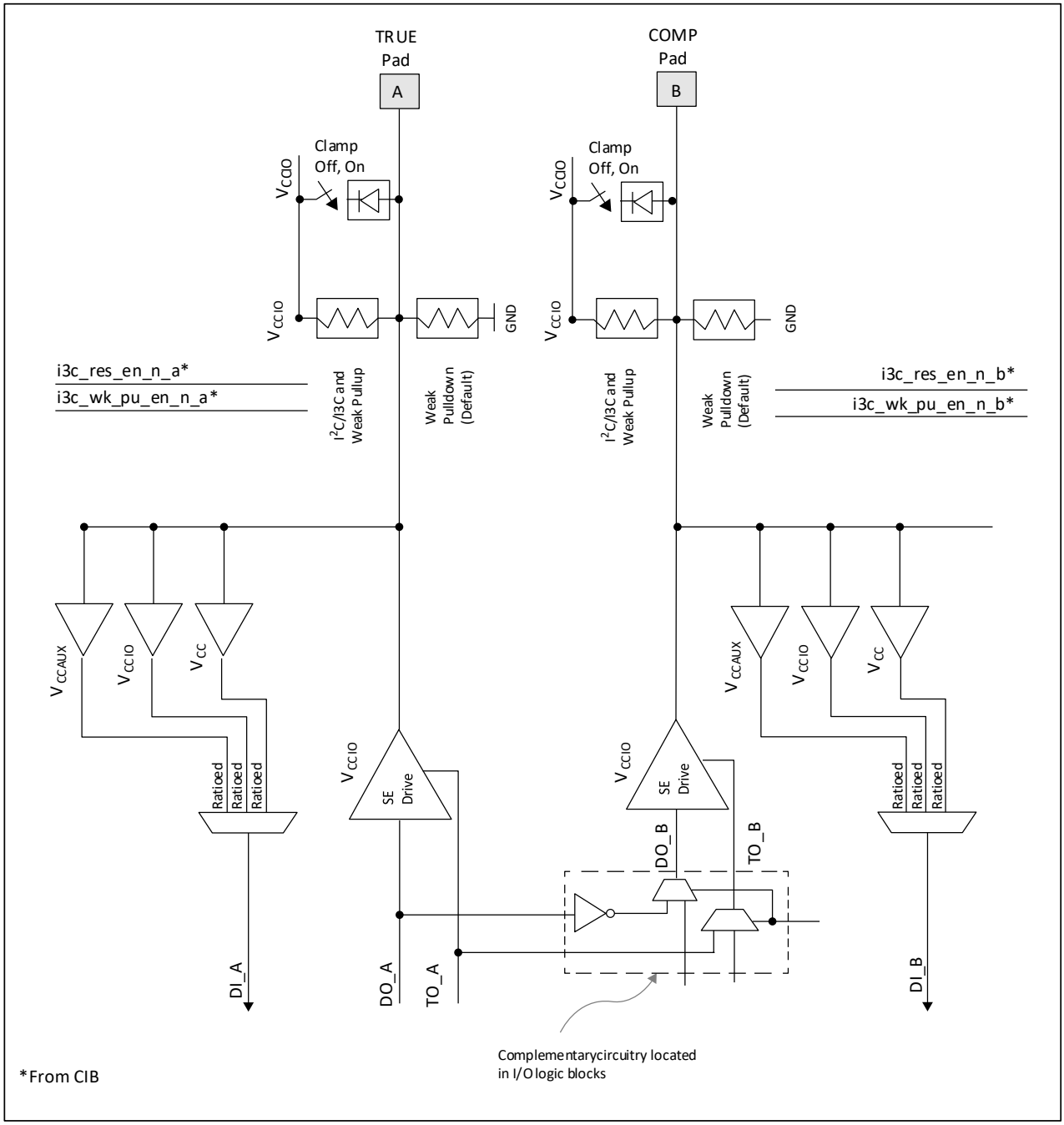

Figure 8.2. Wide Range sysI/O Buffer for Top, Left / Right Side

9. Clock Inputs

The MachXO5-NX device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for general-purpose I/O. When these pins are used for clocking purposes, the user needs to pay attention to minimize signal noise on these pins. Refer to the MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286).

These shared clock input pins, typically labeled GPLL and PCLK, are listed under the Dual Function column of the pinlist .csv file. High-speed differential interfaces (such as MIPI) must route their differential clock pairs into inputs that support differential clocking, specially labeled as PCLKTx_y (+true) and PCLKCx_y (-complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitters. Figure 9.1 shows a typical bypassing circuit.

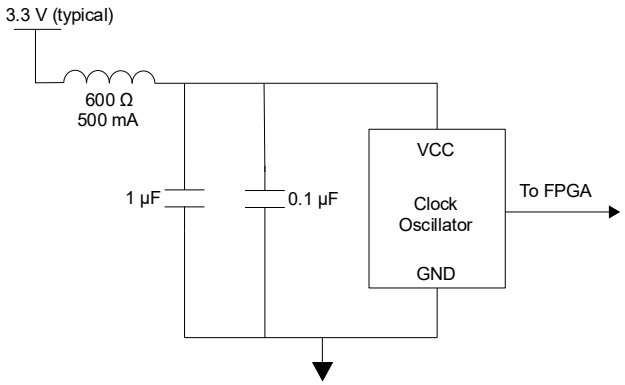

Figure 9.1. Clock Oscillator Bypassing

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS is shown below in Figure 9.2.

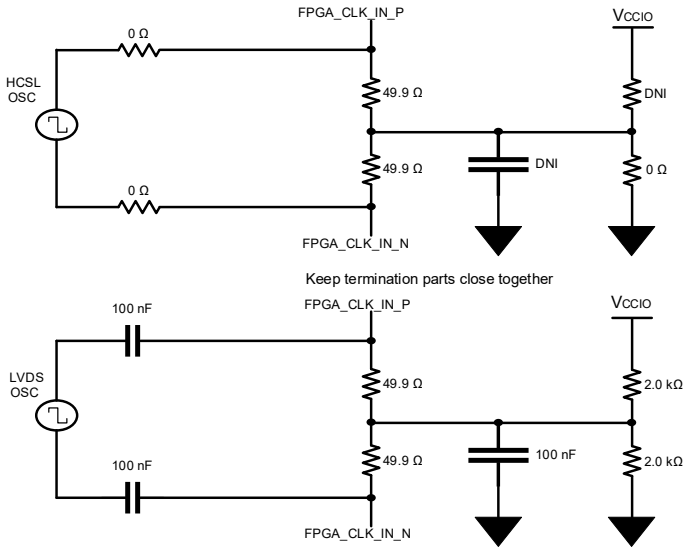

Figure 9.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

9.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enable pin is shown in Figure 9.3.

Note: External board oscillators typically require 5 to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

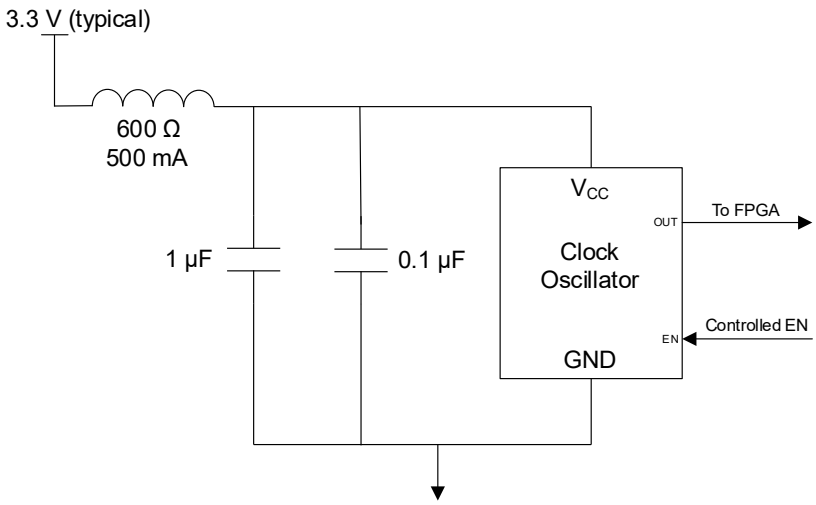

Figure 9.3. Clock Oscillator with Controlled Enable Pin

10. Pinout Considerations

The MachXO5-NX device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to the implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR3, clock resource connectivity, and PLL and DLL usage. Avoid placing noisy I/Os next to sensitive analog I/Os. Refer to MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286) for rules pertaining to these interface types.

10.1. LVDS Pin Assignments

True LVDS outputs are available on I/O pins on the device's bottom banks only (LFMXO5-25/35/65/35T/65T Banks 5, and 6 and LFMXO5-55T/100T Banks 3, 4, and 5). Top, left, and right side I/O banks do not support the True LVDS output standard. Differential input pairing can be found in the pin list csv file.

Emulated LVDS output is available in pairs around all banks and requires external termination resistors. This is described in the sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067).

10.2. HSUL, SSTL, and LVSTL[1] Pin Assignments

The HSUL, SSTL, and LVSTL1 interfaces are reference I/O standards that require an external reference voltage. HSUL, SSTL, and LVSTL1 are supported on the device's bottom banks only (LFMXO5-25/35/65/35T/65T Banks 5, and 6 and LFMXO5-55T/100T Banks 3, 4, and 5).

The VREF pin(s) should get high priority when assigning pins to the PCB. These pins can be found in the Dual Function column with the VREF label. Each bank includes a separate VREF voltage. VREF sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

Connect a 0.1 µF capacitor to ground close to each used VREF pin. The VREF power source should have a relatively low output impedance (≤ 130 Ω).

Note:

1. Only supported in LFMXO5-55T/100T devices.

11. DPHY and SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly length matched differential routing (no larger than ±4 mil length mismatch) with very few discontinuities.

The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. Refer to High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance. In the MachXO5-NX, the DPHY is a soft DPHY implementation.

12. Layout Recommendation

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

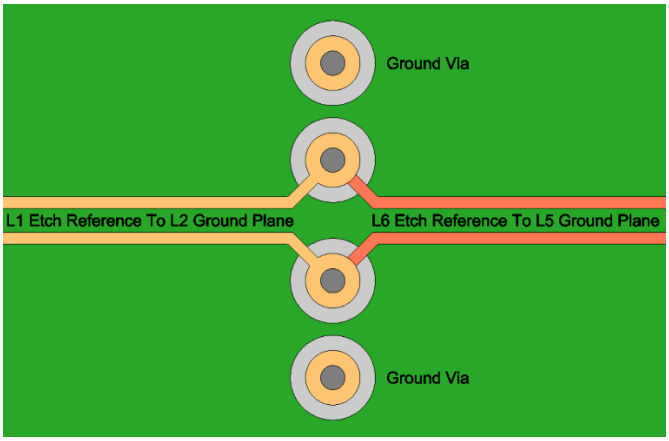

Figure 12.1. Ground Vias Implementation

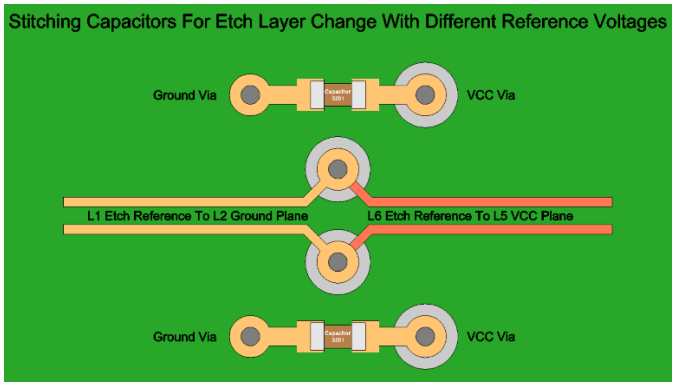

Figure 12.2. Stitching Vias Implementation

6. High-speed signals have a corresponding impedance requirement. Calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to +/-5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

13. Simulation and Board Measurement of Critical Signals

To ensure a design is reliable and will have high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

13.1. Critical Signals

Signals sensitive to Signal Integrity (SI) degradation are considered critical signals which require extra design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

13.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often have reoccurring subscription pricing. The expensive tools can import board design files and can easily supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (ex. Micro-cap) can supply useful basic simulations, but take extra effort to set up SI effects for multiple signals with different transmission line lengths, lossy transmission lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

13.3. Board Measurements

Critical signals should be measured on the actual PCB assembly using an Oscilloscope. Verify proper signaling function and signal integrity (that is, eye diagram, SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (ex. output series termination resistor value).
- Adjust the setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI).

14. Checklist

Table 14.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{CC} and V_{CCECLK} are tied together with a core voltage of 1.0 V ±3% (allowing for 2% noise).		
1.1.2	Use a PCB plane for V_{CC} and V_{CCECLK} core with proper decoupling.		
1.1.3	V_{CC} and V_{CCECLK} core sized to meet power requirement calculation from software.		
1.1.4	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} at 1.8 V ±3% (allowing for 2% noise).		
1.1.5	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} must be quiet and isolated from other switching noises.		
1.1.6	V_{CCAUX} pins ganged together with $V_{CCAUXHx}$ pins. Solid PCB planes are recommended.		
1.1.7	V_{CCAUXA} is sensitive, these pins should be ganged together and use a separate FB + Capacitor filtering. Solid PCB plane is recommended.		
1.2	I/O Supplies		
1.2.1	Wide Range V_{CCIO1} (LFMXO5-25/35/65/35T/65T) 3.3 V Only. Wide Range V_{CCIO0} (LFMXO5-55T/100T) 3.3 V Only.		
1.2.2	Wide Range V_{CCIOx} LFMXO5-25/35/65/35T/65T Banks 0, 2, 3, 4, 7, 8, 9, 11 are between 1.2 V to 3.3 V. Wide Range V_{CCIOx} LFMXO5-55T/100T Banks 1, 2, 6, 7 are between 1.2 V to 3.3 V.		
1.2.3	High Performance V_{CCIOx} LFMXO5-25/35/65/35T/65T Banks 5, 6 are between 1.0 V to 1.8 V. High Performance V_{CCIOx} LFMXO5-55T/100T Banks 3, 4, 5 are between 1.0 V to 1.8 V.		
1.2.4	V_{CCIOx} bank voltage matches sysCONFIG peripheral devices such as system I3C, SPI Flash, and the like.		
1.3	ADC power supply.		
1.3.1	$V_{CCADC18}$ is 1.8 V ±3% (allowing for 2% noise).		
1.3.2	$V_{CCADC18}$ is quiet and isolated.		
1.3.3	Use accurate voltage reference for ADC_REFP[1:0] (≤ ±0.1%).		
1.3.4	If both ADC blocks are not used, and reading internal temperature and voltage rails are not required then leave $V_{CCADC18}$ open.		
1.3.5	Unused ADC Blocks should connect ADC_REFPx, ADC_DPx and ADC_DNx to board ground.		
1.3.6	V_{SSADC} pin should connect to the board's ground plane even if ADC Blocks are unused.		
1.4	SERDES Power Supplies (T parts only)		
1.4.1	V_{CCSDx} and V_{CCSDCK} are at 1.0 V ±5%.		
1.4.2	V_{CCSDx} and V_{CCSDCK} are quiet and isolated from each other and other 1.0 V supplies.		
1.4.3	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ are 1.8 V +5%.		
1.4.4	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ quiet and isolated from each other and other 1.8 V supplies.		
1.4.5	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ bypass capacitor grounds go only to SDx_REFRET.		
1.4.6	Unused Both SERDES Channels Connect to board ground V_{SSSDQ} pins, SDx_RXDP/N [x=0 and 3], SDx_REXT [x=0 and 3], SDx_REFRET [x=0 and 3] and SDQ0_REFCLKP/N. Leave the following open: V_{CCSDx} [x=0 and 3], $V_{CCPLLSDx}$ [x=0 and 3], SDx_TXDP/N [x=0 and 3], $V_{CCAUXSDQ0}$, and V_{CCSDCK}.		
1.4.7	Single Unused SERDES Channel Connect to board ground V_{SSSDQ} pins, along with unused channel's SDx_RXDP/N [x=0 or 3], SDx_REXT [x=0 or 3], and SDx_REFRET [x=0 or 3]. Leave the following open on the unused channel: V_{CCSDx} [x=0 or 3], $V_{CCPLLSDx}$ [x=0 or 3], SDx_TXDP/N [x=0 or 3].		
1.5	Grounds		
1.5.1	All ground pins must be connected to low impedance ground plane.		

	Item	OK	NA
2	**JTAG**		
2.1	Pull-up or Pull-down on JTAG_EN, per Table 6.1.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development.		
2.4	Pull-down on TCK per Table 6.1.		
2.5	Pull-up on TMS per Table 6.1.		
3	**Configuration**		
3.1	Pull-ups or pull-downs on persisted configuration specific pins per Table 6.1 and Table 6.2.		
3.2	V_{CCIO} bank voltages matches sysCONFIG peripheral devices such as SPI Flash.		
4	**Special Pin Assignments**		
4.1	V_{REF} assignments followed for single-ended SSTL inputs.		
4.2	Properly decouple the V_{REF} source.		
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	Differential pair I/O polarity: I/O are named P[T/B/L/R] [Number]_[A/B] Diff pair positive signal connects to name ending in A, Negative connects to name ending in B.		
5.4	Differential clock inputs must use a PCLK pin so the clock input can be routed directly to the edge clock tree.		
5.5	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
5.6	Soft MIPI on HPIO banks only.		
6	**LPDDR3 and DDR3 Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
6.2	Maintain trace length matching to a maximum of ±20 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
6.3	All data groups must reference a ground plane within the stack-up.		
6.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
6.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed).		
6.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched to ±10 mil.		
6.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
6.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched within 10 mil.		
6.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
6.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
6.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		

	Item	OK	NA
6.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		
7	**ADC**		
7.1	When using ADC function, you must use the lower right corner PLL.		
8	**Clock Input**		
8.1	External clock source must be connected to PCLK or GPLL pins.		
8.2	PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the PLL Reference Clock Locking section for more details.		
9	**Layout Recommendations**		
9.1	Power should come from power planes to ensure good power delivery and thermal stability.		
9.2	Placement of analog circuits must be away from digital circuits or high switching components.		
9.3	High speed signals should target clearance of five times trace width from other signals.		
9.4	High speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are ground, else a stitching capacitor should be used.		
9.5	High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.		
10	**Simulation and Board Measurement of Critical Signals**		
10.1	Simulations: Use IBIS model to simulate critical signals for proper signal integrity.		
10.1.1	Simulate Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like).		
10.1.2	Simulate Clock nets (Oscillator Inputs, Output Clocks).		
10.1.3	Simulate Data nets with embedded clocks.		
10.1.4	Simulate Interrupts (Edge Triggered).		
10.1.5	Simulate Logic signals travelling long distances requiring termination.		
10.1.6	Simulation results should be used to optimize each critical signal for best signal integrity: • Define output pin drive strength. • Define output pin slew rate. • Define output pin termination design (ex. output series termination resistor value). • Define setting of internal pin pull-up and pull-down resistors. • Improve PCB layout.		
10.2	Board Measurements: Use Oscilloscope to measure on PCB assembly critical signals for proper function and signal integrity.		
10.2.1	Measure Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like).		
10.2.2	Measure Clock nets (Oscillator Inputs, Output Clocks).		
10.2.3	Measure Data nets with embedded clocks.		
10.2.4	Measure Interrupts (Edge Triggered).		
10.2.5	Measure Logic signals travelling long distances requiring termination.		
10.2.6	Measurement results should be used to optimize each critical signal for best signal integrity: • Adjust output pin drive strength. • Adjust output pin slew rate. • Adjust output pin termination design (ex. output series termination resistor value). • Adjust setting of internal pin pull-up and pull-down resistors.		
10.3	Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI).		

References

- MachXO5-NX web page
- MachXO5-NX Family Data Sheet (FPGA-DS-02102)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- Thermal Management (FPGA-TN-02044)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- Lattice Radiant FPGA design software.
- Lattice Insights for Lattice Semiconductor training courses and learning plans.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.8, October 2025

Section	Change Summary
All	Minor editorial fixes.
Introduction	The statement, *The device family consists of FPGA densities ranging from 25k to 80k logic cells*, has been removed as of revision 1.7.
Clock Inputs	• Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads.* • Added the PLL Reference Clock Locking section.
Checklist	• Added item 5.5 with, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*. • Added *Clock Inputs* under *item 8*.

Revision 1.7, July 2025

Section	Change Summary
All	Minor editorial fixes.
Introduction	Added *Hardware Checklists are developed after Evaluation boards and incorporate optimized designs that supersede the circuitry of Evaluation boards. Customers copying circuits from Evaluation boards should optimize their designs according to the Hardware Checklists*, after the first paragraph of this section.

Power Supplies	• Added *LFMXO5-25/35/65/35T/65T* in this section.
	• Reworked the first paragraph of this section.
	• Reworked Table 2.1. LFMXO5 Power Supplies. Added the following:
	  • *VCCIO[11, 9:0] LFMXO5-25/35/65/35T/65T*
	  • *VCCIO[7 0] LFMXO5-55T/100T*
	  • *VCCSDx T Parts Only*
	  • *VCCSDCK T Parts Only*
	  • *VCCPLLSDx T Parts Only*
	  • *VCCAUXSDQx T Parts Only*
	• Removed Table 2.2 LFMXO5-55T/100T Power Supplies.
	• Replaced *0.25% peak noise* with *0.50% peak noise* in the last sentence of the Power Source section.

Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  • Updated the notes of $V_{CCIO[11, 9: 0]}$.
	  • Added LFMXO5-25/35/65/35T/65T under $V_{CCIO[11, 9: 0]}$.
	  • Updated notes of $V_{CCADC18}$.
	  • Added V_{CCSDx} T Parts Only, V_{CCSDCK} T Parts Only, $V_{CCPLLSDx}$ T Parts Only, and $V_{CCAUXSDQx}$ T Parts Only.
	• Updated the Unused ADC Blocks section.
	  • Added, *Powering $V_{CCADC18}$ allows reading of internal temperature and voltage rails. If both ADC blocks are not used, and reading internal temperature and voltage rails are not required then leave $V_{CCADC18}$ open.*
	  • Removed, *If both ADC blocks are unused leave $V_{CCADC18}$ open*.
	• Updated Table 3.2. Recommended Capacitor Sizes.
	  • Combined the 1.0 µF, 2.2 µF capacitance to the row of 0.1 µF capacitance.
	  • Updated the following for the 22 µF capacitance.
	  • Size Preferred: Replaced 805 with 603
	  • Size Next Best: Replaced 603 with 805

Configuration Considerations	• Updated Table 6.1. JTAG Pin Recommendations.
	  • Replaced *4.7 kΩ resistor* with *4.7 kΩ to 10 kΩ resistor* for the following JTAG pins: TDI/SI, TMS/SCSN, and TDO/SO.
	  • Updated note 1: Replaced *50K and 100K parts* with *LFMXO5-55T/100T*, and replaced *25K parts* with *LFMXO5-25/35/65/35T/65T*.

Section	Change Summary

	• Updated Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins.
	  • Replaced *4.7 kΩ resistor* with *4.7 kΩ to 10 kΩ resistor* for PROGRAMN pin.
	  • Replaced *10 kΩ resistor* with *4.7 kΩ to 10 kΩ resistor* for the following pins: INITN, DONE, and TMS/SCSN.
	  • Updated notes 2 and 3: Replaced *50K and 100K parts* with *LFMXO5-55T/100T*, and replaced *25K* parts with *LFMXO5-25/35/65/35T/65T*.
	• Updated Figure 6.1. Typical Connections for Programming SRAM / FLASH via JTAG / SSPI and Figure 6.2. Typical Connections for Programming SRAM / FLASH via I2C / I3C.

I/O Pin Assignments	• Replaced *I/O Bank 2, I/O Bank 3, Bank 4, I/O Bank 7, Bank 8, and I/O Bank 9* with *LFMXO5-25/35/65/35T/65T Banks 2, 3, 4, 7, 8, 9 and LFMXO5-55T/100T Banks 1, 2, 6, 7* under the Early I/O Release section. • Added *Review device pinlist .csv file for list of pins supporting EIO* under the Early I/O Release section.
Pinout Considerations	• Replaced *LFMXO5-25* with *LFMXO5-25/35/65/35T/65T* under the LVDS Pin Assignments section. • Replaced *LFMXO5-25 Banks 5, 6 and LFMXO5-55T/100T Banks 3, 4, 5* with *LFMXO5-25/35/65/35T/65T Banks 5, and 6 and LFMXO5-55T/100T Banks 3, 4, and 5* under the HSUL, SSTL, and LVSTL Pin Assignments section.
Layout Recommendation	Replaced Figure 12.1 with Figure 12.1. Ground Vias Implementation and Figure 12.2. Stitching Vias Implementation.
Checklist	• Replaced *LFMXO5-15D* with *LFMXO5-25/35/65/35T/65T* under item no. 1.2.1. • Replaced *LFMXO5-25* with *LFMXO5-25/35/65/35T/65T* and added Bank 11 under item no. 1.2.2. • Replaced *LFMXO5-25* with *LFMXO5-25/35/65/35T/65T* under item no. 1.2.3. • Updated the contents of item no. 1.3.4 and item no. 1.3.5.

Revision 1.6, March 2025

Section	Change Summary
All	Minor editorial fixes.
Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components. • Removed the word, *to check*, under the VCCIO[9-0] notes.

Revision 1.5, August 2024

Section	Change Summary
All	• Minor editorial fixes. • Replaced the word *slave* with *target*.
Abbreviations in This Document	Changed *Acronyms* to *Abbreviations* in This Document.
Inclusive Language	Added this section.
Power Supplies	• Updated the description of Table 2.1 from, *the power supplies and the appropriate voltage levels for each supply* to *the LFMXO5-25 power supplies and the appropriate voltage levels for each supply*. • Updated the contents of Table 2.1. LFMXO5 Power Supplies. • Added Table 2.2. LFMXO5-55T/100T Power Supplies.

Power Supply Filtering	• Added the following Power Input notes to $V_{CCIO[9:0]}$ on Table 3.1. Recommended Power Filtering Groups and Components.
	  • *LFMXO5-25*
	  Bank 1: 3.3 V Only
	  Banks 0, 2, 3, 4, 7, 8, 9: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V
	  Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V
	  • *LFMXO5-55T/100T*
	  Bank 0: 3.3 V Only – to check
	  Banks 0, 2, 6, 7, 8, 9: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V

Section	Change Summary

	Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V
	• Updated the recommended filter of $V_{CCPLLSDx}$ from *4.7 µF + 100 nF per pin* to *47 µF + 470 nF per pin* on Table 3.1. Recommended Power Filtering Groups and Components
	• Updated the value SDx_REFRET value on Figure 3.1. Recommended Power Filter.
	  • 100 nF x PIN to 470 nF x PIN
	  • 4.7 µF to 47 µF
	• Reworked section contents of the Unused Both SERDES Quads subsection.
	• Reworked section contents of the Single Unused SERDES Channels subsection.

Pinout Considerations	• Added the statement *only (LFMXO5-25 Banks 5, 6 and LFMXO5-55T/100T Banks 3, 4, 5)* in the LVDS Pin Assignments subsection. • Reworked section contents of the HSUL, SSTL, and LVSTL Pin Assignment subsection.
Simulation and Board Measurement of Critical Signals	Added this section.

Checklist	• Updated Table 14.1. Hardware Checklist.
	  • Added contents to item no. 1.2.1 – Wide Range V_{CCIO0} (LFMXO5-55T/100T) 3.3 V Only.
	  • Added the following contents to item no. 1.2.2:
	  • Wide Range V_{CCIOx} LFMXO5-25 Banks 0, 2, 3, 4, 7, 8, 9 are between 1.2 V to 3.3 V.
	  • Wide Range V_{CCIOx} LFMXO5-55T/100T Banks 1, 2, 6, 7 are between 1.2 V to 3.3 V.
	  • Removed the below contents on item no. 1.2.2.
	  • Wide Range V_{CCIO} (Banks 0, 2, 3, 4, 7, 8, 9) are between 1.2 V to 3.3 V.
	  • Added the following contents to item no. 1.2.3:
	  • High Performance V_{CCIOx} LFMXO5-25 Banks 5,6 are between 1.0 V to 1.8 V.
	  • High Performance V_{CCIOx} LFMXO5-55T/100T Banks 3, 4, 5 are between 1.0 V to 1.8 V.
	  • Removed the below contents on item no. 1.2.3
	  • All High Performance (Banks 5, 6) V_{CCIO} are between 1.0 V to 1.8 V
	  • Added contents to item no. 1.2.4 – V_{CCIOx} bank voltage matches sysCONFIG peripheral devices such as system I3C, SPI Flash, etc.
	  • Removed the below contents on item no. 1.2.4
	  • Configuration V_{CCIO} (Banks 1, 2) match system voltages.
	  • Removed item no. 1.2.5 – $V_{CCIO[9:0]}$ used based on user design.
	  • Added item no. 1.4.6 and item no. 1.4.7.
	  • Added item no. 8 Layout Recommendations
	  • Added item no. 9 Simulation and Board Measurement of Critical Signals

Revision 1.4, April 2024

Section	Change Summary
All	Minor editorial fixes.
Power Supply Filtering	Updated Unused ADC Blocks section. • Removed the last bullet, *Leave ADC inputs floating*. • Updated the second bullet to, *Unused ADC Blocks should connect ADC_REFx, ADC_DPx, and ADC_DNx to board ground*.

Revision 1.3, March 2024

Section	Change Summary
All	Minor editorial fixes.
Disclaimer	Updated this section.
Power Supplies	Updated the nominal voltage value of ADC_REFP[1:0] from *1.2 V to 1.8 V Typical* to *1.0 V to 1.8 V Typical* in Table 2.1. Single-Ended I/O Standards.
Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components:

Section	Change Summary
	• Updated the notes of ADC_REFP[1:0] from *1.2 V to 1.8 V Typical* to *1.0 V to 1.8 V Typical*. • Updated the notes of V_{CCSDCK} from *If SERDES Block not used, leave open* to *If both SERDES blocks are not used, leave open*. • Added Figure 3.1. Recommended Power Filter. • Added the statement, *Leave ADC inputs floating*, to Subsection 3.4 Unused ADC Blocks. • Reworked contents of Subsection 3.5 Unused SERDES Quads.
Power Sequencing	Added this section.
Power Estimation	Added this section.
Configuration Considerations	• Updated Table 6.1. JTAG Pin Recommendations. • Updated table note 1. • Updated the following JTAG Pins: • TDI/SI: 4.7 KΩ pull-up to V_{CCIO}. • TMS/SCSN: 4.7 KΩ pull-up to V_{CCIO} • TDO/SO: 4.7 KΩ pull-up to V_{CCIO} • Added table note 3 and updated table note 2 in Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins. • Added table note, *Leave unused configuration ports open* to Table 6.3. Configuration Pins Needed per Programming Mode. • Added Figure 6.1. Typical Connections for Programming SRAM / FLASH via JTAG / SSPI and Figure 6.2. Typical Connections for Programming SRAM / FLASH via I2C / I3C in this section.
sysI/O	Added this section.
Clock Inputs	Reworked section contents.
Layout Recommendations	Added this section.
Checklist	• Updated the table source of item 2-JTAG, from *Table 5.1* to *Table 6.1*. • Updated the table source of item 3-Configuration from, *Table 5.1 and Table 5.2* to *Table 6.1 and Table 6.2*. • Added the *item 7-ADC,* in the checklist.

Revision 1.2, October 2023

Section	Change Summary
Configuration Considerations	• Added the below table note for Table 5.1 and Table 5.2. • For V_{CCIO} pull-up banks for LFMXO5-25 densities, the JTAG pins are at Bank2, while for LFMXO5-55T and LFMXO5-100T, the JTAG pins are at Bank1. • Updated the PCB Recommendation of Table 5.1 for the following JTAG pins. • TDI/SI • TMS/SCSN • TDO/SO • JTAG_EN • Updated the PCB Connection of Table 5.2 for JTAG_EN. • Updated Figure 7.1; HCSL OSC diagram - changed the resistance from *DNI to 0*.

Revision 1.1, April 2023

Section	Change Summary
Introduction	Added Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) to the list of references.
Power Supplies	• Indicated availability of other supplies for onboard SERDES Blocks and ADCs. • Added V_{CCSDx}, V_{CCSDCK}, $V_{CCPLLSDx}$, and $V_{CCAUXSDQx}$ supplies to Table 2.1. Single-Ended I/O Standards. • In the Power Source subsection, added the recommended peak noise target for SERDES power rails.
Power Supply Filtering	• Changed section heading to Power Supply Filtering and added SERDES to the contents.

Section	Change Summary

	• Reordered subsections.
	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  • Removed *(Single Ended)* from V_{CCAUX}, $V_{CCAUXHx}$ and modified note.
	  • Removed $V_{CCAUXHx\ (Fast\ Differential)}$.
	  • Added V_{CCSDx}, V_{CCSDCK}, $V_{CCPLLSDx}$, and $V_{CCAUXSDQx}$.
	  • Indicated *sensitive* analog circuitry in V_{CCAUXA} note.
	• In Ground Pins subsection, added V_{SSADC} and SDx_REFRET pins.
	• Added the following subsections:
	  • Unused Bank V_{CCIOX}
	  • Unused SERDES Quads
	  • Unused SERDES Channels in a Quad

Configuration Considerations	Updated table note style in Table 5.2. Pull-up/Pull-down Recommendations for Configuration Pins and Table 5.3. Configuration Pins Needed per Programming Mode.
I/O Pin Assignments	Added information on SERDES Block pins.
DPHY and SERDES Pin Considerations	Updated section heading to DPHY and SERDES Pin Considerations.
Checklist	Updated Table 10.1. Hardware Checklist. • Removed former item *1.1.7 $V_{CCAUXHx}$ banks with high-speed differential pair I/O …* and adjusted numbering. • Updated FPGA Power Supplies – Core Supplies items 1.1.1, 1.1.2, 1.1.6, and 1.1.7. • Added FPGA Power Supplies – SERDES Power Supplies.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.0, October 2022

Section	Change Summary
All	Initial release.

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