CrossLink-NX-33 and CrossLinkU-NX Hardware Checklist

Technical Note

FPGA-TN-02308-1.4

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Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
BGA	Ball Grid Array
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
GPLL	General Purpose PLL
HCSL	High Speed Current Steering Logic
HPIO	High-Performance Input/Output
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IBIS	I/O Buffer Information Specification
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PCLK	Primary Clock
PLL	Phase-Locked Loop
POR	Power-On Reset
SERDES	Serializer/Deserializer
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SSTL	Stub Series Terminated Logic
USB	Universal Serial Bus
VBUS	USB Bus Voltage
WRIO	Wide-Range Input/Output

1. Introduction

When designing complex hardware using the CrossLink™-NX-33 and CrossLinkU™-NX devices (hereafter referred to as LIFCL-33 and LIFCL-33U respectively), you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the LIFCL-33/33U devices. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that the reader is familiar with the LIFCL-33/33U device features as described in CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the LIFCL-33 device power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: You should refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- CrossLink-NX 33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280)
- Thermal Management (FPGA-TN-02044)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- CrossLink-NX LIFCL-33 Pinout (FPGA-SC-02040)
- CrossLink-NX LIFCL-33U Pinout (FPGA-SC-02050)
- USB 2.0/3.2 IP Core User Guide (FPGA-IPUG-02237)

2. Power Supplies

The V_{CC}, V_{CCAUXA}, and V_{CCIOX} power supplies are monitored to determine the LIFCL-33/33U device internal Power Good condition during power-up. These supplies need to be at a valid and stable level before the device becomes operational. All other supplies are not monitored during power-up, but need to be at valid and stable level before the device configuration is complete and enters User Mode.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)	Description
V_{CC}, V_{CCECLK}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCPLL}	1.0 V	Power supply for PLL.
V_{CCAUXA}	1.8 V	Auxiliary power supply voltage for core logic.
V_{CCAUX}	1.8 V	Auxiliary power supply voltage for internal analog circuitry Banks 0, 1, and 5[1]. Required for Power Good condition.
$V_{CCAUXH[4:2]}$	1.8 V	Auxiliary power supply voltage for internal analog circuitry Banks 2, 3, and 4.
$V_{CCIO[5:0]}$	Banks 0, 1, 5[1]: 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 2, 3, 4: 1.0 V, 1.2 V, 1.5 V, 1.8 V.	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply: V_{CCIO0} and V_{CCIO1} are used in conjunction with pins dedicated and shared with device configuration, and are required for Power Good condition.
V_{CCAUX_AON} [2]	1.8 V	Auxiliary power for Hardware Always On circuitry.
AVDD33	3.3 V	Analog power supply voltage for Hardened USB block.
AVDD18[2], AVDD18_TX[2], AVDD18_COM[2]	1.8 V	Analog power supply voltage for Hardened USB block.
AVDD[2], AVDD_TX[2]	1.0 V	Analog power supply voltage for Hardened USB block.

Notes:

1. Bank 5 is only supported in LIFCL-33 device.
2. V_{CCAUX_AON}, AVDD33, AVDD18, AVDD18_TX, AVDD18_COM, AVDD, AVDD_TX are only supported in LIFCL-33U device.

The LIFCL-33/33U FPGA devices have a power-on-reset state machine that depends on V_{CC}, V_{CCAUX}, $V_{CCIO[1:0]}$ power supplies. These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies have reached their minimum operating voltages.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

The recommendation is to design voltage regulators to be accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR × expected current draw
- Expected voltage drops due to current measuring resistor's ESR × expected current draw

With 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is especially sensitive to noise as every 10 mV is 1% of the rail voltage. For PLLs, target less than 0.25% peak noise.

Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins.

For the best jitter performance, especially with MIPI functionality, optimize pin assignment to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk to sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs.

2.3. Recommended Power Filtering Groups and Components

Table 2.2. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCECLK}	10 µF x 3 + 100 nF per pin	Core logic. 1.0 V
V_{CCPLL}	120 Ω FB + 10 µF + 100 nF per pin	Power supply for PLL 1.0 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for Core logic. 1.8 V
V_{CCAUX} and $V_{CCAUXH[4:2]}$ Combined Together	120 Ω FB + 10 µF x 2 + 100 nF per pin	Auxiliary power supply pin for internal analog circuitry. V_{CCAUX} Banks 0, 1, 5[1]. $V_{CCAUXH[4:2]}$ Banks 2, 3, 4. 1.8 V
$V_{CCIO[5:0]}$	10 µF + 100 nF per pin	Bank I/O. Unused banks can use a single 100 nF. For banks with lots of outputs or large capacitive loading add one additional 10 µF (or can use a single 22 µF instead of two 10 µF.) Banks 0, 1, 5[1] = 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 2, 3, 4 = 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.
V_{CCAUX_AON} [2]	10 µF + 100 nF	Auxiliary power for Hardware Always On circuitry. 1.8 V
AVDD33[2]	120 Ω FB + 10 µF + 100 nF per pin	Analog power supply voltage for Hardened USB block. 3.3 V
AVDD18[2], AVDD18_TX[2], AVDD18_COM[2] Combined Together	120 Ω FB + 10 µF + 100 nF per pin	Analog power supply voltage for Hardened USB block. 1.8 V
AVDD[2], AVDD_TX[2] Combined Together	120 Ω FB + 10 µF + 100 nF per pin	Analog power supply voltage for Hardened USB block. 1.0 V

Notes:

1. Bank 5 is only supported in LIFCL-33 device.
2. V_{CCAUX_AON}, AVDD33, AVDD18, AVDD18_TX, AVDD18_COM, AVDD, AVDD_TX are only supported in LIFCL-33U device.

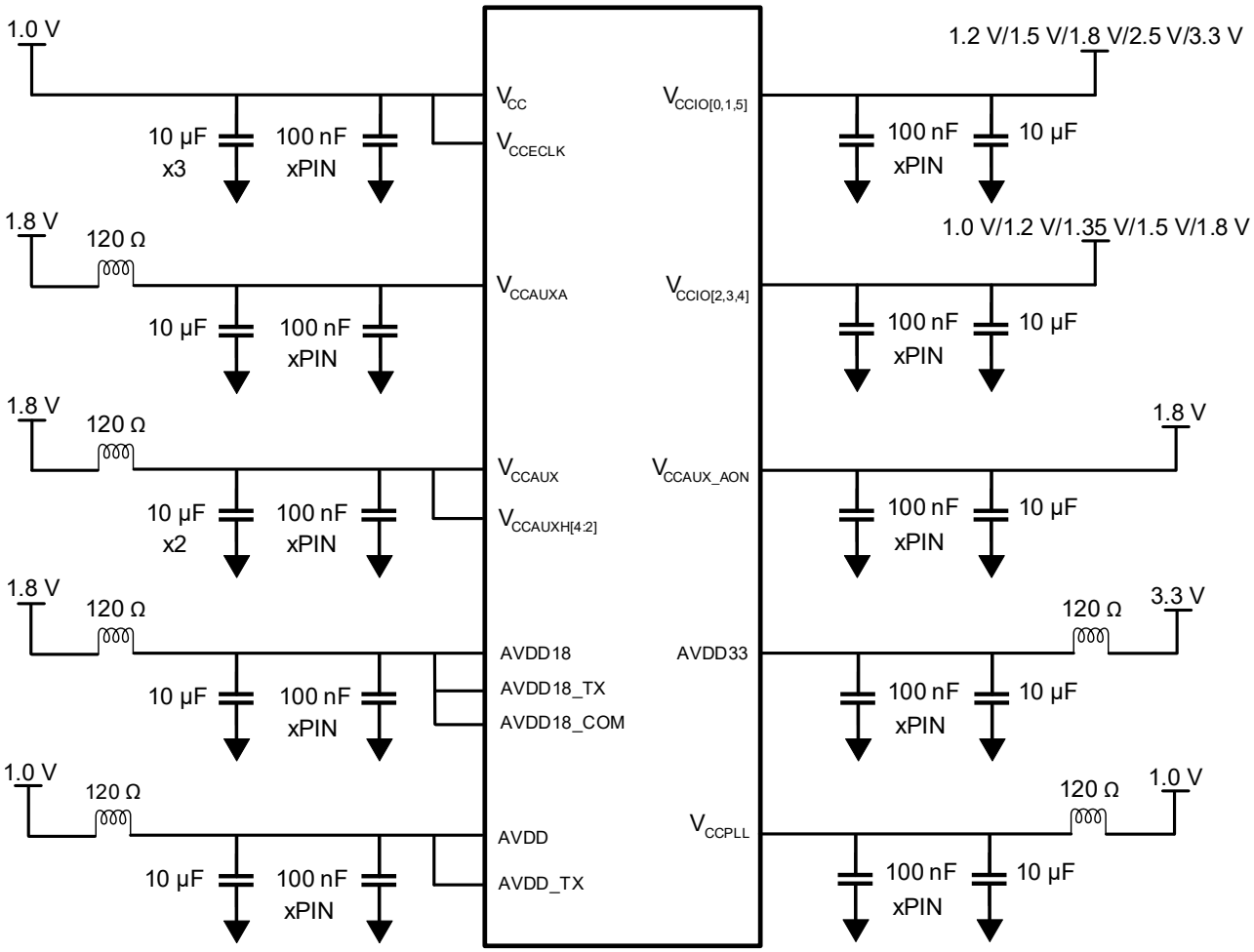

Figure 2.1. Recommended Power Filters

2.4. Unused Bank(s) V_{CCIOx}

- Connect unused V_{CCIOx} to a power rail, do not leave them open.
- Unused banks can use a single 100 nF bypass capacitor.

2.5. Unused Hardware Always On Block (LIFCL-33U only)

- Connect unused V_{CCAUX_AON} to 1.8 V and bypass with a single 100 nF capacitor.
- Add 10 kΩ pull-down resistor to AON_INT pin.

2.6. Unused USB Block (LIFCL-33U only)

- Connect AVDD33 to 3.3 V and bypass with a single 100 nF capacitor.
- Connect AVDD18, AVDD18_TX, and AVDD18_COM to 1.8 V and bypass with a single 100 nF capacitor.
- Connect AVDD and AVDD_TX to 1.0 V and bypass with a single 100 nF capacitor.

2.7. Ground Pins

All ground pins need to be connected to the board's ground plane.

3. Component Selection

3.1. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR x CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.025 Ω and 0.10 Ω depending on current load.
- PLL rails draw low current which allows ferrite beads with ESR ≤ 0.3 Ω.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

3.2. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages and place them close to the power oscillator supply pins with short low inductance connections. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.2.1. Capacitor Dielectric

Use X5R, X7R, and similar dielectrics with good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

3.2.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the voltage rail (maximum). For example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.2.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, recommended capacitor sizes are in Table 3.1.

Table 3.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

4. Power Sequencing

There is no power-up sequence required for the LIFCL-33 device.

5. Power Estimation

Once the LIFCL-33/33U devices' density, package, and logic implementation are decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant™ design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current, and maximum DC and AC current for the given system environmental conditions.
- Thermal considerations are also important. The thermal design of the system environment and LIFCL-33/33U devices should be able to support operating at maximum operating junction temperature.

The above two criteria should be taken into consideration early in the design phase.

6. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024).

The LIFCL-33/33U devices include provisions to configure the FPGA through the JTAG interface or several modes utilizing the sysCONFIG port.

6.1. JTAG

The JTAG port includes a JTAG Enable pin and a 4-pin interface, as shown in Table 6.1.

Table 6.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI/SI	4.7 kΩ pull-up to V_{CCIO1}
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
TDO/SO	4.7 kΩ pull-up to V_{CCIO1}
TCK/SCLK	2.2 kΩ pull-down to GND

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO1} and ground.

6.2. Target SPI and I2C Configuration

While the pins listed in Table 6.2 have internal weak pull resistors, pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground for these pins should be used as indicated under PCB Connection.

Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO0}
INITN	4.7 kΩ pull-up to V_{CCIO1}
DONE	4.7 kΩ pull-up to V_{CCIO1}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)
MCLK	1.0 kΩ to GND (Not installed by default) 1.0 kΩ to V_{CCIO0} (Not installed by default)
MCSN	4.7 kΩ pull-up to V_{CCIO0}
MD0	10 kΩ pull-up to V_{CCIO0} (Not installed by default)
MD1	10 kΩ pull-up to V_{CCIO0} (Not installed by default)
MD2	10 kΩ pull-up to V_{CCIO0} (Not installed by default)
MD3	10 kΩ pull-up to V_{CCIO0} (Not installed by default)
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
SCL/SDA	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO1}

6.3. Configuration Pins Per Programming Mode

Table 6.3 lists the signal pins required for each configuration-programming mode.

Table 6.3. Configuration Pins Needed per Programming Mode[1]

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
MSPI	0	(Default)	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
JTAG	1	JTAG_EN pin[2]	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key[2]	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

Notes:

1. Leave unused Configuration ports open.
2. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

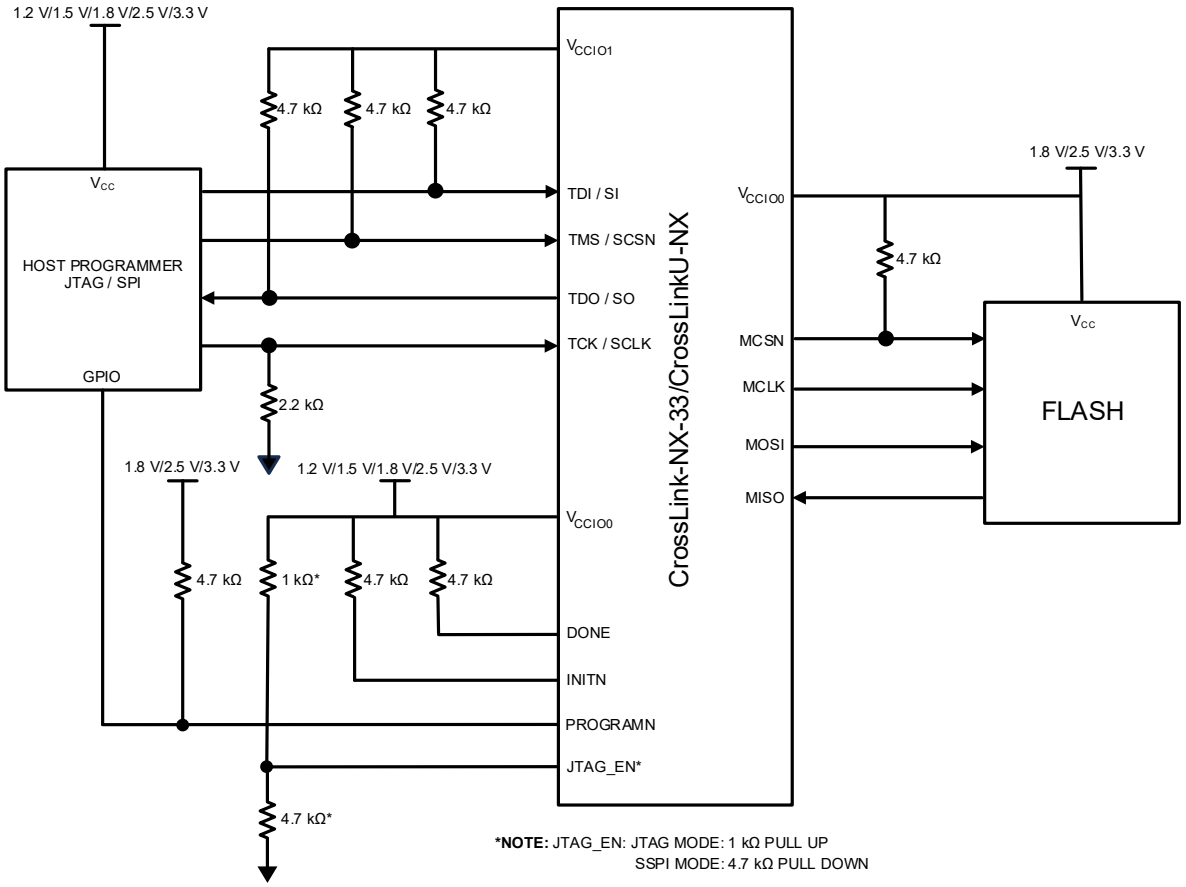

Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI

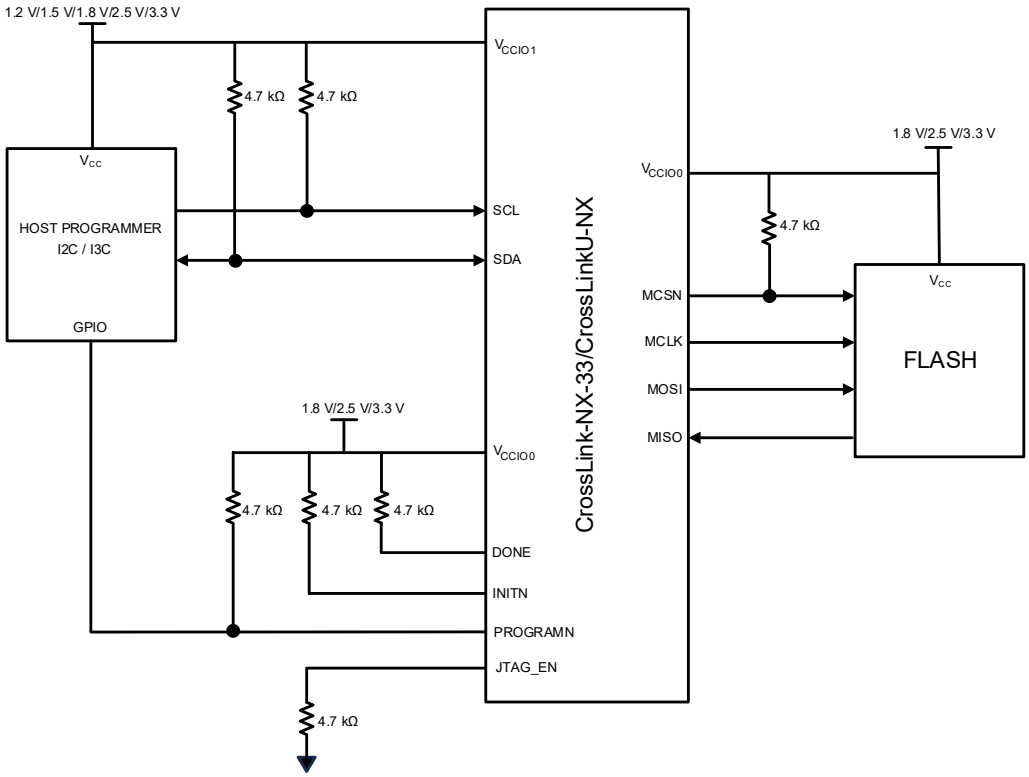

Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C

Some architectures require Bank 0 and Bank 1 to have different bank voltages. One such architecture is illustrated in Figure 6.3. In the event that a control signal, such as PROGRAMN, originates in one voltage domain but is terminated in another, a voltage translating device or circuit must be implemented to reduce excess current leakage or possible device damage. Figure 6.3 shows a voltage translator utilized for PROGRAMN, allowing a 3.3 V driver to drive the 1.8 V bank 0 input buffer safely and efficiently.

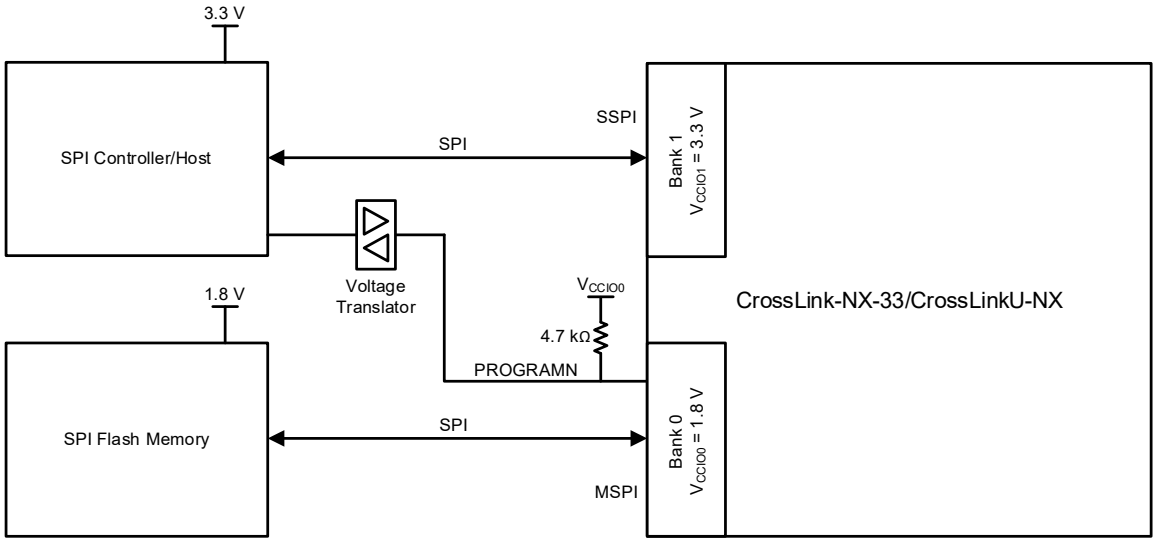

Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks

7. External SPI Flash

The SPI Flash voltage should match the V_{CCIO0} voltage.

It is recommended to use SPI Flash devices that are supported by the Lattice Radiant Programmer.

You can view the list of supported devices by searching for *SPI Flash support* in the Lattice Radiant Programmer Help menu. For SPI Flash devices that are not listed in the *SPI Flash support*, using the **custom flash** option may allow non-supported devices to work.

8. I/O Pin Assignments

Crosstalk coupling is reduced in the device packages of LIFCL-33/33U devices. The PCB board, however, can cause significant noise injection from adjacent I/O pins and PCB traces running close together in parallel for long distances. Simulate any suspicious traces using a PCB crosstalk/Signal Integrity simulation tool to determine if a particular layout needs to be improved.

It is common practice for designers to select pinouts for their system very early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

8.1. Series Termination Resistors

When using series termination resistors, start with a value of 0-Ω due to GPIOs having a relatively high output impedance.

8.2. Functional Blocks Rule-Based Pinout Considerations

The LIFCL-33/33U devices support many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as MIPI, clock resource connectivity, and PLL and DLL usage. Refer to CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280) for rules pertaining to these interface types.

8.3. LVDS and MIPI Pin Assignments

True LVDS and MIPI signaling inputs and outputs are available on HPIO I/O pins in banks 2, 3, and 4. True LVDS and MIPI input pairing can be found under the High-Speed column in the pin-list .csv file.

WRIO I/O pins in banks 0, 1, and 5 do not support true LVDS and MIPI standard, but can support emulated LVDS outputs. Emulated LVDS output are available on pairs of all banks, but this requires external termination resistors. This is described in sysI/O User Guide for Nexus Platform (FPGA-TN-02067).

- Bank voltage must be set to 1.8 V to support LVDS.
- Bank voltage must be set to 1.2 V to support MIPI.

8.4. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards that require an external reference voltage. HSUL and SSTL are supported on HPIO I/O pins in banks 2, 3, and 4 only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

8.5. USB Block Pin Assignments (LIFCL-33U only)

Connect REXT23 pin to ground using a 300 Ω 1% resistor.

Connect VBUS pin to system USB VBUS signal. If USB VBUS signal is not available this pin can be connected to 3.3 V.

USB block uses a 60 MHz oscillator input. The 104-ball package has low input jitter reference clock pins REFIN_CLK_EXT_P/N. The 84-ball package should use a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (–complement); bank 4 recommended.

PCB Layout of USB differential pairs DP/DM, TX_M/P, and RX_M/P should be short length with well-controlled transmission line impedance.

9. sysI/O

LIFCL-33/33U devices provide you the flexibility to configure each I/O according to your requirement. These pins can be configured as input, output, and tri-state. Attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can also be set up.

You can set Pull-up and Pull-down resistors for PULLMODE. The implementation of this resistor is set by using a constant current that has values as specified in Table 9.1.

Table 9.1. Weak Pull-up/Pull-down Current Specifications

Configuration	Parameter	Condition	Min	Max	Unit
Pull-up	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	–30	–150	µA
Pull-down	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	150	µA

LIFCL-33/33U devices also provide special I/O like HPIO and WRIO that can be used for high-speed communication. Figure 9.1 shows the block diagram for HPIO and Figure 9.2 shows the block diagram for WRIO.

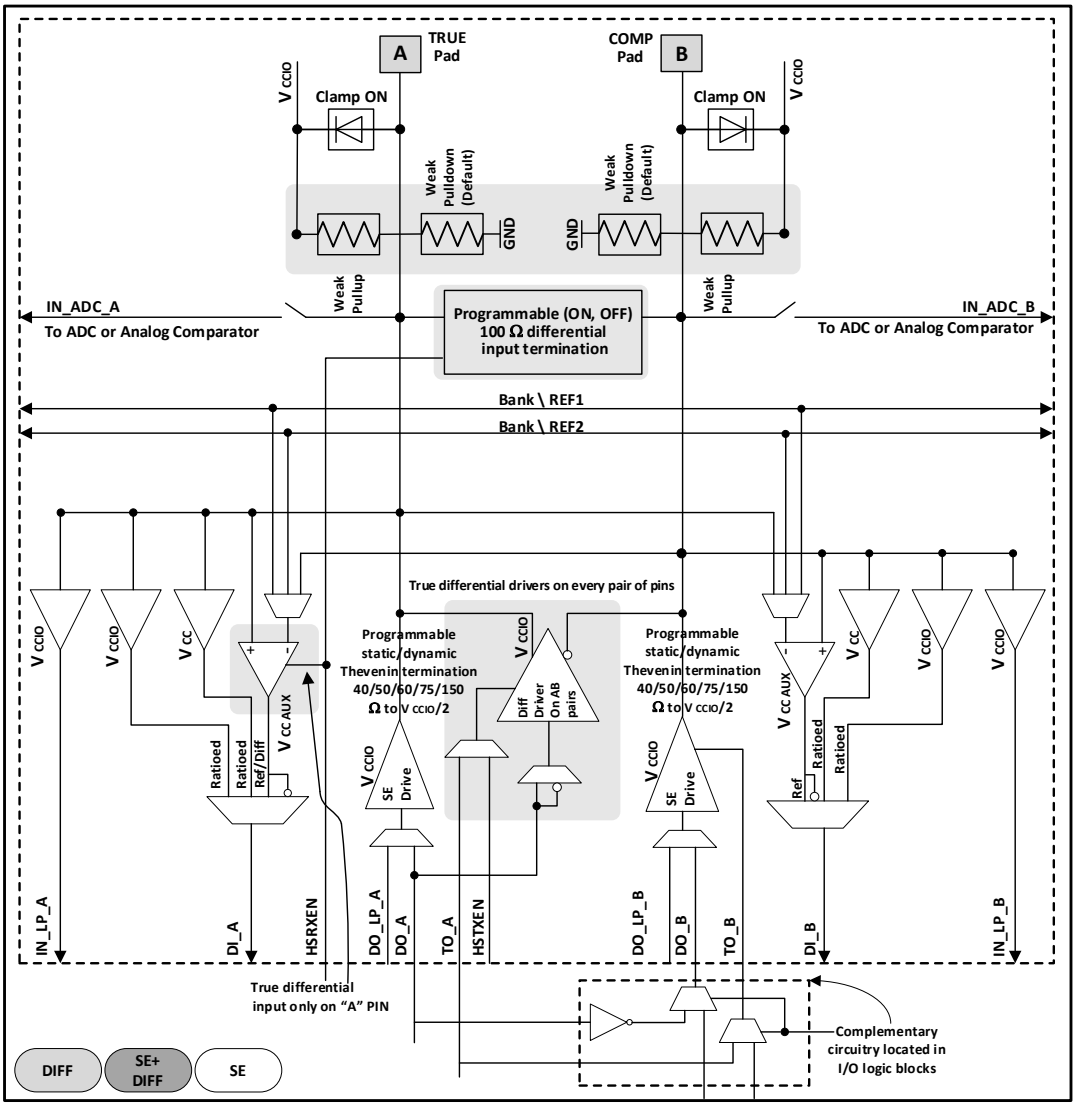

Figure 9.1. High-Performance sysI/O Buffer Pair for Bottom Side

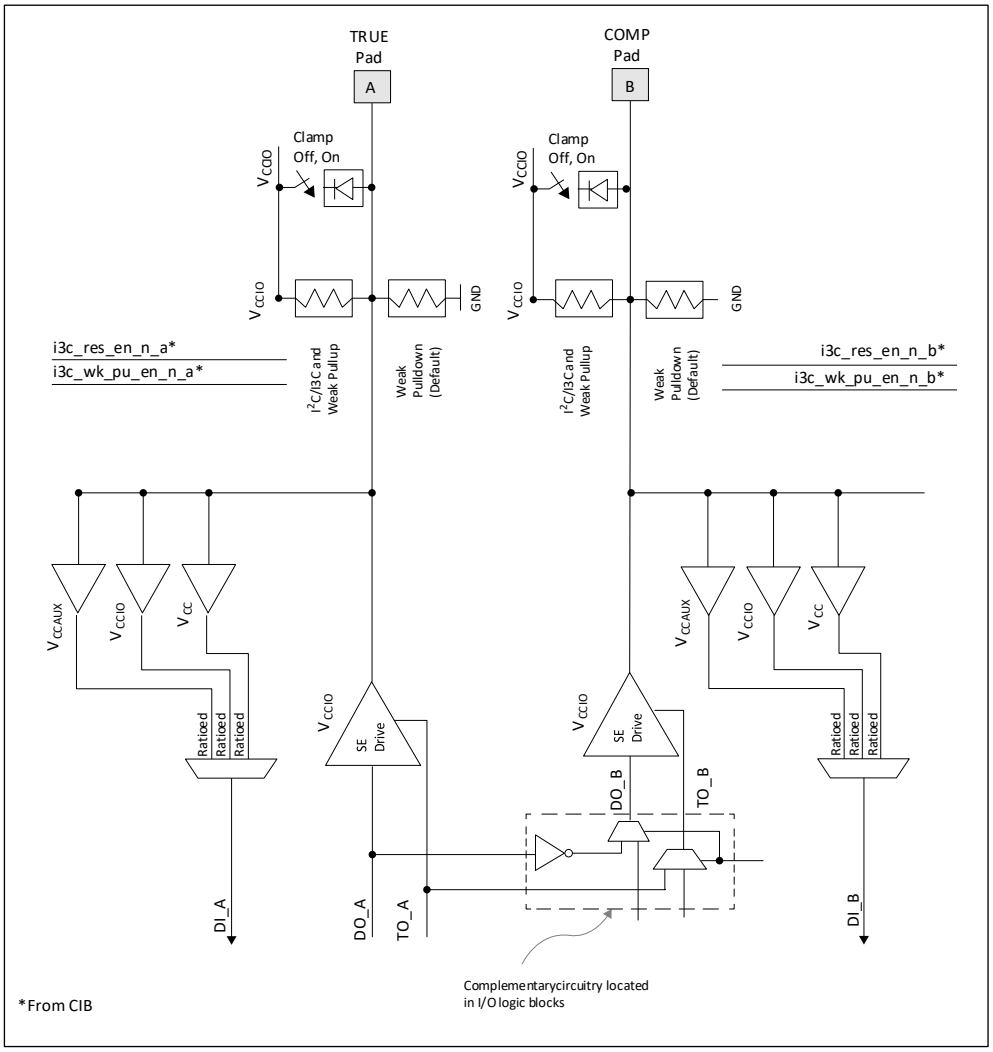

Figure 9.2. Wide-Range sysI/O Buffer for Top and Left/Right Sides

10. Clock Inputs

The LIFCL-33/33U devices provide certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O. When these pins are used for clocking purpose, the user needs to pay attention to minimize signal noise on these pins. Refer to CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280).

These shared clock input pins, typically labeled GPLL and PCLK, can be found under the *Dual Function* column of the pin-list .csv file. High speed differential interfaces (such as MIPI) received by the FPGA device must route their differential clock pair into a pair of inputs that support differential clocking, labeled as PCLKTx_y (+true) and PCLKCx_y (–complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA device, you have to ensure that the oscillator's output voltage to the FPGA device does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

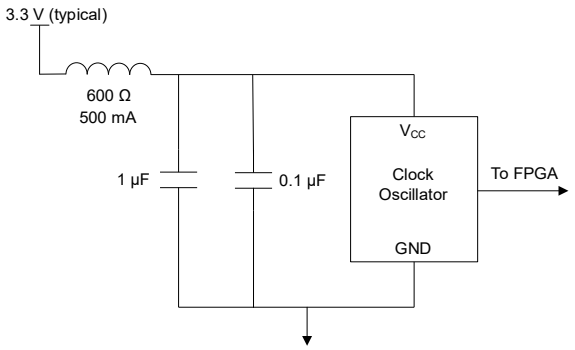

Figure 10.1. Clock Oscillator Bypassing

It is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO} for differential clock inputs to banks with V_{CCIO} voltage of 1.5 V and lower. An LVDS oscillator can also be used if AC coupled and then DC biased at half of the V_{CCIO} voltage. An example of a dual footprint design supporting HCSL and LVDS is as shown in Figure 10.2.

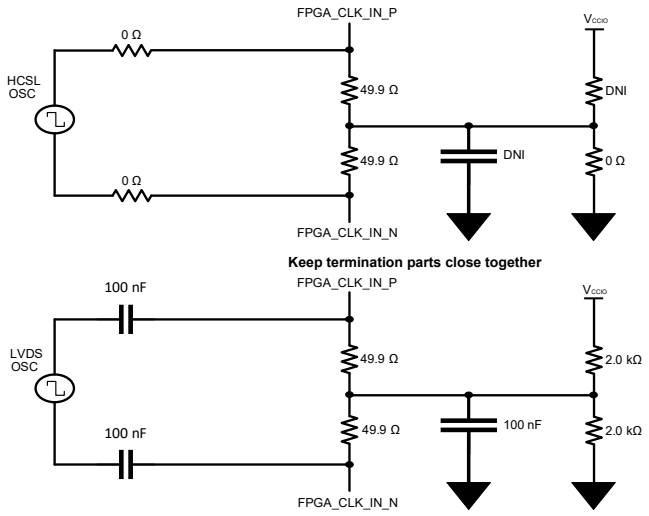

Figure 10.2. PCB Dual Footprint Design Supporting HCSL and LVDS Oscillators

10.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enabled pin is shown in Figure 10.3.

Note: External board oscillators typically require 5 to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

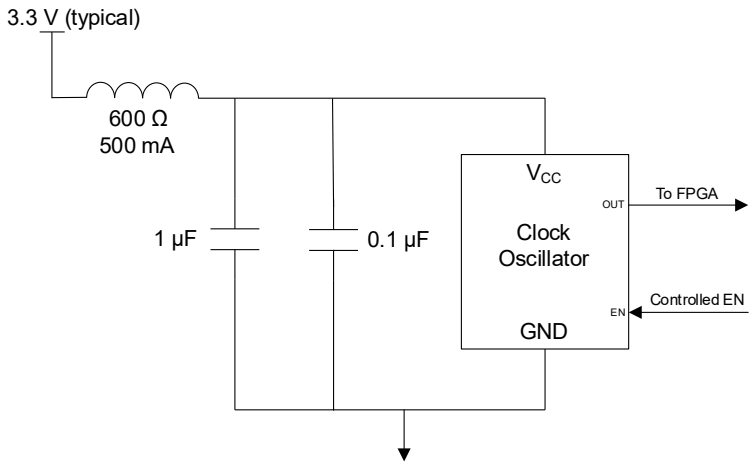

Figure 10.3. Clock Oscillator with Controlled Enable Pin

11. Layout Recommendations

A good design from schematic should also reflect with a good layout for the system design to work without any issues on noise and power distribution. Below are some recommended layouts in general:

1. Power should come from power planes to ensure good power delivery and thermal stability.
2. Each power pin should have its own decoupling capacitor, typically 100 nF, and should be placed as close as possible to each other.
3. Placement of analog circuits must be away from digital circuits or high switching components.
4. High speed signals should target clearance of 5 times trace width from other signals.
5. High speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are ground. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}). See Figure 11.1 for details.

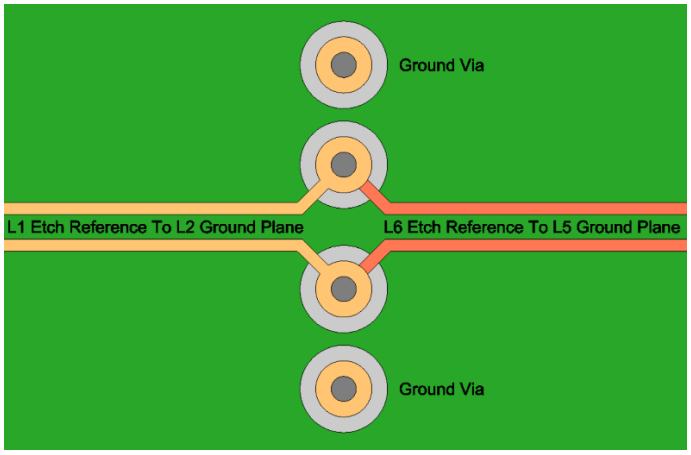

Figure 11.1. Ground Vias Implementation

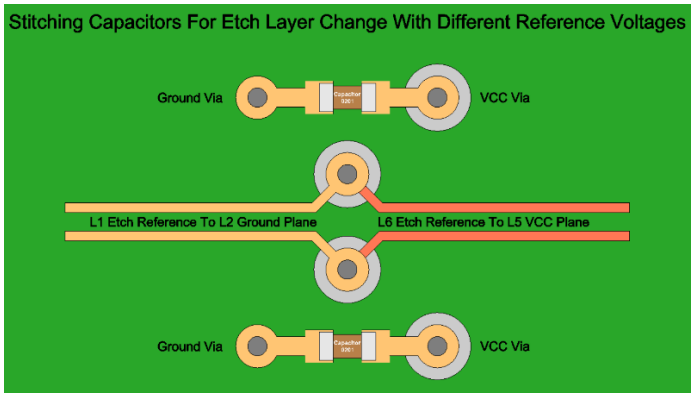

Figure 11.2. Stitching Vias Implementation

6. High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.
7. For differential pairs, make sure to match the length as close as possible. A good rule of thumb is to match up to ±0.1 mm.

Refer to the following documents for further information on layout recommendations:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

12. Simulation and Board Measurement of Critical Signals

To ensure a design is reliable and will have a high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

12.1. Critical Signals

Signals sensitive to Signal Integrity (SI) degradation are considered critical signal which require extra design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, etc.)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

12.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often have reoccurring subscription pricing. The expensive tools can import board design files and can easily supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (ex. Micro-cap) can supply useful basic simulations, but take extra effort to set up SI effects for multiple signals with different transmission line lengths, lossy transmission lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

12.3. Board Measurements

Critical signals should be measured on the actual PCB assembly using an Oscilloscope. Verify proper signaling function and signal integrity (that is, eye diagram, SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (ex. output series termination resistor value).
- Adjust the setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI)

13. Checklist

Table 13.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Main FPGA Supplies		
1.1.1	V_{CC}, V_{CCECLK} at 1.0 V ±5%		
1.1.2	Use a PCB plane for V_{CC}, V_{CCECLK}		
1.1.3	V_{CC} core power supply designed to exceed current requirement calculated from Power Calculator software by at least 25% margin		
1.1.4	V_{CCPLL} at 1.0 V ±5%		
1.1.5	V_{CCAUX}, V_{CCAUXA} and $V_{CCAUXH2/H3/H4}$ at 1.8 V –3%/+5%		
1.1.6	V_{CCAUXA} and $V_{CCAUXH2/H3/H4}$ pins should be ganged together, and a solid PCB plane is recommended. This plane should not be coupled into the V_{CC} core power plane		
1.2	I/O Supplies		
1.2.1	All Wide Range V_{CCIO} (Banks 0,1,5) are between 1.2 V to 3.3 V.		
1.2.2	All High Performance V_{CCIO} (Bank 2,3,4) are between 1.0 V to 1.8 V.		
1.2.3	Connect unused V_{CCIO} to a power rail, do not leave them open. Unused banks can use a single 100 nF bypass capacitor.		
1.2.4	All Configuration V_{CCIO} (Banks 0,1), when used with configuration interfaces (for example, SPI Flash memory devices), need to match voltage specifications.		
1.2.5	$V_{CCIO[5:0]}$ used based on user design		
1.2.6	V_{CCAUX_AON} at 1.8 V –3%/+5% Unused Always On Block can use single 1.8 V 100 nF bypass capacitor.		
1.3	USB Block Supplies		
1.3.1	AVDD33 at 3.3 V –3%/+5% Unused USB block can use single 3.3 V 100 nF bypass capacitor.		
1.3.2	AVDD18, AVDD18_TX, and AVDD18_COM at 1.8 V –3%/+5% Unused USB block can use single 1.8 V 100 nF bypass capacitor.		
1.3.3	AVDD and AVDD_TX at 1.0 V –3%/+5% Unused USB block can use single 1.0 V 100 nF bypass capacitor.		
1.4	All ground pins need to be connected to the board's ground plane, including for unused blocks.		
1.5	Follow recommended power filtering groups and components in Table 2.2.		
2	**JTAG**		
2.1	Pull-up on JTAG_EN to enable JTAG function, per Table 6.2.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development.		
2.4	Pull-down on TCK per Table 6.1.		
2.5	Pull-up on TMS per Table 6.1.		
3	**Configuration**		
3.1	Pull-down on JTAG_EN to disable JTAG and enable shared pins used for configuration, per Table 6.2.		
3.2	Pull-ups or pull-downs, on persisted configuration specific pins per Table 6.1 and Table 6.2.		
3.3	V_{CCIO0}, V_{CCIO1} bank voltage matches sysCONFIG peripheral devices such as SPI Flash.		
4	**External Flash**		
4.1	Flash voltage should match V_{CCIO0} voltage.		
5	**Special Pin Assignments**		
5.1	V_{REF} assignments followed for single-ended SSTL inputs.		
5.2	Properly decouple the VREF source.		

	Item	OK	NA
6	**Critical Pinout Selection**		
6.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280).		
6.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
6.3	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
7	**Series Termination Resistors**		
7.1	When using series termination resistors start with a value of 0 Ω due to GPIOs having a relatively high output impedance.		
8	**MIPI Interface Requirements**		
8.1	Soft MIPI supported on bottom banks 2, 3, and 4.		
8.2	V_{CCIO} set to 1.2 V.		
8.3	Target 100 Ω impedance.		
8.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source.		
8.5	Design differential pairs 'loosely coupled' with separation between positive and negative of a pair of at least twice the etch width (intra-pair spacing).		
8.6	Provide separation from each differential pair of at least six times the etch width (inter-pair spacing).		
8.7	Length match clock and data lane pair traces within 0.1 mm. (Both intra-pair and inter-pair etches).		
8.8	RX at FPGA should have clock differential pair routed to clock pins labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		
8.9	Recommend MIPI Oscillator input use lowest jitter input Bank 4 pin PB6A.		
9	**LVDS Interface Requirements**		
9.1	True LVDS supported on bottom banks 2, 3, and 4.		
9.2	V_{CCIO} set to 1.8 V.		
9.3	Target 100 Ω impedance.		
9.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source.		
9.5	Design differential pairs 'loosely coupled' with separation between positive and negative of a pair of at least twice the etch width (intra-pair spacing).		
9.6	Provide separation from each differential pair of at least six times the etch width (inter-pair spacing).		
9.7	Length match pair traces within 0.1 mm. (Both intra-pair and inter-pair etches.)		
9.8	RX at FPGA should have clock differential pair routed to clock pins labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		
9.9	Recommend LVDS Oscillator input use lowest jitter input Bank 4 pin PB6A.		
10	**USB Interface Requirements**		
10.1	Soft USB		
10.1.1	Soft USB supported on bottom banks 2 and 3.		
10.1.2	V_{CCIO} set to 3.3 V.		
10.1.3	USB pair should use a pair of I/Os that that support input differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		
10.1.4	Add 0-ohm resistors at FPGA USB outputs to allow Signal Integrity source termination tuning.		
10.1.5	Recommend LVDS Oscillator input use lowest jitter input Bank 4 pin PB6A.		
10.2	Hard USB (CrossLinkU-NX only)		
10.2.1	Connect REXT23 pin to ground using a 300 Ω 1% resistor.		
10.2.2	Connect VBUS pin to system USB VBUS signal. If USB VBUS signal is not available this pin can be connected to 3.3 V.		
10.2.3	Hard USB block uses a 60 MHz oscillator input.		
10.2.3.1	The 104-ball package has low input jitter reference clock pins REFIN_CLK_EXT_P/N.		

	Item	OK	NA
10.2.3.2	The 84-ball package should use input Bank 4. For single-ended clock source use pin PB6A. For differential clock source use pin pair PB6A/PB6B.		
10.3	USB Layout		
10.3.1	PCB Layout of USB differential pairs DP/DM, TX_M/P, and RX_M/P should be short length with well-controlled transmission line targeting 90 Ω impedance.		
10.3.2	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source.		
10.3.3	Design differential pairs 'loosely coupled' with separation between positive and negative of a pair of at least twice the etch width (intra-pair spacing).		
10.3.4	Provide separation from each differential pair of at least six times the etch width (inter-pair spacing).		
10.3.5	Length match clock and data lane pair traces within 0.1 mm. (Both intra-pair and inter-pair etches.)		
10.3.6	USB 3 High-Speed pairs can have their polarities swapped to help layout. TX_M/P can have the FPGA's M&P pins going to connector's P&M pins. RX_M/P can have the FPGA's M&P pins going to connector's P&M pins.		
11	**Clock Inputs**		
11.1	External clock source must be connected to PCLK or GPLL pins.		
11.2	PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the PLL Reference Clock Locking section for more details.		
12	**Layout Recommendations**		
12.1	Power should come from power planes to ensure good power delivery and thermal stability.		
12.2	Placement of analog circuits must be away from digital circuits or high switching components.		
12.3	High speed signals should target clearance of 5 times trace width from other signals.		
12.4	High speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are ground, else a stitching capacitor should be used.		
12.5	High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.		
13	**Simulation and Board Measurement of Critical Signals**		
13.1	Simulations: Use IBIS model to simulate critical signals for proper signal integrity.		
13.1.1	Simulate Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, etc.)		
13.1.2	Simulate Clock nets (Oscillator Inputs, Output Clocks).		
13.1.3	Simulate Data nets with embedded clocks.		
13.1.4	Simulate Interrupts (Edge Triggered).		
13.1.5	Simulate Logic signals travelling long distances requiring termination.		
13.1.6	Simulation results should be used to optimize each critical signal for best signal integrity: • Define output pin drive strength. • Define output pin slew rate. • Define output pin termination design (ex. output series termination resistor value). • Define setting of internal pin pull-up and pull-down resistors. • Improve PCB layout.		
13.2	Board Measurements: Use Oscilloscope to measure on PCB assembly critical signals for proper function and signal integrity.		
13.2.1	Measure Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, etc.)		
13.2.2	Measure Clock nets (Oscillator Inputs, Output Clocks).		
13.2.3	Measure Data nets with embedded clocks.		
13.2.4	Measure Interrupts (Edge Triggered).		
13.2.5	Measure Logic signals travelling long distances requiring termination.		

	Item	OK	NA
13.2.6	Measurement results should be used to optimize each critical signal for best signal integrity: • Adjust output pin drive strength. • Adjust output pin slew rate. • Adjust output pin termination design (ex. output series termination resistor value). • Adjust setting of internal pin pull-up and pull-down resistors.		
13.3	Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI)		

References

- CrossLink-NX web page
- CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- CrossLink-NX 33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280)
- Thermal Management (FPGA-TN-02044)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- CrossLink-NX LIFCL-33 Pinout (FPGA-SC-02040)
- CrossLink-NX LIFCL-33U Pinout (FPGA-SC-02050)
- USB 2.0/3.2 IP Core User Guide (FPGA-IPUG-02237)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.4, October 2025

Section	Change Summary
All	Minor editorial fixes.
Abbreviations in This Document	Updated section contents.
Introduction	• Added, *Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists*, after the first paragraph of this section. • Removed the statement, *The LIFCL-33/33U devices include up to 33k Logic Cells*.
Power Supplies	• Updated the table title of Table 2.1 from *Single-Ended I/O Standards* to *Power Supply Description and Voltage Levels*. • Added *VCCPLL* in Table 2.1. Power Supply Description and Voltage Levels, Table 2.2. Recommended Power Filtering Groups and Components and in Figure 2.1. Recommended Power Filters.
Clock Inputs	• Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads.* • Added the PLL Reference Clock Locking section
Layout Recommendations	Replaced Figure 11.1. Recommended Layout with Figure 11.1. Ground Vias Implementation and Figure 11.2. Stitching Vias Implementation.
Checklist	• Added V_{CCPLL} under item 1.1.4. • Added item 6.3, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*. • Added *Clock Inputs* under *item 11.*

Revision 1.3, August 2024

Section	Change Summary
Inclusive Language	Added this section.
Abbreviations in This Document	Added IBIS to this section.
Configuration Considerations	• Changed subsection title from *Slave* SPI and I2C Configuration to *Target* SPI and I2C Configuration. • Changed SPI *Master*/Host to SPI *Controller*/Host in Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks.
Layout Recommendations	• Removed *All* from *Power should come from power planes to ensure good power delivery and thermal stability*. • Added *Target* to *High speed signals should target clearance of 5 times trace width from other signals*. • Changed differential pair length matching from *±4 mils* to *±0.1 mm*.
Simulation and Board Measurement of Critical Signals	Added this section.

Checklist	• Removed from the following from the checklist:
	  • 1.1.6. VCCAUXA and VCCAUXH2/H3/H4 pins should be ganged together and a solid PCB plane is recommended. This plane should not couple into the VCC core power plane.
	  • 1.1.7. All ground pins need to be connected to the board's ground plane.
	  • 1.2.7 and 1.3.4 and moved to 1.5. Follow recommended power filtering groups and components in Table 2.2. Recommended Power Filtering Groups and Components
	• Removed the word *MIPI* from 8.3 and 8.8.
	• Removed the word *LVDS* from 9.8.
	• Renamed Item no. 10 from *Hard USB Interface Requirements* to *USB Interface Requirements* and reworked contents.
	• Added the following to the checklist:

Section	Change Summary
	• 1.3. USB Block Supplies • 1.4. All ground pins need to be connected to the board's ground plane, including for unused blocks. • 1.5. Follow recommended power filtering groups and components in Table 2.2. • 8.9. Recommend MIPI Oscillator input use lowest jitter input Bank 4 pin PB6A. • 9.9 Recommend LVDS Oscillator input use lowest jitter input Bank 4 pin PB6A. • Updated contents of 8.3, 8.5, 8.6, 8.7, 9.3, 9.5, and 9.6. • Added Item no. 11 Layout Recommendations. • Added Item no. 12 Simulation and Board Measurement of Critical Signals.

Revision 1.2, March 2024

Section	Change Summary
Acronyms in This Document	Added *HPIO*, *I/O*, and *WRIO* to the list of acronyms.
Power Supplies	Added Figure 2.1. Recommended Power Filters to Recommended Power Filtering Groups and Components section.
Power Sequencing	Moved previous section *2.8. Power Sequencing* to this section.
Power Estimation	Moved previous section *2.9 Power Estimation* to this section.
Configuration Considerations	Moved previous section *5. Configuration Considerations* to this section and adjusted header, table, and figure numbers accordingly. Updated Table 6.1. JTAG Pin Recommendations: Removed *JTAG_EN* pin. Updated the *PCB Recommendations* for *TDI/SI*, *TMS/SCSN* and *TDO/SO* pins. Updated Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins: Updated the *PCB Connections* for *INITN*, *DONE*, *MCLK*, *MCSN*, and *TMS/SCSN* pins. Updated the *Notes* section of Table 6.3. Configuration Pins Needed per Programming Mode1. Added Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI, Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C and Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks. Added a paragraph about mixed voltage across configuration banks into Configuration Pins Per Programming Mode section.
External SPI Flash	Added this section.
I/O Pin Assignments	Moved previous section *6. I/O Pin Assignments* to this section and adjusted header numbers accordingly.
sysI/O	Added this section.
Clock Inputs	Moved previous section *4. Clock Inputs* to this section and adjusted header and figure numbers accordingly. Updated the paragraphs of this section: Added the phrase: *typically named as GPLL and PCLK*. Made editorial fixes.
Layout Recommendations	Added this section.
Checklist	Moved previous section *7. Checklist* to this section and adjusted header and table numbers accordingly.
References	Added this section.

Revision 1.1, October 2023

Section	Change Summary
All	• Updated document title to CrossLink-NX-33 and CrossLinkU-NX Hardware Checklist. • Added CrossLinkU-NX information. • Used LIFCL-33/33U to refer to the CrossLink-NX-33 and CrossLinkU-NX devices.
Acronyms in This Document	Added USB.

Introduction	In the Introduction section:
	• Added CrossLinkU-NX device support.
	• Updated the titles of the following references:
	  • CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104)
	  • CrossLink-NX 33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280)
	• Added the following references:
	  • CrossLink-NX LIFCL-33U Pinout (FPGA-SC-02050)
	  • USB 2.0/3.2 IP Core User Guide (FPGA-IPUG-02237)

Power Supplies	• Updated Table 2.1. Single-Ended I/O Standards.
	  • In $V_{CCIO[5:0]}$ Voltage (Nominal Value), added 1.0 V for Banks 0,1,5 and removed 1.35 V from Banks 2,3,4.
	  • Added power supplies.
	  • Added footnotes.
	• Updated Table 2.2. Recommended Power Filtering Groups and Components.
	  • Added power inputs.
	  • Added footnotes.
	• Added these subsections:
	  • Unused Hardware Always On Block (LIFCL-33U only)
	  • Unused USB Block (LIFCL-33U only)

Configuration Considerations	Added pins in Table 5.2. Pull-up/Pull-down Recommendations for Configuration Pins.
I/O Pin Assignments	• Updated information on HPIO and WRIO I/O pins support in the LVDS and MIPI Pin Assignments subsection. • Updated information on HPIO I/O pins support in the HSUL and SSTL Pin Assignments subsection. • Added the USB Block Pin Assignments (LIFCL-33U only) subsection.
Checklist	Updated Table 7.1. Hardware Checklist. • Added items under the *FPGA Power Supplies* group. • Added the *USB Interface Requirements* group.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.0, October 2022

Section	Change Summary
All	Initial release.

www.latticesemi.com