Lattice Avant Hardware Checklist

Technical Note

FPGA-TN-02317-1.1

September 2025

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Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
BGA	Ball Grid Array
DC	Direct Current
DLL	Delay-Locked Loop
DDR	Double Data Rate
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
HCSL	High-Speed Current Steering Logic
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
JTAG	Joint Test Action Group
LPDDR	Low-Power Double Data Rate memory
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SSTL	Stub Series-Terminated Logic
SERDES	Serializer/Deserializer
OTP	One-Time Programmable
BBRAM	Battery-Backed RAM
POR	Power-On-Reset
SSO	Simultaneous Switching Output
SI	Signal Integrity
IBIS	I/O Buffer Information Specification
SPI	Serial Peripheral Interface
MSPI	Master SPI (Controller SPI)
SSPI	Slave SPI (Target SPI)
CFGMODE	Configuration Mode Pin
VREF	Voltage Reference
LDO	Low Dropout Regulator
DNI	Do Not Install
HSPICE	High-Speed SPICE (Simulation Program with Integrated Circuit Emphasis)

1. Introduction

When designing complex hardware with the Lattice Avant™ device, you must pay close attention to critical hardware configuration requirements. This technical note outlines key implementation considerations specific to the Avant device. While it does not provide detailed step-by-step instructions, it offers a high-level checklist to support the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

Avant platform comprises of three FPGA variants:

- Avant-E – This variant has Wide Range I/O, High Speed I/O.
- Avant-G – This variant has Wide Range I/O, High Speed I/O, PCIe, Ethernet.
- Avant-X – This variant has Wide Range I/O, High Speed I/O, PCIe, Ethernet, SERDES Channels, DDR5.

This technical note assumes familiarity with the Avant device features as described in the Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107) and Lattice Avant Platform - Specifications Data Sheet (FPGA-DS-02112). These data sheets provide the functional specification for the device, including (but not limited to):

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

This technical note addresses the following critical hardware areas. For additional details, refer to the Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107) and Lattice Avant Platform – Specifications Data Sheet (FPGA-DS-02112):

- Power supplies and how to connect them to the PCB and the associated system.
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Refer to the following documents for detailed recommendations.

- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Thermal Management (FPGA-TN-02044)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SERDES Jitter (TN1084)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- Lattice Avant-E Pinout (FPGA-SC-02037)

2. Power Supplies

At power up the V_{CC}, V_{CCAUX}, V_{CCIO1}, and V_{CCIO2} power supplies are monitored to determine when the Avant device should deassert its internal Power-On Reset (POR) state and enter Power Good condition, initiating device initialization and configuration. These supplies must ramp up monotonically. Other supplies are not monitored during power-up but must reach a valid and stable level before configuration completes.

Table 2.1 lists the required power supplies and their corresponding voltage levels for each supply.

Table 2.1. Supply Rails

Supply Rail	Voltage (Nominal Value)[1]	Description
V_{SS}	—	Ground for internal FPGA logic and I/O
V_{CC}	0.82 V	FPGA core power supply. Required for Power Good condition.
V_{CCJB}[2]	0.82 V or Ground (See Description)	Power supply for JTAG Boundary Scan logic. Connect all VCCJB pins to 0.82 V rail to enable Boundary Scan (BSCAN) shift chain functionality, including SAMPLE, EXTEST, and the like. Connect these pins to ground to reduce static power consumption when BSCAN functionality is not required. Do not leave these pins floating.
$V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7}	0.82 V	Power supply for PLL blocks. Tie all listed PLL supplies together.
V_{CCAUX}	1.8 V	Auxiliary power supply. Used for generating stable drive current for the I/O. Required for Power Good condition.
V_{CCAUXA}	1.8 V	Auxiliary power supply for internal analog circuitry.
V_{CC_BAT}	1.5 V	Optional power supply to allow a battery to preserve the volatile configuration battery backed RAM (BBRAM) when the other DC supplies are absent.
$V_{CCIO[14:0]}$	Wide Voltage Range Banks 0, 1, 2, 12, 13, and 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V. High-Performance Banks 3 – 11: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	I/O driver supply voltage for each bank. Each bank has its own V_{CCIO} supply. V_{CCIO1} and V_{CCIO2} are required for Power Good condition as they are used during configuration.
V_{CCA_MPQx}[3]	0.80 V (≤ 16 Gbps) 0.90 V (> 16 Gbps)	Power supply for the SERDES Blocks' analog circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6
V_{CCH_MPQx}[3]	1.5 V (≤ 16 Gbps) 1.8 V (> 16 Gbps)	Power supply for the SERDES Blocks' digital circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6

Notes:

1. The Avant FPGA device includes a power-on-reset (POR) state machine that depends on several monitored power supplies. These supplies should ramp up monotonically. Device initialization does not proceed until all monitored power supplies reach their minimum operating voltages.
2. This is available only on Avant-E devices.
3. This is available only on Avant-G and Avant-X devices.

2.1. Power Noise

FPGA power rails allow a worst-case operating tolerance of ±3% of their nominal voltages. This tolerance includes all noise sources. An exception is the V_{CC_BAT} rail which supports a wider operating range of 1.0 V to 1.55 V.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 2% of the optimum voltage to allow power noise design margin.

When calculating total voltage regulator tolerance, consider the following:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR × expected current draw
- Expected voltage drops due to current measuring resistor's ESR × expected current draw

With 2% tolerance allocated to the voltage source, the design has a remaining 1% tolerance for noise and layout related issues. The lower voltage rails (< 1.2 V) are especially sensitive to noise (for the 0.82 V rail every 8.2 mV is 1% of the rail voltage).
For SERDES power rails, aim for ≤ 0.5% peak noise; for PLLs, target ≤ 0.25% peak noise.

3. Power Supply Filtering

Providing well-filtered power is essential for all supply rails and especially critical for analog rails. Each supply should be decoupled using appropriate power filters. Bypass capacitors must be placed as close as possible to the device package pins, with minimal trace length to reduce inductance.

For optimal performance, assign pins carefully to avoid placing noisy I/O signals near sensitive functional pins. PCB-related crosstalk often originates from FPGA outputs routed too close to sensitive power supply lines. A careful PCB layout is required to ensure noise immunity, particularly for analog supplies affected by switching noise from FPGA outputs. While this document provides filtering guidelines, robust layout practice is essential to prevent noise coupling into sensitive analog rails.

Extremely low-noise, well-filtered supplies are essential for the Avant SERDES, PLLs and V_{CCAUXA} rail.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	22 µF x 2 + 10 µF x 3 + 100 nF per pin	Core and clock logic. High-current rail; source using a switching regulator. 0.82 V
V_{CCJB}[1]	10 µF + 100 nF per pin	Power supply for JTAG Boundary Scan Logic. Connect to 0.82 V rail to enable BSCAN shift chain functionality, including SAMPLE, EXTEST, and the like. Connect to ground to reduce static power when BSCAN is not needed. Do not leave floating. Filtering capacitors may be omitted if permanently grounded. 0.82 V or Ground (See above description)
$V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} tied together	600 Ω FB 0805 (ESR ≤ 0.06 Ω) + 1.0 µF + 100 nF x4 + 0.01 µF	Sensitive PLL supply. Low current; Use LDO regulator for low noise. Tie all listed PLL supplies together. 0.82 V
V_{CCAUX}	120 Ω FB (ESR ≤ 0.1 Ω) + 10 µF x 2 + 100 nF per pin. For 841 fcCSP packages, add 1.0 µF per pin	Auxiliary power supply for internal analog circuitry. 1.8 V
V_{CCAUXA}	120 Ω FB (ESR <= 0.1 Ω) + 10 µF + 100 nF per pin For 841 fcCSP packages, add 1.0 µF per pin.	Sensitive Auxiliary power supply for internal analog circuitry. This rail must not be combined with V_{CCAUX}. 1.8 V
V_{CC_BAT}	10 µF + 100 nF	Optional power supply to allow a battery to preserve the volatile configuration RAM (BBRAM) when other DC supplies are absent. If not used the rail pin may be left unconnected. 1.5 V

Power Input	Recommended Filter	Notes
V_{CCIOx}	10 µF + 100 nF per pin For 841 fcCSP package add an additional 1.0 µF per pin.	Power supply for I/O banks. x = Specific Bank number. For unused banks, the 10 µF capacitor may be omitted. For banks with > 15 outputs or high capacitive loads, use 22 µF or an additional 10 µF. Use Lattice SSO tool to verify noise levels/ Wide-Range Banks: x = 0, 1, 2, 12, 13, and 14 supported V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V. High-Performance Banks: x = 3 – 11 supported V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.
V_{CCA_MPQx}[2]	0.80 V For data rate ≤ 16 Gbps 0.90 V For data rate > 16 Gbps 120 Ω FB + 10 µF x 2 + 100 nF per pin	Power supply for the SERDES Block analog circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6 Separate FB + Capacitor filter for each V_{CCA_MPQX}.
V_{CCH_MPQx}[2]	1.5 V For data rate ≤ 16 Gbps 1.8 V For data rate > 16 Gbps 120 Ω FB + 10 µF + 100 nF per pin	Power supply for the SERDES Block digital circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6 Separate FB + Capacitor filter for each V_{CCH_MPQX}.

Notes:

1. This is available only on Avant-E devices.
2. This is available only on Avant-G and Avant-X devices.

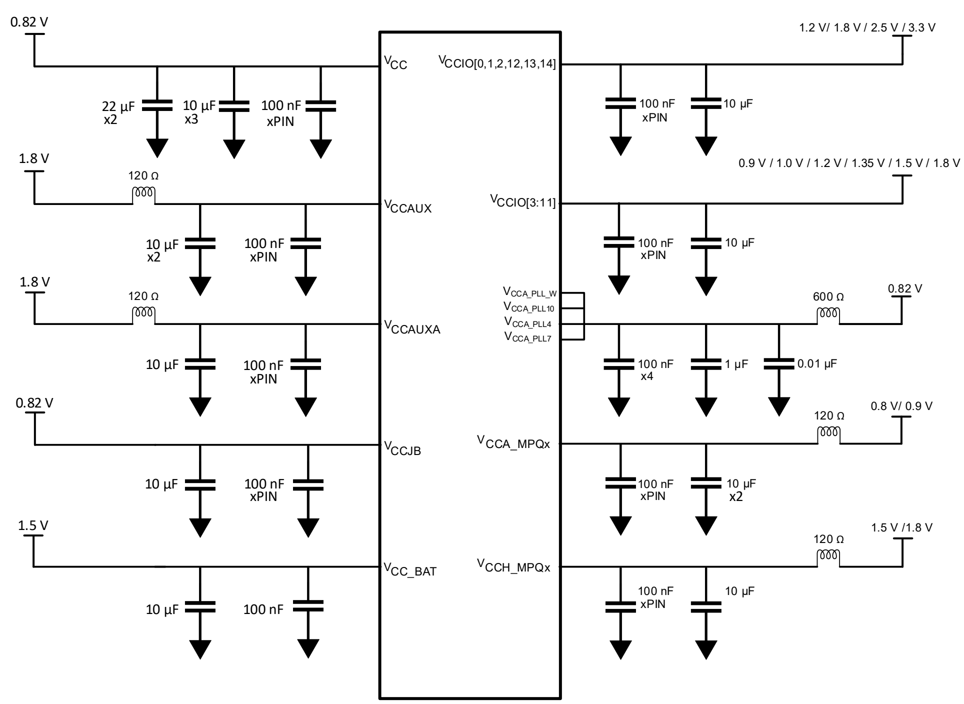

Figure 3.1. Recommended Power Filter

3.2. Ground Pins

All ground pins (V_{SS} and V_{SSR}) need to be connected to the board's ground plane.

3.3. EXT_RES pins

- These pins are dedicated to resistor connection to ground or bank V_{CCIO} only.
- Connect 240 Ω ±1% to ground on banks which use standards LVDS, subLVDS, SLVS, HSUL, POD, MIPI, D-PHY.
- Connect 240 Ω ±1% to VCCIO on banks which use LVSTL_I IO standard.
- Connect 180 Ω ±1% to VCCIO on banks which use LVSTL_II IO standard.
- Leave unconnected if the bank is not using one of the above standards.

Refer to the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for more information.

3.4. ERASEKEY*

The ERASEKEY pin enables secure erasure of customer keys stored in either One-Time Programmable (OTP) memory or Battery-Backed RAM (BBRAM).

Ground the ERASEKEY pin by default, and when not using the ERASEKEY function. By default, the ERASEKEY pin is disabled. It can be permanently enabled by blowing an OTP fuse. Once enabled, the erase function is initiated by asserting the pin HIGH for at least 350 ms.

Selection of OTP or BBRAM is made using BBRAM_EN fuse:

- **BBRAM_EN=0 (Default)**
  Security processor firmware will trigger a hardware state machine to permanently set all bits to 1s in the OTP memory key space.
- **BBRAM_EN=1**
  Security processor firmware will set all bits to 0s in the BBRAM key space.

***Note:** This is available only on Avant-G and Avant-X devices.

3.4.1. ERASEKEY Schematics

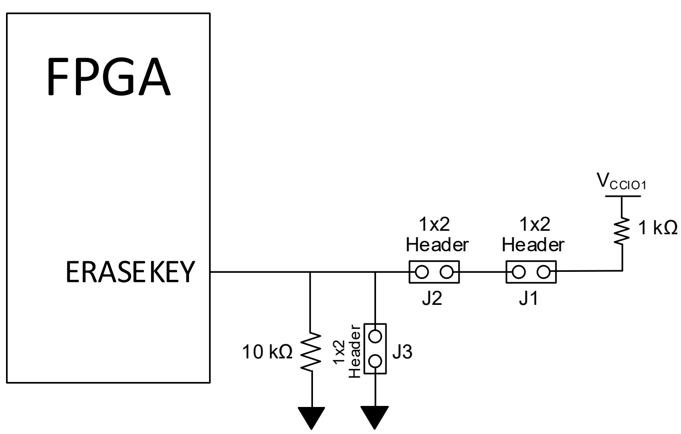

Figure 3.2. ERASEKEY Schematics

Note: J2 and J3 are optional and provide additional protection against accidental ERASEKEY activation.

Default configuration (ERASEKEY pin grounded)

- J1: OPEN
- J2: OPEN
- J3: INSTALLED

To activate ERASEKEY, the ERASEKEY pin must be held high for ≥ 350 ms.

Activation configuration (pin held high ≥ 350 ms)

- J1: INSTALLED
- J2: INSTALLED
- J3: OPEN

After activation, set to default configuration (ERASEKEY pin grounded)

- J1: OPEN
- J2: OPEN
- J3: INSTALLED

3.5. Unused GPIO Pins

All unused GPIO pins can be left open.

3.6. Unused Banks (V_{CCIOx})

- Connect unused V_{CCIOx} pins to a valid power rail. Do not leave them floating.
- Bypass each unused rail pin with 100 nF capacitor.

3.7. Unused SERDES Quads (V_{CCH_MPQx} and V_{CCA_MPQx})

For unused SERDES quads (Avant-G/X only), ground the following pins:

- Power pins VCCH_MPQx and VCCA_MPQx
- Differential Input Pairs MPQx_RXP/N
- Clock reference pins MPQx_REFCLKP/N
- External Reference Resistor Input REXT_MPQx (use 200 Ω)
- Leave differential outputs MPQx_TXP/N, unconnected

3.8. Clock Oscillator Supply Filtering

When using an external reference clock (single-ended or differential), ensure the oscillator's power supply is properly isolated and decoupled. A typical bypassing circuit is shown in Figure 3.3.

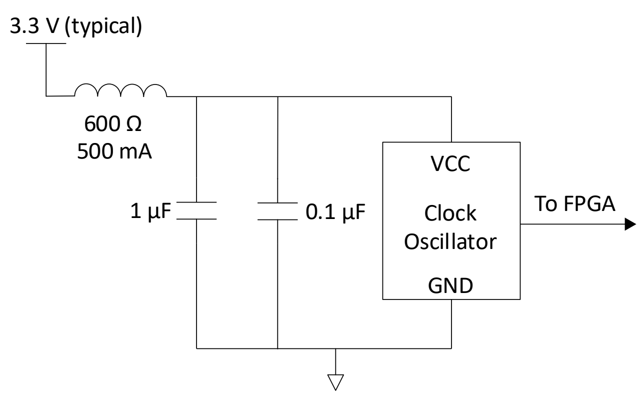

Figure 3.3. Clock Oscillator Bypassing

4. Power

4.1. Power Sequencing

Power sequencing is required when using the E70B or E30B with an external SPI configuration/boot flash whose flash V_{CC} exceeds 1.8 V. In this case, V_{CCIO1} must come up at least 300 µs before V_{CC} (core).

The Lattice Avant device does not require any other power rail sequencing for either power-up or power-down, which can significantly reduce power system cost and complexity.

Note: The internal Power-On-Reset (POR) circuit monitors V_{CC}, V_{CCAUX}, V_{CCIO1}, and V_{CCIO2} during power-up to determine when the device has reached the Power Good condition.

4.2. Power Estimation

After selecting the Avant device density, package, and logic implementation, estimate power consumption of the system environment using the Power Calculator included in the Lattice Radiant™ design tool. When estimating power, consider the following key objectives:

- Ensure power supply capacity accounts for the highest of the following: power-up in-rush current, configuration current, and maximum DC/AC operating current under expected system environmental conditions.
- Confirm that the system environment and the package can maintain the device's junction temperature within the specified maximum operating limit.

Addressing these two criteria early in the design phase ensures accurate power budgeting and thermal planning for the Avant device.

4.3. Ramp Rate

Power supply ramp rate must be monotonic and fall within the following ranges:

- For V_{CCIO} supplies: 0.1 V/ms to 20 V/ms
- For non-V_{CCIO} supplies: 0.1 V/ms to V*****/ 0.2 V/ms

***Note:** V indicates the power supply voltage.

5. Component Selection

5.1. Ferrite Bead Selection

- Most designs perform well with ferrite beads rated between 120 Ω and 240 Ω at 100 MHz.
- The noise voltage caused by ferrite bead ESR × CURRENT should remain below 0.5% of the rail voltage for non-analog rails, and below 0.25% for sensitive analog rails.
- For non-PLL rails, select ferrite beads with ESR between 0.01 Ω and 0.10 Ω based on the expected current load.
- PLL rails draw low current, which allow ferrite beads with ESR ≤ 0.40 Ω.
- Smaller package ferrite beads typically exhibit higher ESR than larger packages of the same impedance rating.
- Within the same package size, higher impedance ferrite beads generally have higher ESR than low impedance ones.

5.2. Capacitor Selection

Select good-quality ceramic capacitors in small packages, and place them as close as possible to the clock oscillator supply pins. *Good quality* bypass capacitors typically meet the following criteria:

5.2.1. Capacitor Dielectric

Use stable dielectric types such as X5R, X7R, and similar, which maintain capacitance within ±20% across the operating temperature range. Avoid dielectrics like Y5V, Z5U, and similar, which exhibit poor capacitance.

5.2.2. Voltage Rating

Capacitor effective capacitance decreases non-linearly under higher DC bias conditions. To ensure capacitance stability, select capacitors with voltage ratings at least 80% higher than the maximum voltage of the rail. For example, for a 3.3 V rail, use bypass capacitors rated at a minimum of 6.3 V.

5.2.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. Note that smaller capacitors within the same voltage rating are typically more expensive than their larger counterparts. Balancing cost and electrical performance, the recommended capacitor size are shown below:

Table 5.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

5.2.4. Mounting Location

Place the 0.1 µF capacitors as close as possible to the Avant FPGA's associated power rail pins. Using 0201-sized 0.1 µF capacitors enables placement on the PCB underside, between via holes beneath the FPGA ball pads.

6. Clock Inputs

The Avant device designates certain pins in each I/O bank for use as clock inputs. These pins are shared and may also function as general-purpose I/O.

When using these pins for clock input, it is critical to minimize signal noise to ensure reliable clock performance. Refer to Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).

These shared clock input pins, typically named GPLL and PCLK are listed under the *Dual Function* column in the device's *pinlist .csv* file. For high-speed differential interfaces (such as MIPI), route the differential clock pair to dedicated differential clock input pins labeled *PCLKTx_y* (+true) and *PCLKCx_y* (-complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

Ensure that the output voltage of any external reference oscillator does not exceed the V_{CCIO} voltage of the target I/O bank. For banks operating at $V_{CCIO} \leq 1.5$ V, use an HCSL oscillator to ensure the clock signal remains with the bank voltage limit. Alternatively, an LVDS oscillator may be used if AC-coupled and DC-biased to half the V_{CCIO} voltage. Figure 6.1. illustrates a dual-footprint PCB layout that supports both HCSL and LVDS oscillators.

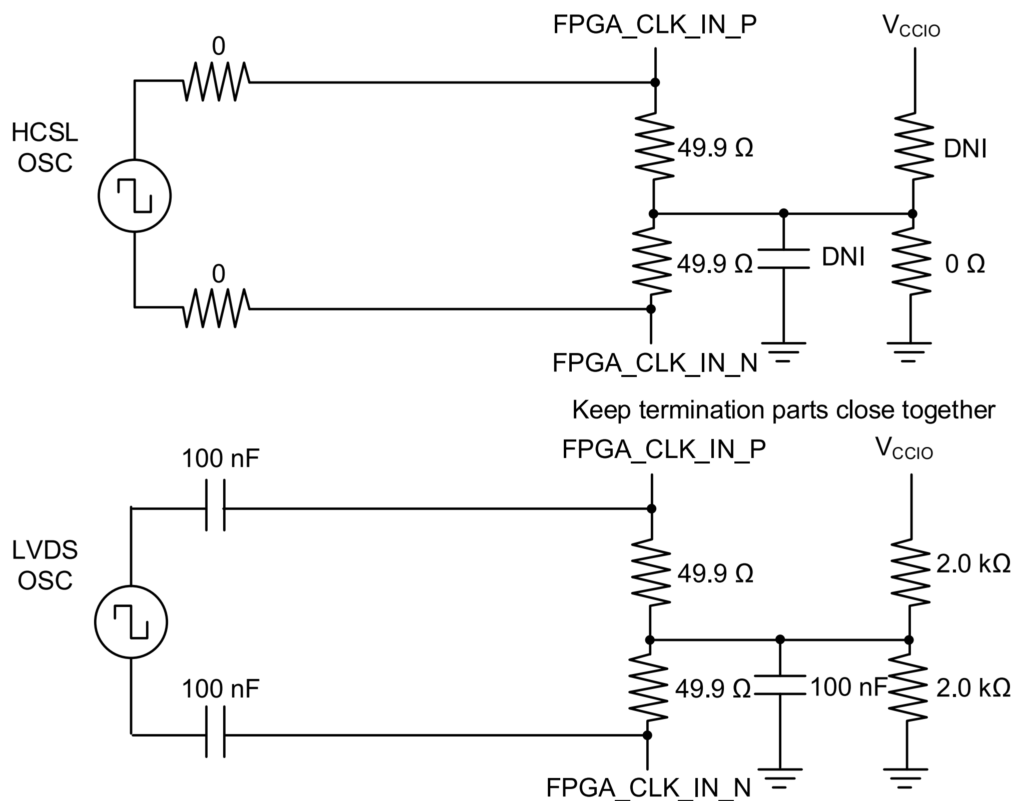

Figure 6.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

7. Configuration Considerations

7.1. JTAG

The Avant device supports configuration via the JTAG interface as well as through various sysCONFIG modes. The JTAG interface uses a 4-pin connection and requires specific PCB design considerations, detailed in Table 7.1.

Table 7.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
CFGMODE	2.0 kΩ pull-down to GND to enable JTAG Configuration
TCK	2.2 kΩ pull-down to GND
TMS	10 kΩ pull-up to V_{CCIO2}
TDI	10 kΩ pull-up to V_{CCIO2}
TDO	10 kΩ pull-up to V_{CCIO2}

The JTAG port enables debugging in the final system. It is recommended that all PCBs provide accessible JTAG pins, even if JTAG is not the primary configuration method. For best results, route the VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND signals to a common test header.

7.2. SPI Configuration

The Avant device supports configuration via both Controller (MSPI) and Target (SSPI) SPI interfaces. The pins listed in Table 7.2 have internal weak pull resistors, pull-up resistors to the appropriate bank V_{CCIO} and pull-down resistors to board ground. It is recommended to provide external pull resistors as indicated on the table.

Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO2}
INITN	10 kΩ pull-up to V_{CCIO2}
DONE	10 kΩ pull-up to V_{CCIO2}
CFGMODE	10 kΩ pull-up to V_{CCIO2} for MSPI Configuration 2.0 kΩ pull-down to GND for SSPI or JTAG Configuration
MCSN	10 kΩ pull-up to V_{CCIO1}
MCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO1} (Not installed by default) Series resistor placed near TX side[1].
MDQ0/MOSI	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ1/MISO	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ2 - MDQ7	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDS	MSPI Octal Mode Data Strobe, 10 kΩ pull-down to GND (Not installed by default)
SCSN	4.7 kΩ pull-up to V_{CCIO2}
SCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ0/MOSI	10 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ1/MISO	10 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ2 - SDQ7	10 kΩ t pull-up to V_{CCIO2} (Not installed by default)
SDS	SSPI Octal Mode Data Strobe, 10 kΩ pull-down to GND (Not installed by default)

Note:

1. Series resistor value depends on the PCB design. It ranges from 0 Ω (PCB impedance: 50 Ω) to 10 Ω (PCB impedance: 60 Ω).

7.3. Configuration Pins per Programming Mode

Table 7.3 summarizes the required signal pins for each supported configuration-programming mode.

Table 7.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
JTAG[1]	2	CFGMODE pin Low	TCLK	Input	1	TCK, TMS, TDI, TDO
MSPI	1	CFGMODE pin High	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
					8[2]	MCLK, MCSN, MDS, MD0, MD1, MD2, MD3, MD4, MD5, MD6, MD7
SSPI	1	CFGMODE pin Low	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
					8[2]	SCLK, SCSN, SDS, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7

Notes:

1. The JTAG port takes precedence over SSPI.
2. This is available only on Avant-G and Avant-X devices.

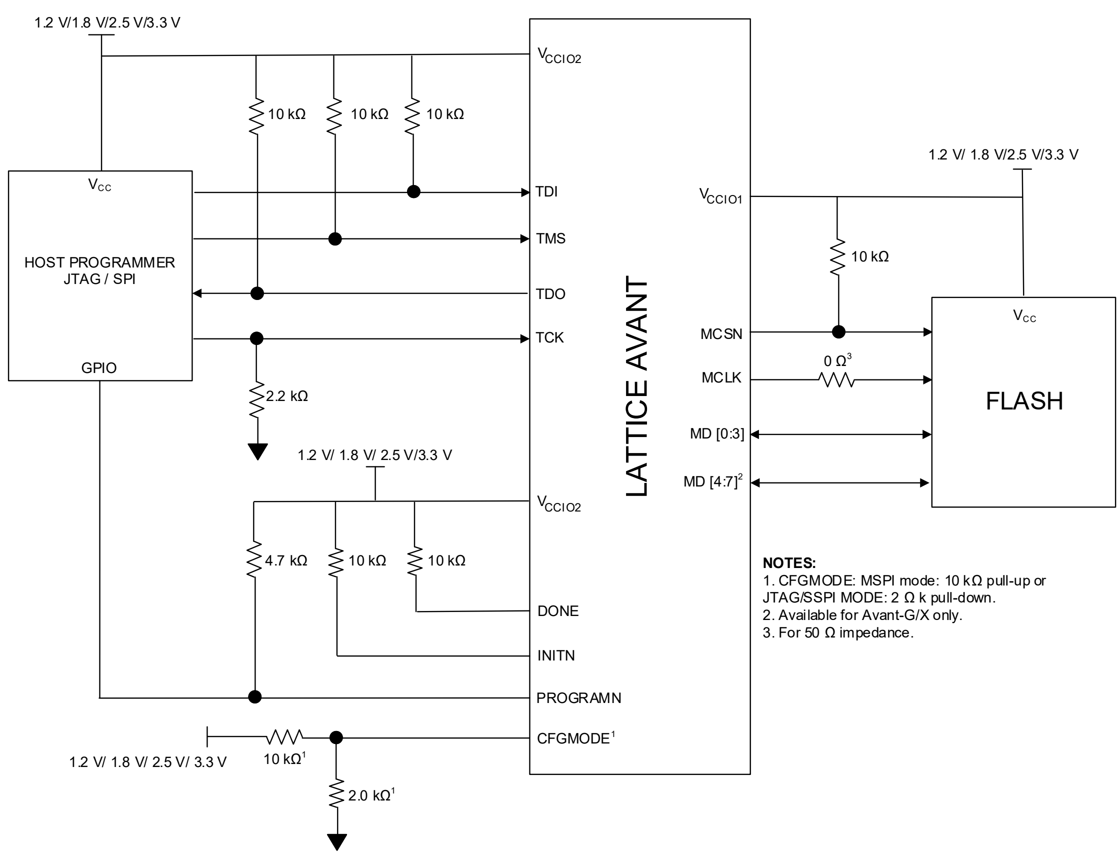

Figure 7.1. Typical Connections for Programming SRAM or External Flash via JTAG

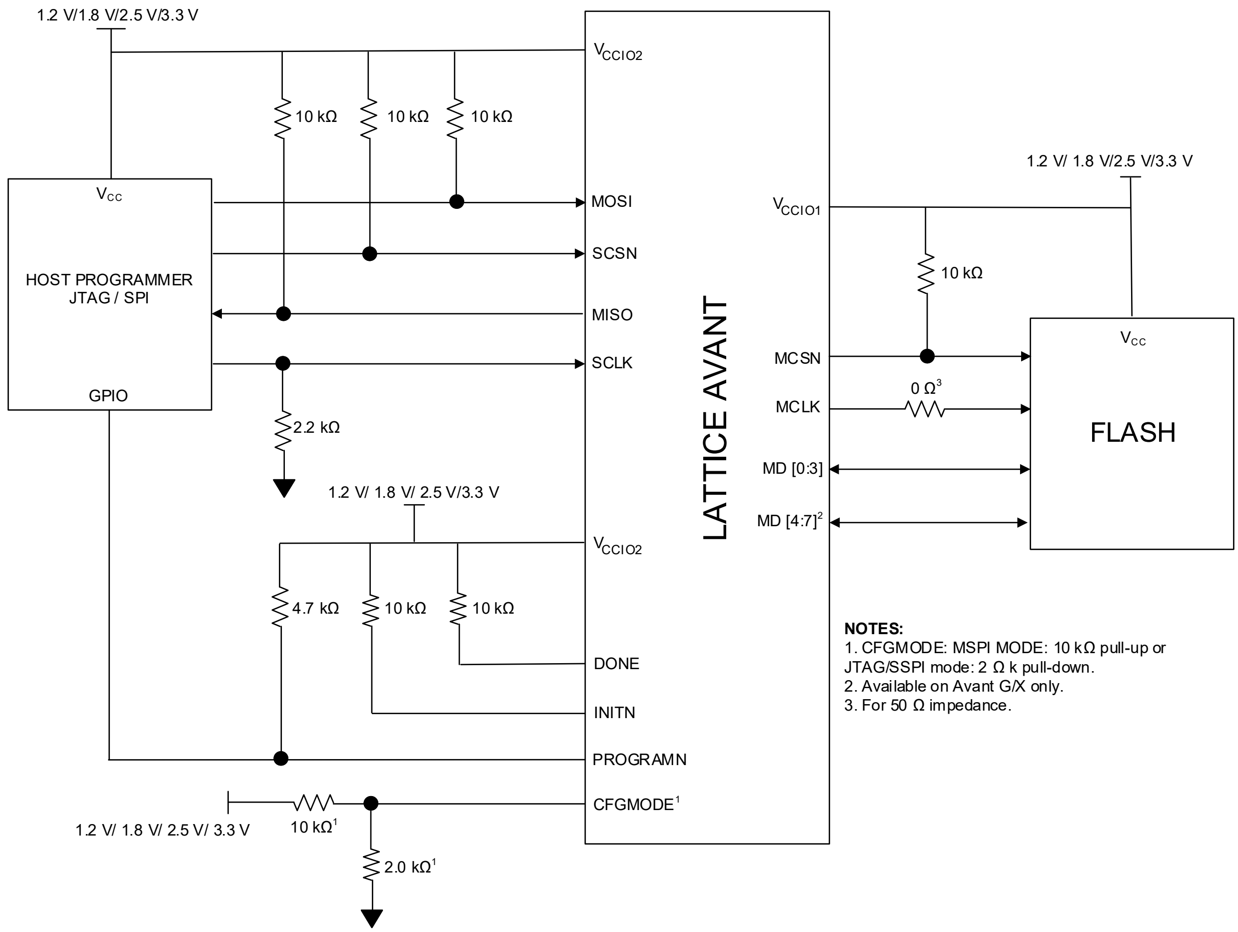

Figure 7.2. Typical Connections for Programming SRAM or External Flash via Target SPI

8. External SPI FLASH

The SPI Flash device voltage must match the V_{CCIO1} voltage level.

It is recommended to use an SPI flash device that is supported by the Lattice Radiant Programmer. To view the list of supported devices, open the Lattice Radiant Programmer, navigate to the **Help** menu, and search for **SPI Flash support**.

If your SPI Flash device is not listed, you may still be able to use it by configuring the **Custom Flash** option in the Radiant Programmer.

9. I/O Pin Assignments

While the Avant device packages help reduce crosstalk coupling, PCB layout can still introduce significant noise due to closely spaced I/O pins and parallel trace routing over long distances. For optimal jitter performance, assign noisy I/O pins away from sensitive power rails such as those for PLL and SERDES. Use PCB crosstalk or signal integrity simulation tool to evaluate and refine potentially problematic trace layouts.

Refer to PCB Layout Recommendations for BGA Packages (FPGA-TN-02024) for layout and breakout guidance.

Designers typically select FPGA pinouts early in the design cycle, which requires careful planning. For the FPGA designer, this requires detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

9.1. Early I/O Release

The Avant device supports an Early I/O Release feature, enabling I/Os to assume predefined drive states early during the bitstream processing. The Early I/O release feature releases the I/O after processing the I/O configuration which is located near the head of the bitstream data. Once data is programmed in the left/right Memory Interface Block (MIB) the I/O is released to a predefined state. Enable this feature by setting EARLY_IO_RELEASE to ON in the Lattice Radiant Device Constraint Editor.

9.2. Series Termination Resistors

When using series termination resistors, locate the resistors close to the transmitting pins.

Configuration pins to external devices (such as, SPI FLASH) default to 50RS (50 Ω) drive strength. For these pins, start with a value of 0 Ω for PCB impedance of 50 Ω. For higher PCB impedances increase the series termination resistance, for example 10 Ω for PCB impedance of 60 Ω.

Optimum series termination resistance value for user mode output pins depends on PCB etch impedance and selected output drive strength. Use IBIS models to simulate and determine the optimal starting resistance value. Further, test with oscilloscope and optimize the series termination resistance of critical signals for best signal integrity.

10. Functional Blocks Rule-Based Pinout Considerations

Avant devices support a wide range of high-speed interfaces, each with specific rule-based pinout requirements that must be considered during PCB design. Pinout selection should be guided by a clear understanding of the FPGA's internal interface building block. These include IOLOGIC blocks such as Soft MIPI, clock resource connectivity, and PLL usage. Refer to the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for rules pertaining to these interface types.

10.1. LVDS, MIPI, and Differential Pair Assignments

True LVDS and MIPI signaling inputs and outputs are available on the bottom-side I/O pins of the FPGA device (High-Performance banks 3 – 11). Differential input pairing under the High-Speed column in the *pinlist .csv* file.

- The *positive signal* of a differential pair should connect to an I/O pin ending in 'A' (such as, HPIOx_yA).
- The *negative signal* of a differential pair should connect to an I/O pin ending in 'B' (such as, HPIOx_yB).

The Wide Range banks (0, 1, 2, 12, 13, 14) on the top side I/O banks do not support true LVDS or MIPI standards, but can emulate LVDS outputs using external termination resistors. For implementation details, refer to the Lattice Avant sysI/O User Guide (FPGA-TN-02297).

- Set the bank voltage to 1.8 V to support LVDS.
- Set the bank voltage to 1.2 V to support MIPI.

10.2. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are reference I/O standards that require an external reference voltage (V_{REF}). These standards are supported only on the bottom-side High-Performance Banks (3 – 11).

- V_{REF} pin(s) should be prioritized during PCB pin assignment.
- These pins are labeled V_{REF} in the *Dual Function* column of the *pinlist .csv* file.
- Each bank has its own V_{REF} voltage, which sets the threshold for the referenced input buffers.
- Each I/O is individually configurable based on the bank's supply and reference voltages.

10.3. LVSTL I and LVSTL II Pin Assignments

The LVSTL I and LVSTL II interfaces require external reference resistor and are supported only on the device bottom-side High-Performance Banks (3 – 11).

- These pins are labeled *RES_EXT* in the *Dual Function* column of the *pinlist .csv* file.
- Each bank has a separate RES_EXT voltage.
- Refer to the EXT_RES pins subsection for resistor values and implementation details.
- For the pinout and grouping requirements of memory-mapped interfaces, see the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).

10.4. SERDES Pin Considerations

High-speed signaling requires meticulous PCB design to maintain proper transmission line characteristics.

- Ensure a continuous ground reference is maintained along high-speed signal paths.
- Differential pairs must be tightly length-matched, with a maximum mismatched of ±4 mil (±0.1 mm).
- Minimize discontinuities such as vias in high-speed routes.

For detailed design guidance, refer to the High-Speed PCB Design Considerations (FPGA-TN-02178).

11. Layout Recommendations

A good schematic design should be reflected in a good layout to ensure proper noise and power distribution. Below are some of the recommended layouts in general.

1. All power must come from power planes to ensure reliable power delivery and thermal stability.
2. Each power pin should have its own decoupling capacitor, typically 100 nF, placed as close as possible to the pin.
3. Place analog circuits away from digital circuits and high-switching components.
4. High-speed signals should maintain a clearance of five times the trace width from other signals.
5. High-speed signals transitioning between layers should include a corresponding ground via if both reference planes are ground. If the reference plane V_{CC}; use a stitching capacitor between ground and V_{CC}.

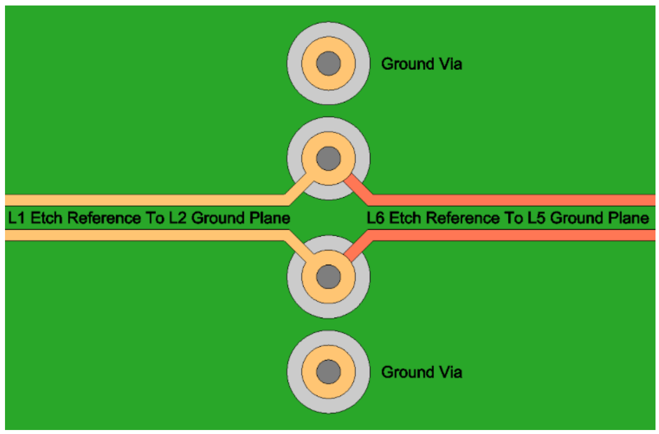

Figure 11.1 Ground Vias Implementation

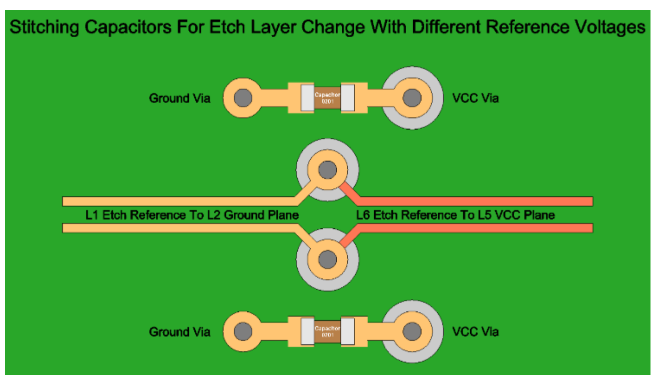

Figure 11.2 Stitching Vias Implementation

6. High-speed signals have specific impedance requirements. Calculate the necessary trace width and differential gaps based on the stack-up, and verify dimensions with the PCB vendor.
7. For differential pairs, match trace lengths as closely as possible—ideally within ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

12. Simulation and Board Measurement of Critical Signals

To ensure design reliability and high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

12.1. Critical Signals

Signals sensitive to signal integrity (SI) degradation are considered critical and require additional design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like.)
- Clocks (oscillator inputs, output clocks)
- Data with embedded clocks
- Interrupts (edge-triggered)
- Logic signals travelling long distances requiring termination

12.2. Simulation

Lattice Semiconductor provides an IBIS (I/O Buffer Information Specification) file for use with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often require a recurring subscription fee. The expensive tools can import board design files and can easily supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (such as Micro-cap) can provide basic simulations, but require additional effort to model SI effects across multiple signals with varying transmission line lengths, lossy lines, and crosstalk.

Use simulation results to optimize each critical signal for signal integrity:

- Set output pin drive strength
- Set output pin slew rate
- Design output pin termination (such as, output series termination resistor value)
- Configure internal pin pull-up and pull-down resistors
- Refine PCB layout

12.3. Board Measurements

Measure critical signals on the assembled PCB using an oscilloscope. Verify proper signal function and integrity (that is, eye diagram, SI parameters).

Use measurement results to optimize each critical signal for signal integrity:

- Adjust output pin drive strength
- Adjust output pin slew rate
- Modify output pin termination design (such as, output series termination resistor value).
- Configure internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for common signaling standards (such as, USB, MIPI)

13. SSO (Simultaneous Switching Output) Design Check

Users should verify designs to ensure they do not experience functional failures due to SSO voltage drops (sometimes call SSO noise, Ground Bounce, or Power Bounce).

SSO voltage drops result from package inductance combined with dynamic switching current which causes Ldi/dt voltage drops.

The Lattice SSO Tool should be used to estimate SSO voltage drop.

13.1. SSO Failures – Each of the following can lead to SSO failures

1. Many simultaneous switching outputs in the same I/O bank. The more outputs that switch simultaneously, the greater the ***di*** current, and consequently, the greater the Ldi/dt voltage drops.
2. I/O slew rates set to FAST (and sometimes MEDIUM). Faster slew rates reduce the ***dt*** time and thus increase Ldi/dt voltage drops.
3. I/O output current set high (for example, 8 mA – 16 mA). Higher I/O output current increases the ***di*** current and, therefore, the Ldi/dt voltage drops.
4. I/O capacitive loading is relatively high (especially > 15 pF). High capacitance loading increases the ***di*** current and, therefore, the Ldi/dt voltage drops.
5. I/O banks with low voltage rails (for example LVCMOS 1.0 V – LVCMOS 1.5 V) have smaller voltage margins and are more susceptible to Ldi/dt ground and power violations.

13.2. SSO Mitigations

1. Split up simultaneous switching outputs across multiple banks (where timing permits.) Fewer simultaneous outputs per bank reduce the ***di*** current and, therefore, the Ldi/dt voltage drops.
2. Reduce I/O slew rates to MEDIUM or preferably SLOW, if timing allows. Increasing slew time increases ***dt*** and reduces Ldi/dt voltage drops.
3. Reduce I/O output current (for example 4 mA), where timing and signal quality permit. Lower output current reduces ***di*** current and, therefore, Ldi/dt voltage drops.
4. Reduce I/O capacitive loading (this typically requires PCB design changes). Lower capacitance reduces ***di*** current and, therefore, Ldi/dt voltage drops.
5. Increase I/O bank voltage rails (this often requires PCB design changes). If the above mitigations are insufficient, increasing bank voltage can improve absolute voltage margins and ensure enough design margin for reliable operation.

14. Checklist

Table 14.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	System Supplies		
1.1.1	Voltage rails have ±3% tolerance. Use a voltage regulator with ≤ ±2% tolerance to allow ±1% power noise.		
1.1.2	Follow Table 3.1 for proper decoupling of each power rail.		
1.1.3	V_{CC} and V_{CCA_PLLx} at 0.82 V ±3%.		
1.1.4	V_{CCJB} at 0.82 V ±3% to enable JTAG Boundary Scan functions. V_{CCJB} connected to ground to save static power if/when JTAG Boundary Scan functions are not needed.		
1.1.5	Use a PCB plane for V_{CC} core with proper decoupling.		
1.1.6	V_{CC} core sized to meet power requirement calculation from software.		
1.1.7	V_{CCCLK}, V_{CCHP}, V_{CCA_PLLx} must be quiet and isolated from other switching noise and from each other.		
1.1.8	V_{CCAUX} and V_{CCAUXA} at 1.8 V ±3%.		
1.1.9	V_{CCAUX} and V_{CCAUXA} must be quiet and isolated from other switching noise and from each other.		
1.1.10	V_{CCAUX} pins should be tied together, and a solid PCB plane is recommended.		
1.1.11	V_{CCAUXA} pins are sensitive and should be filtered separately from V_{CCAUX} pins.		
1.1.12	V_{CC_BAT} pin at 1.5 V +3%/-33% ; if not used, leave pin open.		
1.2	I/O Supplies		
1.2.1	All Wide Range V_{CCIO} (Banks 0, 1, 2, 12, 13, and 14) V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V.		
1.2.2	All High-Performance banks (3 – 11) V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.		
1.2.3	V_{CCH_MPQx} pins must be quiet and isolated from other switching noises.		
1.3	SERDES Power Supplies		
1.3.1	V_{CCA_MPQx} pins: 0.80 V for data rates ≤ 16 Gbps 0.90 V for data rate > 16 Gbps.		
1.3.2	V_{CCA_MPQx} pins must be quiet and isolated from other switching noise.		
1.3.3	V_{CCH_MPQx} pins: 1.50 V for data rates ≤ 16Gbps 1.8 V for data rates > 16Gbps.		
1.4	Grounds		
1.4.1	All ground pins must be connected to a low-impedance, dedicated ground plane.		
1.5	Unused Blocks		
1.5.1	Connect unused V_{CCIOx} pins to a power rail. Do not leave them open. It is recommended to bypass unused rail pins with a 100 nF capacitor.		
1.5.2	Connect unused quads V_{CCH_MPQx} and V_{CCA_MPQx} pins to ground. Tie also reference pins $M_{PQx\_REFCLKP}$ and $M_{PQx\_REFCLKN}$ to ground.		
1.6	Power Sequencing		
1.6.1	The only power-up sequencing required for the Avant device is that any V_{CCIO} set to 1.8 V must come up with V_{CCAUX}. This is easily met by using the same power source for both V_{CCIO} set to 1.8 V and V_{CCAUX}.		
2	**JTAG**		
2.1	CFGMODE pin pulled high with 10 kΩ resistor or low using a 2.0 kΩ resistor, per Table 7.1.		
2.2	Keep CFGMODE accessible on the PCB to recover the JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on the PCB, especially during development.		
2.3.1	JTAG header: VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND.		

	Item	OK	NA
2.4	Apply a pull-down resistor on TCK, as specified in Table 7.1.		
2.5	Apply a pull-up resistor on TMS, TDI, and TDO, as specified in Table 7.1.		
3	**MSPI and SSPI Configuration**		
3.1	V_{CCIO1}, V_{CCIO2} bank voltages must match sysCONFIG peripheral devices (for example, SPI Flash, external connections).		
3.2	CFGMODE pin Apply a 10 kΩ pull-up resistor to V_{CCIO2} for MSPI configuration. Apply a 2.0 kΩ pull-down resistor to GND for SSPI configuration.		
3.3	Apply pull-up or pull-down resistors to persisted configuration-specific pins as specified in Table 7.1 and Table 7.2.		
4	**External Flash**		
4.1	The external Flash device voltage must match the V_{CCIO1} voltage.		
5	**Special Pin Assignments**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources, per the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).		
5.2	Shared general-purpose I/O are used as inputs for FPGA PLLs and clock input signals.		
5.3	Bank Voltage		
5.3.1	Set the bank voltage to 1.8 V to support LVDS signaling.		
5.3.2	Set the bank voltage to 1.2 V to support MIPI signaling.		
5.4	Referenced I/O standards.		
5.4.1	HSUL and SSTL are supported on the device’s bottom banks only (High-Performance banks 3 –11).		
5.4.2	Decouple the VREF pin using a 0.1 µF capacitor.		
5.5	Termination impedance: Rext[1] Resistor.		
5.5.1	LVSTL I require a 240 Ω ±1% resistor from Rext[1] to VCCIOx for proper termination impedances.		
5.5.2	LVSTL II requires a 180 Ω ±1% resistor from Rext[1] to VCCIOx for proper termination impedances.		
5.5.3	For POD or SSTL I/O standards, connect a 240 Ω resistor from Rext[1] to ground.		
5.5.4	For non-memory I/O standards, leave open.		
6	**Clock Inputs**		
6.1	High-speed differential interfaces (such as MIPI), when received by the FPGA, must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		
6.2	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
6.3	When providing an external reference clock to the FPGA, ensure that the oscillator’s output voltage does not exceed the bank’s voltage.		
6.4	For banks with $V_{CCIO} \leq 1.5$ V, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank’s V_{CCIO}. An LVDS oscillator may also be used if AC-coupled and DC-biased at half the V_{CCIO}. See Figure 6.1.		
7	**MIPI Interface Requirements**		
7.1	Soft MIPI is supported only on bottom banks (High-Performance banks 3 – 11).		
7.2	Set V_{CCIOX} to 1.2 V.		
7.3	Target 100 Ω impedance.		
7.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and the destination or source.		
7.5	Design differential pairs as *loosely coupled* with separation between the positive and negative traces of a pair of at least twice the etch width (intra-pair spacing).		
7.6	Provide separation between each differential pair of at least six times the etch width (inter-pair spacing).		
7.7	Match the lengths of clock and data lane pair traces within 0.1 mm for both intra-pair and inter-pair etches.		
7.8	The RX at the FPGA should have the clock differential pair routed to clock pins labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		

	Item	OK	NA
8	**LVDS Interface Requirements**		
8.1	LVDS is supported only on bottom banks (High-Performance banks 3 – 11).		
8.2	Set V_{CCIOX} to 1.8 V.		
8.3	Target 100 Ω impedance.		
8.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and the destination or source.		
8.5	Design differential pairs as *loosely coupled* with separation between the positive and negative traces of a pair of at least twice the etch width (intra-pair spacing).		
8.6	Provide separation between each differential pair of at least six times the etch width (inter-pair spacing).		
8.7	Match the lengths of clock and data lane pair traces within 0.1 mm for both intra-pair and inter-pair etches.		
8.8	The RX at the FPGA should have the clock differential pair routed to clock pins labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		
9	**LPDDR4 and DDR Interface Requirements**		
9.1	LPDDR4 and DDR interfaces are supported only on bottom banks (High-Performance banks 3 – 11).		
9.2	Set V_{CCIOX} to 1.1 V for LPDDR4 or 1.2V for DDR4.		
9.3	Target 100 Ω impedance for differential pair signal.		
9.4	Design differential pairs *loosely coupled* with separation between positive and negative traces of a pair of at least twice the etch width.		
9.5	Data group		
9.5.1	Route DQ, DM, and DQS signals should be routed in a data group with similar routing and matched via counts. Avoid using more than three vias between the FPGA controller and memory device.		
9.5.2	Each data group has specific DQS pins and groupings, which can be checked in *Pinlist.csv* under the DQS column.		
9.5.3	All data groups must reference a ground plane within the stack-up.		
9.5.4	Maintain trace length matching to a maximum of ±4 mil (±0.1 mm) between any DQ or DM signal and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
9.5.5	Differential pair of DQS to DQS_N trace lengths should be matched to a maximum of ±4 mil (±0.1 mm).		
9.5.6	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±4 mil (±0.1 mm).		
9.5.7	Assigned FPGA I/O within a data group may be swapped to allow clean layout. Do not swap DQS assignments.		
9.5.8	Resistor terminations (DQ), placed in a fly-by fashion at the FPGA, are highly recommended. Stub-style terminations, if used, should not include a stub longer than 600 mil.		
9.6	Control group		
9.6.1	CKE, CS, ODT, RESET signals should be routed as a group with similar routing and matched via counts. Avoid using more than three vias between the FPGA controller and memory device.		
9.6.2	The control group must be reference to a ground plane within the stack-up.		
9.6.3	Maintain trace length matching within ±4 mil (±0.1 mm) among signals in the control group. Use careful serpentine routing to meet this requirement.		
9.7	Address and Command Group		
9.7.1	Address, WE, RAS, CAS, ACT signals should be routed as a group within similar routing and matched via counts. Avoid using more than three vias between the FPGA controller and memory device.		
9.7.2	The address and command group must be reference to a ground plane within the stack-up.		
9.7.3	Maintain trace length matching within ±4 mil (±0.1 mm) among signals in the address and command group. Use careful serpentine routing to meet this requirement.		
9.7.4	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub-style terminations, if used, should not include a stub longer than 600 mils.		
9.7.5	Address and control signals may be referenced to a power plane if a ground plane is not available; however, ground reference is preferred.		

	Item	OK	NA
9.8	Clock		
9.8.1	The clock signal must be reference to a ground plane within the stack-up.		
9.8.2	CK to CK_N trace lengths must be matched within ±4 mil (±0.1 mm).		
9.8.3	The clock signal should match with the data group and address and command group within ±4 mil (±0.1 mm).		
9.9	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
9.10	DDR trace reference must be a solid ground plane without slots or breaks. It should remain continuous between the FPGA and the memory device.		
9.11	Address and control signals should be routed on a separate PCB layer from DQ, DQS, and DM signals to minimize crosstalk.		
10	**SERDES (Avant-G/X only)**		
10.1	Use a continuous ground reference plane for all serial channels.		
10.2	Match differential pair trace lengths within ±4 mil (±0.1 mm).		
10.3	Maintain proper high-speed transmission line routing with at least 10 times spacing from the reference plane to other signals.		
10.4	Do not route other signals above or below high-speed SERDES traces unless proper isolation is provided.		
10.5	Ensure the dedicated reference clock input from the clock source meets both DC and AC requirements.		
10.6	Reference clock termination resistors may be required to ensure compatible signaling levels. See Figure 6.1.		
10.7	External AC coupling capacitors may be required to ensure compatibility with common-mode voltage levels.		
11	**Layout Notes**		
11.1	Use 0201-size 0.1 µF capacitors to fit on the opposite side of the PCB from the Avant FPGA, between ball pad via holes.		
11.2	When using series termination resistors, place them close to the transmitting pin. Configuration pins connected to external devices (for example SPI FLASH) default to 50RS (50 Ω) drive strength. For these, start with a 0 Ω resistor for a PCB impedance of 50 Ω. For higher PCB impedances, increase the series termination resistance accordingly (for example, 10 Ω for 60 Ω impedance). The optimum series termination resistance for user-mode output pins depends on PCB etch impedance and selected output drive strength. Use IBIS model simulations to determine a starting value, then validate and optimize using oscilloscope measurements for best signal integrity.		
11.3	Match the lengths of differential pair traces (positive and negative) within ±4 mil (±0.1 mm) to maintain signal integrity data rates up to 25 Gbps.		
12	**Simulation and Board Measurement of Critical Signals**		
12.1	Simulations: Use the IBIS model to simulate critical signals for proper signal integrity.		
12.1.1	Simulate differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like).		
12.1.2	Simulate clock nets (oscillator inputs, output clocks).		
12.1.3	Simulate data nets with embedded clocks.		
12.1.4	Simulate interrupts (edge-triggered).		
12.1.5	Simulate logic signals traveling long distances that require termination.		
12.1.6	Simulation results should be used to optimize each critical signal for optimal signal integrity: • Define output pin drive strength • Define output pin slew rate • Define output pin termination design (for example, output series termination resistor value) • Define settings of internal pin pull-up and pull-down resistors Improve PCB layout.		
12.2	Board Measurements: Use an oscilloscope to measure on PCB assembly critical signals for proper function and signal integrity.		

	Item	OK	NA
12.2.1	Measure differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like).		
12.2.2	Measure clock nets (oscillator inputs, output clocks).		
12.2.3	Measure data nets with embedded clocks.		
12.2.4	Measure interrupts (edge-triggered).		
12.2.5	Measure logic signals traveling long distances that require termination.		
12.2.6	Measurement results should be used to optimize each critical signal for optimal signal integrity: • Adjust output pin drive strength • Adjust output pin slew rate • Adjust output pin termination design (for example, output series termination resistor value) • Adjust settings of internal pin pull-up and pull-down resistors.		
12.3	Specification compliance testing is recommended for popular signaling methods (for example, USB, MIPI).		
13	**SSO (Simultaneous Switching Output)**		
13.1	When a bank has many outputs that switch simultaneously, internal SSO noise may be generated, which, if excessive, can cause unreliable operation. It is recommended that you verify your design using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
13.2	You should verify your design using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
13.3	Reducing SSO Noise.		
13.4	Reduce the number of I/Os switching simultaneously in a bank. (Stagger output switching into smaller groups).		
13.5	Reduce output current drive on switching I/Os (for example, configure for 4 mA instead of 8 mA).		
13.6	Distribute a large group of I/Os across multiple banks instead of placing all in the same bank.		
13.7	Add virtual ground pins to the bank. Connect an I/O to ground on the PCB and program it to output a low at maximum current.		
13.8	Add virtual V_{CCIO} pins to the bank. Connect an I/O to the bank's V_{CCIO} rail on the PCB and program it to output a high at maximum current.		
13.9	When a bank has many outputs that switch simultaneously, internal SSO noise may be generated, which, if excessive, can cause unreliable operation. It is recommended that you verify your design using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
13.10	You should verify your design using the Lattice Simultaneous Switching Output (SSO) calculator tool.		

Note:

1. The REXT resistor value is 200 Ω.

References

- Avant-E web page
- Avant-G web page
- Avant-X web page

A variety of technical notes for the Lattice Avant platform are available.

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant Hardware Checklist (FPGA-TN-02317)
- Lattice High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107)
- Lattice Avant Platform - Specifications Data Sheet (FPGA-DS-02112)
- Lattice Avant Power User Guide (FPGA-TN-02291)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)
- IP Cores and Reference Designs for Avant Devices
- Kits, Boards, and Demonstrations for Avant Devices

Other references:

- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

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For frequently asked questions, please refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, September 2025

Section	Change Summary
All	Minor editorial fixes.
Abbreviation in This Document	Updated this section.
Introduction	• Added, *Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists*, after the first paragraph of this section. • Removed the statement, *The device family consists of FPGA densities ranging from 196k to 477k Logic Cells*.

Power Supplies	• Updated Table 2.1. Supply Rails.
	  • Replaced V_{CCA_PLLx} with $V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} and removed *x = Specific PLL number* in the description.
	  • Removed old note 2 – *If V_{CCIO} is set to 1.8 V, it must share the same power source as V_{CCAUX}*.

Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components. • Updated the values of V_{CC_PLLx} and replaced V_{CC_PLLx} *with $V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} tied together*. • Updated V_{CC_PLLx} values and replaced V_{CC_PLLx} with $V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} in Figure 3.1. Recommended Power Filter. • Added the ERASEKEY section. • Added an External Reference Resistor (REXT_MPQx) value of *200 Ω* in the Unused SERDES Quads section.
Power	• Reworked the Power Sequencing section. • Reworked the Ramp Rate section.
Clock Inputs	• Added *GPLL* and *PCLK*. • Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*.
Layout Recommendations	Replaced Figure 11.1 Recommended Layout with Figure 11.1 Ground Vias Implementation and Figure 11.2 Stitching Vias Implementation.
Checklist	• Removed old item 1.2.3 – *Any V_{CCIO} set to 1.8 V must come up with V_{CCAUX}. This is easily met by using the same power source for both V_{CCIO} set to 1.8 V and V_{CCAUX}*. • Added item 6.2, *For single-ended I/Os, use only PCLKT pins as primary CLK pads.* • Added a note that *REXT resistor value is 200 Ω*.

Revision 1.0, December 2024

Section	Change Summary
Power Supply Filtering	Reworked EXT_RES pins section.

Revision 0.82, November 2024

Section	Change Summary
All	• Minor editorial fixes. • Changed *Master* to *Controller*. • Changed *Slave* to *Target*.
Inclusive Language	Added this section.

Section	Change Summary
Abbreviations in This Document	Replaced *Acronyms* with *Abbreviations*.
Power Supplies	Removed VCCCLK and VCCHP in Table 2.1. Supply Rails.

Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  ◦ Removed VCCCLK and VCCHP.
	  ◦ VCCAUX, VCCAUXA, and VCCIOX – added a recommended filter for 841 fcCSP package.
	  ◦ VCCIOX – added the statement, *check SSO noise level using Lattice SSO tool* under the Notes column.
	• Added Figure 3.1. Recommended Power Filter.
	• Added EXT_RES pins subsection.
	• Added Unused GPIO Pins subsection.
	• Added the bullet, *Differential output Pairs MPQx_TXP/N, leave open* under the Unused SERDES Quads subsection.

Power	Added Ramp Rate subsection.

Configuration Considerations	• Changed the pull-down resistor of CFGMODE from *10 kΩ* to *2 kΩ* in Table 7.1. JTAG Pin Recommendations.
	• Replaced the statement, *For best results, route the TCK, TMS, TDI, TDO, and CFGMODE signals to a common test header along with VCCIO2 and ground. Adding signals PROGRAMN and DONE increase debug usability,* with *For best results, route the VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND signals to a common test header,* under the JTAG subsection.
	• Updated Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins.
	  ◦ Changed the pull-down resistor of CFGMODE from *10 kΩ* to *2 kΩ*.
	  ◦ Changed the pull-up resistor of MCSN from 4.7 *kΩ* to 10 *kΩ*.
	  ◦ MCLK - added a series resistor placing near the TX side.
	  ◦ SCSN – replaced VCCIO1 with VCCIO2.
	  ◦ Added table note 1 - Series resistor value depends on the PCB design, range from 0 Ω for PCB impedance of 50 Ω to 10 Ω for PCB impedance of 60 Ω.
	• Added table note 2 – Available in Avant-G/X only in Table 7.3. Configuration Pins Needed per Programming Mode.
	• Added Figure 7.1. Typical Connections for Programming SRAM or External Flash via JTAG and Figure 7.2. Typical Connections for Programming SRAM or External Flash via Target SPI.

External SPI Flash	Added this section.
I/O Pin Assignments	• Reworked the Series Termination Resistors subsection. • Removed the Simultaneous Switching Outputs (SSO) Noise subsection.
Functional Block Rule-Based Pinout Considerations	Reworked the LVSTL 1 and LVSTL II Pin Assignments subsection.
Layout Recommendations	Added this section.
Simulation and Board Measurement of Critical Signals	Added this section.
SSO (Simultaneous Switching Output) Design Check	Added this section.
Checklist	Reworked this section.

Revision 0.81, November 2023

Section	Change Summary
Disclaimers	Updated this section.
Power Supplies	Added new supply rail V_{CCIB} and its Voltage and Description information in Table 2.1. Supply Rails.

Section	Change Summary
Power Supply Filtering	• Added power input V_{CCJB} and its Recommended Filter and Notes information in Table 3.1. Recommended Power Filtering Groups and Components. • Added ground pins *(VSS and VSSR)* in Ground Pins section. • Updated Unused SERDES Quads (V_{CCH_MPQx} and V_{CCA_MPQx}) section.
Clock Inputs	Updated Figure 6.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators.
Checklist	Added new FPGA power supply *V_{CCJB} @ 0.82 V ±3% to enable JTAG Boundary Scan functions. V_{CCJB} Connected to ground to save static power if/when JTAG Boundary Scan functions not needed.* in Table 14.1. Hardware Checklist.
References	Added this section.

Revision 0.80.1, May 2023

Section	Change Summary
All	Minor adjustments in formatting across the document.
Power Supplies	• Changed numbering from Section 1.1 to Section 2. • Updated Table 2.1. Supply Rails. • Added Power Noise section and updated Power Source section.
Power Supply Filtering	Updated Table 3.1. Recommended Power Filtering Groups and Components.
Clock Inputs	• Changed numbering from Section 3 to Section 6. • Deleted Figure 6.1.
Configuration Considerations	Changed numbering from Section 4 to Section 7.
I/O Pin Assignments	• Changed numbering from Section 5 to Section 8. • Added Simultaneous Switching Outputs (SSO) Noise section.
Functional Blocks Rule-Based Pinout Considerations	• Updated the title of LVDS, MIPI, and Differential Pair Assignments section from LVDS and MIPI Assignments. • Added sentence The positive signal of a differential pair should connect to an I/O ending in 'A' (ex. HPIOx_yA). The negative signal of a differential pair should connect to an I/O ending in 'B' (ex. HPIOx_yB) in LVDS, MIPI, and Differential Pair Assignments. • Added LVSTL I, LVSTL II, and Other I/O Standards Termination Impedance Rext Resistor section.
Checklist	Updated Table 10.1. Hardware Checklist.

Revision 0.80, December 2022

Section	Change Summary
All	Preliminary release.

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