Lattice Avant Hardware Checklist

Technical Note

FPGA-TN-02317-1.0

December 2024

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
BGA	Ball Grid Array
DC	Direct Current
DLL	Delay-Locked Loop
DDR	Double Data Rate
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
HCSL	High-Speed Current Steering Logic
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
JTAG	Joint Test Action Group
LPDDR	Low-Power Double Data Rate memory
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SSTL	Stub Series-Terminated Logic
SERDES	Serializer/Deserializer

1. Introduction

When designing complex hardware using the Lattice Avant™ device, the user must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the Avant device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

Avant platform comprises of three FPGA variants:

- Avant-E – This variant has Wide Range I/O, High Speed I/O.
- Avant-G – This variant has Wide Range I/O, High Speed I/O, PCIe, Ethernet.
- Avant-X – This variant has Wide Range I/O, High Speed I/O, PCIe, Ethernet, SERDES Channels, DDR5.

The device family consists of FPGA densities ranging from 196k to 477k Logic Cells. This technical note assumes that the reader is familiar with the Avant device features as described in the Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107) and Lattice Avant Platform - Specifications Data Sheet (FPGA-DS-02112). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

The critical hardware areas covered in this technical note are listed below. Refer to the Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107) and Lattice Avant Platform – Specifications Data Sheet (FPGA-DS-02112) for details.

- Power supplies and how to connect them to the PCB and the associated system.
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Refer to the following documents for detailed recommendations.

- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Thermal Management (FPGA-TN-02044)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02150)
- LatticeSC™ SERDES Jitter (TN1084)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- Lattice Avant-E Pinout (FPGA-SC-02037)

2. Power Supplies

At power up the V_{CC}, V_{CCAUX}, V_{CCIO1}, and V_{CCIO2} power supplies are monitored to determine when the Avant should de-assert its internal Power-On Reset state and enter Power Good condition, which starts device initialization and configuration. These supplies should come up monotonically. Other supplies are not monitored during power-up but need to be at valid and stable level before the device configuration is complete.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Supply Rails

Supply Rail	Voltage (Nominal Value)[1]	Description
V_{SS}	—	Ground for internal FPGA logic and I/O
V_{CC}	0.82 V	FPGA core power supply. Required for Power Good condition.
V_{CCJB}[3]	0.82 V or Ground (See Description)	Power supply for JTAG Boundary Scan logic. Connect all VCCJB pins to 0.82 V rail to enable Boundary Scan (BSCAN) shift chain functionality, including SAMPLE, EXTEST, and the like. Connect these pins to Ground to reduce static power consumption when BSCAN functionality is not required or no longer required. These pins should not be floated.
V_{CCA_PLLx}	0.82 V	Power supply for PLL blocks. x = Specific PLL number.
V_{CCAUX}	1.8 V	Auxiliary power supply. Used for generating stable drive current for the I/O. Required for Power Good condition.
V_{CCAUXA}	1.8 V	Auxiliary power supply for internal analog circuitry.
V_{CC_BAT}	1.5 V	Optional power supply to allow a battery to preserve the volatile configuration battery backed RAM (BBRAM) when the other DC supplies are absent.
$V_{CCIO[14:0]}$[2]	Wide Voltage Range Banks 0, 1, 2, 12, 13, and 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V. High-Performance Banks 3 – 11: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply. V_{CCIO1} and V_{CCIO2} have pins used for device configuration and are required for Power Good condition.
V_{CCA_MPQx}[4]	0.80 V For data rate <= 16 Gbps 0.90 V For data rate > 16 Gbps	Power supply for the SERDES Blocks' analog circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6
V_{CCH_MPQx}[4]	1.5 V For data rate <= 16 Gbps 1.8 V For data rate > 16 Gbps	Power supply for the SERDES Blocks' digital circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6

Note:

1. The Avant FPGA device has a power-on-reset state machine that depends on several power supplies. These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies reach minimum operating voltages.
2. If V_{CCIO} is set to 1.8 V, they must come from the same power supply as V_{CCAUX}.
3. Available on Avant-E only.
4. Available on Avant-G/X only.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±3% of the nominal voltages, with the exception of V_{CC_BAT} rail which allows 1.0 V to 1.55 V operation. The 3% tolerance includes any noises.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 2% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator’s feedback pin which sets regulator’s output voltage
- Expected voltage drops due to power filtering ferrite bead’s ESR × expected current draw
- Expected voltage drops due to current measuring resistor’s ESR × expected current draw

With 2% tolerance allocated to the voltage source, the design has a remaining 1% tolerance for noise and layout related issues. The lower voltage rails (< 1.2 V) are especially sensitive to noise (for the 0.82 V rail every 8.2 mV is 1% of the rail voltage).

For SERDES power rails, it is recommended to target a maximum 0.5% peak noise. For PLLs, target less than 0.25% peak noise.

3. Power Supply Filtering

Providing a quiet filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with very short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk to sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

It is critical to have very low-noise highly filtered supplies for the Avant SERDES, PLLs and V_{CCAUXA} rail.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	22 µF x 2 + 10 µF x 3 + 100 nF per pin	Core and clock logic. High current rail, source using switching regulator. 0.82 V
V_{CCJB}[1]	10 µF + 100 nF per pin	Power supply for JTAG Boundary Scan logic. Connect all VCCJB pins to 0.82 V rail to enable Boundary Scan (BSCAN) shift chain functionality, including SAMPLE, EXTEST, and the like. Connect these pins to Ground to reduce static power consumption when BSCAN functionality is not required or no longer required. Designs that permanently ground these pins can omit filtering capacitors for these pins. These pins should not be floated. 0.82 V or Ground (See above description)
V_{CCA_PLLx}	600 Ω FB (ESR ≤ 0.4 Ω) + 1.0 µF + 100 nF	Sensitive power supply for PLL blocks. Low current, use LDO regulator for low noise. Separate FB + Capacitor filter for each V_{CCA_PLLx}. 0.82 V
V_{CCAUX}	120 Ω FB (ESR ≤ 0.1 Ω) + 10 µF x 2 + 100 nF per pin. For 841 fcCSP package add an additional 1.0 µF per pin.	Auxiliary power supply for internal analog circuitry. 1.8 V
V_{CCAUXA}	120 Ω FB (ESR <= 0.1 Ω) + 10 µF + 100 nF per pin For 841 fcCSP package add an additional 1.0 µF per pin.	Sensitive Auxiliary power supply for internal analog circuitry. This rail must not be combined with V_{CCAUX}. 1.8 V
V_{CC_BAT}	10 µF + 100 nF	Optional power supply to allow a battery to preserve the volatile configuration RAM (BBRAM) when other DC supplies are absent. If not used the rail pin may be left unconnected. 1.5 V

Power Input	Recommended Filter	Notes
V_{CCIOx}	10 µF + 100 nF per pin For 841 fcCSP package add an additional 1.0 µF per pin.	Power supply for I/O banks. x = Specific Bank number. Unused banks can remove the 10 µF. Banks with lots of outputs (> 15) or large capacitive loading should replace the 10 µF with a 22 µF (or add a second 10 µF) and check SSO noise levels using Lattice SSO tool. Wide-Range Banks: x = 0, 1, 2, 12, 13, and 14 supported V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V. High-Performance Banks: x = 3 – 11 supported V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.
V_{CCA_MPQx}[2]	0.80 V For data rate ≤ 16 Gbps 0.90 V For data rate > 16 Gbps 120 Ω FB + 10 µF x 2 + 100 nF per pin	Power supply for the SERDES Block analog circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6 Separate FB + Capacitor filter for each V_{CCA_MPQX}.
V_{CCH_MPQx}[2]	1.5 V For data rate ≤ 16 Gbps 1.8 V For data rate > 16 Gbps 120 Ω FB + 10 µF + 100 nF per pin	Power supply for the SERDES Block digital circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6 Separate FB + Capacitor filter for each V_{CCH_MPQX}.

Note:

1. Available on Avant-E only.
2. Available on Avant-G/X only.

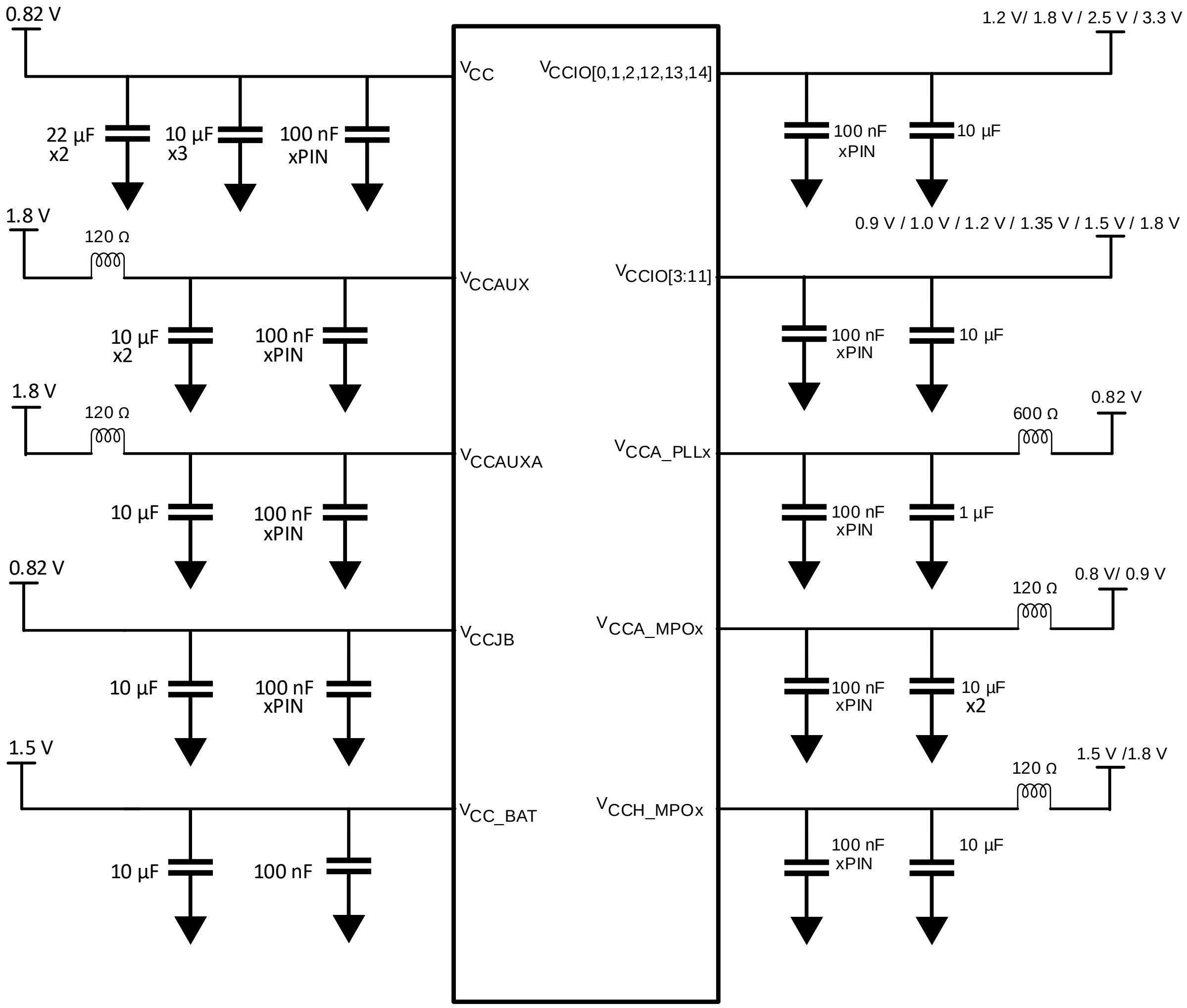


Figure 3.1. Recommended Power Filter

3.2. Ground Pins

All ground pins (VSS and VSSR) need to be connected to the board's ground plane.

3.3. EXT_RES pins

- These pins are dedicated for resistor connection to ground or bank V_{CCIO} only.
- Connect 240 Ω ±1% to ground on banks which use standards LVDS, subLVDS, SLVS, HSUL, POD, MIPI, D-PHY.
- Connect 240 Ω ±1% to VCCIO on banks which use LVSTL_I IO standard.
- Connect 180 Ω ±1% to VCCIO on banks which use LVSTL_II IO standard.
- Leave unconnected if bank is not using one of the above standards.

Refer to the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for more information.

3.4. Unused GPIO Pins

All unused GPIO pins can be left open.

3.5. Unused Banks (V_{CCIOx})

- Connect unused V_{CCIOx} pins to a power rail. Do not leave them open.
- Recommend bypassing unused rail pin with a 100 nF.

3.6. Unused SERDES Quads* (V_{CCH_MPQx} and V_{CCA_MPQx})

Unused SERDES Quad's should connect to ground the following pins:

- Power pins VCCH_MPQx and VCCA_MPQx
- Differential Input Pairs MPQx_RXP/N
- Clock reference pins MPQx_REFCLKP/N
- External Reference Resistor Input REXT_MPQx
- Differential output Pairs MPQx_TXP/N, leave open.

***Note:** Available on Avant-G/X only.

3.7. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator is recommended. A typical bypassing circuit is shown in Figure 3.2.

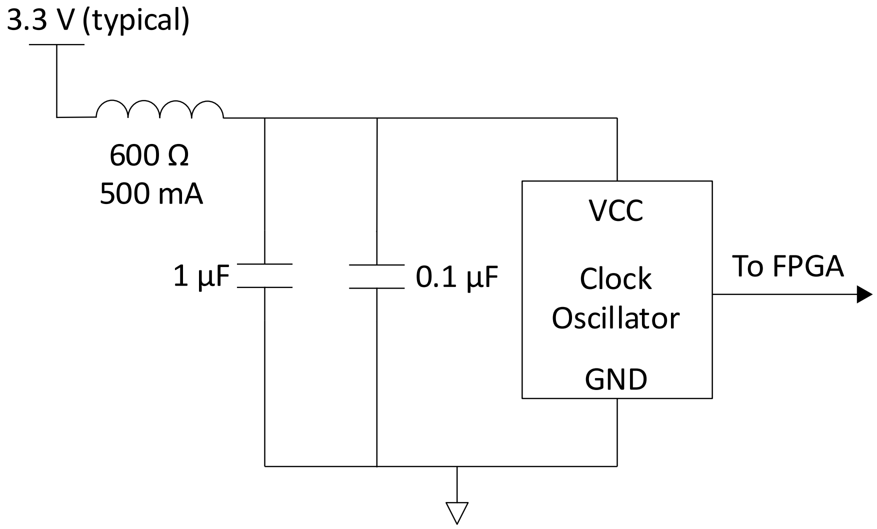


Figure 3.2. Clock Oscillator Bypassing

4. Power

4.1. Power Sequencing

The only power up sequencing required for the Avant device is any V_{CCIO} set to 1.8 V must come up with V_{CCAUX}. This is easily met by using the same power source for both V_{CCIO} set to 1.8 V and V_{CCAUX}.

Note: Power supplies V_{CC}, V_{CCAUX}, V_{CCIO1}, and V_{CCIO2} are monitored by an internal Power-On-Reset (POR) circuit to determine the Avant's internal Power Good condition during power-up.

4.2. Power Estimation

Once the Avant device density, package, and logic implementation are decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant™ design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current, and maximum DC and AC current for the given system environmental conditions.
- The ability for the system environment and Avant device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, the Avant device power requirements can be taken into consideration early in the design phase.

4.3. Ramp Rate

Power supply ramp rate should meet the 0.2 V/ms to 50 V/ms specification and must be monotonic.

5. Component Selection

5.1. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR × CURRENT should be < 0.5% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.01 Ω and 0.10 Ω depending on current load.
- PLL rails draw low current, which allow ferrite beads with ESR ≤ 0.40 Ω.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

5.2. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the clock oscillator supply pins as practically possible. *Good quality* capacitors for bypassing generally meet the following requirements:

5.2.1. Capacitor Dielectric

Use dielectrics such as X5R, X7R, and similar which have good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

5.2.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should target at least 80% higher than the voltage rail (maximum). Example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

5.2.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, the following capacitor sizes are recommended:

Table 5.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

5.2.4. Mounting Location

Keep the 0.1 µF capacitors close the Avant FPGA's associated power rail pins. Selecting 0201 size 0.1 µF capacitors allows them to fit on the opposite side of the PCB from the Avant FPGA between ball pad via holes.

6. Clock Inputs

The Avant device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purpose, you need to pay attention to minimize signal noise on these pins. Refer to Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).

These shared clock input pins can be found under the Dual Function column of the pinlist .csv file.

High-speed differential interfaces (such as MIPI) being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. For banks with V_{CCIO} voltage of 1.5 V and lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC coupled and then DC biased at half the V_{CCIO} voltage. An example of a dual footprint design supporting HCSL and LVDS shown in Figure 6.1.

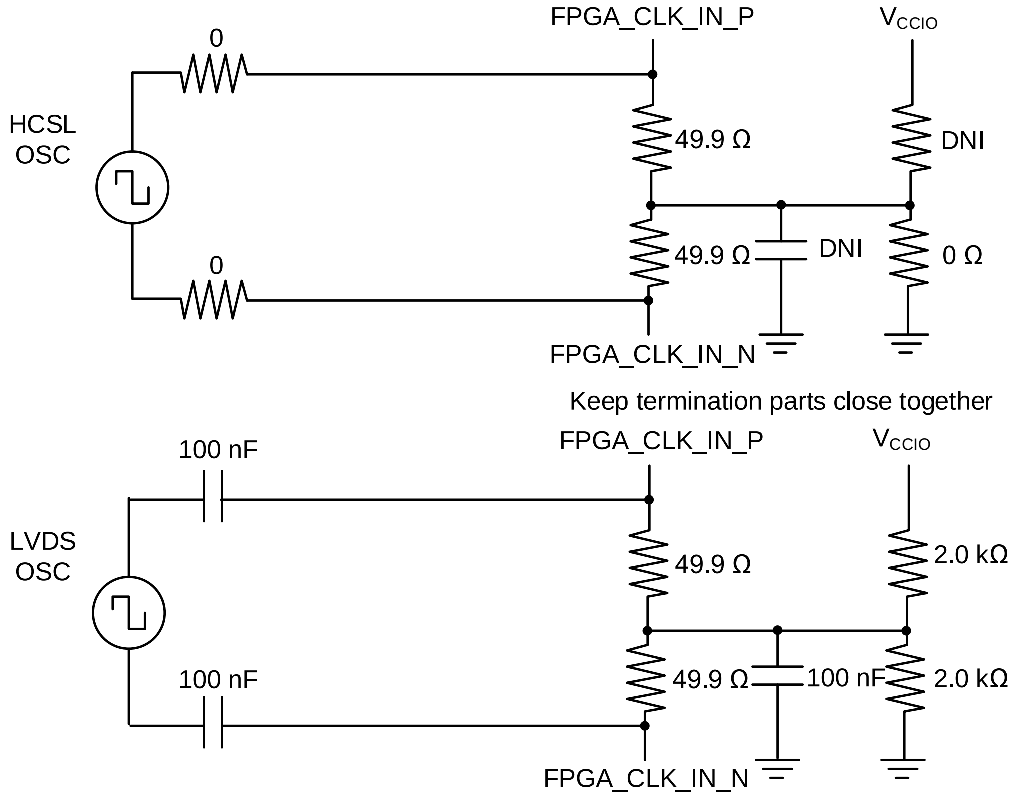


Figure 6.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

7. Configuration Considerations

7.1. JTAG

The Avant device includes provisions to configure the FPGA through the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface that requires PCB considerations, as shown in Table 7.1.

Table 7.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
CFGMODE	2.0 kΩ pull-down to GND to enable JTAG Configuration
TCK	2.2 kΩ pull-down to GND
TMS	10 kΩ pull-up to V_{CCIO2}
TDI	10 kΩ pull-up to V_{CCIO2}
TDO	10 kΩ pull-up to V_{CCIO2}

The JTAG port enables debugging in the final system. Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. For best results, route the VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND signals to a common test header.

7.2. SPI Configuration

The Avant device includes provisions to configure the FPGA through Controller and Target Serial Peripheral Interface (SPI) ports.

The pins listed in Table 7.2 have internal weak pull resistors, pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground. It is recommended to provide external pull resistors as indicated in the table.

Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO2}
INITN	10 kΩ pull-up to V_{CCIO2}
DONE	10 kΩ pull-up to V_{CCIO2}
CFGMODE	10 kΩ pull-up to V_{CCIO2} for MSPI Configuration 2.0 kΩ pull-down to GND for SSPI or JTAG Configuration
MCSN	10 kΩ pull-up to V_{CCIO1}
MCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO1} (Not installed by default) Series resistor placing near TX side[1].
MDQ0/MOSI	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ1/MISO	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ2 - MDQ7	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDS	MSPI Octal Mode Data Strobe, 10 kΩ pull-down to GND (Not installed by default)
SCSN	4.7 kΩ pull-up to V_{CCIO2}
SCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ0/MOSI	10 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ1/MISO	10 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ2 - SDQ7	10 kΩ t pull-up o V_{CCIO2} (Not installed by default)
SDS	SSPI Octal Mode Data Strobe, 10 kΩ pull-down to GND (Not installed by default)

Note:

1. Series resistor value depends on the PCB design. It ranges from 0 Ω (PCB impedance: 50 Ω) to 10 Ω (PCB impedance: 60 Ω).

7.3. Configuration Pins per Programming Mode

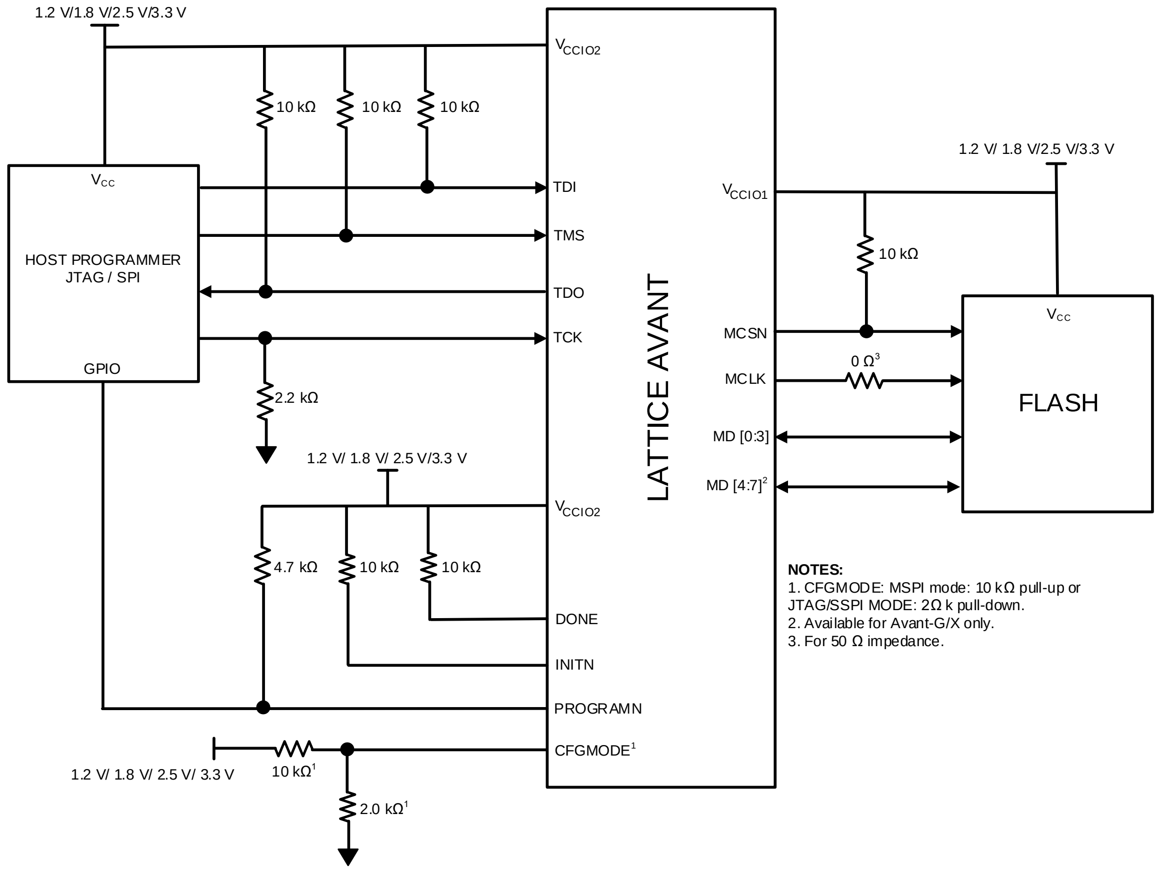
Table 7.3 lists the signal pins required for each configuration-programming mode.

Table 7.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
JTAG[1]	2	CFGMODE pin Low	TCLK	Input	1	TCK, TMS, TDI, TDO
MSPI	1	CFGMODE pin High	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
					8[2]	MCLK, MCSN, MDS, MD0, MD1, MD2, MD3, MD4, MD5, MD6, MD7
SSPI	1	CFGMODE pin Low	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
					8[2]	SCLK, SCSN, SDS, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7

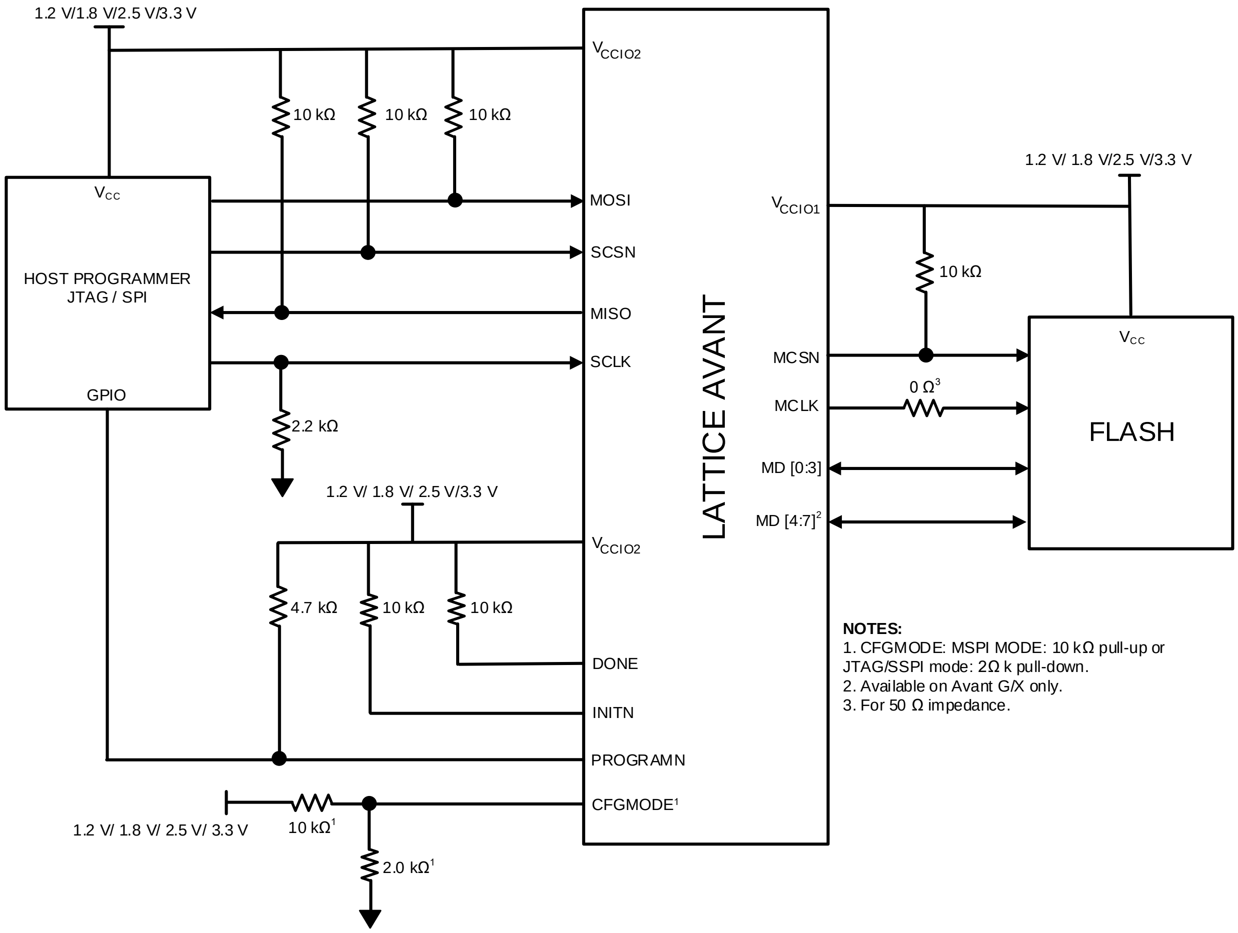
Note:

1. JTAG port takes precedence over SSPI.
2. Available on Avant-G/X only.



NOTES:
1. CFGMODE: MSPI mode: 10 kΩ pull-up or JTAG/SSPI MODE: 2Ω k pull-down.
2. Available for Avant-G/X only.
3. For 50 Ω impedance.

Figure 7.1. Typical Connections for Programming SRAM or External Flash via JTAG



NOTES:
1. CFGMODE: MSPI MODE: 10 kΩ pull-up or JTAG/SSPI mode: 2Ω k pull-down.
2. Available on Avant G/X only.
3. For 50 Ω impedance.

Figure 7.2. Typical Connections for Programming SRAM or External Flash via Target SPI

8. External SPI FLASH

The Flash Voltage should match the V_{CCIO1} voltage.

It is recommended to use SPI flash device that is supported in the Lattice Radiant Programmer. To see the supported list of devices go to the Lattice Radiant Programmer, under the **Help** menu choose **Help**, then search for **SPI Flash support**.

For SPI flash devices that are not listed in the **SPI Flash support**, using the custom flash option may allow a non-supported device to work.

9. I/O Pin Assignments

Crosstalk coupling is reduced in the Avant device packages. The PCB board, however, can cause significant noise injection from adjacent I/O pins and PCB traces running close together in parallel for long distances. For the best jitter performance choose pin assignments that keep noisy I/O pins away from sensitive power rails (ex. PLL & SERDES power pins). Simulate any suspicious traces using a PCB crosstalk/Signal Integrity simulation tool to determine if a particular layout needs to be improved.

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024).

It is common practice for designers to select pinouts for their system early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

9.1. Early I/O Release

The Avant device supports an Early I/O release feature, which allows the I/O to assume user-defined drive states at the beginning of bitstream processing. The Early I/O release feature releases the I/O after processing the I/O configuration which is located near the head of the bitstream data. Once data is programmed in the left/right Memory Interface Block (MIB) the I/O is released to a predefined state. This feature is enabled by setting the EARLY_IO_RELEASE preferences to ON in the Lattice Radiant Device Constraint Editor.

9.2. Series Termination Resistors

When using series termination resistors, locate the resistors close to the transmitting pins.

Configuration pins to external devices (example SPI FLASH) default to 50RS (50 Ω) drive strength. For these pins, start with a value of 0 Ω for PCB impedance of 50 Ω. For higher PCB impedances increase the series termination resistance, for example 10 Ω for PCB impedance of 60 Ω.

Optimum series termination resistance value for user mode output pins depends on PCB etch impedance and selected output drive strength. It is recommended to simulate using IBIS model for starting resistance value. Further, test with Oscilloscope and optimize the series termination resistance of critical signals for best signal integrity.

10. Functional Blocks Rule-Based Pinout Considerations

The Avant family of devices supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as Soft MIPI, clock resource connectivity, and PLL usage. Refer to the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for rules pertaining to these interface types.

10.1. LVDS, MIPI, and Differential Pair Assignments

True LVDS and MIPI signaling inputs and outputs are available on I/O pins on the bottom side of the FPGA device (High Performance banks 3 – 11). Differential input pairing can be found under the High-Speed column in the pin-list .csv file.

The positive signal of a differential pair should connect to an I/O ending in ‘A’ (ex. HPIOx_yA). The negative signal of a differential pair should connect to an I/O ending in ‘B’ (ex. HPIOx_yB).

The Wide Range banks (0, 1, 2, 12, 13, 14) on the top side I/O banks do not support true LVDS and MIPI standard but can support emulated LVDS outputs using external termination resistors. This is described in the Lattice Avant sysI/O User Guide (FPGA-TN-02297).

Bank voltage must be set to 1.8 V to support LVDS.

Bank voltage must be set to 1.2 V to support MIPI.

10.2. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards that require an external reference voltage. HSUL and SSTL are supported on the device bottom banks only (High Performance banks 3 – 11). The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

10.3. LVSTL I and LVSTL II Pin Assignments

The LVSTL I and LVSTL II interface requires external reference resistor. LVSTL I and LVSTL II are supported on the device bottom banks only (High Performance banks 3 – 11). These pins can be found in the dual function column with RES_EXT label. Each bank includes a separate RES_EXT voltage.

Go to EXT_RES pins subsection for the values and implementations.

For the pinout and grouping requirements of the memory mapped interface, see the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for more information.

10.4. SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly length matched differential routing with no more than ±4 mil (±0.1 mm) length mismatch. Route with few discontinuities (that is., vias).

Refer to the High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance.

11. Layout Recommendations

A good design from schematic should also reflect with a good layout for the system design to work without any issues on noise and power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes, this is to ensure good power delivery and thermal stability.
2. Each Power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. Placement of analog circuits must be away from digital circuits or high switching components.
4. High speed signals should have a clearance of 5 times trace width from other signals.
5. High speed signals that transition from one layer to another should have a corresponding transition ground via if both reference planes are ground. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

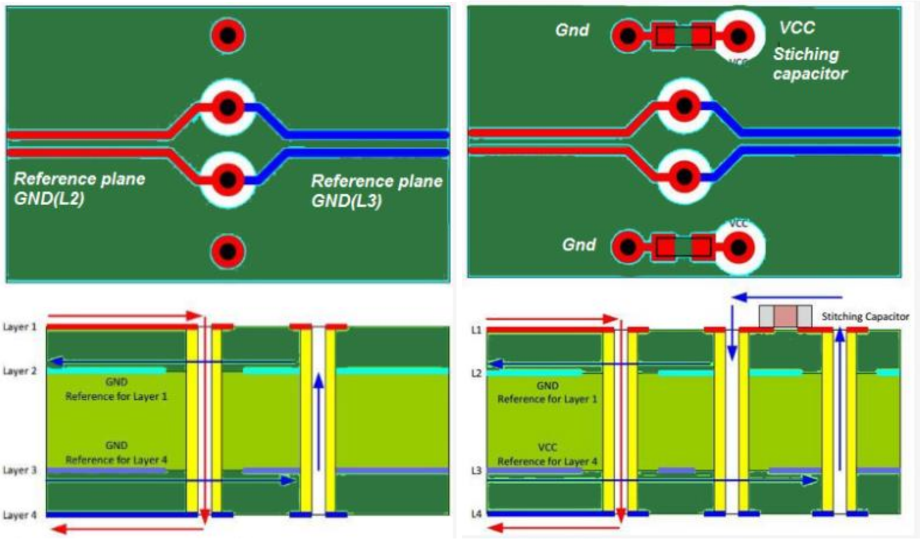


Figure 11.1 Recommended Layout

6. High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.
7. For differential pairs, be sure to match the length as close as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

12. Simulation and Board Measurement of Critical Signals

To ensure a design is reliable and will have high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

12.1. Critical Signals

Signals sensitive to Signal Integrity (SI) degradation are considered critical signal which require extra design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like.)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

12.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often have reoccurring subscription pricing. The expensive tools can import board design files and can easily supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (ex. Micro-cap) can supply useful basic simulations, but take extra effort to setup SI effects for multiple signals with different transmission line lengths, lossy transmission lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

12.3. Board Measurements

Critical signals should be measured on the actual PCB assembly using an oscilloscope. Verify proper signaling function and signal integrity (that is, eye diagram, SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (ex. output series termination resistor value).
- Adjust setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI)

13. SSO (Simultaneous Switching Output) Design Check

Users should verify designs that will not have functional failures due to SSO voltage drops (sometimes call SSO Noise, Ground Bounce, or Power Bounce).

SSO voltage drops are caused by package inductance combined with dynamic switching current causing Ldi/dt voltage drops.

The Lattice SSO Tool should be used to provide SSO voltage drop estimates.

13.1. SSO Failures – Each of the following can lead to SSO failures

1. Many simultaneous switching outputs in the same I/O bank.
   The more simultaneous switching outputs in a bank the greater the 'di' current, and thus greater Ldi/dt voltage drops.
2. I/O slew rates set to FAST (and sometimes MEDIUM).
   Faster slew rates reduce the 'dt' time, and thus increase the Ldi/dt voltage drops.
3. I/O output current set high (ex. 8 mA – 16 mA).
   The greater the I/O output current the greater the 'di' current, and thus greater Ldi/dt voltage drops.
4. I/O capacitive loading is relatively high (especially > 15 pF)
   High capacitance loading increases the 'di' current, and thus increases Ldi/dt voltage drops.
5. I/O Banks with low voltage rails (ex. LVCMOS 1.0 V – LVCMOS 1.5 V) have small voltage margins and are more susceptible to Ldi/dt ground and power violations.

13.2. SSO Mitigations

1. Split up simultaneous switching outputs into multiple banks (where timing permits.)
   The fewer simultaneous switching outputs in a bank the lower the 'di' current, and thus lower Ldi/dt voltage drops.
2. Reduce I/O slew rates to MEDIUM or even better SLOW if timing allows.
   The increase in slew time increases ‘dt’ and thus reduces Ldi/dt voltage drops.
3. Reduce I/Os output current (ex. 4 mA), where timing and signal quality permit.
   Reducing the I/O output current reduces 'di' current, and thus reduces Ldi/dt voltage drops.
4. Reduce I/Os capacitive loading (this usually requires PCB design changes).
   Reducing capacitive loading reduces 'di' current, and thus reduces Ldi/dt voltage drops.
5. Increase I/O Bank voltage rails (this often requires PCB design changes). When above mitigations do not provide enough design margin, then increasing I/O Bank voltage can increase absolute voltage margins and provide enough design margin for reliable operation.

14. Checklist

Table 14.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	System Supplies		
1.1.1	Voltage rails have ±3% tolerance. Use voltage regulator ≤ ±2% tolerance to allow for ±1% power noise.		
1.1.2	Follow Table 3.1 for proper decoupling of each power rail.		
1.1.3	V_{CC} and V_{CCA_PLLx} at 0.82 V ±3%.		
1.1.4	V_{CCJB} at 0.82 V ±3% to enable JTAG Boundary Scan functions. V_{CCJB} Connected to ground to save static power if/when JTAG Boundary Scan functions not needed.		
1.1.5	Use a PCB plane for V_{CC} core with proper decoupling.		
1.1.6	V_{CC} core sized to meet power requirement calculation from software.		
1.1.7	V_{CCCLK}, V_{CCHP}, V_{CCA_PLLx} Must be quiet and isolated from other switching noises and each other.		
1.1.8	V_{CCAUX} and V_{CCAUXA} at 1.8 V ±3%.		
1.1.9	V_{CCAUX} and V_{CCAUXA} Must be quiet and isolated from other switching noises and each other.		
1.1.10	V_{CCAUX} pins should be ganged together, and a solid PCB plane is recommended.		
1.1.11	V_{CCAUXA} pins are sensitive and should be filtered separately from V_{CCAUX} pins.		
1.1.12	V_{CC_BAT} pin at 1.5 V +3%/-33% if used, if not used leave pin open.		
1.2	I/O Supplies		
1.2.1	All Wide Range V_{CCIO} (Banks 0, 1, 2, 12, 13, and 14) V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V.		
1.2.2	All High Performance (Banks 3 – 11) V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.		
1.2.3	Any V_{CCIO} set to 1.8 V must come up with V_{CCAUX}. This is easily met by using the same power source for both V_{CCIO} set to 1.8 V and V_{CCAUX}.		
1.2.4	V_{CCH_MPQx} pins must be quiet and isolated from other switching noises.		
1.3	SERDES Power Supplies		
1.3.1	V_{CCA_MPQx} pins at 0.80 V For data rate ≤ 16 Gbps; 0.90 V For data rate > 16 Gbps.		
1.3.2	$_{VCCA\_MPQx}$ pins must be quiet and isolated from other switching noises.		
1.3.3	V_{CCH_MPQx} pins at 1.50 V For data rate ≤ 16Gbps; 1.8 V For data rate > 16Gbps.		
1.4	Grounds		
1.4.1	All ground pins must be connected to low impedance dedicated ground plane.		
1.5	Unused Blocks		
1.5.1	Connect unused V_{CCIOx} pins to a power rail. Do not leave them open. Recommend bypassing unused rail pin with a 100 nF.		
1.5.2	Connect unused Quad's V_{CCH_MPQx} and V_{CCA_MPQx} pins to ground. Also tie reference pins $M_{PQx\_REFCLKP}$ and $M_{PQx\_REFCLKN}$ to ground.		
1.6	Power Sequencing		
1.6.1	The only power up sequencing required for the Avant device is any V_{CCIO} set to 1.8 V must come up with V_{CCAUX}. This is easily met by using the same power source for both V_{CCIO} set to 1.8 V and V_{CCAUX}.		
2	**JTAG**		
2.1	CFGMODE pin pulled high 10 kΩ or low using 2.0 kΩ per Table 7.1.		
2.2	Keep CFGMODE accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development.		
2.3.1	JTAG Header: VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND.		
2.4	Pull-down on TCK per Table 7.1.		
2.5	Pull-up on TMS, TDI, and TDO per Table 7.1.		

	Item	OK	NA
3	**MSPI and SSPI Configuration**		
3.1	V_{CCIO1}, V_{CCIO2} bank voltage matches sysCONFIG peripheral devices (SPI Flash, External connections).		
3.2	CFGMODE pin 10 kΩ pull-up to VCCIO2 for MSPI Configuration. CFGMODE pin 2.0 kΩ pull-down to GND for SSPI Configuration.		
3.3	Pull-ups or pull-downs on persisted configuration specific pins per Table 7.1 and Table 7.2		
4	**External Flash**		
4.1	Flash voltage should match V_{CCIO1} voltage.		
5	**Special Pin Assignments**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	Bank Voltage		
5.3.1	Bank voltage must be set to 1.8 V to support LVDS.		
5.3.2	Bank voltage must be set to 1.2 V to support MIPI.		
5.4	Referenced I/O standards.		
5.4.1	HSUL and SSTL are supported on the device bottom banks only (High Performance banks 3 – 11).		
5.4.2	Decouple the VREF pin using a 0.1 µF capacitor.		
5.5	Termination Impedance Rext Resistor.		
5.5.1	LVSTL I require a 240 Ω ±1% resistor from Rext to VCCIOx for proper termination impedances.		
5.5.2	LVSTL II requires a 180 Ω ±1% resistor from Rext to VCCIOx for proper termination impedances.		
5.5.3	For POD or SSTL I/O standards connect a 240 Ω resistor from Rext to Ground.		
5.5.4	For non-memory I/O standards leave open.		
6	**Clock Inputs**		
6.1	High-speed differential interfaces (such as MIPI) being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (–complement).		
6.2	When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage.		
6.3	For banks with VCCIO voltage of 1.5 V and lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's VCCIO. An LVDS oscillator can also be used if AC coupled and then DC biased at half the VCCIO voltage. See Figure 6.1.		
7	**MIPI Interface Requirements**		
7.1	Soft MIPI supported on bottom banks 3 – 11.		
7.2	V_{CCIOX} set to 1.2 V.		
7.3	Target 100 Ω impedance.		
7.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source.		
7.5	Design differential pairs 'loosely coupled' with separation between positive and negative of a pair of at least twice the etch width (intra-pair spacing).		
7.6	Provide separation from each differential pair of at least six times the etch width (inter-pair spacing).		
7.7	Length match clock and data lane pair traces within 0.1 mm. (Both intra-pair and inter-pair etches.).		
7.8	RX at FPGA should have clock differential pair routed to clock pins labelled PCLKTx_y (+true) and PCLKCx_y (–complement).		
8	**LVDS Interface Requirements**		
8.1	LVDS supported on bottom banks 3 – 11.		
8.2	V_{CCIOX} set to 1.8 V.		
8.3	Target 100 Ω impedance.		
8.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source.		

	Item	OK	NA
8.5	Design differential pairs 'loosely coupled' with separation between positive and negative of a pair of at least twice the etch width (intra-pair spacing).		
8.6	Provide separation from each differential pair of at least six times the etch width (inter-pair spacing).		
8.7	Length match clock and data lane pair traces within 0.1 mm. (Both intra-pair and inter-pair etches.)		
8.8	RX at FPGA should have clock differential pair routed to clock pins labelled PCLKTx_y (+true) and PCLKCx_y (–complement).		
9	**LPDDR4 and DDR Interface Requirements**		
9.1	LPDDR4 and DDR supported on bottom banks 3 – 11.		
9.2	V_{CCIOX} set to 1.1 V (LPDDR4) or 1.2V (DDR4).		
9.3	Target 100 Ω impedance for differential pair signal.		
9.4	Design differential pairs 'loosely coupled' with separation between positive and negative of a pair of at least twice the etch width.		
9.5	Data group		
9.5.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
9.5.2	Each Data group has specific DQS pins and groupings that can be checked in Pinlist.csv under DQS column.		
9.5.3	All data groups must reference a ground plane within the stack-up.		
9.5.4	Maintain trace length matching to a maximum of ±4 mil (±0.1 mm) between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
9.5.5	Differential pair of DQS to DQS_N trace lengths should be matched to a maximum of ±4 mil (±0.1 mm).		
9.5.6	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±4 mil (±0.1 mm).		
9.5.7	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
9.5.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
9.6	Control group		
9.6.1	CKE, CS, ODT, RESET signals should be routed in a group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
9.6.2	Control group must be referenced to a ground plane within the stack-up.		
9.6.3	Maintain trace length matching to a maximum of ±4 mil (±0.1 mm) between the control group. Use careful serpentine routing to meet this requirement.		
9.7	Address and Command Group		
9.7.1	Address, WE, RAS, CAS, ACT signals should be routed in a group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
9.7.2	Address and Command group must be referenced to a ground plane within the stack-up.		
9.7.3	Maintain trace length matching to a maximum of ±4 mil (±0.1 mm) between the Address and Command group. Use careful serpentine routing to meet this requirement.		
9.7.4	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		
9.7.5	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
9.8	Clock		
9.8.1	Clock signal must be referenced to a ground plane within the stack-up.		
9.8.2	CK to CK_N trace lengths must be matched to within ±4 mil (±0.1 mm).		
9.8.3	Clock signal should match with Data group and Address & Command Group within ±4 mil (±0.1 mm).		

	Item	OK	NA
9.9	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
9.10	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
9.11	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
10	**SERDES (Avant-G/X only)**		
10.2	Use continuous ground reference plane to serial channels.		
10.3	Match differential pair trace lengths to within ±4 mil (±0.1 mm).		
10.4	Maintain good high-speed transmission line routing with at least 10X the spacing to reference plane to other signals.		
10.5	Do not pass other signals on the PCB above or below the high-speed SERDES without isolation.		
10.6	Dedicated reference clock input from clock source meets the DC and AC requirements.		
10.7	Ref clock termination resistors may be needed for compatible signaling levels. See Figure 6.1.		
10.8	External AC coupling caps may be required for compatibility to common-mode levels.		
11	**Layout Notes**		
11.1	Selecting 0201 size 0.1 µF capacitors allows them to fit on the opposite side of the PCB from the Avant FPGA between ball pad via holes.		
11.2	When using series termination resistors locate the resistors close to the transmitting pin. Configuration pins to external devices (example SPI FLASH) default to 50RS (50 Ω) drive strength. For these, pins start with a value of 0 Ω for PCB impedance of 50 Ω. For higher PCB impedances increase the series termination resistance, example: 10 Ω for PCB impedance of 60 Ω. Optimum series termination resistance value for user mode output pins depends on PCB etch impedance and selected output drive strength. It is recommended to simulate using IBIS model for starting resistance value. Further, test with Oscilloscope and optimize the series termination resistance of critical signals for best signal integrity.		
11.3	Length matching a differential pair's positive and negative traces within ±4 mil (±0.1 mm) of each other will prevent signal integrity degradation up to 25 Gbps.		
12	**Simulation and Board Measurement of Critical Signals**		
12.1	Simulations: Use IBIS model to simulate critical signals for proper signal integrity.		
12.1.1	Simulate Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like).		
12.1.2	Simulate Clock nets (Oscillator Inputs, Output Clocks).		
12.1.3	Simulate Data nets with embedded clocks.		
12.1.4	Simulate Interrupts (Edge Triggered).		
12.1.5	Simulate Logic signals travelling long distances requiring termination.		
12.1.6	Simulation results should be used to optimize each critical signal for best signal integrity: • Define output pin drive strength. • Define output pin slew rate. • Define output pin termination design (ex. output series termination resistor value). • Define setting of internal pin pull-up and pull-down resistors. Improve PCB layout.		
12.2	Board Measurements: Use Oscilloscope to measure on PCB assembly critical signals for proper function and signal integrity.		
12.2.1	Measure Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like).		
12.2.2	Measure Clock nets (Oscillator Inputs, Output Clocks).		
12.2.3	Measure Data nets with embedded clocks.		
12.2.4	Measure Interrupts (Edge Triggered).		
12.2.5	Measure Logic signals travelling long distances requiring termination.		

	Item	OK	NA
12.2.6	Measurement results should be used to optimize each critical signal for best signal integrity: • Adjust output pin drive strength. • Adjust output pin slew rate. • Adjust output pin termination design (ex. output series termination resistor value). • Adjust setting of internal pin pull-up and pull-down resistors.		
12.3	Specification compliance testing is recommended for popular signalling methods (ex. USB, MIPI).		
13	**SSO (Simultaneous Switching Output)**		
13.1	When a bank has many outputs that switch all at the same time there can be generated internal SSO noise which if too large can cause unreliable operation. It is recommended that user verify their designs using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
13.2	Designers should verify their designs using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
13.3	Reducing SSO Noise		
13.4	Have less I/O in a bank switch at the same time. (Stagger output switching into smaller groups).		
13.5	Reduce output current drive on the switching I/O (ex. configure for 4 mA instead of 8 mA).		
13.6	Split up a large group of I/O across multiple banks instead of all in the same bank.		
13.7	Add virtual ground pins to the bank. Connect an I/O to ground on the PCB and program the I/O to output a low at maximum output current.		
13.8	Add virtual VCCIO pins to the bank. Connect an I/O to the bank's VCCIO rail on the PCB and program the I/O to output a high at maximum output current.		
13.9	When a bank has many outputs that switch all at the same time there can be generated internal SSO noise which if too large can cause unreliable operation. It is recommended that user verify their designs using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
13.10	Designers should verify their designs using the Lattice Simultaneous Switching Output (SSO) calculator tool.		

References

- Avant-E web page
- Avant-G web page
- Avant-X web page

A variety of technical notes for the Lattice Avant platform are available.

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant Hardware Checklist (FPGA-TN-02317)
- Lattice High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107)
- Lattice Avant Platform - Specifications Data Sheet (FPGA-DS-02112)
- Lattice Avant Power User Guide (FPGA-TN-02291)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)
- IP Cores and Reference Designs for Avant Devices
- Kits, Boards, and Demonstrations for Avant Devices

Other references:

- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, December 2024

Section	Change Summary
Power Supply Filtering	Reworked EXT_RES pins section.

Revision 0.82, November 2024

Section	Change Summary
All	• Minor editorial fixes. • Changed *Master* to *Controller*. • Changed *Slave* to *Target*.
Inclusive Language	Added this section.
Abbreviations in This Document	Replaced *Acronyms* with *Abbreviations*.
Power Supplies	Removed VCCCLK and VCCHP in Table 2.1. Supply Rails.

Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  • Removed VCCCLK and VCCHP.
	  • VCCAUX, VCCAUXA, and VCCIOX – added a recommended filter for 841 fcCSP package.
	  • VCCIOX – added the statement, *check SSO noise level using Lattice SSO tool* under the Notes column.
	• Added Figure 3.1. Recommended Power Filter.
	• Added EXT_RES pins subsection.
	• Added Unused GPIO Pins subsection.
	• Added the bullet, *Differential output Pairs MPQx_TXP/N, leave open* under the Unused SERDES Quads subsection.

Power	Added Ramp Rate subsection.

Configuration Considerations	• Changed the pull-down resistor of CFGMODE from *10 kΩ* to *2 kΩ* in Table 7.1. JTAG Pin Recommendations.
	• Replaced the statement, *For best results, route the TCK, TMS, TDI, TDO, and CFGMODE signals to a common test header along with VCCIO2 and ground. Adding signals PROGRAMN and DONE increase debug usability,* with *For best results, route the VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND signals to a common test header,* under the JTAG subsection.
	• Updated Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins.
	  • Changed the pull-down resistor of CFGMODE from *10 kΩ* to *2 kΩ*.
	  • Changed the pull-up resistor of MCSN from 4.7 *kΩ* to 10 *kΩ*.
	  • MCLK - added a series resistor placing near the TX side.
	  • SCSN – replaced VCCIO1 with VCCIO2.
	  • Added table note 1 - Series resistor value depends on the PCB design, range from 0 Ω for PCB impedance of 50 Ω to 10 Ω for PCB impedance of 60 Ω.
	• Added table note 2 – Available in Avant-G/X only in Table 7.3. Configuration Pins Needed per Programming Mode.
	• Added Figure 7.1. Typical Connections for Programming SRAM or External Flash via JTAG and Figure 7.2. Typical Connections for Programming SRAM or External Flash via Target SPI.

External SPI Flash	Added this section.
I/O Pin Assignments	• Reworked the Series Termination Resistors subsection. • Removed the Simultaneous Switching Outputs (SSO) Noise subsection.
Functional Block Rule-Based Pinout Considerations	Reworked the LVSTL 1 and LVSTL II Pin Assignments subsection.
Layout Recommendations	Added this section.

Section	Change Summary
Simulation and Board Measurement of Critical Signals	Added this section.
SSO (Simultaneous Switching Output) Design Check	Added this section.
Checklist	Reworked this section.

Revision 0.81, November 2023

Section	Change Summary
Disclaimers	Updated this section.
Power Supplies	Added new supply rail V_{CCJB} and its Voltage and Description information in Table 2.1. Supply Rails.
Power Supply Filtering	• Added power input V_{CCJB} and its Recommended Filter and Notes information in Table 3.1. Recommended Power Filtering Groups and Components. • Added ground pins *(VSS and VSSR)* in Ground Pins section. • Updated Unused SERDES Quads* (V_{CCH_MPQx} and V_{CCA_MPQx}) section.
Clock Inputs	Updated Figure 6.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators.
Checklist	Added new FPGA power supply *V_{CCJB} @ 0.82 V ±3% to enable JTAG Boundary Scan functions. V_{CCJB} Connected to ground to save static power if/when JTAG Boundary Scan functions not needed.* in Table 14.1. Hardware Checklist.
References	Added this section.

Revision 0.80.1, May 2023

Section	Change Summary
All	Minor adjustments in formatting across the document.
Power Supplies	• Changed numbering from Section 1.1 to Section 2. • Updated Table 2.1. Supply Rails. • Added Power Noise section and updated Power Source section.
Power Supply Filtering	Updated Table 3.1. Recommended Power Filtering Groups and Components.
Clock Inputs	• Changed numbering from Section 3 to Section 6. • Deleted Figure 6.1.
Configuration Considerations	Changed numbering from Section 4 to Section 7.
I/O Pin Assignments	• Changed numbering from Section 5 to Section 8. • Added Simultaneous Switching Outputs (SSO) Noise section.
Functional Blocks Rule-Based Pinout Considerations	• Updated the title of LVDS, MIPI, and Differential Pair Assignments section from LVDS and MIPI Assignments. • Added sentence The positive signal of a differential pair should connect to an I/O ending in 'A' (ex. HPIOx_yA). The negative signal of a differential pair should connect to an I/O ending in 'B' (ex. HPIOx_yB) in LVDS, MIPI, and Differential Pair Assignments. • Added LVSTL I, LVSTL II, and Other I/O Standards Termination Impedance Rext Resistor section.
Checklist	Updated Table 10.1. Hardware Checklist.

Revision 0.80, December 2022

Section	Change Summary
All	Preliminary release.

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