



Lattice Avant sysI/O User Guide

Preliminary Technical Note

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ# 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
DDR	Double Data Rate
ESD	Electrostatic Discharge
HDL	Hardware Description Language
HPIO	High-Performance Input/Output
HSUL	High-Speed Unterminated Logic
I3C	MIPI Improved Inter-Integrated Circuit
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
ODT	On-Die Termination
PIO	Programmable Input/Output
POD	Pseudo Open Drain
PVT	Process Voltage Temperature
SLVS	Scalable Low-Voltage Signaling
SSO	Simultaneous Switching Output
SSTL	Stub Series Terminated Logic
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
WRIO	Wide Range Input/Output

1. Introduction

The sysI/O™ buffers in the Lattice Avant™ FPGAs are designed to support a wide range of interfaces. Two types of I/O are offered, wide range (WR) I/O on the top and high performance (HP) I/O on the bottom. These give the ability to easily interface with other devices using advanced system I/O standards. This technical note describes the sysI/O standards available and how to implement them using Lattice Radiant™ design software. For detailed information about supported sysI/O standards, refer to [Lattice Avant Platform – Overview Data Sheet \(FPGA-DS-02107\)](#).

2. sysI/O Overview

The key features of the sysI/O block are:

- Wide range I/O (WRIO) bank supports single-ended standards only. High-performance I/O (HPIO) banks support both differential standards and single-ended standards.
- WRIO bank located on the Top of the device operates with VCCIO of 3.3 V down to 1.2 V.
HPIO bank located on the Bottom side operates with VCCIO of 1.8 V down to 0.9 V.
- WRIO bank support pull-up (weak), pull-down (weak) and bus-keeper mode, HPIO bank support pull-up (weak), pull-down (weak), bus-keeper, I3C pull-up, and Failsafe (LVDS Receiver only) mode.
- Bottom HPIO banks support on-chip programmable differential input 100 Ω termination. Single-end termination with a programmable resistor is supported in all banks.
- Always-On inputs Hysteresis on LVCMOS.
- All banks support runt pulse glitch filter.
- Programmable Slew Rate on all outputs.
- Programmable Open Drain on all outputs.
- ESD protection diodes on all GPIO in all banks.
- Support xSPI Interface, for both configuration and user mode on WRIO's.
- HPIO bank support programmable Thevenin input dynamically On-die Termination (ODT) (30/34/40/48/60/80/120/240 Ω) this is available on every input pin. ODT can be connected to VCCIO, VSSIO, or parallel.
- Per I/O Support configuration earlier than bitstream configuration both on WRIO's and HPIO's, the I/O buffer and IOLOGIC are configured by LMMI registers.

3. sysI/O Banking Scheme

LAV-AT-E/G/X70 devices have fifteen banks, LAV-AT-E/G/X50 devices have thirteen banks, and LAV-AT-E/G/X30 devices have eleven banks.

Top side banks are WR I/O supporting V_{CCIO} up to 3.3 V. There is a total of 52 I/O distributed into three WR I/O banks. LAV-AT-E/G/X70, LAV-AT-E/G/X50, and LAV-AT-E/G/X30 devices have another three WR I/O banks, amounting to a total of six WR I/O banks (104 I/O).

Bottom side banks are high-performance (HP) I/O supporting V_{CCIO} up to 1.8 V, each HP bank has 52 I/O. In addition, high-performance banks support internal trainable VREF signal (VREF_INT) and external VREF (VREF_EXT). External VREF enters the bank through the configurable I/O.

Figure 3.1 shows the location of each bank of the LAV-AT-E/G/X30 device, six banks on the top side and five banks on the bottom side. Figure 3.2 shows the location of each bank of the LAV-AT-E/G/X50 device, six banks on the top side and seven banks on the bottom side. Figure 3.3 shows the location of each bank of the LAV-AT-E/G/X70 device, with six banks on the top side and nine banks on the bottom side.

Note: SerDes is supported in Avant-AT-G/X families.

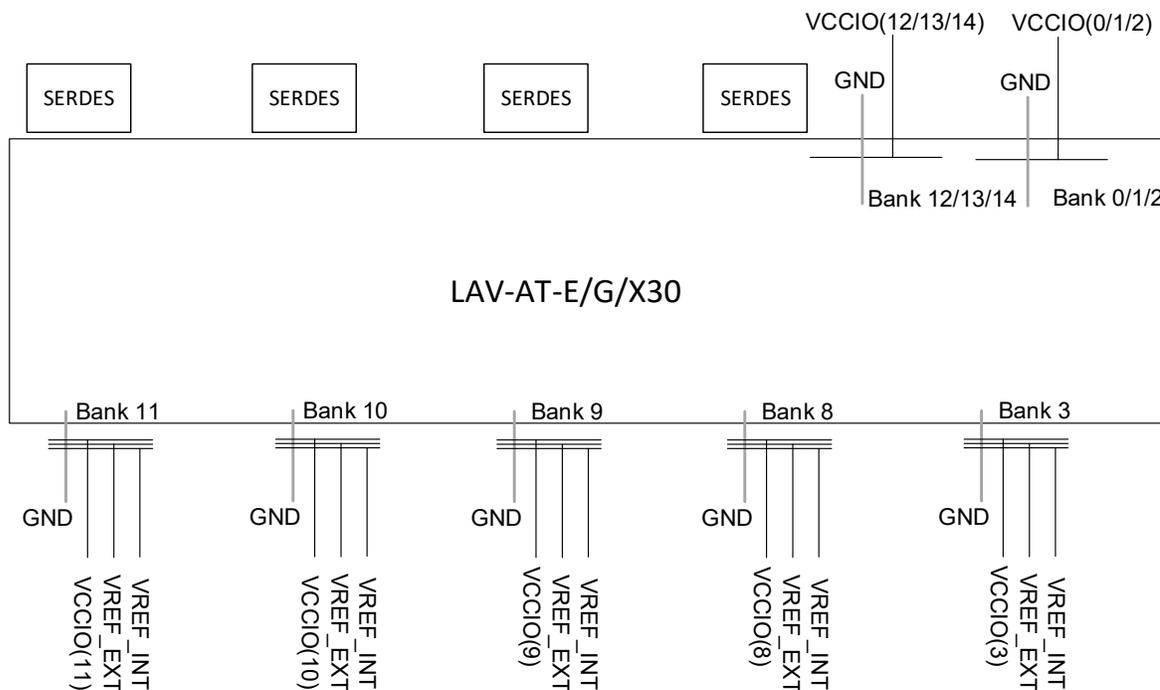


Figure 3.1. LAV-AT-E/G/X30 sysI/O Banking

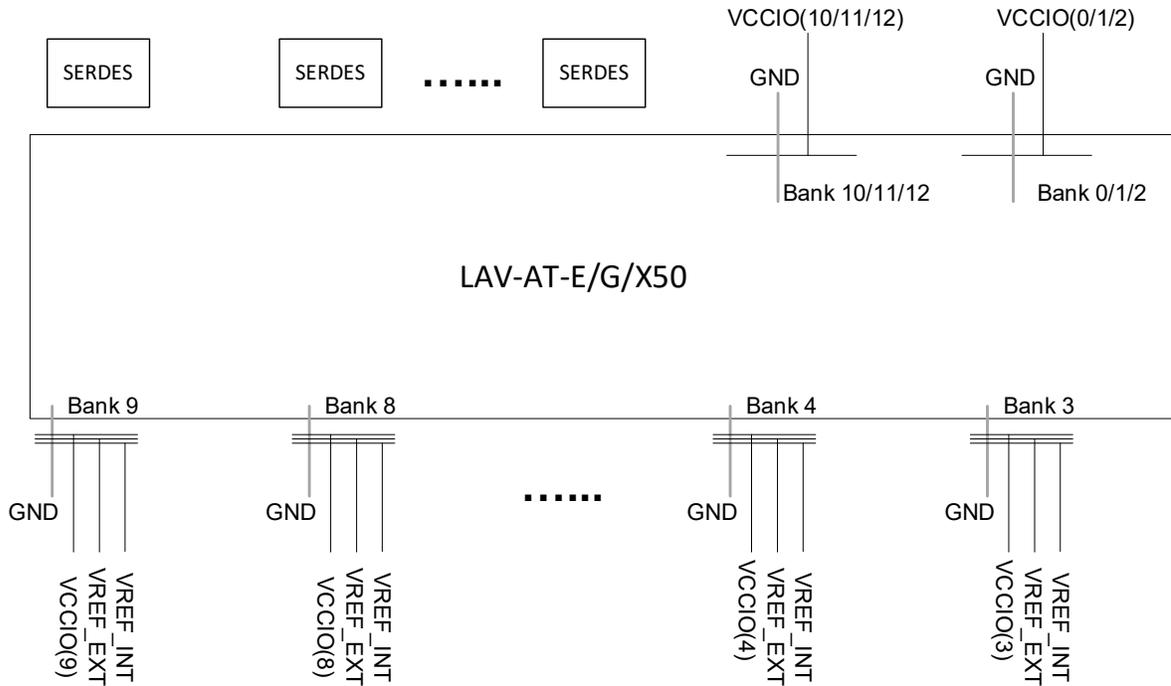


Figure 3.2. LAV-AT-E/G/X50 sysI/O Banking

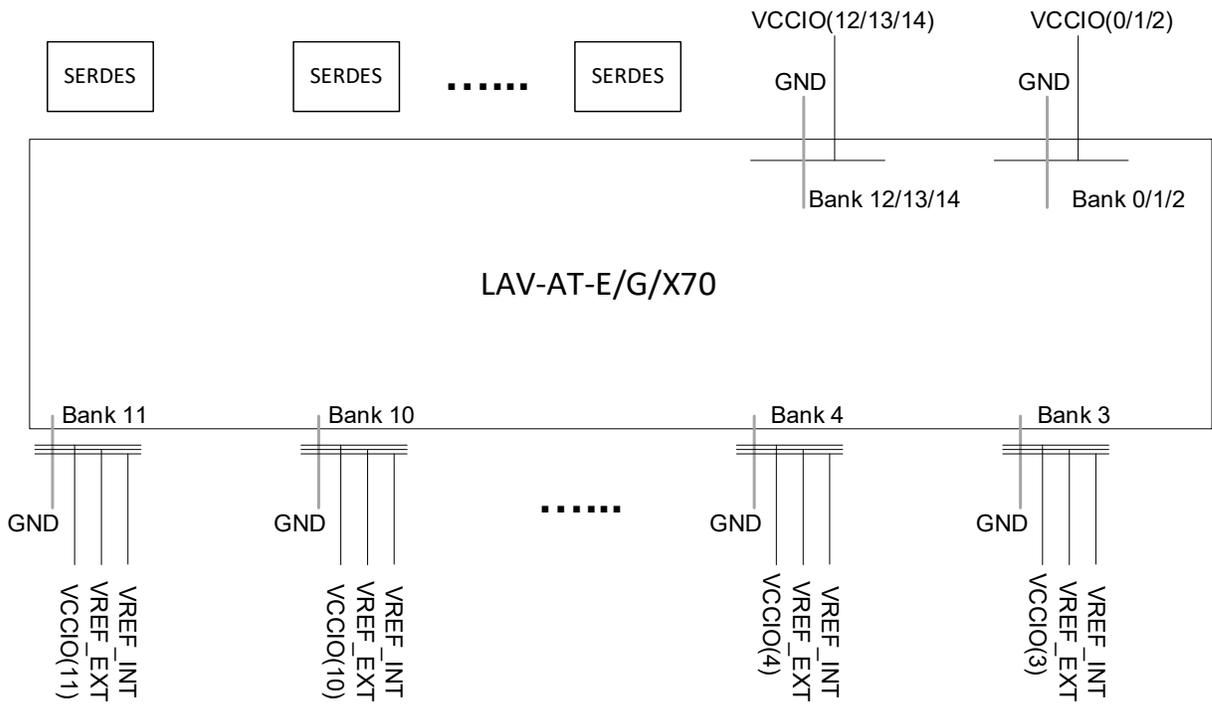


Figure 3.3. LAV-AT-E/G/X70 sysI/O Banking

3.1. VCC (0.82 V)

This is the core supply. This V_{CC} supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.

3.2. VCCIO Wide Range (1.2 V/1.8 V/2.5 V/3.3 V)

Top side banks have a V_{CCIO} supply that operates from 3.3 V down to 1.2 V.

3.3. VCCIO High Performance (0.9 V/1.0 V/1.1 V/1.2 V/1.35 V/1.8 V)

Bottom side banks operate with V_{CCIO} of 1.8 V down to 0.9 V. Standards such as LVDS, SSTL, HSUL, LVSTL, POD, and SLVS are only supported on these banks.

3.4. VCCAUX (1.8 V)

In addition to the bank V_{CCIO} supplies and a V_{CC} core logic supply, Avant devices have a VCCAUX auxiliary supply that powers the differential and referenced input buffers.

3.5. Standby

Using Standby mode dynamically powers down the bank. It disables the differential/reference receiver, true differential driver, current mirrors, and bias circuits.

In Standby mode, differential drivers and differential input buffers can be powered down to save power. Standby mode is enabled on a bank-by-bank basis. Each bank has user-routed input signals to enable Standby (dynamic power-down) mode.

3.6. High-Performance sysI/O Buffer Pairs (On Bottom Side)

The I/O pair consists of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The PAD A referenced input buffer can also be configured as a differential input. Each I/O has a weak pull-up, pull-down, or bus-keeper feature. These are disabled in output mode. The two pads in the pair are referred to as True and Comp, where the True pad is associated with the positive side of the differential I/O and the Comp or complement pad is associated with the negative side.

Programmable Thevenin input termination (30/34/40/48/60/80/120/240 Ω) is available on every input pin dynamically. In case of open drain, the termination can be parallel and connected to VCCIO or VSSIO. This type of termination is called Open Drain Termination (ODT).

Every pair also has a programmable 100 Ω differential input termination resistor. Every pair also has a true LVDS and SLVS200 TX driver. They have an independent tri-state capability.

The single-ended driver associated with the complementary pad can be optionally driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a DIFF I/O pair.

When this option is selected, the tri-state control for the driver associated with the complementary pad is driven by the same signal as the tri-state control for the driver associated with the true pad.

Refer to the High-Performance sysI/O block diagram in [Figure 3.4](#).

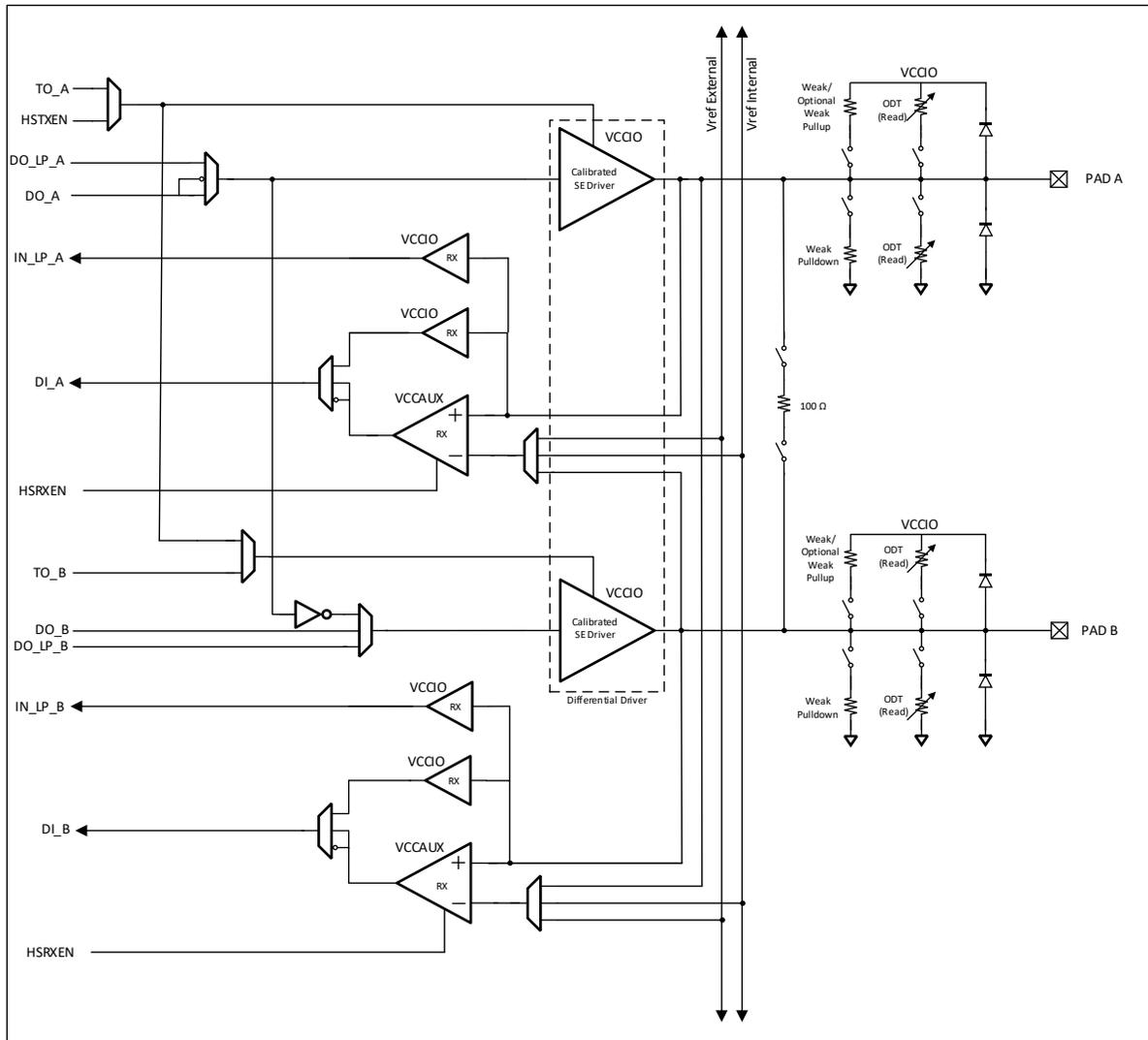


Figure 3.4. High-Performance sysI/O Buffer Pair for Bottom Side

3.7. Wide Range sysI/O Buffer Pair (On Top Sides)

The I/O pair consists of two single-ended output drivers and two sets of single-ended input buffers (ratioed only). Each I/O has a weak pull-up, pull-down, bus-keeper feature. These are disabled in output mode. The two pads in the pair are referred to as True and Comp, where the True pad is associated with the positive side of the Complementary I/O, and the Comp or complement pad is associated with the negative.

The single-ended driver associated with the complementary pad can be optionally driven by the complement of the data that drives the single-ended driver associated with the True pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a Complementary I/O pair. When this option is selected, the tri-state control for the driver associated with the complement pad is driven by the same signal as the tri-state control for the driver associated with the true pad.

Figure 3.5 shows the Wide Range I/O pair block diagram.

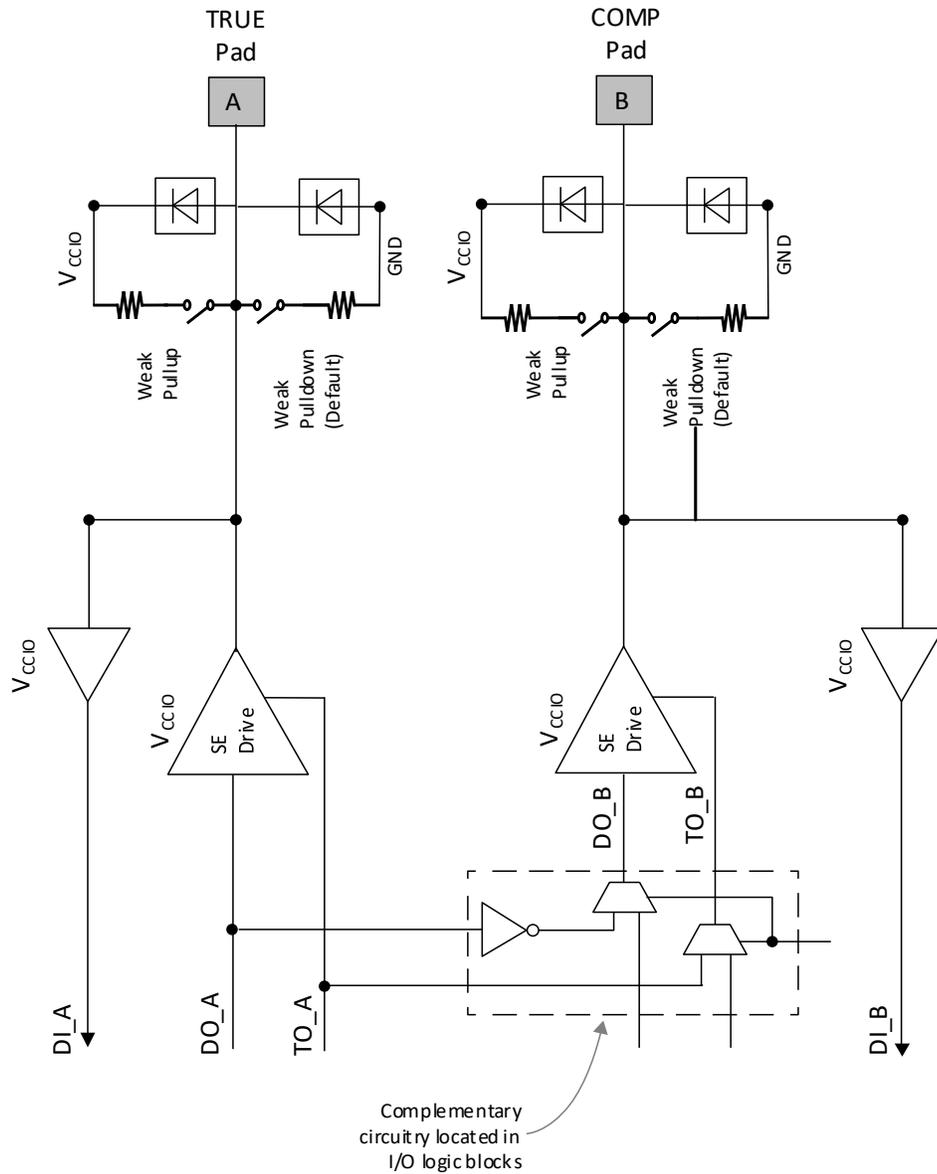


Figure 3.5. Wide Range sysI/O Buffer for Top Side

4. V_{CCIO} Requirement for I/O Standards

Each I/O bank of a device built on the Avant has a separate V_{CCIO} supply pin that can be connected to 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.8 V for bottom banks and 1.2 V, 1.8 V, 2.5 V, 3.3 V for the top banks. These voltages are used to power the output I/O standard and source the drive strength for the output. On the input side, each pad is connected to ratioed V_{CCIO} input buffers.

For HPIO, the supply voltage can be higher than the I/O voltage because the I/O uses a ratioed input buffer.

Table 4.1. Input Mixed Mode for Wide Range Input Buffers

V _{CCIO} (V)	Input Signaling (V)			
	LVC MOS12	LVC MOS18	LVC MOS25	LVC MOS33
1.2	✓	—	—	—
1.8	—	✓	—	—
2.5	—	—	✓	—
3.3	—	—	—	✓

Table 4.2. Input Mixed Mode for High-Performance Input Buffers

V _{CCIO} (V)	Input Signaling (V)			
	LVC MOS09	LVC MOS10	LVC MOS12	LVC MOS18
0.9	✓	—	—	—
1.0	✓	✓	—	—
1.2	✓	✓	✓	—
1.8	✓	✓	✓	✓

5. sysI/O Buffer Configurations

This section describes the various sysI/O features available on Avant devices.

5.1. Programmable Drive Strength

All single-ended drivers have programmable drive strength. Table 5.1 show the programmable drive strength of all the I/O standards available in devices built on Avant devices. The maximum current allowed per bank as well as the package thermal limit current should be taken into consideration when selecting the drive strength.

Table 5.1. Programmable Drive Strength Values at Various V_{CCIO} Voltages

Output Standard	Drive	DiffDrive	V _{CCIO}
Single Ended Interfaces			
LVC MOS33	4 mA, 8 mA, 12 mA, 50RS ¹	—	3.3
LVC MOS25	4 mA, 8 mA, 12 mA, 50RS ¹	—	2.5
LVC MOS18	4 mA, 8 mA, 12 mA, 50RS ¹	—	1.8
LVC MOS12	4 mA, 8 mA , 12mA	—	1.2
LVC MOS10	2 mA, 4 mA, 8 mA	—	1.0
LVC MOS09	2 mA, 4 mA, 8 mA	—	0.9
LVC MOS33 (Open Drain)	4 mA, 8 mA , 12 mA	—	3.3
LVC MOS25 (Open Drain)	4 mA, 8 mA , 12 mA	—	3.3, 2.5
LVC MOS18 (Open Drain)	4 mA, 8 mA , 12 mA	—	3.3, 2.5, 1.8
LVC MOS12 (Open Drain)	4 mA, 6 mA, 8 mA , 12 mA	—	3.3, 2.5, 1.8,
LVC MOS10 (Open Drain)	2 mA, 4 mA, 8 mA	—	1.8, 1.2, 1.0
LVC MOS09 (Open Drain)	2 mA, 4 mA, 8 mA	—	1.8, 1.2, 1.0,
HSUL12	34 Ω , 40 Ω, 48 Ω	—	1.2
SSTL135	34 Ω , 40 Ω	—	1.35
POD11	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.1
POD12	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.2
LVSTL11_I	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.1
LVSTL11_II	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.1
Differential Interfaces			
LVDS	—	3.5 mA	1.8
SLVS	—	2.0 mA	1.2, 1.8
SUBLVDSE	50RS ¹	—	1.8
LVDSE	12 mA	—	2.5
HSUL12D	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.2
SSTL135D	34 Ω , 40 Ω	—	1.35
LVSTL11D_I	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.1
LVSTL11D_II	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.1
POD11D	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.1
POD12D	34 Ω , 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, 240 Ω	—	1.2

Notes:

- 50RS is an additional drive strength setting to mitigate reflection issues when driving an unterminated open transmission line trace of 50 Ω.
- For output standards that have multiple drive values, the default drive values are in **bolds**.

5.2. Programmable Slew Rate

The single-ended output buffer for each device I/O pin has programmable output slew rate control that can be configured for either low-noise (SLEWRATE=SLOW) or high-speed (SLEWRATE=FAST) performance. Each I/O pin has an individual slew rate control that allows designers to specify slew rate control on a pin-by-pin basis. Slew rate control affects both the rising and falling edges. Slew rates vary as a function of drive and PVT conditions. Slow slew rate reduces SSO noise as well as reflections for WRIO if only WRIO is applicable. The software default for slew rate is SLEWRATE=SLOW. Slow slew rate reduces SSO noise as well as reflections for WRIO and HPIO if both types are applicable.

Differential standards are not impacted by slew rate settings. However, slew rate settings have some impact on emulated differential standards, as they use single-ended output buffers and complementary outputs.

5.3. Tri-state Control

On the output side, each single-ended driver has a separate tri-state control. The differential driver has a tri-state control as well.

5.4. Open-Drain Control

In addition to the tri-state control, the single-ended drivers also support open-drain operation on each I/O independently. Unlike non-open drain output which consists of a source and sink section, an open-drain output is composed of only the sink section of the output driver. You can implement an open-drain output by turning on the OPENDRAIN attribute in the software.

5.5. Differential Input Termination

Lattice Avant devices support a programmable 100 Ω input termination between all pairs on the bottom banks. The input termination of 100 Ω can be programmed between on and off. Figure 5.1 shows the discrete off-chip and on-chip solutions for dedicated differential input termination. The differential termination is implemented using parallel legs that turn on and off to compensate for PVT variation.

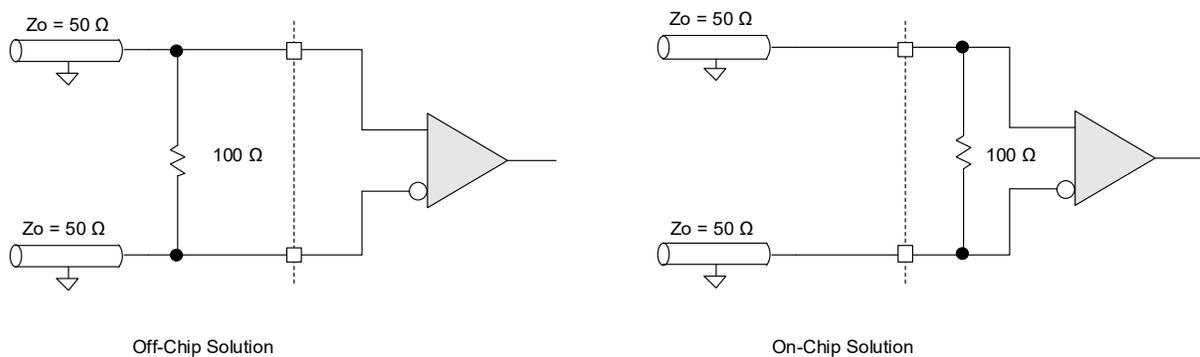


Figure 5.1. Off-Chip and On-Chip Solutions

5.6. ESD Protection Diode

ESD protection Diode to all I/O banks. I/O pins are clamped to VCCIO and GND by the ESD diode.

5.7. Soft MIPI D-PHY Support

The following primitive should be used when implementing soft MIPI D-PHY I/O in Avant devices for High Speed (HS) as well as Low Power (LP) mode for RX and TX. MIPI primitive is supported in HP banks on the bottom side of the device.

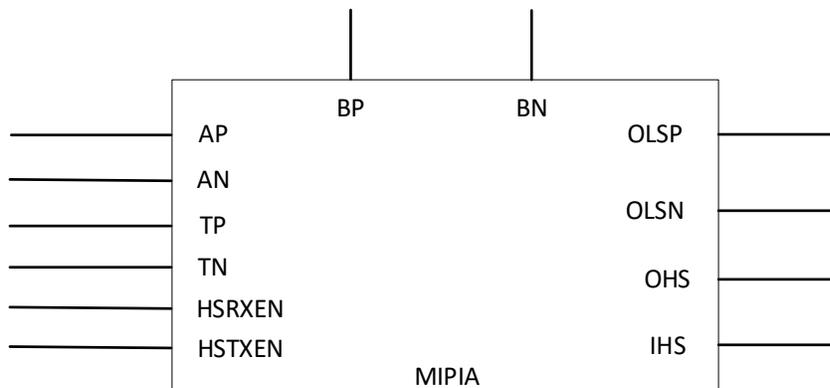


Figure 5.2. MIPI Primitive Symbol

Table 5.2. MIPI Port List

Port	I/O	Description
BP	I/O	Bidirectional PAD A used for D-PHY Clock/Data in both HS and LP mode
BN	I/O	Bidirectional PAD B used for D-PHY Clock/Data in both HS and LP mode
AP	I	Input from fabric to PAD A – used for LP Tx function only
AN	I	Input from fabric to PAD B – used for LP Tx function only
HSRXEN	I	Enable to receive HS differential signals
HSTXEN	I	Enable to transmit HS differential signals
TP	I	Tri-state for PAD A
TN	I	Tri-state for PAD B
OLSP	O	LP Rx signal from BP
OLSN	O	LP Rx signal from BN
OHS	O	HS Rx signal from BP/BN differential
IHS	I	De-serialized input from DDR output register

When IO_TYPE is MIPI, the MIPI primitive above should be instantiated in the design. Otherwise, the software Design Rule Check (DRC) errors out. The output from the MIPI D-PHY buffer can only be used with the Double Data Rate (DDR) registers. Refer to [Lattice High-Speed I/O and External Memory Interface User Guide \(FPGA-TN-02300\)](#) for details on building MIPI D-PHY interfaces.

6. Software sysI/O Attributes

The sysI/O attributes can be specified in the Hardware Description Language (HDL), using Device Constraint Editor, or in Pre-Synthesis Constraint Editor/Post-Synthesis Timing Constraint Editor (.ldc/.pdc).

6.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The V_{CCIO} required to set these I/O standards is embedded in the attribute names. Table 6.1 lists the available I/O types.

Table 6.1. IO_TYPE Attribute Values

sysI/O Signaling Standard	IO_TYPE
Default	LVCOMS33/LVCOMS18 ¹
LVDS	LVDS
LVDS Emulation	LVDSSE
Sub-LVDS	SUBLVDS
Sub-LVDS Emulation	SUBLVDSSE
SLVS	SLVS
MIPI_DPHY	MIPI_DPHY
LVSTL 1.1V Class I	LVSTL11_I
LVSTL 1.1V Class II	LVSTL11_II
LVSTL 1.1V Class I Differential	LVSTL11D_I
LVSTL 1.1V Class II Differential	LVSTL11D_II
POD 1.1V	POD11
POD 1.1V Differential	POD11D
POD 1.2V	POD12
POD 1.2V Differential	POD12D
HSUL 1.2V	HSUL12
HSUL 1.2V Differential	HSUL12D
SSTL 1.35V	SSTL135
HSUL 1.2V	HSUL12
LVC MOS 3.3V	LVC MOS33
LVC MOS 2.5V	LVC MOS25
LVC MOS 1.8V	LVC MOS18
LVC MOS 1.2V	LVC MOS12
LVC MOS 1.0V	LVC MOS10
LVC OS 0.9V	LVC OS09

Note:

1. If PIO is placed to WR bank, the default value is LVCOS33. If PIO is placed to HP bank, the default value is LVCOS18.

6.2. PULLMODE

The PULLMODE options can be enabled for each I/O pin independently. The PULLMODE settings are not available when I/O pins are programmed as output. It is available for I/O pins in Input mode and Bi-direction mode.

Values: UP, DOWN, NONE, I3C, FAILSAFE¹, KEEPER

Default: DOWN for standards mentioned above. Others defaulted to NONE.

Note:

1. FAILSAFE is only available for LVDS input. PULLMODE in FAILSAFE mode enables the pull-up for the P input and pull-down for the N input in LVDS.

6.3. HYSTERESIS

Hysteresis is always enabled when LVCMOS Receive is enabled. There is no built-in hysteresis in the differential receiver.

Values: ON, NA

Default: ON for LVCMOS for input and bidirectional standards. Others defaulted to NA.

6.4. VREF

Each bank supports external VREF and internal VREF. Each I/O pair can be configured to select either one of the available VREF signals. DDR5, LPDDR4, and DDR4 must use internal VREF.

Values: OFF, VREF_EXT, VREF_INT

Default: OFF.

6.5. OPENDRAIN

The OPENDRAIN option is available for all LVCOMS output buffers.

An I/O can be assigned independently to be an open drain when this attribute is turned on.

Values: OFF, ON

Default: OFF

6.6. SLEWRATE

Each I/O pin has an individual slew rate control. This allows you to specify slew rate control on a pin-by-pin basis. Slew rate control is not a valid attribute for inputs.

Values: SLOW, FAST, NA

Default: SLOW

Hardware default: SLOW

6.7. DIFFRESISTOR

This attribute is used to provide differential termination. It is available only for differential I/O types.

Values: OFF, 100

Default: OFF

6.8. TERMINATION

The I/O supports single-ended input parallel termination to $V_{CCIO}/2$. All input parallel terminations use a Thevenin termination scheme.

Values: OFF, 34, 40, 48, 60, 80, 120, 240

Default: OFF

6.9. DRIVE STRENGTH

The DRIVE STRENGTH attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used. Refer to Table 5.2 for programmable drive strength of all the I/O standards available in devices built on Avant devices.

6.10. LOC

This location attribute can be used to make pin assignments to the I/O ports in the design. This attribute is used when the pin assignments are made in HDL source code or in constraint editor.

Appendix A. HDL Attributes

IO_TYPE

VHDL:

```
ATTRIBUTE IO_TYPE: string;  
ATTRIBUTE IO_TYPE OF portA: SIGNAL IS "LVCMOS18";  
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";  
ATTRIBUTE IO_TYPE OF portC: SIGNAL IS "LVCMOS25";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" DRIVE="12" PULLMODE="UP" SLE- WRATE="FAST"*/;
```

OPENDRAIN

VHDL:

```
ATTRIBUTE OPENDRAIN: string;  
ATTRIBUTE OPENDRAIN OF q_lvcoms33_17: SIGNAL IS "ON";
```

Verilog:

```
output [4:0] portA /* synthesis attribute OPENDRAIN of q_lvcoms33_17 is ON */;
```

DRIVE

VHDL:

```
ATTRIBUTE DRIVE: string;  
ATTRIBUTE DRIVE OF portD: SIGNAL IS "8";
```

Verilog:

```
output [4:0] portA /* synthesis DRIVE = "8" */;
```

DIFFDRIVE

VHDL:

```
ATTRIBUTE DIFFDRIVE: string;  
ATTRIBUTE DIFFDRIVE OF portF: SIGNAL IS "3.5";
```

Verilog:

```
output [4:0] portF/* synthesis IO_TYPE="LVDS" DIFFDRIVE="3.5" */;
```

TERMINATION

VHDL:

```
ATTRIBUTE TERMINATION: string;  
ATTRIBUTE TERMINATION OF portF: SIGNAL IS "60";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCOMS18" TERMINATION = "60"*/;
```

DIFFRESISTOR

VHDL:

```
ATTRIBUTE DIFFRESISTOR: string;  
ATTRIBUTE DIFFERESISTOR OF portF: SIGNAL IS "100";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVDS" DIFFRESISTOR = "100"*/;
```

PULLMODE

VHDL:

```
ATTRIBUTE PULLMODE: string;  
ATTRIBUTE PULLMODE OF portF: SIGNAL IS "UP";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" PULLMODE = "UP"*/;
```

SLEWRATE

VHDL:

```
ATTRIBUTE SLEWRATE: string;  
ATTRIBUTE SLEWRATE OF portF: SIGNAL IS "FAST";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" SLEWRATE = "FAST"*/;
```

HYSTERESIS

VHDL:

```
ATTRIBUTE HYSTERESIS: string;  
ATTRIBUTE HYSTERESIS OF portF: SIGNAL IS "ON";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS25" HYSTERESIS = "ON"*/;
```

LOC

VHDL:

```
ATTRIBUTE LOC : string;  
ATTRIBUTE LOC OF output_vector : SIGNAL IS "H5";
```

Verilog:

```
Input rst /* synthesis LOC="H5" */ ;
```

VREF

To set User Vref Locate:

1. After opening the design project, choose **Tools > Device Constraint Editor**.
2. Select the **Global** tab at the bottom of the view.
3. Double click the cell beside **Vref Locate**. A dialog opens.
4. For each available site, click on the desired row and enter a unique name in the **VREF Name** field.

Syntax

```
ldc_create_vref -name <vref_name> -site <site_value>
```

where:

<vref_name> = string

<site_value> = already pre-filled by Radiant.

For more details regarding I/O type, see the sysIO User Guide for your target device family.

Example

This constraint assigns a custom site name TEST_SITE to the selected site.

```
ldc_create_vref -name TESTING_SITE 8
```

Appendix B. sysI/O Buffer Design Rules

- Only one V_{CCIO} level is allowed in a given bank. As such, all IO_TYPES of that bank should be compatible with the V_{CCIO} level.
- Banks at the top side of the device can support single-ended I/O and emulated outputs differential.
- Bottom banks support differential inputs and outputs as well as single-ended I/O.
- When an output is configured as an OPENDRAIN, the PULLMODE is set to NONE.
- When an output is configured as an OPENDRAIN, it can be placed independent of V_{CCIO} .
- When a ratioed input buffer is placed in a bank with a different V_{CCIO} (mixed mode), the Pull mode options of Up are no longer available.
 - The IO_TYPE attribute for a differential buffer can only be assigned to the TRUE pad. The Lattice Radiant™ design tool automatically assigns the other I/O of the differential pair to the complementary pad.
- DIFFRESISTOR termination is available on all sysI/O pairs of bottom banks.
- If none of the pins are used for a given bank, the V_{CCIO} of the bank can be tied to any power rail.
- EXT_RES pins are dedicated for resistor connection to ground or bank VCCIO only.
 - Connect $240\ \Omega \pm 1\%$ to ground on banks which use standards LVDS, subLVDS, SLVS, HSUL, POD, MIPI, D-PHY.
 - Connect $240\ \Omega \pm 1\%$ to VCCIO on banks which use LVSTL_I IO standard.
 - Connect $180\ \Omega \pm 1\%$ to VCCIO on banks which use LVSTL_II IO standard.
 - Leave unconnected if bank is not using one of the above standards.

Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface

sysI/O buffer attributes can be assigned using Device Constraint Editor in the Lattice Radiant software. The Port Assignments Sheet lists all the ports in a design and all the available sysI/O attributes in multiple columns. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the PULLMODE, DRIVE, SLEWRATE, and other attributes list only the valid entries for that IO_TYPE.

Pin locations can be locked by using the Pin column of the Port Tab Sheet or by using the Pin Tab Sheet. You can right click on a cell and go to **Assign Pins** to see a list of available pins.

In Device Constraint Editor, go to **Design > Constraint DRC** to look for incorrect pin assignments.

All the preferences assigned using the Device Constraint Editor are written into the post-synthesis constraint file (.pdc).

Figure C.1 shows the Port Sheet of the Device Constraint Editor.

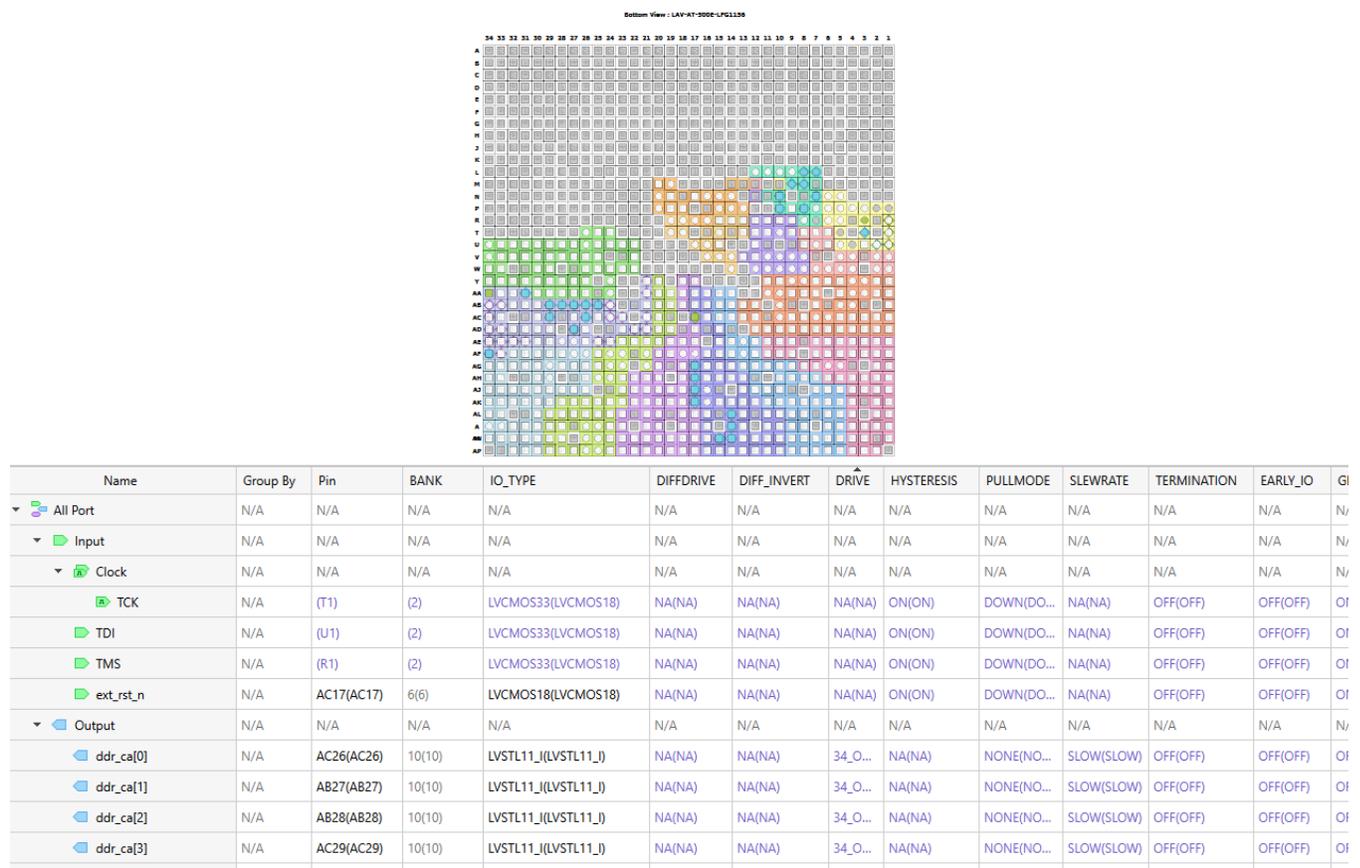


Figure C.1. Port Sheet of Device Constraint Editor

For further information on how to use Device Constraint Editor, refer to the Lattice Radiant Help documentation, available in the Help menu option of the software.

References

- [Avant-E web page](#)
- [Avant-G web page](#)
- [Avant-X web page](#)
- [IP Cores and Reference Designs for Avant Devices](#)
- [Kits, Boards, and Demonstrations for Avant Devices](#)

A variety of technical notes for the Lattice Avant platform are available.

- [High-Speed PCB Design Considerations \(FPGA-TN-02178\)](#)
- [Lattice Avant Embedded Memory User Guide \(FPGA-TN-02289\)](#)
- [Lattice Avant Hardware Checklist \(FPGA-TN-02317\)](#)
- [Lattice High-Speed I/O and External Memory Interface User Guide \(FPGA-TN-02300\)](#)
- [Lattice Avant Platform - Overview Data Sheet \(FPGA-DS-02107\)](#)
- [Lattice Avant Platform - Specifications Data Sheet \(FPGA-DS-02112\)](#)
- [Lattice Avant Power User Guide \(FPGA-TN-02291\)](#)
- [Lattice Avant sysCLOCK PLL Design and User Guide \(FPGA-TN-02298\)](#)
- [Lattice Avant sysDSP User Guide \(FPGA-TN-02293\)](#)
- [Lattice Avant sysCONFIG User Guide \(FPGA-TN-02299\)](#)
- [Lattice Avant sysI/O User Guide \(FPGA-TN-02297\)](#)
- [Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide \(FPGA-UG-02039\)](#)
- [sub-LVDS Signaling Using Lattice Devices \(FPGA-TN-02028\)](#)
- [Thermal Management \(FPGA-TN-02044\)](#)
- [Using TraceID \(FPGA-TN-02084\)](#)

Other references:

- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans
- [Lattice Radiant](#) FPGA design software

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.84, February 2026

Section	Change Summary
Abbreviations in This Document	Renamed this section.
Introduction	Minor editorial edit.
sysI/O Overview	Updated the following statement regarding sysI/O block key feature: <i>Bottom HPIO banks support on-chip programmable differential input 100 Ω termination. Single-end termination with a programmable resistor is supported in all banks.</i>
sysI/O Banking Scheme	<ul style="list-style-type: none"> Minor editorial edit. Updated Figure 3.4. High-Performance sysI/O Buffer Pair for Bottom Side.
VCCIO Requirement for I/O Standards	Added the following statement: <i>For HPIO, the supply voltage can be higher than the I/O voltage because the I/O uses a ratioed input buffer.</i>
sysI/O Buffer Configurations	<ul style="list-style-type: none"> Updated Table 5.1. Programmable Drive Strength Values at Various VCCIO Voltages and the table caption. Removed Table 5.2. Programmable Drive Strength Values at Various VCCIO Voltages for High-Performance Output Driver. Editorial edit to the 5.5. Differential Input Termination section.
Software sysI/O Attributes	<ul style="list-style-type: none"> Added the following statement in the DRIVE STRENGTH section: <i>Refer to Table 5.2 for programmable drive strength of all the I/O standards available in devices built on Avant devices.</i> Removed Table 6.2. Drive Strength Values.
Appendix B. sysI/O Buffer Design Rules	<ul style="list-style-type: none"> Updated the following statement: <i>If none of the pins are used for a given bank, the VCCIO of the bank can be tied to any power rail.</i> Added these statements: <ul style="list-style-type: none"> <i>EXT_RES pins are dedicated for resistor connection to ground or bank VCCIO only.</i> <i>Connect 240 Ω \pm1% to ground on banks which use standards LVDS, subLVDS, SLVS, HSUL, POD, MIPI, D-PHY.</i> <i>Connect 240 Ω \pm1% to VCCIO on banks which use LVSTL_I IO standard.</i> <i>Connect 180 Ω \pm1% to VCCIO on banks which use LVSTL_II IO standard.</i> <i>Leave unconnected if bank is not using one of the above standards.</i>

Revision 0.83, September 2024

Section	Change Summary
Acronyms in This Document	Updated this section.
sysI/O Banking Scheme	<ul style="list-style-type: none"> Changed <i>LAV-AT-E/G/X30 devices have eight banks</i> to <i>LAV-AT-E/G/X30 devices have eleven banks</i>. Changed <i>LAV-AT-E/G/X70 devices and LAV-AT-E/G/X50 devices have another three WR I/O banks for a total of six WR I/O banks (104 I/O)</i> to <i>LAV-AT-E/G/X70, LAV-AT-E/G/X50, and LAV-AT-E/G/X30 devices have another three WR I/O banks, amounting to a total of six WR I/O banks (104 I/O)</i>. Changed <i>Figure 3.1 shows the location of each bank of the LAV-AT-E/G/X30 device, three banks on the top side and five banks on the bottom side</i> to <i>Figure 3.1 shows the location of each bank of the LAV-AT-E/G/X30 device, six banks on the top side and five banks on the bottom side</i>. Updated Figure 3.1. LAV-AT-E/G/X30 sysI/O Banking.
References	Updated this section.

Revision 0.82, April 2024

Section	Change Summary
Software sysI/O Attributes	<ul style="list-style-type: none"> Added the note: <i>FAILSAFE is only available for LVDS input. PULLMODE in FAILSAFE mode enables the pull-up for the P input and pull-down for the N input in LVDS in the PULLMODE section.</i> Updated Table 6.2. Drive Strength Values: <ul style="list-style-type: none"> Bolded the default drive values for <i>Output Standards</i> that have multiple drive values. Added a table note on the default drive value.

Revision 0.81, November 2023

Section	Change Summary
Disclaimer	Updated this section.
SysI/O Banking Scheme	Updated the below information: <ul style="list-style-type: none"> Replaced <i>LAV-AT-500</i> with <i>LAV-AT-E/G/X70</i> Replaced <i>LAV-AT-300</i> with <i>LAV-AT-E/G/X50</i> Replaced <i>LAV-AT-200</i> with <i>LAV-AT-E/G/X30</i>
VCCIO Requirements for I/O Standards	Deleted " <i>These three buffers are connected to VCC, VCCIO, and VCCAUX respectively.</i> "
sysI/O Buffer Configurations	Removed output standards <i>UVCCIO</i> and <i>UGND</i> in Table 5.2. Programmable Drive Strength Values at Various VCCIO Voltages for High-Performance Output Drive.
Software sysI/O Attributes	Removed output standards <i>UVCCIO</i> and <i>UGND</i> in Table 6.1. IO_TYPE Attribute Values and Table 6.2. Drive Strength Values.
References	Added this section.

Revision 0.80.1, April 2023

Section	Change Summary
All	Minor adjustments in formatting across the document.
Inclusive Language	Added this section.
sysI/O Overview	Added bullet information "Support xSPI Interface, for both configuration and user mode on WRIO's." in sysI/O Overview section.
sysI/O Banking Scheme	Updated the below figures to include Serdes banks: <ul style="list-style-type: none"> Figure 3.1. LAV-AT-200 sysI/O Banking Figure 3.2. LAV-AT-300 sysI/O Banking Figure 3.3. LAV-AT-500 sysI/O Banking
Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface	Added Figure C.1. Port Sheet of the Device Constraint Editor.
Technical Support Assistance	Added Lattice FAQ website link.

Revision 0.80, November 2022

Section	Change Summary
sysI/O Overview	Updated support interface for configuration and user mode on WRIOs.
sysI/O Banking Scheme	Updated Figure 3.1. LAV-AT-200 sysI/O Banking, Figure 3.2. LAV-AT-300 sysI/O Banking, Figure 3.3. LAV-AT-500 sysI/O Banking, Figure 3.4. High-Performance sysI/O Buffer Pair for Bottom Side, and Figure 3.5. Wide Range sysI/O Buffer for Top Side.
VCCIO Requirement for I/O Standards	Deleted 0.6 V value.

Section	Change Summary
sysI/O Buffer Configurations	<ul style="list-style-type: none"> Added Slow slew rate reduces SSO noise as well as reduces reflections for WRIO'. (If only applicable WRIO). The software default for slew rate is SLEWRATE=SLOW. Slow slew rate reduces SSO noise as well as reduces reflections. (If applicable both WRIO and HPIO). in Section 5.2. Programmable Slew Rate. Updated from MIPI to MIPIA in Figure 5.2. MIPI Primitive Symbol.
Software sysI/O Attributes	<ul style="list-style-type: none"> Updated IO_TYPE values. Deleted Section 6.11. DIN/DOOUT.
Appendix A. HDL Attributes	Updated Termination values in Appendix A – HDL Attributes.
Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface	Removed Figure C.1. Port Tab of Device Constraint Editor.

Revision 0.70, May 2022

Section	Change Summary
All	Advance release.



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