



1D Filter Module - Lattice Radiant Software

User Guide

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LSB	Least Significant Bit
MSB	Most Significant Bit
RTL	Register Transfer Level

1. Introduction

The 1D Filter Module has three modes: 1D Symmetric, 1D Asymmetric Serial, and 1D Asymmetric Parallel, which support configurable number of taps each with its own coefficient.

1.1. Features

The key features of 1D Filter Module include:

- Supports the following modes:
 - 1D Symmetric
 - 1D Asymmetric Serial
 - 1D Asymmetric Parallel
- Configurable number of taps
- Supports both Positive and Negative Symmetric for 1D Symmetric Mode only
- Configurable Reset Mode
- Configurable data width and sign representation for Data A and B
- Configurable Bus Ordering

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- `_n` are active low
- `_i` are input signals
- `_o` are output signals

1.2.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

The 1D Filter Module filters the input data according to the following general equation:

$$result = \sum_{n=0}^{NUM_OF_TAPS-1} (A_n * B_n)$$

The following sections provides information on the 1D Filter Module modes:

- 1D Asymmetric Serial
- 1D Asymmetric Parallel
- 1D Symmetric

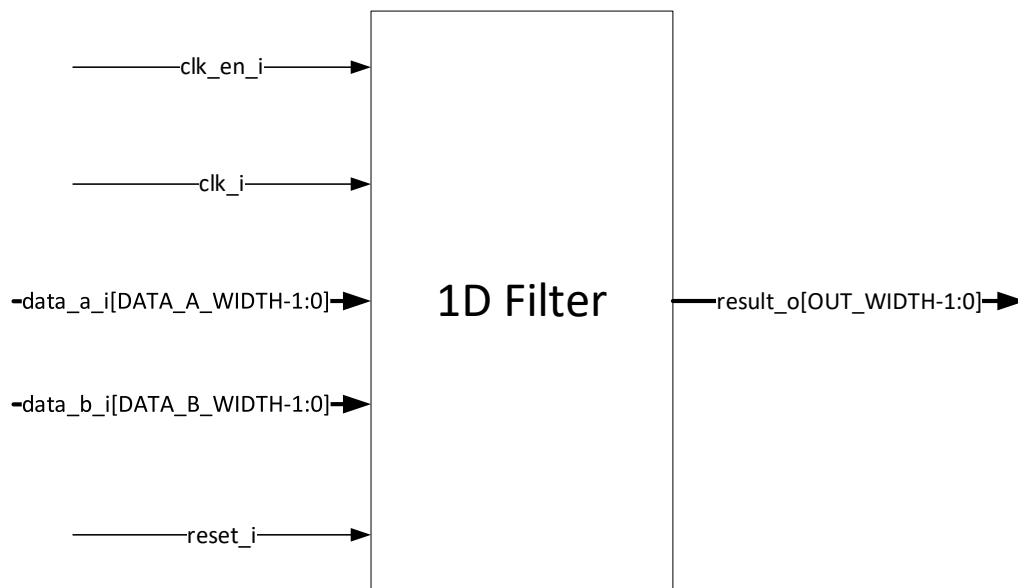


Figure 2.1. 1D Filter Block Diagram

2.1. 1D Asymmetric Serial Mode

data_a_i width = DATAA Width,

data_b_i width = Number of Taps * DATAB Width.

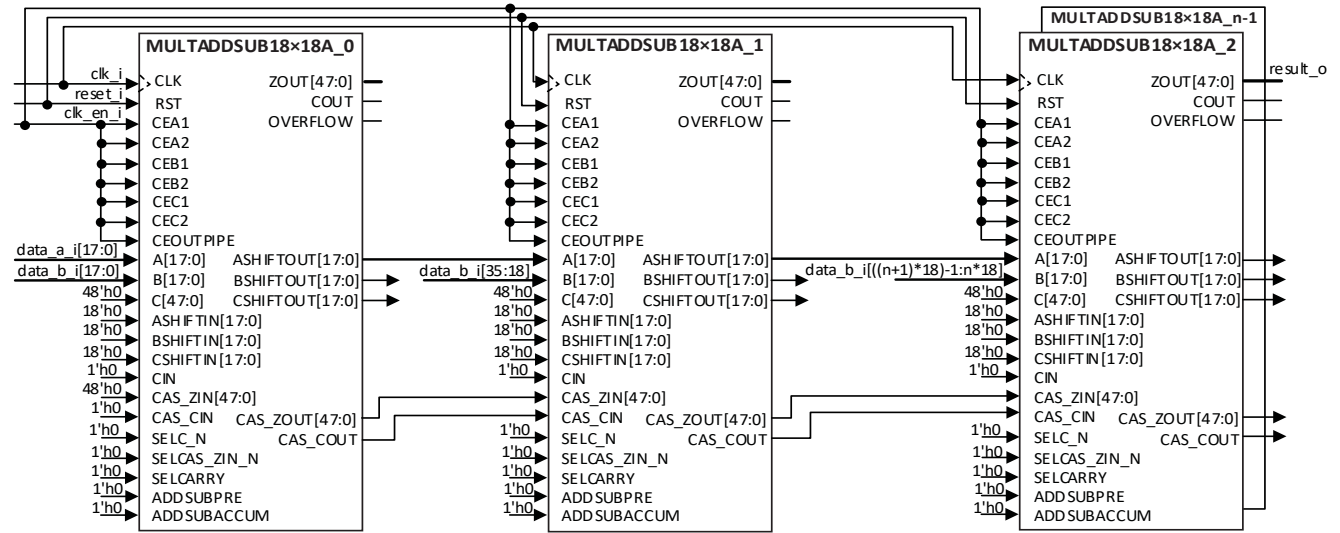
A is a data input that is provided serially, B is an input for coefficients which is provided in a parallel way.

For this mode, the output data is calculated as follows:

$$result = \sum_{n=0}^{NUM_OF_TAPS-1} (A_n * B[(n + 1) * DATAB - 1 : n * DATAB])$$

1D filter on Asymmetric Serial Mode have output latency which can be calculated as Number of Taps + 3.

Figure 2.2 shows 1D asymmetric serial DSP implementation of an 18-bit data inputs with n number of taps. data_a_i input is serially shifted from one DSP to another while data_b_i input is provided in parallel. Filter output is the output of the last DSP on the cascaded DSP chain.



where n = Number of Taps

Figure 2.2. 1D Asymmetric Serial Filter Block Diagram

2.2. 1D Asymmetric Parallel Mode

data_a_i width = Number of Taps * DATAA Width,

data_b_i width = Number of Taps * DATAB Width.

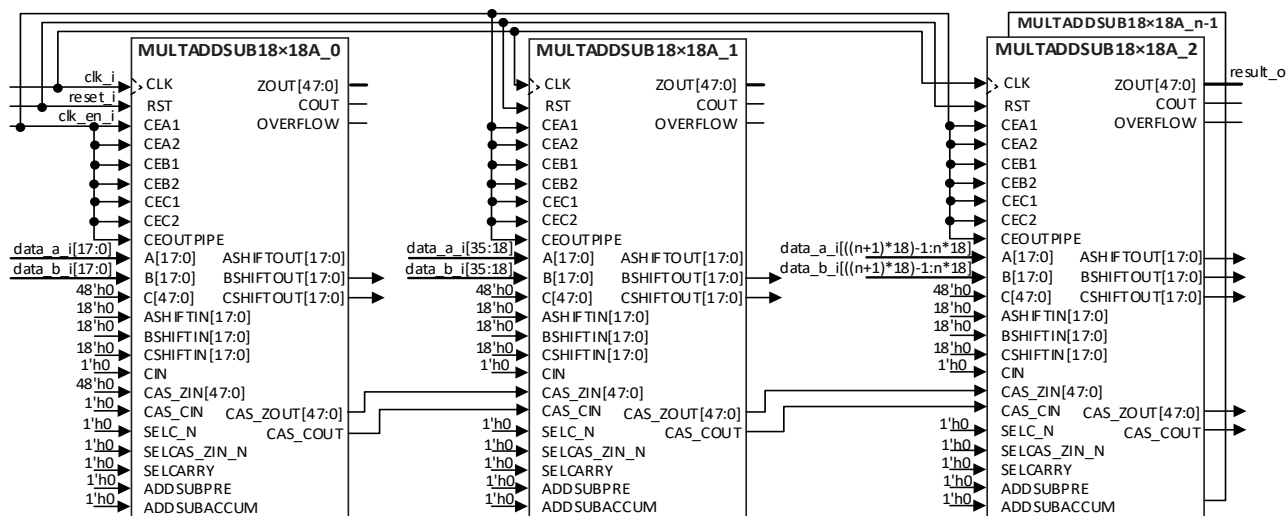
A is a data input, B is an input for coefficients; both are provided in a parallel way.

For this mode, the output data is calculated as follows:

$$result = \sum_{n=0}^{NUM_OF_TAPS-1} (A[(n+1) * DATAA - 1:n * DATAA] * B[(n+1) * DATAB - 1:n * DATAB])$$

1D filter on Asymmetric Parallel Mode with any Number of Taps has output latency of 4.

Figure 2.3 shows 1D asymmetric parallel DSP implementation of an 18-bit data inputs with n number of taps. Both data_a_i and data_b_i are provided in parallel to each DSP. Filter output is the output of the last DSP on the cascaded DSP chain.



where n = Number of Taps

Figure 2.3. 1D Asymmetric Parallel Filter Block Diagram

2.3. 1D Symmetric Mode

data_a_i width = DATAA Width,

data_b_i width:

- when the *Number of Taps* is odd, data_b_i width = $\frac{\text{Number of Taps} + 1}{2} * \text{DATAB Width}$,
- when the *Number of Taps* is even, data_b_i width = $\frac{\text{Number of Taps}}{2} * \text{DATAB Width}$.

For this mode, the output data is calculated as follows:

$$\text{result} = \sum_{n=0}^{K-1} (A_n + A_{(K-n)}) * B[(n+1) * \text{DATAB} - 1:n * \text{DATAB}],$$

where

- $K = \frac{\text{Number of Taps} + 1}{2}$, when *Number of Taps* is odd, and
- $K = \frac{\text{Number of Taps}}{2}$, when *Number of Taps* is even.

1D filter on Symmetric Mode with even or odd Number of Taps have output latency of 4.

Figure 2.4 shows 1D symmetric filter DSP implementation of an 18-bit data inputs with even number of taps. The sample below has 6 taps. The total number of DSP to be used is calculated by, Number of DSP = (Number of Taps)/2. data_a_i is provided to all the instantiated DSP which is also added to delayed data_a_i. The number of registers on the chain used is calculated by, Number of Register = Number of Taps – 1. The result of the last register on the chain is added to data_a_i input of the first DSP on the chain, result of the second to the last register is added to data_a_i input of the second DSP on the chain and so on up until the last DSP on the chain. data_b_i are provided in parallel to each DSP. Filter output is the output of the last DSP on the cascaded DSP chain.

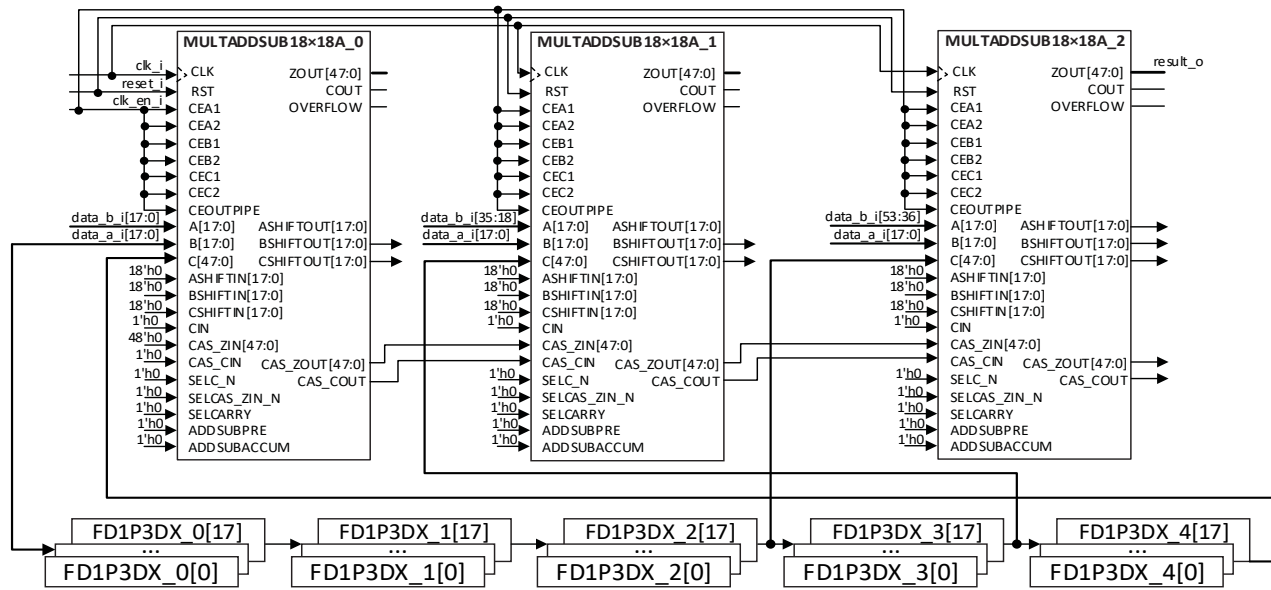


Figure 2.4. 1D Symmetric Filter with Even number of Taps Block Diagram

Figure 2.5 shows 1D symmetric filter DSP implementation of an 18-bit data inputs with odd number of taps. The sample below has 5 taps. The total number of DSP to be used is calculated by, Number of DSP = Number of Taps/2 + 1, truncated to the nearest whole. data_a_i is provided to all the instantiated DSP which is also added to delayed data_a_i. The number of registers on the chain used is calculated by, Number of Register = Number of DSP + 1. The result of the last register on the chain is added to data_a_i input of the first DSP on the chain, result of the second to the last register is added to data_a_i input of the second DSP on the chain and so on up until on the last DSP on the chain. data_b_i are provided in parallel to each DSP. Filter output is the output of the last DSP on the cascaded DSP chain.

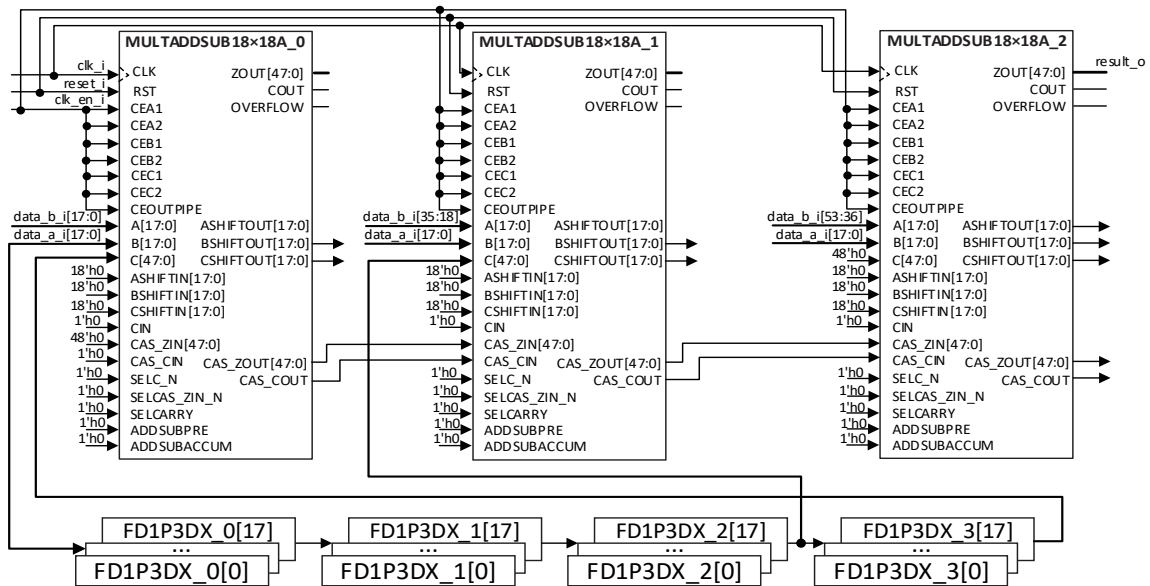


Figure 2.5. 1D Symmetric Filter with Odd number of Taps Block Diagram

2.4. Signal Descriptions

Table 2.1. 1D Filter Module Signal Description

Port Name	I/O	Width	Description
Clock and Reset Ports			
clk_i	In	1	System clock input.
reset_i	In	1	Reset input.
User Interface Ports			
clk_en_i	In	1	Clock enable input.
data_a_i	In	<i>DATAA Width</i> ¹	Input data for port A.
data_b_i	In	<i>DATAB Width</i> ¹	Input data for port B.
result_o	Out	<i>OUT_WIDTH</i> ²	Output data result.

Note:

- The bit width of some signals is set by the attribute. Refer to [Table 2.2](#) for the description of these attributes.
- If *DATAA Width* ≤ 9 and *DATAB Width* ≤ 9, then *OUT_WIDTH* = *DATAA Width* + *DATAB Width* + 6;
 - If at least one of *DATAA Width* or *DATAB Width* > 9, then *OUT_WIDTH* = *DATAA Width* + *DATAB Width* + 18.

2.5. Attribute Summary

The configurable attributes of the 1D Filter Module are shown in [Table 2.2](#) and are described in [Table 2.3](#). The attributes can be configured through the IP Catalog Module/IP wizard of the Lattice Radiant™ software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Configuration			
Mode	1D Symmetric, 1D Asymmetric Serial, 1D Asymmetric Parallel	1D Asymmetric Serial	—
Number of Taps	2–N	2	For <i>Mode</i> == 1D Symmetric, N = 360 else N = 180.
Symmetric	Positive, Negative	Positive	Available if <i>Mode</i> == 1D Symmetric
Reset Mode	Sync, Async	Sync	—
DATAA Sign	Signed, Unsigned	Signed	Available if <i>Symmetric</i> == Positive
DATAA Width	2–18	18	—
DATAB Sign	Signed, Unsigned	Signed	Available if <i>Symmetric</i> == Positive
DATAB Width	2–18	18	—
Bus Ordering Style	Big Endian [MSB : LSB], Little Endian [LSB : MSB]	Big Endian [MSB : LSB]	—

Table 2.3. Attributes Descriptions

Attribute	Description
Configuration	
Mode	Specifies the mode of 1D Filter Module. Refer to the Functional Description section for more details.
Number of Taps	Specifies the number of taps.
Symmetric	Specifies the Symmetric of the 1D Filter Module. Selectable values are Positive and Negative Symmetric.
Reset Mode	Specifies the mode of reset that is used.
DATAA Sign	Specifies the sign representation for port data_a_i.
DATAA Width	Specifies the data width for port A. The exact value of this attribute can be calculated depending on the type of Mode. Refer to the Functional Description section for more details.
DATAB Sign	Specifies the sign representation for port data_b_i.
DATAB Width	Specifies the data width for port B. The exact value of this attribute can be calculated depending on the type of Mode. Refer to the Functional Description section for more details.
Bus Ordering Style	Specifies the bus ordering of input and output data ports. Big Endian: the data_a_i, data_b_i and result_o busses ordering is from MSB to LSB. Little Endian: the data_a_i, data_b_i and result_o busses ordering is from LSB to MSB.

3. IP Generation, Simulation, and Validation

This section provides information on how to generate the IP module using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant software user guide.

3.1. Generating and Synthesizing the IP

The Lattice Radiant software allows you to customize and generate modules and IPs and integrate them into the device architecture. The procedure for generating the 1D Filter Module in Lattice Radiant software is described below.

To generate the 1D Filter Module:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the IP Catalog tab, double-click on **1D_Filter** under **Module, DSP_Arithmetic_Modules** category.
3. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

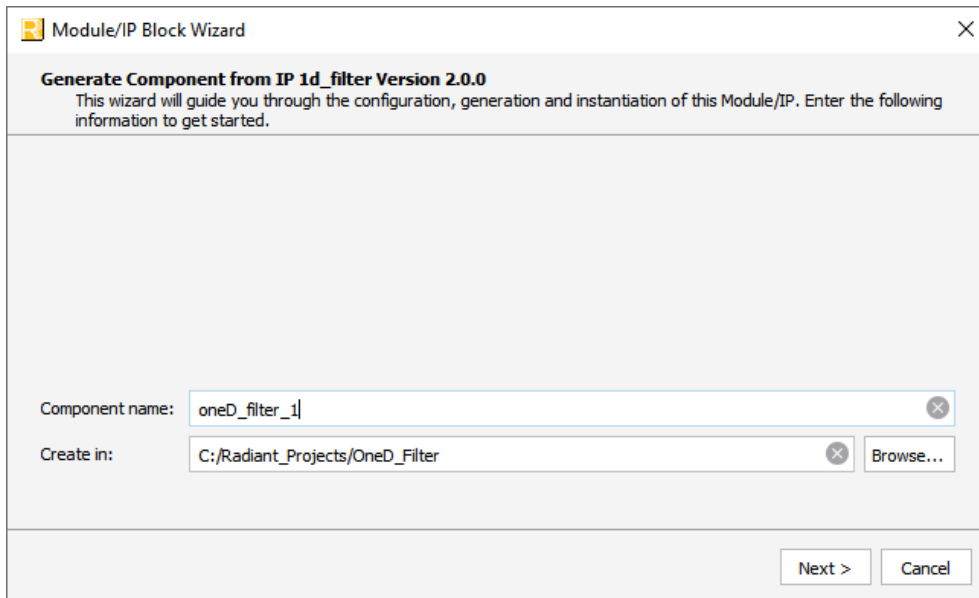


Figure 3.1. Module/IP Block Wizard

4. In the module dialog box of the **Module/IP Block Wizard** window, customize the selected 1D Filter Module using drop-down menus and check boxes. For a sample configuration, see [Figure 3.2](#). For configuration options, see the [Attribute Summary](#) section.

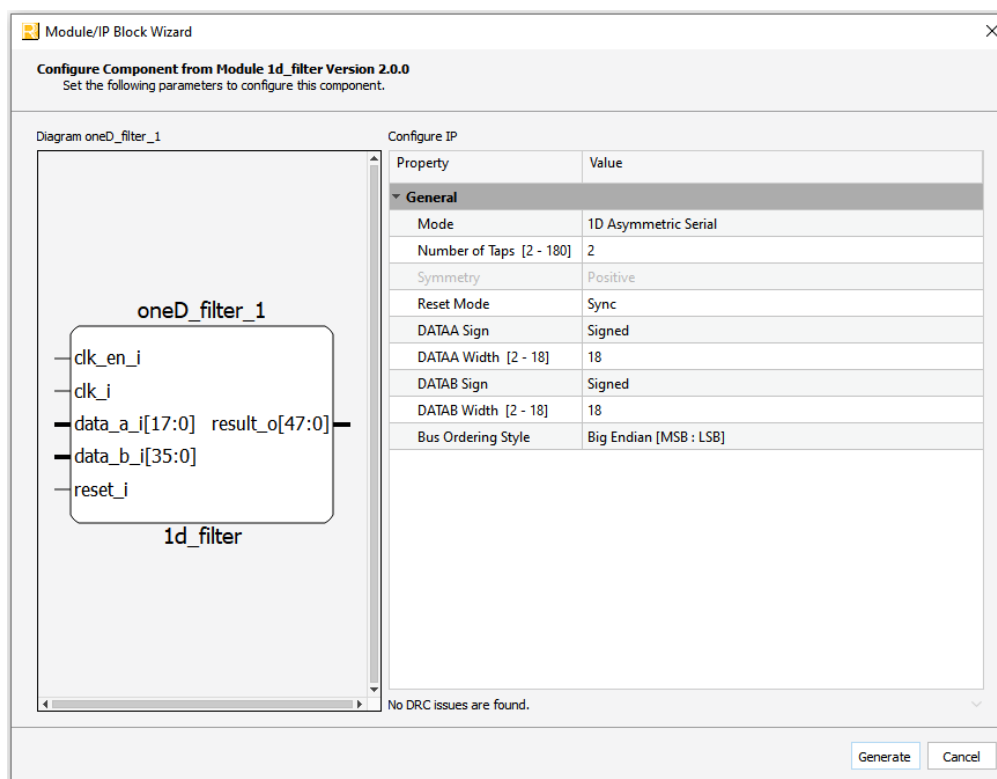


Figure 3.2. Configure User Interface of 1D Filter Module

5. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in [Figure 3.3](#).

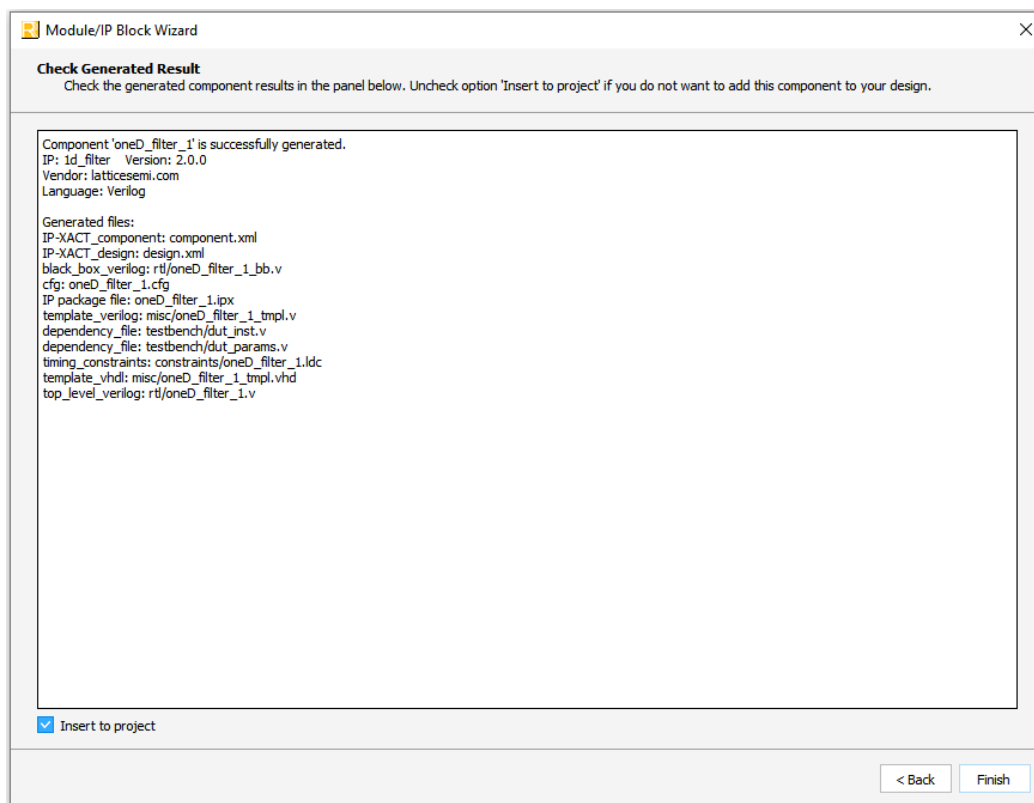


Figure 3.3. Check Generating Result

- Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in [Figure 3.1](#).

The generated 1D Filter Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in [Table 3.1](#).

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.
eval/constraints.pdc	IP constraint file.
testbench/tb_top.v	Test bench template; you can edit this to match your specific needs.
testbench/dut_params.v	Instantiated version of the <IP_name>.v file for simulation use
testbench/dut_ints.v	Top level parameters of the generated RTL file

Radiant flow supports loop count to a certain limit. The steps below should be performed for IP configurations that exceed this loop limit and fail synthesis.

In the Radiant project, navigate to **Project**. Then, select **Active Strategy**. Depending on the synthesis tool used, update the following:

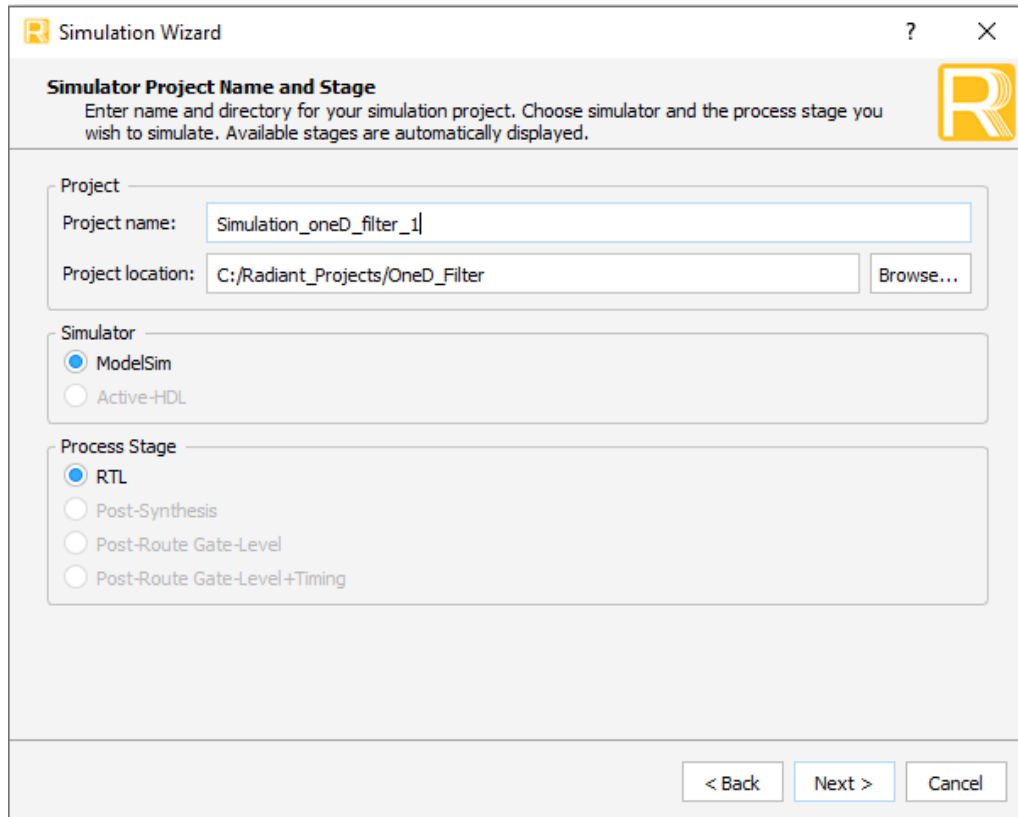
- For 1D Asymmetric Parallel Filter: Loop Limit Value = DATAA Width * Number of Taps or Loop Limit Value = DATAB Width * Number of Taps, whichever is larger.
- For 1D Asymmetric Serial Filter: Loop Limit Value = DATAB Width * Number of Taps
- For 1D Symmetric Filter: Loop Limit Value = DATA_B_WIDTH*(Number of Taps/2+1)
 - For SynplifyPro, select **Synplify Pro Settings**. On the **Command Line Options**, add value `set_option -looplimit <Loop Limit Value>`.
 - For Lattice LSE, select **LSE Settings**. Change default **Loop Limit** value to the calculated value based on formula above.

3.2. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator may require additional steps.

To run functional simulation using the default simulator:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in [Figure 3.4](#).



The **Simulation Wizard** dialog box is shown. It has a title bar with a question mark and a close button. The main area is titled **Simulator Project Name and Stage** with a subtitle: "Enter name and directory for your simulation project. Choose simulator and the process stage you wish to simulate. Available stages are automatically displayed." There is a Lattice logo in the top right corner of the main area.

The dialog is divided into three sections:

- Project**: Contains a "Project name:" text box with the value "Simulation_oneD_filter_1" and a "Project location:" text box with the value "C:/Radiant_Projects/OneD_Filter" and a "Browse..." button.
- Simulator**: Contains two radio buttons: "ModelSim" (selected) and "Active-HDL".
- Process Stage**: Contains four radio buttons: "RTL" (selected), "Post-Synthesis", "Post-Route Gate-Level", and "Post-Route Gate-Level+Timing".

At the bottom right, there are three buttons: "< Back", "Next >", and "Cancel".

Figure 3.4. Simulation Wizard

- Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

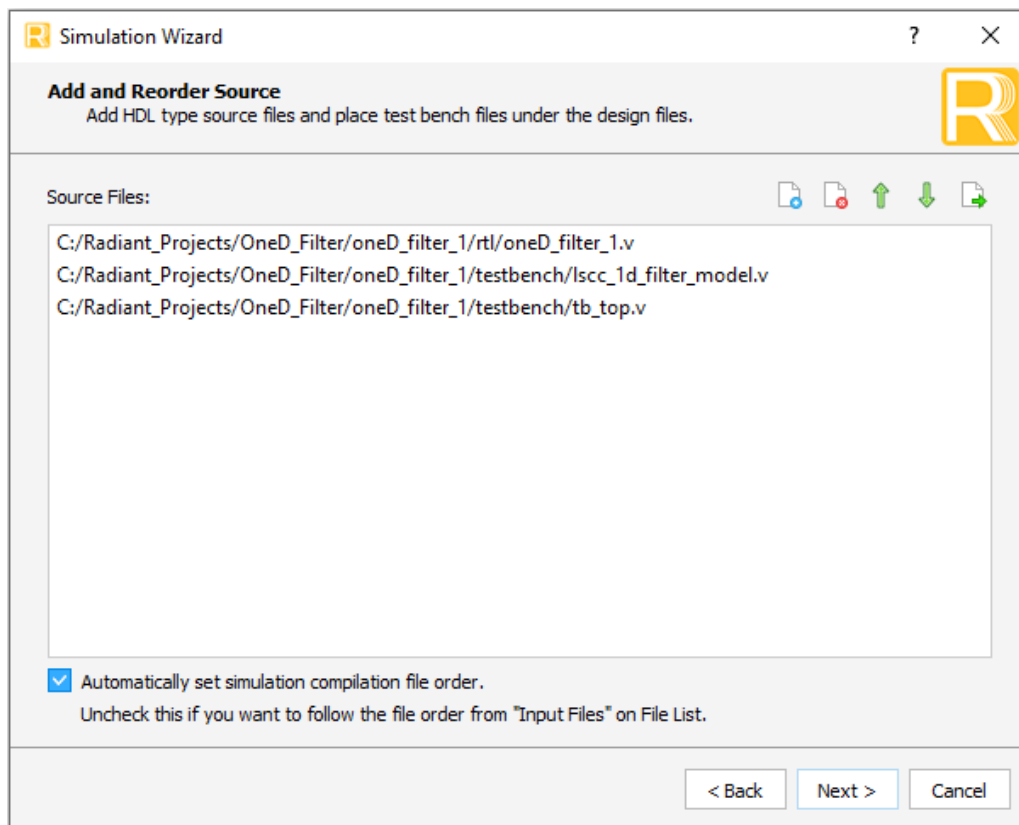


Figure 3.5. Adding and Reordering Source

- Click **Next**. The **Summary** window is shown.
- Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software suite. The results of the simulation in our example are provided in Figure 3.6.

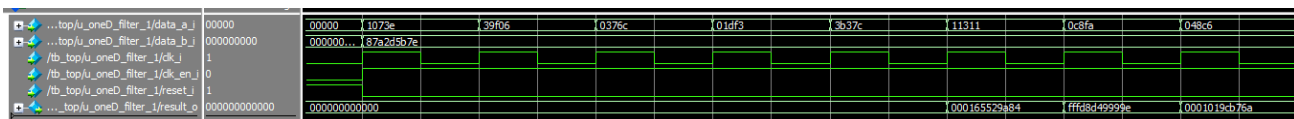


Figure 3.6. Simulation Waveform

3.3. Constraining the IP

You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA. Add the content of the following IP constraint file to your design constraints:

`<IP_Instance_Path>/<IP_Instance_Name>/eval/constraints.pdc.`

The constraint file has been verified during IP evaluation with the IP instantiated directly in the top-level module. You can modify the constraints in this file with thorough understanding of the effect of each constraint.

To use this constraint file, copy the content of *constraints.pdc* to the top-level design constraint for post-synthesis. Refer to [Lattice Radiant Timing Constraints Methodology](#) for details on how to constraint your design.

3.4. IP Evaluation

There is no restriction on the IP evaluation of this module.

Appendix A. Resource Utilization

Table A.1 and Table A.2 show the resource utilization of the 1D Filter Module for LAV-AT-E70-3LFG1156I and LAV-AT-E70-1LFG1156I devices, using Synplify Pro of the Lattice Radiant software. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization using LAV-AT-E70-3LFG1156I

Configuration	Clk Fmax (MHz)*	Registers	LUTs ²	EBRs	DSPs
Default	250	0	0	0	2
DATAA Width = 2, DATAB Width = 2, Others are default	250	0	0	0	2
Mode = 1D Symmetric, Symmetry = Negative, Others are default	250	18	0	0	1
Number of Taps = 5, Others are default	250	0	0	0	5

***Note:** Fmax is generated when the FPGA design only contains 1D Filter Module and the target frequency is 200 MHz. The obtained Fmax values may be reduced when user logic is added to the FPGA design.

Table A.2. Resource Utilization using LAV-AT-E70-1LFG1156I

Configuration	Clk Fmax (MHz)*	Registers	LUTs ²	EBRs	DSPs
Default	250	0	0	0	2
DATAA Width = 2, DATAB Width = 2, Others are default	250	0	0	0	2
Mode = 1D Symmetric, Symmetry = Negative, Others are default	250	18	0	0	1
Number of Taps = 5, Others are default	250	0	0	0	5

***Note:** Fmax is generated when the FPGA design only contains 1D Filter Module and the target frequency is 200 MHz. The obtained Fmax values may be reduced when user logic is added to the FPGA design.

References

- [Avant-E Web Page](#)
- [Avant-G Web Page](#)
- [Avant-X Web Page](#)
- [IP Cores for Avant devices](#)
- [Lattice Radiant](#) FPGA design software
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Document Revision 1.1, Lattice Radiant SW version 2023.2, December 2023

Section	Change Summary
All	Performed minor editorial fixes.
Disclaimers	Updated this section.
IP Generation, Simulation, and Validation	- Updated Table 3.1. Generated File List. - Added section 3.3 Constraining the IP.
Resource Utilization	- Updated device names from <i>LAV-AT-500E-</i> to <i>LAV-AT-E70-</i>. - Updated <i>Clk Fmax</i> values in Table A.1. Resource Utilization using LAV-AT-E70-3LFG1156I and Table A.2. Resource Utilization using LAV-AT-E70-1LFG1156I.
References	Added relevant links.
Technical Support Assistance	Added link to the Lattice Answer Database.

Document Revision 1.0, Lattice Radiant SW version 2022.1, November 2022

Section	Change Summary
All	- Updated 1D Filter mode names: - changed 1D Symmetry to 1D Symmetric; - changed 1D Asymmetry Serial to 1D Asymmetric Serial; - changed 1D Asymmetry Parallel to 1D Asymmetric Parallel.
Functional Description	- Newly added Figure 2.2. 1D Asymmetric Serial Filter Block Diagram; Figure 2.3. 1D Asymmetric Parallel Filter Block Diagram; Figure 2.4. 1D Symmetric Filter with Even number of Taps Block Diagram ; and Figure 2.5. 1D Symmetric Filter with Odd number of Taps Block Diagram. - Added descriptions for above figures. - Added latency information for each 1D Filter mode.
IP Generation, Simulation, and Validation	- Updated the name for section 3 to IP Generation, Simulation, and Validation. - Deleted the original section 3.1 Licensing the IP. - Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure User Interface of 1D Filter Module, Figure 3.3. Check Generating Result, and Figure 3.6. Simulation Waveform. - Added loop count limit information in the section Generating and Synthesizing the IP. - Newly added the section Constraining the IP You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA. Add the content of the following IP constraint file to your design constraints: <pre><IP_Instance_Path>/<IP_Instance_Name>/eval/constraints.pdc.</pre> The constraint file has been verified during IP evaluation with the IP instantiated directly in the top-level module. You can modify the constraints in this file with thorough understanding of the effect of each constraint. To use this constraint file, copy the content of <i>constraints.pdc</i> to the top-level design constraint for post-synthesis. Refer to Lattice Radiant Timing Constraints Methodology for details on how to constraint your design. - IP Evaluation.
Appendix A. Resource Utilization	Newly added this section.

Document Revision 0.80, Lattice Radiant SW version 3.2, May 2022

Section	Change Summary
All	Initial release.



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