Avant MIPI D-PHY Module

User Guide

FPGA-IPUG-02193-1.1

December 2023

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CIL	Control Interface Logic
CSI	Camera Serial Interface
DSI	Display Serial Interface
FPGA	Field Programmable Gate Array
HS	High-speed
IP	Intellectual Property
MIPI	Mobile Industry Processor Interface
LP	Low-power
PHY	Physical
PLL	Phase-locked Loop

1. Introduction

1.1. Overview

Mobile Industry Processor Interface (MIPI) D-PHY bus is a physical serial data communication layer on which protocols like Camera Serial Interface 2 (CSI-2) and Display Serial Interface (DSI) run. It physically connects the camera sensor to the application processor for CSI-2 and the application processor to the display device for DSI, as shown in Figure 1.1.

The Lattice Semiconductor MIPI D-PHY IP incorporates one clock lane and a configurable number of data transmission lanes. The MIPI D-PHY IP supports one, two, and four data lanes.

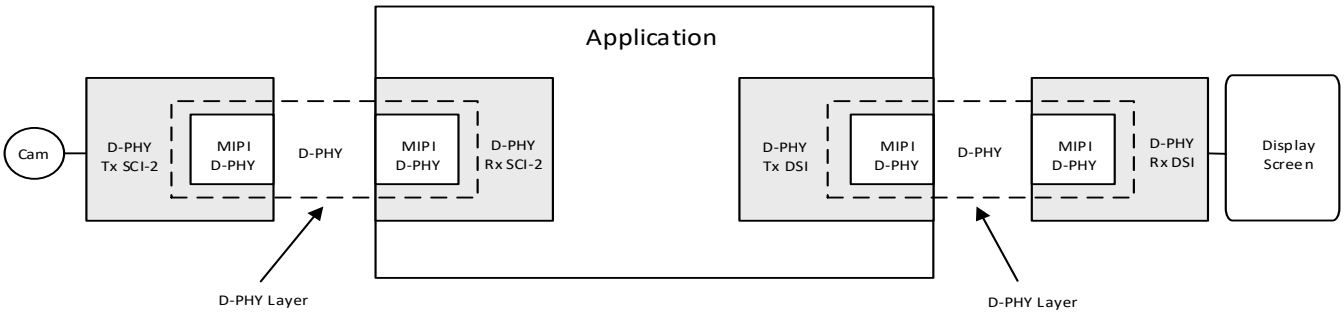

Figure 1.1. MIPI D-PHY Module

Every data lane of the transmitter/receiver consists of data_p_io and data_n_io, either being a differential pair or two single-ended wires. The clock lane consists of clk_p_io and clk_n_io, either being a differential pair or two single-ended wires. Data transmission occurs on these paired wires connecting receiver and transmitter communicating modules.

1.2. Features

- Interfaces to MIPI CSI-2/DSI, Rx, and Tx devices
- Supports unidirectional High-Speed (HS) operation mode
- Supports bidirectional Low-Power (LP) operation mode
- Deserializes and serializes HS data into byte data packets
- Provides methods for contention detection and termination switching
- Supports one, two, three, and four data lanes and one clock lane
- Configurable Rx/Tx
- External reference clock source
- The supported rate is up to 1500 Mbps per lane
- Supported gearing 8x
- MIPI_DPHY I/O type
- Interface Clock Frequency 40 MHz to 750 MHz

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals
- _*io* are bi-directional input/output signals

2. Functional Description

2.1. Overview

Each lane of MIPI D-PHY Module includes both the HS and LP modes.

The HS modules operate in a differential manner. They utilize the low voltage swing of the payload data signals to transfer the information. It contains an on-die termination between Dp and Dn. The LP module, an unterminated module, operates in a single-ended manner.

For transmitting the payload data, which are image data, all types of MIPI D-PHY IPs use high-speed modules. For transmitting the control and status information, all types of MIPI D-PHY IPs use the low-power modules utilizing low-frequency signals.

The bandwidth can be increased by increasing the number of data lanes. By increasing the number of lanes, the same quantity of data can be transmitted on multiple lanes in lesser time. MIPI D-PHY Module uses a forward source synchronous clock, which is used by all the data lanes of the MIPI D-PHY receiver for capturing high-speed data signals.

2.1.1. Operation Mode

The Global Operation Module controls the HS request path and timing using attributes in Table 2.2.

This module controls the timing entering HS and coming from HS entering to LP. Figure 2.1 shows the LP-to-HS transition flow diagram for data lanes.

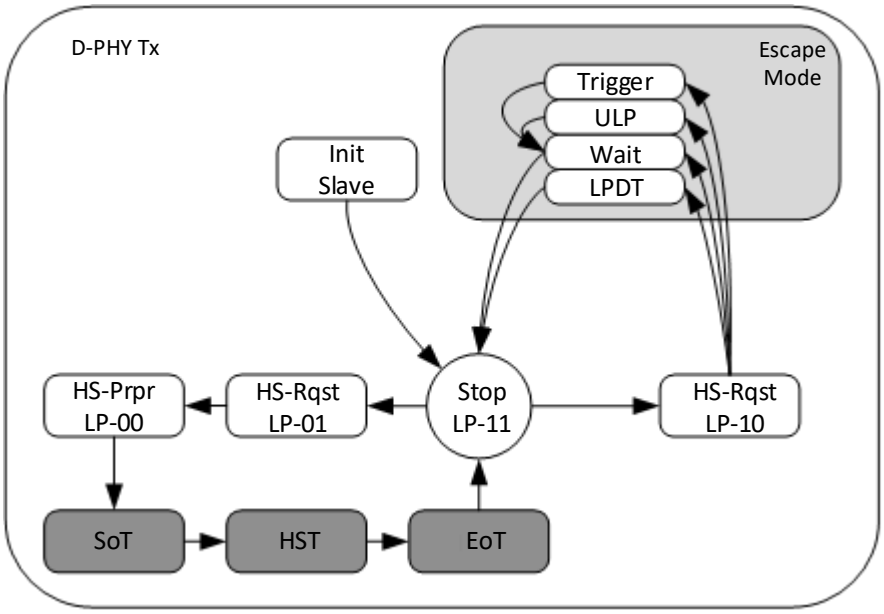

Figure 2.1. MIPI D-PHY Tx LP to HS Transition Flow Diagram on Data Lanes

During normal operation, a data lane is either in control mode or in high-speed mode.

For sending payload data, which are image data, the transmitter drives a particular sequence on data lanes to enter the receiver from low-power mode to high-speed mode.

As part of the initialization of D-PHY, initially, all the lanes are held at LP11 state for a specified time. This LP11 state is also known as the stop state. After this, for sending the image data, the transmitter drives a particular sequence on the receiver to enter the receiver lanes from low-power mode to high-speed mode. The high-speed entry sequence (Figure 2.2) consists of driving LP11->LP01->LP00 (LP->HS transition) on the differential lane. On successful reception of this sequence, the high-speed receiver module enables its termination to receive the high-speed differential data.

After the LP-to-HS transition, the transmitter sends HS Zeros (V(Dn)>V(Dp)) for a specified amount of time to make sure that the receiver is enabled properly before any payload data is transmitted.

Before the payload data of every HS burst on each lane, the transmitting D-PHY inserts a sync sequence (00011101). This sync sequence is used by the data lanes of the receiving D-PHY to establish synchronization with the high-speed payload data.

The LP11 state brings back the data lane from high-speed mode to low-power mode.

After every HS burst, the data lanes go to LP11 state. A single HS burst represents the image data corresponding to one of the horizontal lines of an image and the LP11 state in between the HS bursts represent the blanking periods.

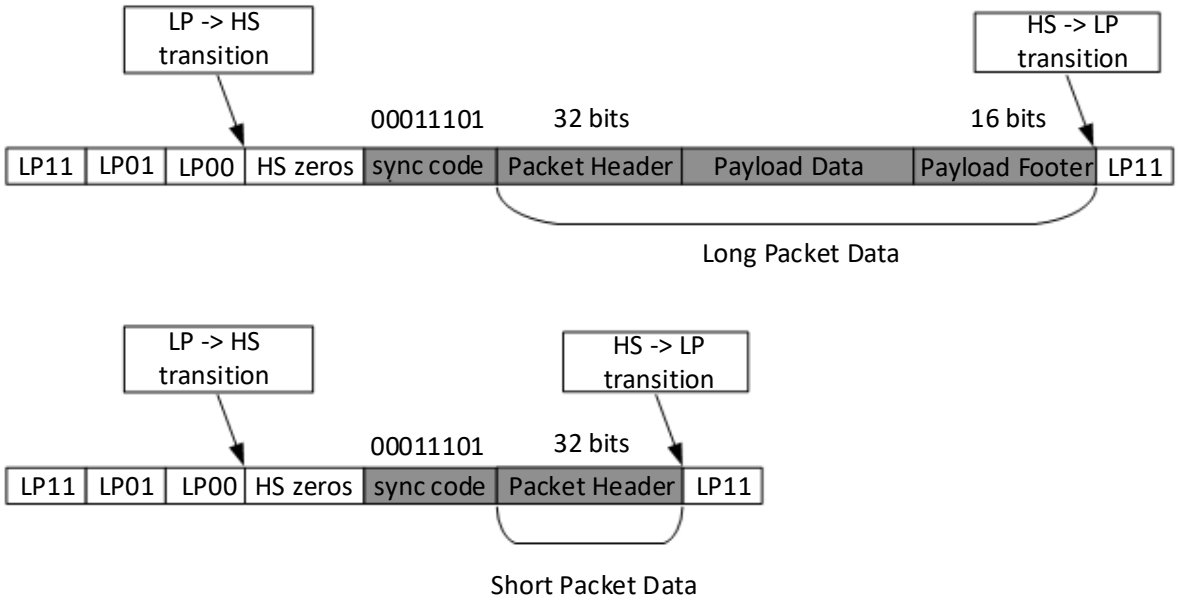

Figure 2.2. High-Speed Entry Sequence and Payload Data Transmission Cycle on Data Lanes

2.2. Signal Description

A list of input and output signals along with their descriptions is shown in Table 2.1.

Table 2.1. MIPI D-PHY Module Port Descriptions

Port Name	Direction	Mode/Configuration	Description
Clock and Reset			
clk_byte_o	Out	—	Byte clock
sync_clk_i	In	—	GDDR SYNC reference clock
clk_p_io, clk_n_io	In/Out	—	MIPI D-PHY clock lane
lp_tx_clk_p_i	In	Available when Interface Type is *Transmit*.	Low-power transmit positive lane clock
lp_tx_clk_n_i	In	Available when Interface Type is *Transmit*.	Low-power transmit negative lane clock
sync_rst_i	In	—	GDDR SYNC reset
MIPI D-PHY High-Speed Tx			
hs_tx_en_i	In	Available when Interface Type is *Transmit*.	High-speed transmit mode data enable
hs_tx_data_i[DW[1]-1:0]	In	Available when Interface Type is *Transmit*.	High-speed transmit data
hs_tx_clk_en_i	In	Available when Interface Type is *Transmit*.	High-speed transmit mode clock enable
MIPI D-PHY High-Speed Rx			
hs_rx_en_i	In	Available when Interface Type is in *Receive*.	High-speed receive mode enable
hs_tx_cil_ready_o[NUM_of_LANES – 1:0]	Out	Available when Interface Type is *Transmit* and *DPHY Mode* = *CIL Bypassed*	This active high signal indicates that TxDataHS is accepted by the corresponding lane to be serially transmitted.
data_lane_ss_o[NUM_of_LANES – 1:0]	Out	Available when Interface Type is *Receive* and *DPHY Mode* = *CIL Bypassed*	This active high signal indicates that the corresponding lane is currently in Stop state.
MIPI D-PHY Low Power Tx			
lp_tx_data_p_i[BUS_WIDTH – 1:0]	In	Available when Interface Type is *Transmit*.	Low-power transmit positive data lane
lp_tx_data_n_i[BUS_WIDTH – 1:0]	In	Available when Interface Type is *Transmit*.	Low-power transmit negative data lane
lp_tx_data_en_i	In	Available when Interface Type is *Transmit*.	Low-power transmit data enable
lp_tx_en_i	In	Available when Interface Type is *Transmit*.	Low-power transmit enable
MIPI D-PHY Low Power Rx			
lp_rx_en_i	In	Available when Interface Type is *Receive*.	Low-power receive mode enable
lp_rx_clk_p_o	Out	Available when Interface Type is *Receive*.	Low-power receive positive lane clock
lp_rx_clk_n_o	Out	Available when Interface Type is *Receive*.	Low-power receive positive lane clock
lp_rx_data_p_o[BUS_WIDTH – 1:0]	Out	Available when Interface Type is *Receive*.	Low-power receive data positive
lp_rx_data_n_o[BUS_WIDTH – 1:0]	Out	Available when Interface Type is *Receive*.	Low-power receive data negative

Port Name	Direction	Mode/Configuration	Description
MIPI DPHY			
data_p_io[NUM_of_LANES – 1:0], data_n_io[NUM_of_LANES – 1:0]	In/Out	—	MIPI D-PHY data lanes
Misc			
pll_clkop_i	In	Available when Interface Type is *Transmit* and DPHY PLL Mode is *External*.	Input clock from external PLL
pll_clkos_i	In	Available when Interface Type is *Transmit* and DPHY PLL Mode is *External*.	90-degree shifted input clock from external PLL
pll_lock_i	In	Available when Interface Type is *Transmit* and DPHY PLL Mode is *External* or Interface Type is *Receive*.	Lock signal from external PLL
ready_o	Out	—	Ready from DPHY or PLL

Notes:

- DW = BUS_WIDTH* GEAR
- BUS_WIDTH – Number of D-PHY Lanes, 1, 2, 4, available on the user interface.
- GEAR – Number of bits to be transferred

2.3. Attribute Summary

MIPI D-PHY module configuration attributes summary is shown in Table 2.2.

Table 2.3 shows the attributes description.
All attributes can be configured from the General tab of the Lattice Radiant™ software user interface.

Table 2.2. Attributes Table

Attribute	Selectable Values	Value Entry Format	Defaults	Dependency on Other Attributes	Additional Requirements
Interface Type	Transmit, Receive	Pull-down Menu	Receive	—	—
MIPI Interface Application	CSI2, DSI	Pull-down Menu	CSI2	—	—
DPHY Module Type	Soft MIPI DPHY	Pull-down Menu	Soft MIPI DPHY	—	—
DPHY PLL Mode	Internal, External	Pull-down Menu	External	*Interface Type* = Transmit	—
Interface Clock Frequency (MHz)	40–750	Real Number Field	160 MHz	*DPHY Module Type* = Soft MIPI DPHY For CSFBGA121, FFG672, and LFG672 packages, 40–750 MHz Other available packages, 40 – 625 MHz	—
Interface Data Rate (Mbps)	80–1500	Calculated	320 Mbps	*DPHY Module Type* = Soft MIPI DPHY For the LFG672 package, 80–1500 Mbps Other available packages, 80–1250 Mbps	Display for information only
Gearing Ratio	1:8	Pull-down Menu	1:8	*Interface Type* = Receive	—
	8:1			*Interface Type* = Transmit	
Bus Width	1, 2, 4	Integer Field	1	—	—

Attribute	Selectable Values	Value Entry Format	Defaults	Dependency on Other Attributes	Additional Requirements
Reference Clock Frequency (MHz)	24–200	Integer Field	24	*Interface Type* = Transmit	—

Table 2.3. Attributes Description

Attributes	Description
Interface Type	Selects interface type as Receive or Transmit.
MIPI Interface Application	Protocol or application to be interfaced with MIPI DPHY
DPHY Module Type	Selects DPHY module implementation.
DPHY PLL Mode	Selects using Lattice PLL Soft IP or external PLL.
Interface Clock Frequency (MHz)	MIPI interface input clock frequency
Interface Data Rate (Mbps)	Data rate to be used by MIPI DPHY interface
Gearing Ratio	Selects gearing ratio.
Bus Width	Total number of data lanes
Reference Clock Frequency (MHz)	PLL input clock frequency

3. IP Generation, Simulation, and Validation

This section provides information on how to generate the IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant software user guide.

3.1. Generating the IP

The Lattice Radiant software allows you to customize and generate modules and IPs and integrate them into the device architecture.

To generate MIPI D-PHY Module in Lattice Radiant software:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **MIPI_DPHY** under **Module, Architecture_Modules, IO** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

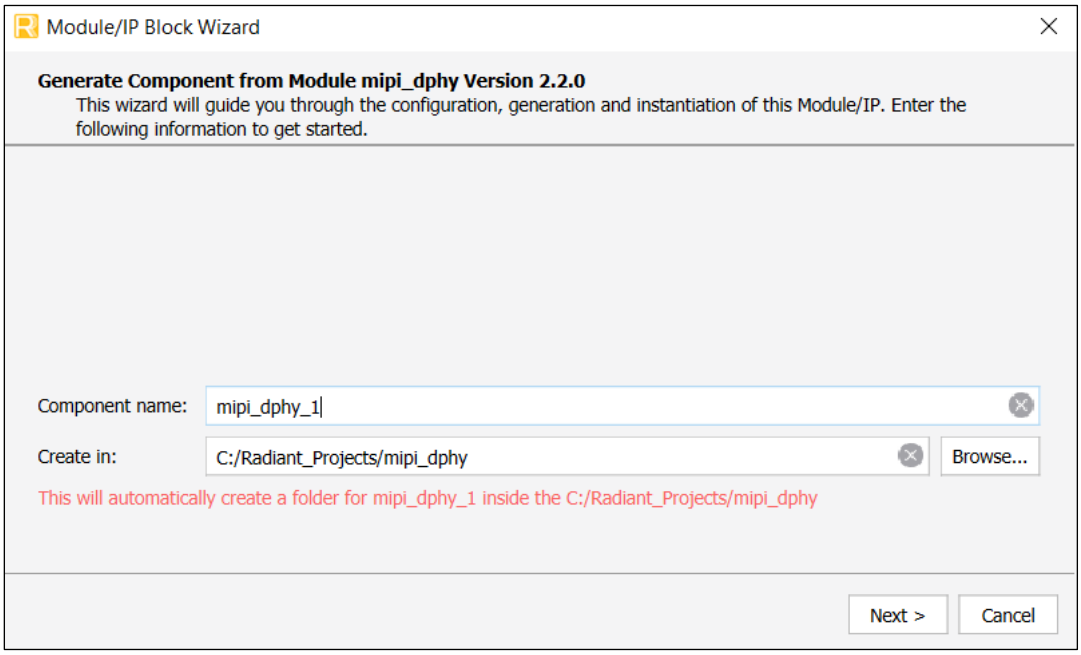

Figure 3.1. Module/IP Block Wizard

3. In the module dialog box of the **Module/IP Block Wizard** window, customize the selected MIPI D-PHY Module using drop-down menus and checkboxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

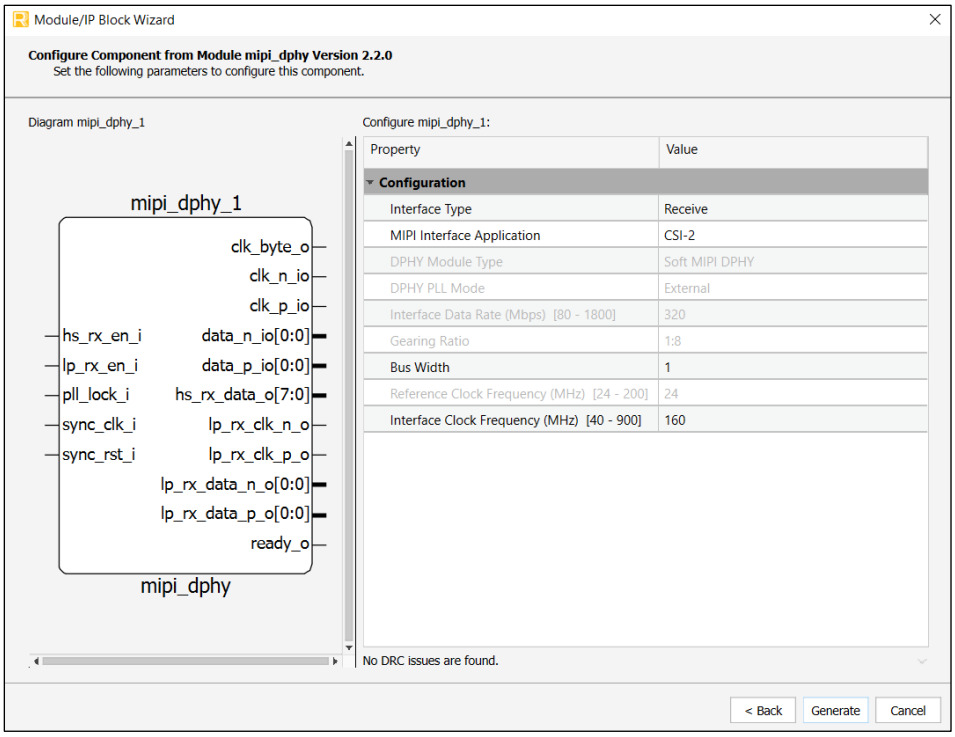

Figure 3.2. Configure Block of MIPI D-PHY Module

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results, as shown in Figure 3.3.

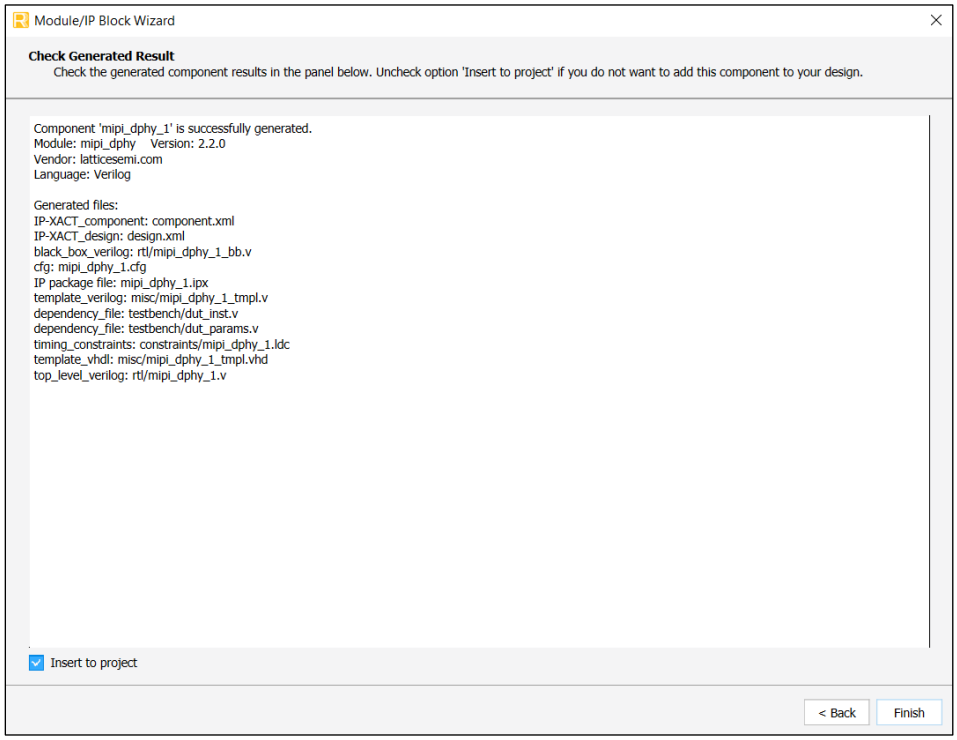

Figure 3.3. Check Generated Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields are shown in Figure 3.1.

The generated MIPI D-PHY module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated with the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
eval/constraints.pdc	IP constraint file
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.2. Running Functional Simulation

After the IP is generated, functional simulation can be performed using different simulators available. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator, however, may require additional steps.

To run the functional simulation using the default simulator:

1. Click the  icon located on the toolbar to initiate Simulation Wizard, as shown in Figure 3.4.

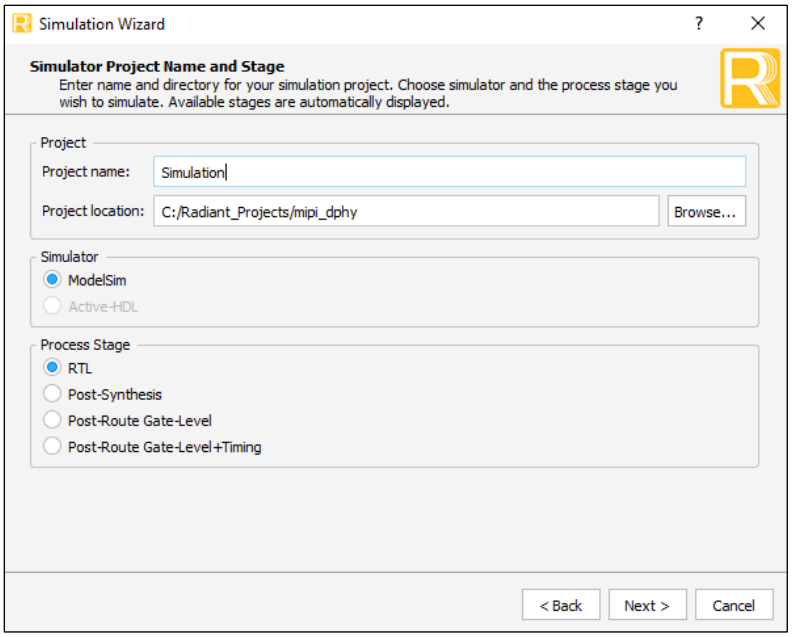

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

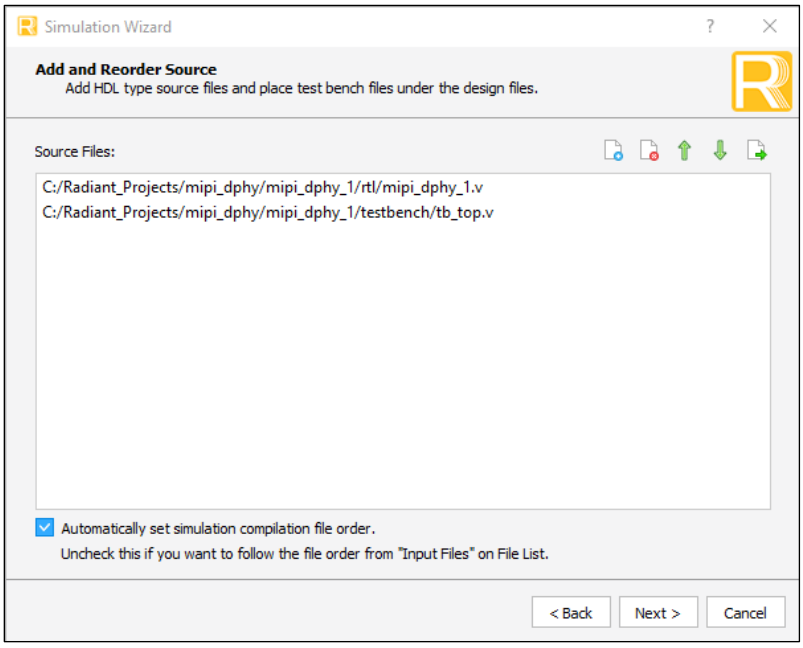

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The Summary window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software Suite.

The results of the simulation in our example are provided in Figure 3.6.

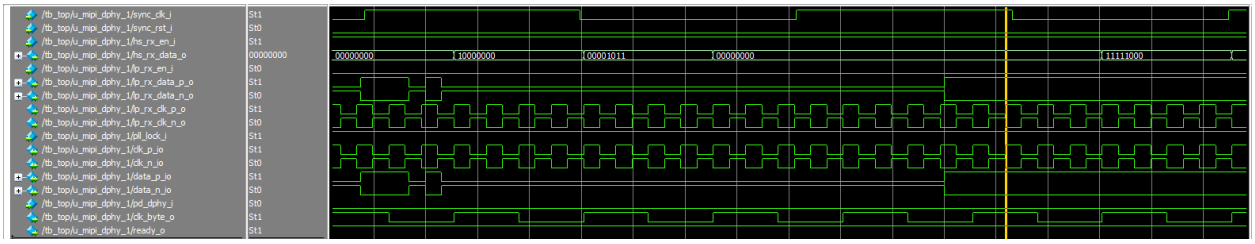

Figure 3.6. Simulation Waveform

3.3. Constraining the IP

It is the responsibility of the user to provide proper timing and physical design constraints to ensure that the design meets the desired performance goals on the FPGA. The content of the following IP constraint file can be added to the user design constraints:

<IP_Instance_Path>/<IP_Instance_Name>/eval/constraints.pdc.

The above constraint file has been verified during IP evaluation with the IP instantiated directly in the top-level module. The constraint in this file can be modified given a complete understanding of the effect of the constraint.

To use this constraint file, copy the content of constraints.pdc to the top-level design constraint for post-synthesis.

Refer to Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059) for details on how to constraint the design.

3.4. IP Evaluation

There is no restriction on the IP evaluation of this module.

Appendix A. Resource Utilization

MIPI D-PHY module resource utilization are shown on Table A.1 and Table A.2 using LAV-AT-E70-3LFG1156I and LAV-AT-E70-1LFG1156I devices with Synplify Pro of Lattice Radiant software. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization using LAV-AT-E70-3LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Default	225	10	32	0	0
Receive, DSI MIPI Interface Application, four data lanes, others are default	225	10	32	0	0
Transmit, Internal DPHY PLL, 200 MHz Reference Clock, 900 MHz Interface Clock, others are default	225	11	33	0	0
Transmit, DSI MIPI Interface, Internal DPHY PLL, four data lanes, 200 MHz Reference Clock, 900 MHz Interface Clock, others are default	225	11	35	0	0

Notes:

1. Fmax is generated when the FPGA design only contains the MIPI D-PHY module and the target frequency is 225 MHz. MIPI DPHY module supports up to 900 MHz ECLK and 225 MHz SCLK. These values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.

Table A.2. Resource Utilization using LAV-AT-E70-1LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Default	225	10	32	0	0
Receive, DSI MIPI Interface Application, four data lanes, others are default	225	10	32	0	0
Transmit, Internal DPHY PLL, 200 MHz Reference Clock, 900 MHz Interface Clock, others are default	225	11	33	0	0
Transmit, DSI MIPI Interface, Internal DPHY PLL, four data lanes, 32 MHz Reference Clock, others are default	225	11	35	0	0

Notes:

1. Fmax is generated when the FPGA design only contains the MIPI D-PHY module and the target frequency is 225 MHz. MIPI DPHY module supports up to 900 MHz ECLK and 225 MHz SCLK. These values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic, distributed RAM*, and *ripple logic*.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow, and Tasks, as well as on the Simulation Flow, see the Lattice Radiant software user guide.

For more information, refer to:

- Lattice Avant-E Family Devices Web Page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

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For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, December 2023

Section	Change Summary
All	Changed the document title from *Avant MIPI D-PHY Module – Lattice Radiant Software* to *Avant MIPI D-PHY Module*.
Disclaimers	Updated this section.
Inclusive Language	Newly added this section.
IP Generation, Simulation, and Validation	• Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure Block of MIPI D-PHY Module, and Figure 3.3. Check Generated Result. • Newly added the *eval/constraints.pdc* Attribute in Table 3.1. Generated File List. • Newly added the Constraining the IP section.

Resource Utilization	• Changed the part number *LAV-AT-500E-3LFG1156I* to *LAV-AT-E70-3LFG1156I*.
	• Changed the part number *LAV-AT-500E-1LFG1156I* to *LAV-AT-E70-1LFG1156I*.
	• In Table A.1. Resource Utilization using LAV-AT-E70-3LFG1156I, changed LUTs value from *31* to *32* for the following two Configurations:
	  • default;
	  • receive, DSI MIPI Interface Application, four data lanes, others are default.
	• In Table A.2. Resource Utilization using LAV-AT-E70-1LFG1156I, changed LUTs value from *31* to *32* for the following two Configurations:
	  • default;
	  • receive, DSI MIPI Interface Application, four data lanes, others are default.

References	Newly added links to Avant-E Family Devices Web Page and Lattice Insights for Lattice Semiconductor training courses and learning plans.
Technical Support Assistance	Newly added the link to Lattice Answer Database.

Revision 1.0, November 2022

Section	Change Summary
Functional Description	Removed the signals pd_dphy_i and hs_tx_data_en_i from Table 2.1.
IP Generation, Simulation, and Validation	• Revised the title from 'IP Generation and Evaluation' to 'IP Generation, Simulation, and Validation' • Deleted the section 'Licensing the IP' • Revised the title of section 3.1 from 'Generation and Synthesis' to 'Generating the IP' • Revised the figures Figure 3.1, Figure 3.2, and Figure 3.3 • Revised the title of section 3.3 from 'Hardware Evaluation' to 'IP Evaluation'
Appendix A. Resource Utilization	Added Appendix A. Resource Utilization section

Revision 0.80, May 2022

Section	Change Summary
All	Initial release.

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