DDR Memory PHY Module

IP Version: v2.5.0

User Guide

FPGA-IPUG-02195-1.4

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
APB	Advanced Peripheral Bus
AXI4	Advanced eXtensible Interface 4
BL	Burst Length
BLTS	Bit-Level Trim Sweep
CA	Command and Address
CS	Chip Select
CBT	Command Bus Training
DBI	Data Bus Inversion
DDR	Double Data Rate
DDRPHY	DDR Physical Layer
DFI	DDR PHY Interface
DM	Data Mask
DQ	Data
DQS	Data Strobe
ECC	Error Correction Code
ECLK	Edge Clock
FPGA	Field Programmable Gate Array
HPIO	High Performance I/O
I/F	Interface
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate Generation 4
LVSTL	Low Voltage Swing Terminated Logic
MC	Memory Controller
MR	Mode Register
MRS	Mode Register Set
ODT	On-Die Termination
PRBS	Pseudorandom Binary Sequence
PVT	Process, Voltage, and Temperature
RTL	Register Transfer Level
SCL	Self-Calibration Logic
SCLK	System Clock
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SSN	Simultaneous Switching Noise
TCL	Tool Command Language
VREF	Voltage Reference

1. Introduction

The Lattice Semiconductor DDR Memory PHY Module for Avant and Nexus 2 Devices implements the DFI 4.0 Specification (© Cadence Design Systems, Inc.). The DDRPHY IP Module is a hardened block in Lattice Avant and Nexus 2 devices that describes the interoperation between a Memory Controller and Physical Interface (PHY). The DDRPHY IP Module provides training and clocking control for the following SDRAM protocols: DDR4 and LPDDR4. The IP Module is implemented in System Verilog HDL using the Lattice Radiant™ software integrated with the Lattice Synthesis Engine (LSE) and Synplify Pro® synthesis tools.

1.1. Quick Facts

Table 1.1 presents a summary of the DDRPHY IP Module.

Table 1.1. Quick Facts

IP Requirements	Supported Devices	DDR4 mode – Lattice Avant, Certus-N2 LPDDR4 mode – Lattice Avant, Certus-N2
	IP Changes[1]	For a list of changes to the IP, refer to the DDR Memory PHY IP Release Notes (FPGA-RN-02072)
Resource Utilization	Supported User Interfaces	DFI for PHY access APB for configuration access
	Resources	Refer to Appendix A. Resource Utilization Table A.1 and Table A.2
Design Tool Support	Lattice Implementation[2]	IP Core v2.5.0 - Lattice Radiant software 2025.2
	Synthesis	Lattice Synthesis Engine Synopsys® Synplify Pro for Lattice
	Simulation	For a list of supported simulators, refer to the Lattice Radiant Software User Guide

Notes:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.
2. Lattice Implementation indicates the IP version release coinciding with the software version release. Check the software for IP version compatibility with earlier or later software versions.

1.2. Features

The DDRPHY IP Module supports the following key features for DDR4 and LPDDR4 SDRAM.

1.2.1. DDR4

The DDRPHY Module, when configured in DDR4 mode, supports the following key features for Avant and Nexus 2 devices:

- DDR4 SDRAM protocol, compliant to DDR4 JEDEC Standard
  - DDR4 SDRAM speeds ranging from 350 MHz to 1,200 MHz (700 Mbps to 2,400 Mbps)
- Memory Interface features:
  - Interface data widths of x16, x32, and x64
  - Interface data widths of x40 and x72 are also supported when Sideband ECC is enabled
  - x8 and x16 DDR4 device support (8:1 DQ:DQS ratio)
  - Configurable CAS latencies for Reads and Writes based on target interface speed
  - 8:1 gearing mode (4:1 DDR4-to-FPGA clock frequency ratio)
- Supports component (DRAM soldered on the board) and UDIMM
- Memory Training features:
  - Automatic DDR4 initialization

- Write Leveling
- Read Training
- Write Training
- Self-Calibrating Logic

- Includes dedicated PLL for clock generation

Table 1.2. DDR4 Features Overview

Key Features	DDR4 Support Details
Device Format	Component, DIMM not yet supported
Data Widths	x16, x32, x40, x64, x72
PHY Interface	DFI
Configuration Interface	APB
Maximum Data Rate	Refer to Table 1.6 and Table 1.7
Other Features[1]	
Error Correction Code (ECC)	Yes
Dual-rank	Yes
Data Bus Inversion (DBI)	Not yet supported, for reads, No for writes
On-Die Termination (ODT)	Yes, for DQ, No for CA
Bit Swizzle	Not yet supported
Training[1]	
Initialization	Yes
CS Training	Not yet supported
Write Leveling	Yes
Read Training	Yes
Write Training	Yes
Automatic VREF Training	Not yet supported
Self-Calibrating Logic	Yes
Bit-Level Trim Sweep	Not yet supported
2-D Vref Training	Not yet supported

Note:

1. *Yes* implies that a configurable option exists to enable or disable the feature. *No* implies that the feature is currently not supported and will not be supported in the future.

1.2.2. LPDDR4

The DDRPHY Module, when configured in LPDDR4 mode, supports the following key features for Avant and Nexus 2 Devices:

- LPDDR4 SDRAM protocol, compliant to LPDDR4 JEDEC Standard
  - LPDDR4 SDRAM speeds ranging from 350 MHz to 1,200 MHz (700 Mbps to 2,400 Mbps)
- Memory Interface features:
  - Interface data widths of x16, x32, and x64
  - 8:1 gearing mode (4:1 LPDDR4-to-FPGA clock frequency ratio)
- Memory Training features:
  - Automatic LPDDR4 initialization
  - Command Bus Training
  - Write Leveling
  - Read Training
  - Write Training
  - VREF Training
  - Self-Calibrating Logic
  - Bit-Level Trim Sweep

  - 2-D Vref Training
- Includes internal programmable VREF
- Includes dedicated PLL for clock generation
- Bit Swizzle (DQ bit swizzle within the DQS group)

Table 1.3. LPDDR4 Features Overview

Key Features	LPDDR4 Support Details
Device Format	Component
Data Widths	x16, x32, x64
PHY Interface	DFI
Configuration Interface	APB
Maximum Data Rate	Refer to Table 1.6 and Table 1.7
Other Features[1]	
Dual-rank	Yes
Data Bus Inversion (DBI)	Yes, for reads, No for writes
On-Die Termination (ODT)	Yes for DQ and CA
Bit Swizzle	Yes for DQ, Not yet supported for CA and DQS Group
Training[1]	
Initialization	Yes
Command Bus Training	Yes
Write Leveling	Yes
Read Training	Yes
Write Training	Yes
Automatic VREF Training	Yes
Self-Calibrating Logic	Yes
Bit-Level Trim Sweep	Yes
2-D Vref Training	Yes

Note:

1. *Yes* implies that a configurable option exists to enable or disable the feature. *No* implies that the feature is currently not supported and will not be supported in the future.

1.3. IP Validation Summary

The DDRPHY IP Module supports Avant-AT-E, Avant-AT-G, Avant-AT-X, and Nexus 2 devices. Table 1.4 and Table 1.5 summarize the compilation, simulation, and hardware validation for the DDRPHY IP.

Table 1.4. Avant IP Validation Summary

Device/Mode	Compilation	Simulation	Hardware
DDR4			
Avant-AT-E	Yes	Yes	No
Avant-AT-G	Yes	Yes	No
Avant-AT-X	Yes	Yes	No
LPDDR4			
Avant-AT-E	Yes	Yes	Yes[1, 3]
Avant-AT-G	Yes	Yes	Yes[1, 2, 3]
Avant-AT-X	Yes	Yes	Yes[1, 2, 3]

Notes:

1. Supports x16 and x32 data widths only. The data width of x64 is not hardware validated.
2. Supports up to 1,066 MHz only. 1,200 MHz is not yet hardware validated.
3. Supports single rank only. Dual rank is not yet hardware validated.

Table 1.5. Nexus 2 IP Validation Summary

Device/Mode[1]	Compilation	Simulation	Hardware
DDR4			
Nexus 2	Yes	Yes	No
LPDDR4			
Nexus 2	Yes	Yes	No

Note:

1. Nexus 2 supports only DDR4 and LPDDR4 interfaces.

1.4. Licensing and Ordering Information

The DDRPHY IP is provided at no additional cost with the Lattice Radiant software.

1.5. Minimum Device Requirements

The DDRPHY IP Module supports Avant E/G/X and Nexus 2 devices. Table 1.6 and Table 1.7 summarize the minimum device requirements for the DDRPHY IP Module.

Table 1.6. Avant Minimum Device Requirements

Device/Mode	DDR Data Width	DDR Ranks	Maximum Interface Speed	Supported Speed Grades
DDR4				
Avant-AT-E/G/X	x16, x32, x40, x64, x72	1	933 MHz (1,866 Mbps)	1, 2, 3
Avant-AT-E/G/X	x16, x32, x40, x64, x72	1, 2	1,066 MHz (2,133 Mbps)	2, 3
Avant-AT-E/G/X	x16, x32, x40, x64, x72	1	1,200 MHz (2,400 Mbps)	3
LPDDR4				
Avant-AT-E/G/X	x16, x32, x40, x64, x72	1	933 MHz (1,866 Mbps)	1, 2, 3
Avant-AT-E/G/X	x16, x32, x40, x64, x72	1, 2	1,066 MHz (2,133 Mbps)	2, 3
Avant-AT-E/G/X	x16, x32, x40, x64, x72	1	1,200 MHz (2,400 Mbps)	3

Table 1.7. Nexus 2 Minimum Device Requirements

Device/Mode	DDR Data Width	DDR Ranks	Maximum Interface Speed	Supported Speed Grades
DDR4				
Nexus 2	x16, x32, x40	1	933 MHz (1,866 Mbps)	1, 2, 3
Nexus 2	x16, x32, x40	1, 2	1,066 MHz (2,133 Mbps)	2, 3
Nexus 2	x16, x32, x40	1	1,200 MHz (2,400 Mbps)	3
LPDDR4				
Nexus 2	x16, x32, x40	1	933 MHz (1,866 Mbps)	1, 2, 3
Nexus 2	x16, x32, x40	1, 2	1066 MHz (2,133 Mbps)	2, 3
Nexus 2	x16, x32, x40	1	1200 MHz (2,400 Mbps)	3

1.6. Naming Conventions

This section provides information regarding terminology used within this document.

1.6.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.6.2. Signal Names

Signal Names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

2. Functional Description

This section provides a detailed functional description of the DDRPHY IP Module, including information regarding clock and reset handling, available user data and configuration interfaces, the calibration sequence, and operation descriptions.

2.1. IP Architecture

The DDRPHY Module consists of three main blocks: the DDRPHY Software Primitive, the DDRPHY Hard IP, and the Training Engine. Figure 2.1 shows the DDRPHY Module sub-blocks and their connectivity.

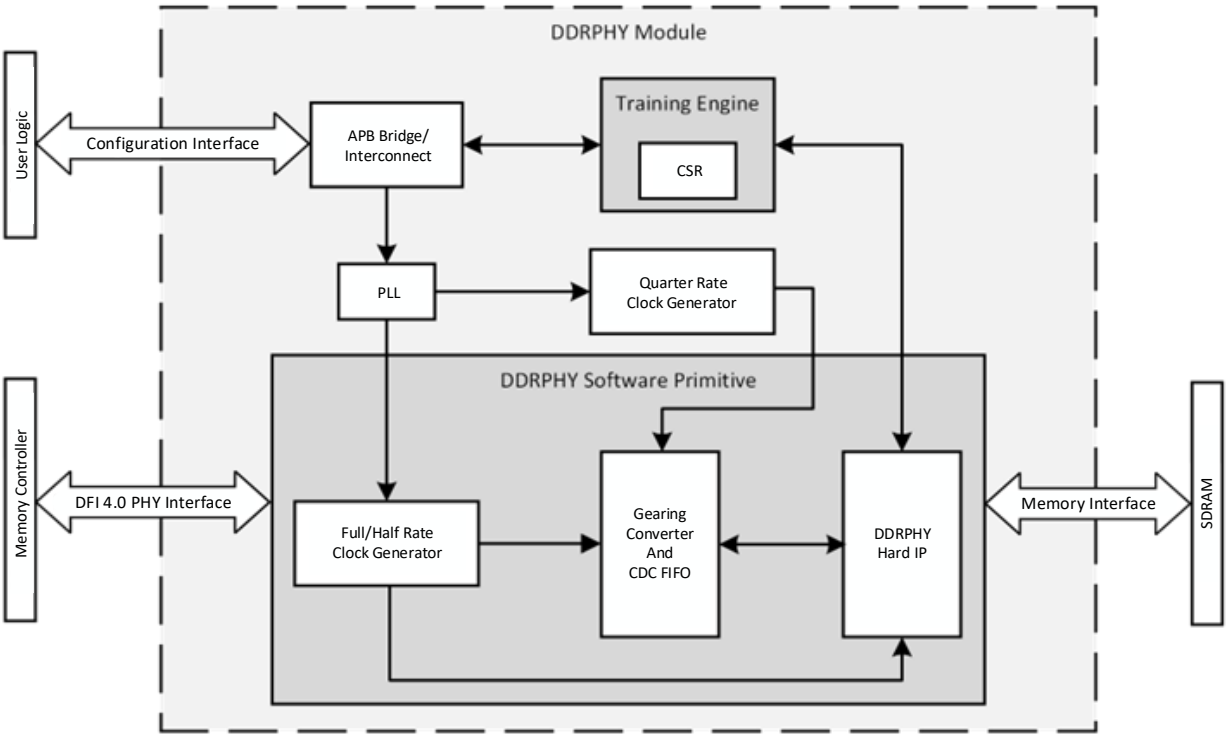

Figure 2.1. DDRPHY IP Module Functional Diagram

The configuration interface provides access to the Training Engine and the Configuration Set Registers (CSRs), which configure the DDRPHY and perform the DDR4 and LPDDR4 training sequences. The PHY interface allows users to initiate command, address, control, and read/write operations via a memory controller to the external DDR4/LPDDR4 SDRAM. The memory interface enables the selected Lattice FPGA to communicate with the external DDR4/LPDDR4 memory. For more information on the PHY and configuration interfaces, refer to the User Interfaces section of this User Guide.

2.1.1. Hardened DDRPHY Software Primitive

The Hardened DDRPHY consists of the following submodules:

- Full/Half Rate Clock Generator
- Gearing Converter and CDC FIFO
- DDRPHY Hard IP

2.1.1.1. Full/Half Rate Clock Generator

The DDRPHY Software Primitive contains a full-rate and half-rate clock generator, which utilizes dedicated PLLs and clock routing to enable high-frequency operation. The PLL provides a full-rate clock (ECLK) to the Hard IP and the half-rate clock (SCLK) to the Hard IP, and Gearing Converter, and CDC FIFO.

2.1.1.2. Gearing Converter and Clock Domain Crossing FIFO

The DDRPHY Hard IP implements a frequency ratio of 1:2 (4:1 gearing). The gearing converter and CDC FIFO convert this to a frequency ratio of 1:4 (8:1 gearing). The gearing converter implements 2:1 and 1:2 gearing to allow DFI signals to run at half-rate. The CDC FIFO ensures signal integrity when transferring data to and from FPGA fabric.

2.1.2. Hardened DDRPHY IP

The DDRPHY Hard IP implements the DFI 4.0 Standard. It connects to High Performance I/O (HPIO) to support high-frequency operation and allow reuse of FPGA I/O for other functions when the DDRPHY Hard IP is not utilizing the I/O. The DDRPHY Hard IP translates the PHY interface signals (DFI) from the fabric to memory interface signals for DDR4/LPDDR4 SDRAM.

2.1.3. Soft Training Engine

The Training Engine reads instructions from system memory and initializes and trains the external DDR4/LPDDR4 memory. It achieves this by accessing the Configuration Set Registers of the DDRPHY Module, PLL, and DDRPHY Hard IP. You issue commands to the Training Engine to perform reads and writes to these registers, allowing them to handle interrupts and obtain details during the memory training sequence.

2.2. Clocking

The DDRPHY IP Module, when configured for DDR4 and LPDDR4 interfaces, requires a differential input reference clock: pll_refclk_i. You need to provide this clock via an external source, an internal oscillator, or a dedicated PLL. This clock routes through a dedicated PLL within the DDRPHY IP to generate the Edge Clock (ECLK) and System Clock (SCLK). The ECLK signal clocks the I/O modules internally within the IP Core, and SCLK clocks the IP Core. The Primary Clock (PCLK) signal implements clock synchronization logic to synchronize SCLK and ECLK.

The DFI interface for the DDRPHY Module operates off the sclk_o signal and resets via the dfi_reset_n_i signal. The configuration interface for the DDRPHY IP Module operates off the pclk_i signal and resets via the preset_n_i signal. The clock for the configuration interface is the same one that implements clock synchronization for SCLK and ECLK. Refer to the Clock and Reset Signal Description section of this user guide for information regarding the clocks and resets for DDR4 and LPDDR4 memory interfaces.

2.3. Reset

The DDRPHY IP Module contains an asynchronous active high reset: rst_i. This signal requires a minimum pulse width of 2× the pclk_i period. When asserted, the external SDRAM resets to its default value. The DDRPHY Module contains internal logic that synchronously de-asserts the internal reset once rst_i is de-asserted, so you do not need to worry about implementing their own de-assertion logic.

The preset_n_i signal is an asynchronous active low reset, which you must ensure is synchronously de-asserted to pclk_i. Refer to the Clock and Reset Signal Description section of this user guide for information regarding the clocks and resets for DDR4 and LPDDR4 memory interfaces.

2.4. User Interfaces

This section describes the supported protocols for data and configuration interfaces available to the user and supported by a DDR4/LPDDR4 Memory Controller.

2.4.1. DFI 4.0 PHY Interface

The DFI 4.0 I/F defines how control and data information communicate between a memory controller and PHY. For more information regarding the DFI 4.0 Interface, refer to the DFI 4.0 Specification. The DFI I/F operates off the sclk_o signal and resets via the dfi_reset_n_i signal. Refer to the Clock and Reset Signal Description section of this user guide for more details. For additional information on the available user DFI signals, refer to the DFI 4.0 Interface Signal Description section and the Operation Descriptions section of this user guide.

2.4.2. APB Configuration Interface

The configuration interface allows users to initialize and train the memory interface. The APB I/F is a low-power protocol intended for accessing programmable control registers. It is not pipelined and is a synchronous protocol with a single address bus and two data buses: write and read. The DDRPHY does not support APB write strobe commands. For more information regarding the APB protocol, refer to the AMBA APB Protocol Specification.

The DDRPHY IP Module leverages this protocol to initialize and train the interface between FPGA logic and external SDRAM. The APB I/F operates off the pclk_i signal and resets via the preset_n_i signal. Refer to the Clock and Reset Signal Description section of this user guide for more details.

2.5. Calibration

To ensure proper device functionality, you must initialize and train the external memory. The DDRPHY Module consists of a soft RISC-V CPU located inside the Training Engine that executes the initialization and training routines for DDR4 and LPDDR4. Table 2.1 summarizes the calibration or training stages supported for each memory protocol by the DDRPHY IP.

Table 2.1. Calibration Summary

	Command Bus Training	Write Leveling	Read Training	Write Training	VREF Training	Self-Calibrating Logic	Bit-Level Trim Sweep	2-D Vref Training
DDR4	No	Yes	Yes	Yes	Yes	Yes	Not Yet Supported	Not Yet Supported
LPDDR4	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

To start the initialization and training sequence for the SDRAM device, you should execute the following steps via the configuration interface:

1. Ensure that the DDRPHY Module's PLL is in the lock state by polling the PHY Clock Register (PHY_CLOCK) until the pll_lock signal asserts (PHY_CLOCK[1]=1).
2. Enable initialization and training by writing to the Training Operation Register (TRN_OP_REG) as follows:
   - For 1,333 Mbps and below, set TRN_OP_REG=0x0DF. This enables initialization, command-bus training, write leveling, read training, write training, and 1D Vref training sequences to run.
   - For 1,600 Mbps and 1,866 Mbps, set TRN_OP_REG=0x1DF to perform bit-level trim sweep in addition to the above.
   - For 2,133 Mbps and 2,400 Mbps, set TRN_OP_REG=0x3DF to perform bit-level trim sweep and 2D Vref training in addition to the above. This is necessary for the two highest data rates.

   For simulation purposes, shorten the initialization and training sequences by writing 0x01C to TRN_OP_REG. For more information, refer to the Register Description section of this user guide.
3. Pull the CPU and Training Engine out of reset by writing 1'b1 to the Reset Register (RESET_REG). This begins the initialization and training sequence.

4. Wait until initialization and training completes using one of the following methods:
   - Poll the Status Register (TRN_STATUS_REG) until the bit_lvl_trim_sweep_done signal asserts (TRN_STATUS_REG[16]=1). This indicates that the bit-level trim sweep has completed, which is the final stage in the initialization and training process.
   - Wait for the trn_done_int signal (INT_STATUS_REG[0]=1) or the trn_error_int signal (INT_STATUS_REG[1]=1) to assert in the Interrupt Status Register (INT_STATUS_REG). This method requires the trn_done_en signal (INT_ENABLE_REG[0]=1) and the trn_err_en signal (INT_ENABLE_REG[1]=1) to be asserted in the Interrupt Enable Register (INT_ENABLE_REG).

After completing the above steps, the DDRPHY Module is ready for DFI access. Once init_done_o asserts, the RISC-V CPU and Training Engine enter reset to save power.

2.5.1. Command Bus Training (CBT)

The goal of Command Bus Training (CBT) is to delay the command and address signals as necessary to optimize the CA window. When setting the cbt_en signal high (TRN_OP_REG[1]=1), the Memory Controller performs CBT according to the DDR4 JEDEC Standard and LPDDR4 JEDEC Standard. This centers the entire CA bus relative to ddr_ck_o by aligning the rising edge of CK to the middle of the CA valid window. The DDR4/LPDDR4 memory then provides feedback to user through the DQ line, which the Memory Controller uses to determine if additional adjustment is required.

During this time, the DDR clock, ddr_ck_o, stops before and after CBT. This is expected as the clock is switches between low frequency (50 MHz) and high frequency (LPDDR4 interface speed) operation, as outlined in the DDR4 JEDEC Standard and LPDDR4 JEDEC Standard. Upon successful completion of CBT, ddr_ca_o centers to the eye of ddr_ck_o, ensuring correct behavior during high frequency operation.

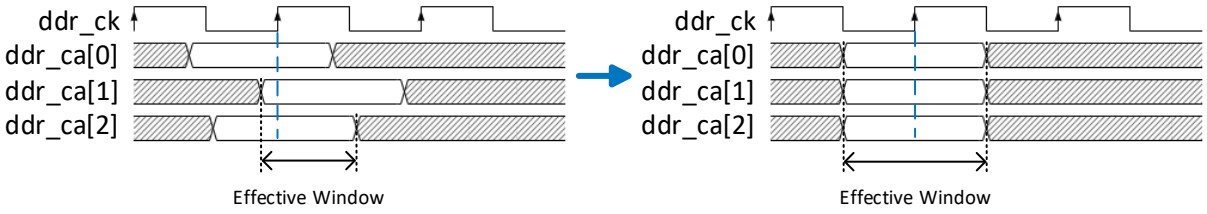

Figure 2.2. Command Bus Training

2.5.2. Write Leveling

The purpose of write leveling is to delay each Data Strobe (DQS) relative to the DDR clock during write operations so they are edge-aligned. This addresses the CK to DQS timing skew introduced with the adoption of Fly-By Topology, which reduces Simultaneous Switching Noise (SSN) by allowing different memory components to receive write commands at different times. Setting the write_lvl_en signal high (TRN_OP_REG[2]=1) enables write leveling on all available ranks. During this process, the ddr_dqs_o signal is delay until a 0-to-1 transition on ddr_ck_o is captured by the dqs rising edge of the SDRAM device. The SDRAM memory then provides feedback of the captured clock signal value through the DQ line to determine if additional adjustment is required.

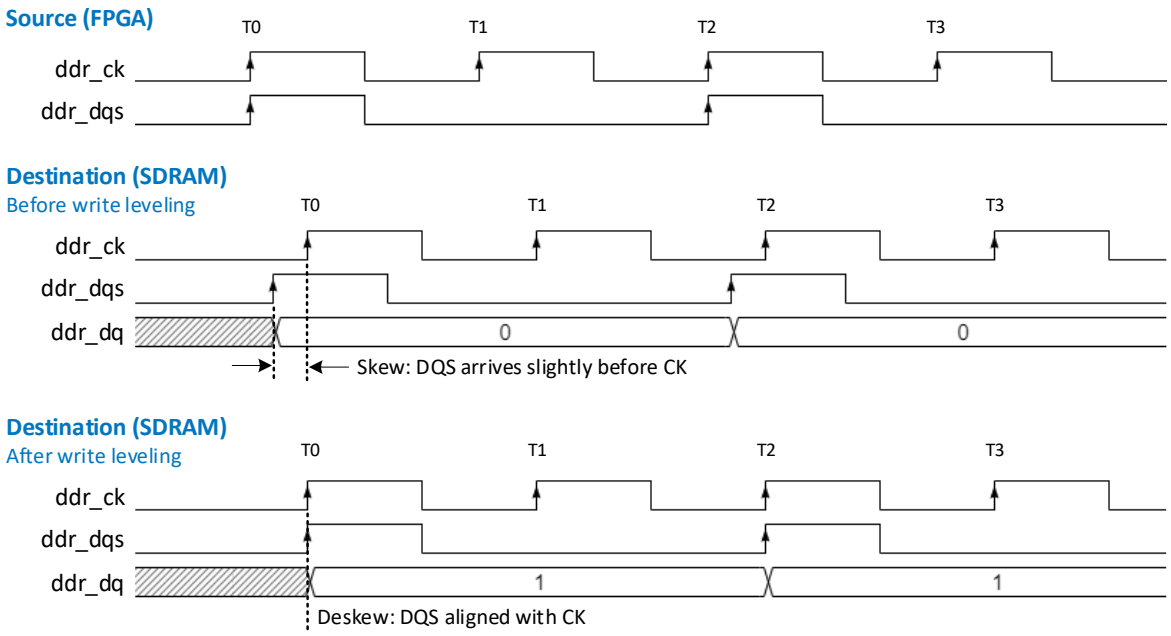

Figure 2.3. Write Leveling

2.5.3. Read Training (Read Bit-Leveling)

The purpose of read training, or read DQ-bit leveling, is to center-align DQS relative to the DQ window. Setting the read_trn_en signal high (TRN_OP_REG[3]=1), enables read training. This compensates for unpredictable delays on DQ which can lead to skew between each input DQ and its respective DQS. During this process, a continuous 1-0-1-0 pattern is read from SDRAM on DQ, where DQS is delayed by 90 degrees. The DQ is then delayed and advanced to capture both edges of ddr_dq_io reading a 0, resulting in the DQ valid window. This indicates how far/close the rising edge of ddr_dqs_io is from ddr_dq_io to determine the amount of delay/advancement needed to align the rising edge of ddr_dqs_io to the ddr_dq_io valid window.

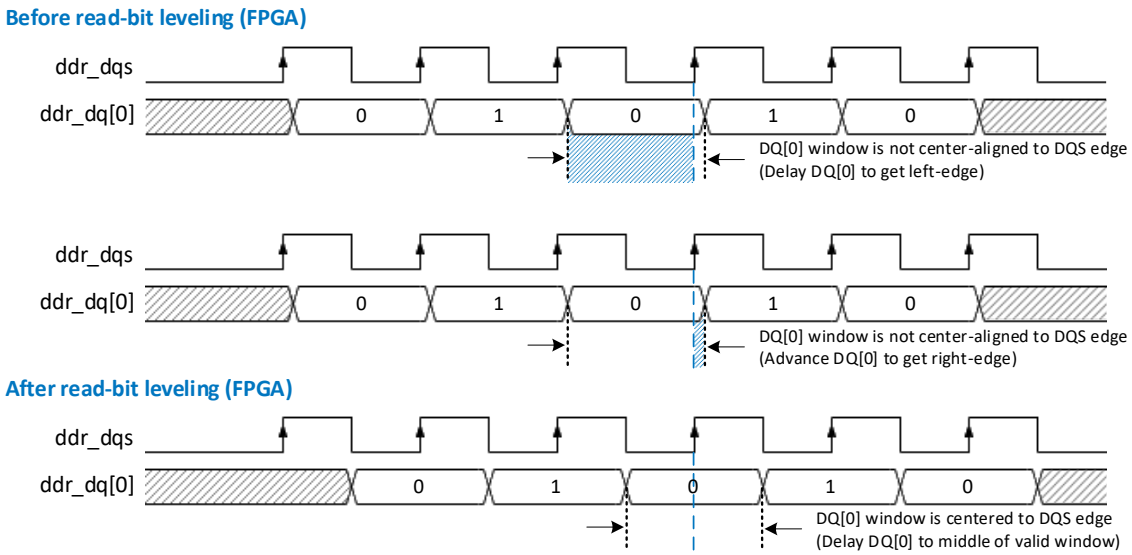

Figure 2.4. Read DQ-Bit Leveling

2.5.3.1. Read Training Limitation for LPDDR4 at 350MHz and 400MHz

Running Read Training at 350MHz and 400MHz (700Mbps and 800Mbps) will cause failure in the DDRPHY Hard IP because the adjustable read delay is less than the DQ period, and thus, the center of the DQ Valid window cannot be found. The Read DQS-DQ path is balanced in the DDRPHY Hard IP and thus, the default value delay value of 0 works at these speeds. The Self-Calibrating Logic (SCL) will confirm that the default read delay is okay. When the SCL passes, the data access will also pass. Because of this, the DDR Memory PHY Module cannot detect failure at Read Training (TRN_STATUS_REG.read_training_err=0) for these speeds even when you force the DQ bits to 0 during simulation. When the DDRPHY Hard IP detects Read Training error at these speeds, it will still be marked as pass (TRN_STATUS_REG.read_training_done=1). The read training error status can properly detect errors at 533MHz and up.

2.5.4. Write Training (Write Bit-Leveling)

The purpose of write training, or write DQ-bit leveling, is to center-align DQS relative to the DQ window. Setting the write_trn_en signal high (TRN_OP_REG[4]=1) enables write training. To achieve alignment, you must write a continuous 1-0-1-0 pattern to SDRAM and read it back to ensure successful writes. During this process, DQ delays and advances to capture both edges of ddr_dq_io successfully writing a 0, resulting in the DQ valid window. This indicates how far/close the rising edge of ddr_dqs_io is from ddr_dq_io to determine the amount of delay/advancement needed to align the rising edge of ddr_dqs_io to the ddr_dq_io valid window.

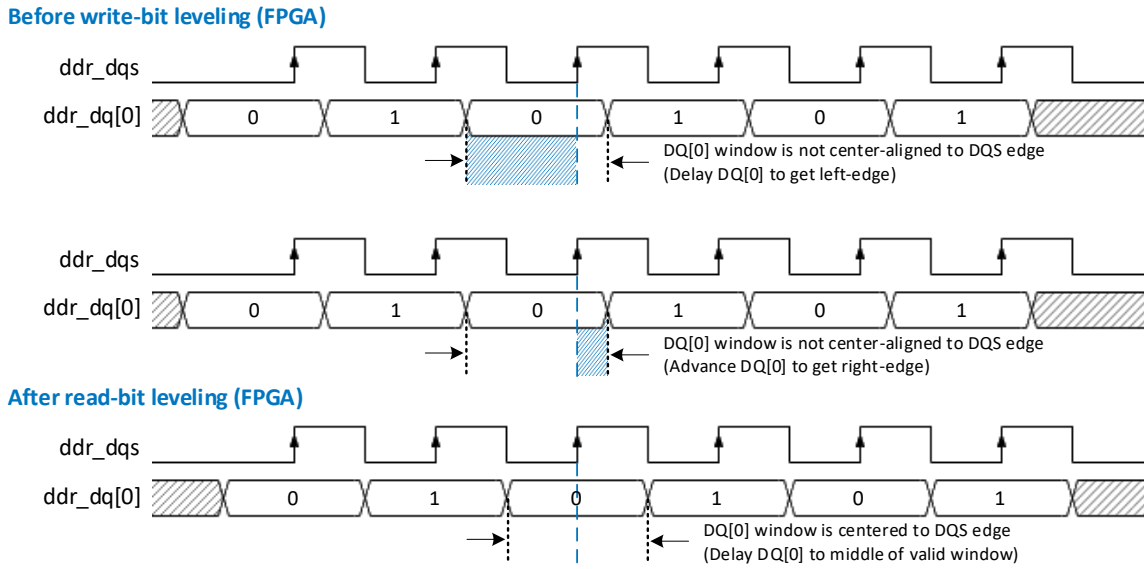

Figure 2.5. Write DQ-Bit Leveling

2.5.5. VREF Training

The goal of VREF training is to provide stable and robust memory access by maximizing margins on command, address, chip select, and data signals. VREF training occurs as part of CBT, read training, and write training. Setting the ca_vref_training_en (TRN_OP_REG[5]=1), mc_vref_training_en (TRN_OP_REG[6]=1), and mem_vref_training_en (TRN_OP_REG[7]=1) signals high enables VREF training during CBT, reading training, and write training.

The voltage reference decides if a signal is registered as high (1) or low (0). Due to PVT variations and ODT drive/impedance matching, the internal voltage reference on DDR4/LPDDR4 can fluctuate, causing the center of the eye to move. VREF training consists of repeating the CBT, read training, and write training steps across different VREF values to find the center of the vertical valid window to maximize margins during operation.

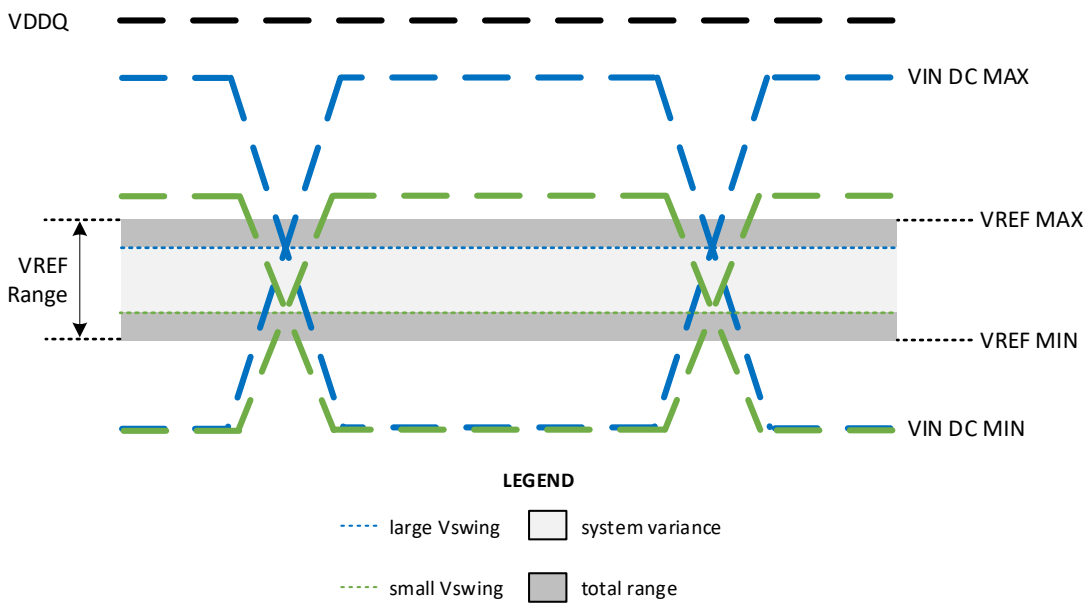

Figure 2.6. VREF Training

2.5.6. Self-Calibrating Logic (SCL)

The purpose of self-calibrating logic is to eliminate any DDR timing issues during DDR4/LPDDR4 read and write operations by performing the following:

- Clock Domain Crossing (CDC)
- Latency Calibration

The goal of SCL CDC is to ensure sufficient margins during read operations by finding the center between the rising edge of ddr_ck_o and the falling edge of the next input ddr_dqs_io. This is achieved by performing 2 writes to SDRAM and then continuously reading data back while performing internal delay adjustments. Figure 2.7 shows the circuit for implementing the read capture logic, where the data_capture_clk is the variable delay clock, which SCL tunes to optimize setup and hold margins when clocking data from the input SDRAM DQS domain (ddr_dqs_io) to the DDRPHY clock domain represented as full_rate_clk.

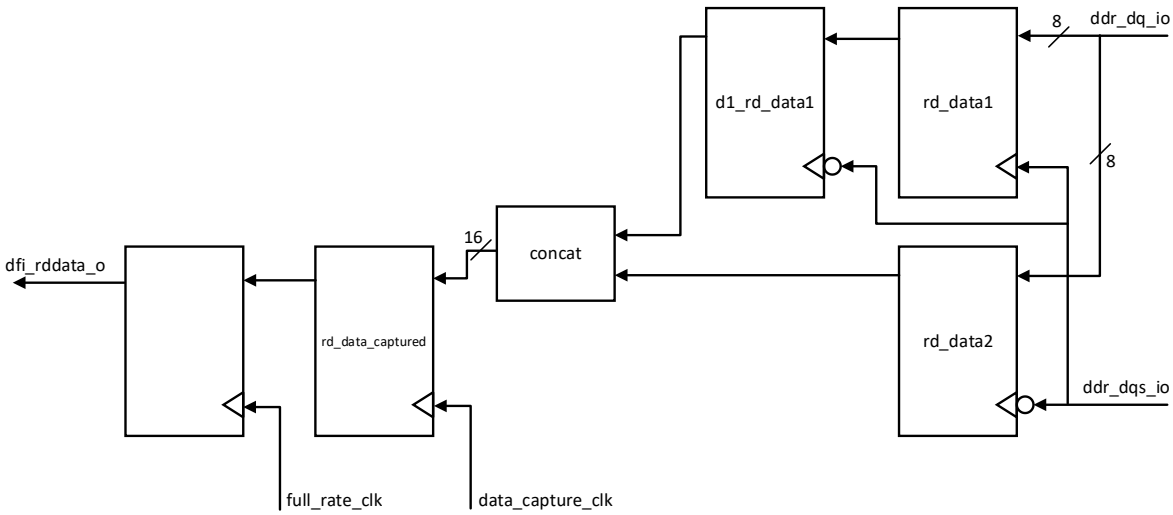

Figure 2.7. Self-Calibrating Logic CDC Training Circuit

During the SCL routine, the DDRPHY searches for the falling edge of input DQS. Once found, the valid data following the DQS falling edge is captured in the rd_data_captured register and held for clocking into the PHY clock domain. SCL finds the center between the rising edge of the full_rate_clk and the falling edge of the next input DQS strobe, shown by points A and B in Figure 2.8. The point that gives the largest setup and hold margins (point B) is set as the active edge location for the captured read data.

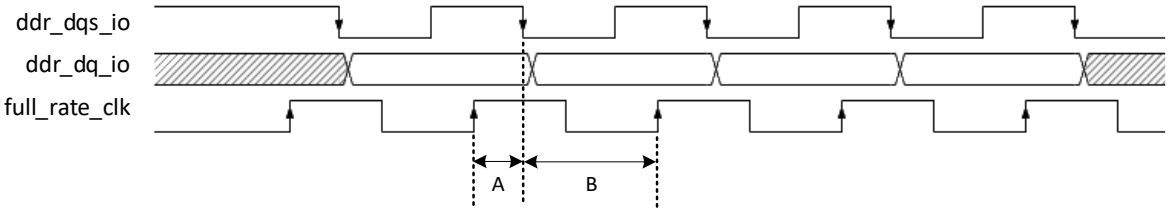

Figure 2.8. Self-Calibrating Logic CDC Timing Diagram

In the latency calibration stage, you determine the best clock phase to capture the incoming data. The captured data from the rd_data_captured register is passed into the circuit shown in Figure 2.9, where SCL incrementally adjusts the multiplexer select signal (main_clk_delta_dly) until the proper data (dfi_rddata_o) is received relative to full_rate_clk.

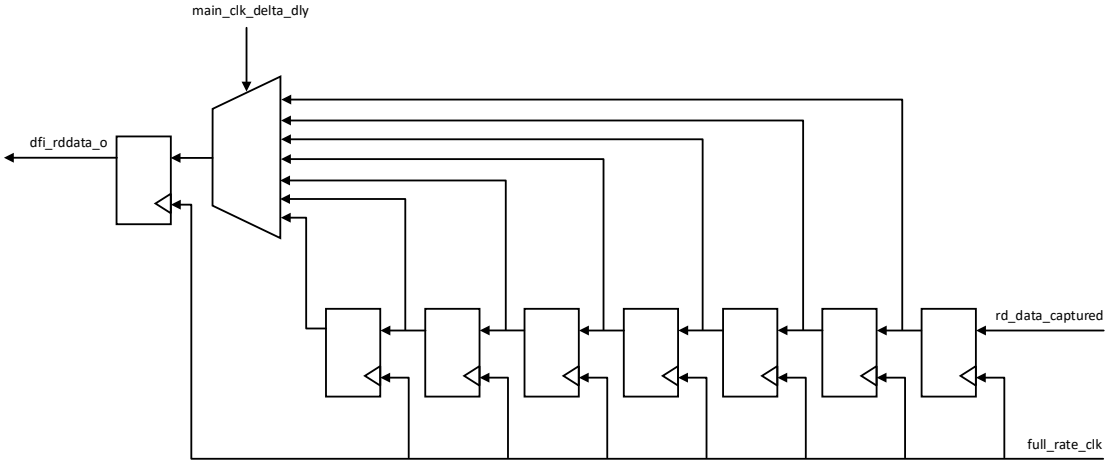

Figure 2.9. Self-Calibrating Logic Latency Training

2.5.7. Bit-Level Trim Sweep (BLTS)

The purpose of bit-level trim sweep is to ensure proper alignment and sampling of the rising edge of DQS relative to DQ during DDR4/LPDDR4 write and read operations. Bit-level trim sweep helps to account for system SI/PI related variations/jitter introduced for high-speed applications running at 800 MHz – 1,200 MHz (1,600 Mbps – 2,400 Mbps). Setting the bit_lvl_trim_sweep_en (TRN_OP_REG[8]=1) signal high enables bit-level trim sweep.

Bit-level trim sweep is similar to read bit-leveling and write bit-leveling training stages. However, it helps to calibrate the DQS-DQ timing for complex and random transitions, compared to the simple 1-0-1-0 pattern completed in read bit-leveling and write bit-leveling training stages. Run bit-level trim sweep after SCL for frequencies greater than or equal to 800 MHz.

At high-level, the Bit-Level Trim Sweep performs the following:

1. Save the trained DQ delay values from the previous Read Training/Write Training.
2. Increase the delay of all DQ bits of the active DQS groups by 1 tap.
3. Perform DDR write and read with different aggressor-victim DQ patterns, capitalizing on the weakness of the I/O standard. This uses the worst-case DQ pattern to better find the data valid window.
4. Check data integrity for all DQ and keep track of the maximum/minimum passing delay for each bit.

5. Repeat steps 2, 3, and 4 until all DQ bits has failed.
6. Revert the delay of all DQ bits to the saved values in step 1.
7. Repeat steps 2, 3, and 4 but use decrement instead of increment in step 2.
8. Get the average of the minimum passing delay and the maximum passing delay for each DQ bit and program it to the target DQ bit.

The DDRPHY Module performs read-side BLTS first, followed by the write-side BLTS.

2.5.8. 2-D Vref Training

At top speeds 2133Mbps and 2400Mbps, the actual eye opening is smaller as the high/low times are shorter. This requires more careful selection of the Vref. Each DQS Group has its own Vref setting which will be optimized for each of them. The 2D Vref training is only available for the DDRPHY-side Vref. This is not available for the DRAM side Vref because the DDRPHY has only 1 CS signal per rank and thus, it cannot set different Vref for each of the DRAM channel/chip in the same rank. This training step is only available for LPDDR4, it is not yet available for DDR4.

At the 2D At high Level, the 2-D Vref Training performs the following:

1. Set the Vref for each DQS group to the previous VREF Training value + 5.
2. Perform read-side BLTS.
3. Find the minimum DQ bit window for each DQS group and record them,
4. Decrement the Vref setting for each DQS group by 1 tap.
5. Repeat steps 2, 3 and 4 for 20x. Note that this training is lengthy so only 20-tap Vref sweep was performed. The sweep range was chosen based on the FPGA's I/O characteristics.
6. Find the optimal Vref setting for each DQS group based on the records from step 3 and use them as the trained Vref settings.
7. Run read-side BLTS again using the trained Vref settings.

2.6. Operation Descriptions

The DFI4.0 specifies several interfaces for training specific signals. The DDRPHY Module does not require these signals as it operates independently to fully perform the calibration sequence.

Note these special connectivity requirements:

- The dfi_rddata_en_p0_i and dfi_rddata_en_p2_i signals may be provided as a per byte lane output from the controller, with all bits having identical timing. The PHY requires only one dfi_rddata_en input. Connect the LSB (bit 0) of the controller's dfi_rddata_en to PHY dfi_rddata_en. The same connection applies to dfi_wrdata_en_p0_i and dfi_wrdata_en_p2_i.
- The turn_off_addr_ctrl_drv_i signal is a special PHY input that the memory controller can use to dynamically turn off the DRAM clock and command/address outputs during self-refresh to save power. If the controller does not support this feature, you can turn off the DRAM clock and command/address outputs using a software-programmable register bit if required. During memory initialization, the DDRPHY module asserts the turn_off_addr_ctrl_drv_i signal internally to turn off these DRAM clock and command/address outputs during reset and CKE wait periods.

When controlling the timing of the turn_off_addr_ctrl_drv_i assertion (logic 1) after issuing a self-refresh entry command on the DFI bus via a memory controller, follow the JEDEC spec for clock shut off after entering self-refresh mode. Add an additional 5 sclk_o margin to ensure that the DFI command propagation through the PHY is satisfied before the assertion.

When de-asserting turn_off_addr_ctrl_drv_i (logic 0) before issuing a self-refresh exit command, you need an additional 5 sclk_o margin to ensure that turn_off_addr_ctrl_drv_i propagates to the I/Os and the clock output turns on and stabilizes before issuing the self-refresh exit command on the DFI bus.

2.7. Bit Swizzle

The DDRPHY Foundation IP is hardened, the connection from the DDRPHY pins to the FPGA I/O are fixed. However, there are times that board routing can be improved significantly when the DQ bits can be swizzled or swapped around within the DQS group. For example, when using LPDDR4 device width of x16, you can swizzle each DQ bit within the lower byte and upper byte respectively, but you cannot swizzle the DQ bits from the lower byte to the upper byte and vice versa. Also, you cannot swizzle the lower byte DQS/DQ/DMI as a group to the upper byte DQS/DQ/DMI and vice versa because swizzling across the DQS group is not yet supported. This feature is currently only available for LPDDR4.

When you performed DQ bit swizzle on your board's FPGA to DRAM device connection, you should set the Bit Swizzle Settings accordingly so that the DDR Memory PHY module can perform the correct DQ reverse bit swizzle during training and during data access on the DFI I/F as shown in Figure 2.10. By implementing the DQ bit reverse swizzle, the Data on the DFI side will reach the DRAM device pins with the same data mapping as if no DQ bit swizzling happened.

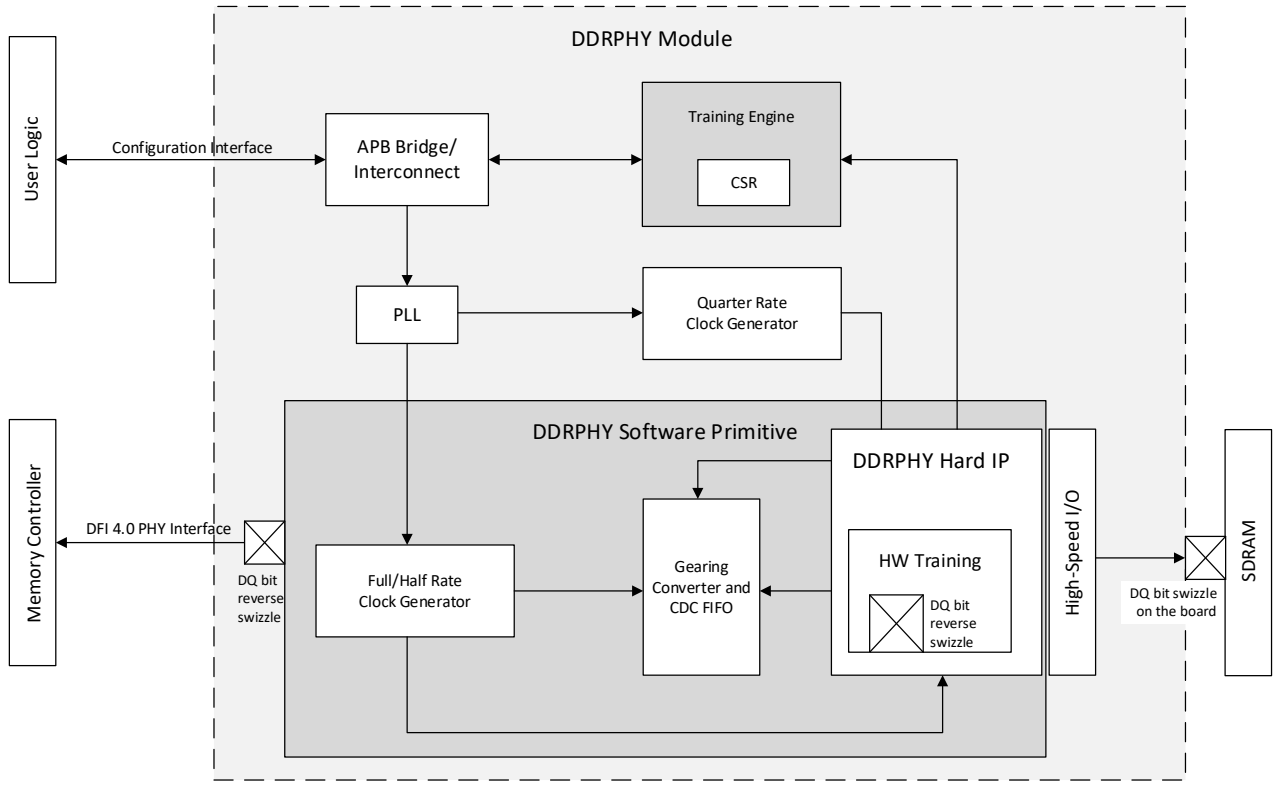

Figure 2.10. Bit Swizzle Feature Block Diagram

2.7.1. DQ Bit Swizzle Example

An example DQ Bit Swizzled connection on the board is shown in Figure 2.11.

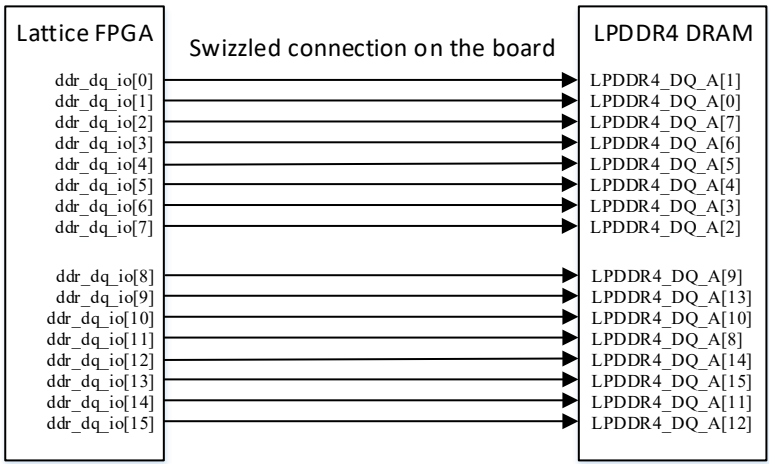

Figure 2.11. Example LPDDR4 DQ Bit Swizzle within DQS Group

You should set the corresponding settings in the IP GUI as shown in Figure 2.12. The Bit Swizzle Tab will appear when you check the option.

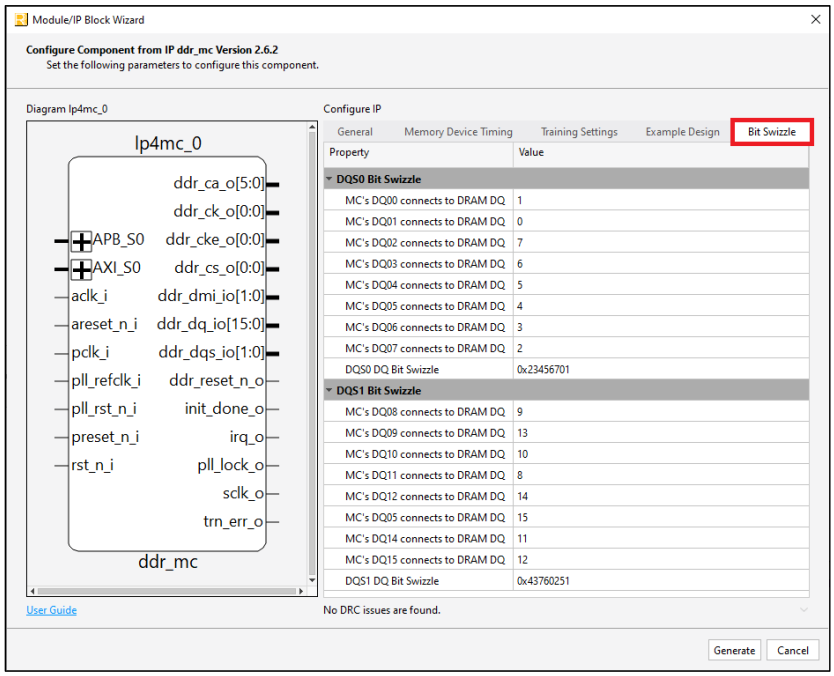

Figure 2.12. Example LPDDR4 Bit Swizzle Settings

3. IP Parameter Description

The following tables show and describe the configurable attributes of the DDRPHY IP Module. You can configure these attributes through the IP Catalog's Module/IP Block Wizard of the Lattice Radiant software. Refer to the Designing and Simulating the IP section of this user guide for information on how to configure and generate the DDRPHY Module.

3.1. DDR4 Parameters

This section describes the parameters available in the *General and Training Settings* tabs of the IP parameter editor for DDR4 interfaces.

3.1.1. DDR4 General

Table 3.1. DDR4 General Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Interface Type	DDR4	—	—
I/O Buffer Type	POD12	POD12	Display only
Gearing Ratio	8:1	8:1	Display only
Enable Side-Band ECC	Checked, Unchecked	Unchecked	—
Read Latency	10	10	*DDR Memory Frequency = 666 MHz*
	10, 11, 12	12	*DDR Memory Frequency = 800 MHz*
	12, 13, 14	12	*DDR Memory Frequency = 933 MHz*
	14, 15, 16	14	*DDR Memory Frequency = 1,066 MHz*
	15, 16, 17, 18	16	*DDR Memory Frequency = 1,200 MHz*
Write Latency	9	9	*DDR Memory Frequency = 666 MHz*
	9, 11	9	*DDR Memory Frequency = 800 MHz*
	10, 12	10	*DDR Memory Frequency = 933 MHz*
	11, 14	11	*DDR Memory Frequency = 1,066 MHz*
	12, 16	12	*DDR Memory Frequency = 1,200 MHz*
Data Bus Width	16, 32, 64	32	—
	40, 72	—	If Enable Sideband ECC == Checked
Enable Training CPU	Checked	Checked	Display only *Disabling the Internal RISC-V CPU is not yet supported*.

Table 3.2. DDR4 Clock Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Enable PLL	Checked	Checked	Display only
DDR Memory Frequency (MHz)	666, 800, 933, 1066, 1200	800	—
System Clock Frequency (MHz)	Calculated	N/A	Display only Calculated based on the selection for *DDR Memory Frequency.*
Reference Clock Frequency (MHz)	10-800	100	—
DDR Memory Actual Frequency (MHz)	Calculated	N/A	Display only Based on the selection for *DDR Memory Frequency.*

Table 3.3. DDR4 Clock/Address/Command Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Number of Clocks	1, 2	1	—
Number of Chip Selects (Rank)	1, 2	1	—
Address Width	14	14	Display only
Number of Chip ODT	1, 2	1	Based on the selection for *Number of Chip Selects.*
BA Width	2	2	Display only
BG Width	2	2	Display only

Table 3.4. DDR4 General Definitions

Attribute	Description
General Group	
DDR Interface Type	Specifies the SDRAM Memory interface: DDR4.
I/O Buffer Type	I/O Standard for the memory interface signals. This is fixed to POD12 for DDR4 but the command/address/control signals should be terminated to VTT on the board. Please see note 2 of Table 4.5.
Gearing Ratio	Specifies the ratio relationship between the DDR data speed and the memory controller speed.
Enable Sideband ECC	Enables error-correction code (ECC) for single-bit error correction and double-bit error detection.
Enable DBI	Enables data bus inversion (DBI) for better signal integrity and read/write margins.
Read Latency	Specifies the delay from issuing a read command to receiving of read data from SDRAM. Set this based on the target DRAM's datasheet.
Write Latency	Specifies the delay from issuing a write command to providing of write data to SDRAM. Set this based on the target DRAM's datasheet.
Data Bus Width	Specifies the total number of data pins in the memory interface.
Enable Training CPU	Enables RISC-V subsystem to support initialization and training of the memory device. *Disabling is not yet supported*.
Clock Settings Group	
Enable PLL	Enables PLL
DDR Memory Frequency (MHz)	Speed at which the memory controller issues commands to the memory device.
System Clock Frequency (MHz)	Speed to clock the memory controller.
Reference Clock Frequency (MHz)	Indicates the PLL reference clock speed.
DDR Command Actual Frequency (MHz)	Specifies the actual operating frequency of the memory interface (calculated by the PLL – includes tolerance)
Clock/Address/Command Group	
Number of DDR Clocks	Specifies the number of CK/CK# clock pairs to be driven to the SDRAM.
Number of Chip Selects	Specifies the number of Chip Select (CS) signals to be driven to SDRAM.
Address Width	Specifies number of address pins in memory interface, dependent on the SDRAM density.
Number of Chip ODT	Specifies the number of ODT bits.
BA Width	Specifies the row and column address of SDRAM.
BG Width	Specifies the bank group address of SDRAM.

3.1.2. DDR4 Training Settings

Table 3.5. DDR4 Training Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
DDR Clock Delay Value	0-20	15	—
DDR Clock Delay Value Incr/Decr	Checked/Unchecked	Checked	—
CS Delay Value	0-20	15	—
CS Delay Value Incr/Decr	Checked/Unchecked	Checked	—
Address Control Delay Value	0-20	4	—
Address Clock Delay Value Incr/Decr	Checked/Unchecked	Unchecked	—
Memory DQ_Vref Value for Rank0	0-114	25	—
Memory DQ_Vref Value for Rank1	0-114	25	Enabled when *Number of Ranks*==2
MC DQS Grp<0,1> Vref Value	0-127	80	—
MC DQS Grp<2,3> Vref Value	0-127	80	Enabled when *DDR Bus Width*>=32
MC DQS Grp<4,7> Vref Value	0-127	80	Enabled when *DDR Bus Width*>=64

Table 3.6. DDR4 PHY I/O Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
CK/CS Slew Rate	Slow, Fast	Fast	—
Command Address Slew Rate	Slow, Fast	Fast	—
DQS Slew Rate	Slow, Fast	Fast	—
DQ/DMI Slew Rate	Slow, Fast	Fast	—
MC CA Output Impedance	240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω	34 Ω	—
MC DQ Output Impedance	240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω	34 Ω	—
MC ODT Value	240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω	60 Ω	—

Table 3.7. DDR4 Memory ODT Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
RTT_WR Value	Dynamic ODT OFF, RZQ/1, RZQ/2, RZQ/3, Hi-Z	Dynamic ODT OFF	—
RTT_NOM Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6, RZQ/7	RZQ/5	—
RTT_PARK Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6, RZQ/7	Disable	—

Table 3.8. DDR4 Training Settings Definitions

Attribute[1]	Description
Training Settings Group	
DDR Clock Delay Value	Specifies the DDR clock delay so that the first DQS toggle is at CK = 0 during write leveling. It is recommended to increase this value if write leveling fails.
DDR Clock Delay Value Incr/Decr	Specifies the adjustment direction. Checked: DDR Clock Delay Value is added to the ddr_ck_o signal. Unchecked: DDR Clock Delay Value is subtracted from the ddr_ck_o signal.
CS Delay Value	Specifies the DDR CS delay value.

Attribute[1]	Description
CS Delay Value Incr/Decr	Specifies the adjustment direction. Checked: CS Delay Value is added to the ddr_cs_o signal. Unchecked: CS Delay Value is subtracted from the ddr_cs_o signal.
Address Control Delay Value	Specifies the DDR address/control signals delay. It is recommended to increase this value if the command bus training fails.
Address Clock Delay Value Incr/Decr	Specifies the adjustment direction. Checked: Address Control Delay Value is added to the DDR address/control signals. Unchecked: Address Control Delay Value is subtracted from the DDR address/control signals.
Memory DQ_Vref Value for Rank<0,1>	Specifies the DRAM DQ_Vref Value to be written to the DDR4 MR6 VR(DQ) and VREF(DQ) for Rank0/Rank1. When the register field TRN_OP_REG.mem_vref_training_en=0, this will be used as the final DRAM DQ Vref.
MC DQS Grp<0,1> Vref Value	Specifies the MC DQ_Vref Value for each DQS group when DQ_Vref training is disabled by setting TRN_OP_REG.mc_vref_training_en=0. The theoretical mV value is: Vref decimal value × 5 mV.
DDR4 MC I/O Settings	
CK/CS Slew Rate	Specifies the CK/CS driver strength.
Command Address Slew Rate	Specifies the CA driver strength.
DQS Slew Rate	Specifies the DQS driver strength.
DQ/DMI Slew Rate	Specifies the DQ/DMI driver strength.
MC CA Output Impedance	Memory controller CA I/O impedance to reach VDDQ threshold.
MC DQ Output Impedance	Memory controller DQ I/O impedance to reach VDDQ threshold.
MC ODT Value	Memory controller termination resistance value at FPGA.
DDR4 Memory ODT Settings	
RTT_WR Value	Specifies the RTT_WR value that is written to MR2 in DDR4 memory.
RTT_NOM Value	Specifies the RTT_NOM value that is written to MR1 in DDR4 memory.
RTT_PARK Value	Specifies the RTT_PARK value that is written to MR5 in DDR4 memory.

Note:

1. Modify these attributes only when you encounter an error during DDR4 memory training. Use them only when skipping DDR4 training during simulation. You can also skip training on hardware when set correctly, but this is not recommended as the delays and VREFs will not adjust according to environmental temperature variations.

3.2. LPDDR4 Parameters

This section describes the parameters available in the *General and Training Settings* tabs of the IP parameter editor for LPDDR4 interfaces.

3.2.1. LPDDR4 General

Table 3.9. LPDDR4 General Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Interface Type	LPDDR4	—	—
I/O Buffer Type	LVSTL11_I, LVSTL11_II	LVSTL11_I	—
Gearing Ratio	8:1	8:1	Display only
Enable Sideband ECC	Checked, Unchecked	Unchecked	Display only *ECC is not yet supported.*
Enable Read DBI	Checked, Unchecked	Unchecked	—
Read Latency	Calculated	N/A	Display only Calculated based on the selection for *DDR Memory Frequency.*

Attribute	Selectable Values	Default	Dependency on Other Attributes
Write Latency	Calculated	N/A	Display only Calculated based on the selection for *DDR Memory Frequency.*
Data Bus Width	16, 32, 64	32	—
Enable Training CPU	Checked	Checked	Display only *Disabling the Internal RISC-V CPU is not yet supported*.
Enable Bit Swizzle	Checked, Unchecked	Unchecked	—

Table 3.10. LPDDR4 Clock Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Enable PLL	Checked	Checked	Display only
DDR Memory Frequency (MHz)	350, 400, 533, 666, 800, 933, 1066, 1200	933	—
System Clock Frequency (MHz)	Calculated	N/A	Display only Calculated based on the selection for *DDR Memory Frequency.*
Reference Clock Frequency (MHz)	25, 50, 100	100	—
DDR Memory Actual Frequency (MHz)	Calculated	N/A	Display only Based on the selection for *DDR Memory Frequency.*

Table 3.11. LPDDR4 Clock/Address/Command Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Number of Clocks	1, 2	1	—
Number of Chip Selects (Rank)	1, 2	1	—
Address Width	14	14	Display only

Table 3.12. LPDDR4 General Definitions

Attribute	Description
General Group	
DDR Interface Type	Specifies the SDRAM Memory interface: LPDDR4.
I/O Buffer Type	I/O Standard for the memory interface signals.
Gearing Ratio	Specifies the ratio relationship between the DDR data speed and the memory controller speed.
Enable Sideband ECC	Enables error-correction code (ECC) for single-bit error correct and double-bit error detection (not yet supported).
Enable DBI	Enables data bus inversion (DBI) for better signal integrity and read/write margins .
Read Latency	Specifies the delay from issuing of a read command to receiving read data from SDRAM.
Write Latency	Specifies the delay from issuing of a write command to providing write data to SDRAM.
Data Bus Width	Specifies the total number of data pins in the memory interface.
Enable Training CPU	Enables RISC-V subsystem to support initialization and training of the memory device. (disabling is not yet supported)
Enable Bit Swizzle	Enables Bit Swizzle feature. Once checked, the Bit Swizzle Tab will be shown in the IP GUI. You can enable this if swizzling the DQ bit connection on the board will improve the LPDDR4 signal routing on the board.

Attribute	Description
Clock Settings Group	
Enable PLL	Enables PLL
DDR Memory Frequency (MHz)	Speed at which the memory controller issues commands to the memory device.
System Clock Frequency (MHz)	Speed to clock the memory controller.
Reference Clock Frequency (MHz)	Indicates the PLL reference clock speed.
DDR Command Actual Frequency (MHz)	Specifies the actual operating frequency of the memory interface (calculated by the PLL – includes tolerance).
Clock/Address/Command Group	
Number of Clocks	Specifies the number of CK/CK# clock pairs to be driven to SDRAM.
Number of Chip Selects	Specifies the number of chip select (CS) signals to be driven to SDRAM.
Address Width	Specifies number of address pins in memory interface, dependent on the SDRAM density.

3.2.2. LPDDR4 Training Settings

Table 3.13. LPDDR4 Training Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
DDR Clock Delay Value	0-20	4	—
DDR Clock Delay Value Incr/Decr	Checked/Unchecked	Checked	—
CS Delay Value	0-20	0	—
CS Delay Value Incr/Decr	Checked/Unchecked	Checked	—
Address Control Delay Value	0-20	0	—
Address Clock Delay Value Incr/Decr	Checked/Unchecked	Unchecked	—
Memory CA_Vref Value for Rank0	0-114	25	—
Memory CA_Vref Value for Rank1	0-114	25	Enabled when *Number of Ranks*==2
Memory DQ_Vref Value for Rank0	0-114	25	—
Memory DQ_Vref Value for Rank1	0-114	25	Enabled when *Number of Ranks*==2
MC DQS Grp<0,1> Vref Value	0-127	40	—
MC DQS Grp<2,3> Vref Value	0-127	40	Enabled when *DDR Bus Width*>=32
MC DQS Grp<4,7> Vref Value	0-127	40	Enabled when *DDR Bus Width*>=64

Table 3.14. LPDDR4 PHY I/O Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
CK/CS Slew Rate	Slow, Fast	Fast	—
Command Address Slew Rate	Slow, Fast	Fast	—
DQS Slew Rate	Slow, Fast	Fast	—
DQ/DMI Slew Rate	Slow, Fast	Fast	—
MC CA Output Impedance	240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω	34 Ω	—
MC DQ Output Impedance	240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω	34 Ω	—
MC ODT Value	240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω	48 Ω	—

Table 3.15. LPDDR4 Memory ODT Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
CA_ODT Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/2	—
DQ_ODT Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/4	—
SoC_ODT Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/6	—
CK_ODT Override Enable	Checked, Unchecked	Unchecked	—
CS_ODT Override Enable	Checked, Unchecked	Unchecked	—
CA_ODT Override Disable	Checked, Unchecked	Unchecked	—
ODT-CS/CA/CLK Disable	Checked, Unchecked	Unchecked	—
Pull-Down Drive Strength	RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/6	—

Table 3.16. LPDDR4 Training Settings Definitions

Attribute[1]	Description
Training Settings Group	
DDR Clock Delay Value	Specifies the DDR clock delay so that the first DQS toggle is at CK = 0 during write leveling. It is recommended to increase this value if write leveling fails.
DDR Clock Delay Value Incr/Decr	Specifies the adjustment direction. Checked: DDR Clock Delay Value is added to the ddr_ck_o signal. Unchecked: DDR Clock Delay Value is subtracted from the ddr_ck_o signal.
CS Delay Value	Specifies the DDR CS delay value.
CS Delay Value Incr/Decr	Specifies the adjustment direction. Checked: CS Delay Value is added to the ddr_cs_o signal. Unchecked: CS Delay Value is subtracted from the ddr_cs_o signal.
Address Control Delay Value	Specifies the DDR address/control signals delay. It is recommended to increase this value if the command bus training fails.
Address Clock Delay Value Incr/Decr	Specifies the adjustment direction. Checked: Address Control Delay Value is added to the DDR address/control signals. Unchecked: Address Control Delay Value is subtracted from the DDR address/control signals.
Memory CA_Vref Value for Rank<0,1>	Specifies the DRAM CA_Vref Value to be written to LPDDR4 DRAM's MR12 VR-CA and VREF(CA) for Rank0/Rank1. This should be set based on SI/PI simulation for the target board design.
Memory DQ_Vref Value for Rank<0,1>	Specifies the DRAM DQ_Vref Value to be written to LPDDR4 DRAM's MR14 VR(DQ) and VREF(DQ) for Rank0/Rank1. When the register field TRN_OP_REG.mem_vref_training_en=0, this will be used as the final DRAM DQ Vref.
MC DQS Grp<0,1> Vref Value	Specifies the MC DQ_Vref Value for each DQS group when DQ_Vref training is disabled by setting the register field TRN_OP_REG.mc_vref_training_en=0. The theoretical mV value is: Vref decimal value × 5 mV.
LPDDR4 MC I/O Settings	
CK/CS Slew Rate	Specifies the CK/CS driver strength.
Command Address Slew Rate	Specifies the CA driver strength.
DQS Slew Rate	Specifies the DQS driver strength.
DQ/DMI Slew Rate	Specifies the DQ/DMI driver strength.
MC CA Output Impedance	Memory controller CA I/O impedance to reach the VDDQ threshold.
MC DQ Output Impedance	Memory controller DQ I/O impedance to reach the VDDQ threshold.
MC ODT Value	Memory controller termination resistance value at FPGA.

Attribute[1]	Description
LPDDR4 Memory ODT Settings	
CA_ODT Value	Memory side CA ODT resistance value.
DQ_ODT Value	Memory side DQ ODT resistance value.
CK_ODT Override Enable	Overrides the default CK ODT value for the non-terminating rank when option is checked. Refer to MR22 in LPDDR4 device datasheet for more details.
CS_ODT Override Enable	Overrides the default CS ODT value for the non-terminating rank when option is checked. Refer to MR22 in LPDDR4 device datasheet for more details.
CA_ODT Override Disable	Disables the termination for CA when option is checked. Refer to MR22 in LPDDR4 device datasheet for more details.
ODT-CS/CA/CLK Disable	Disables ODT for CS/CA/CLK when option is checked.
Pull-Down Drive Strength	Specifies drive strength for pull-down resistor.

Note:

1. Modify these attributes only when you encounter an error during LPDDR4 memory training.

3.2.3. Bit Swizzle Settings

This section describes the attributes for swapping the DQ bits within the DQS group. This is only shown when you check the *Enable Bit Swizzle* attribute. You may use this when swapping the DQ bits will help you improve the routing on the board.

Table 3.17. LPDDR4 Bit Swizzle Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
DQS0 Bit Swizzle			
MC's DQ<00,01,02,03,04,05,06,07> connects to DRAM DQ	0, 1, 2, 3, 4, 5, 6, 7	0/1/2/3/ 4/5/6/7	If *Enable Bit Swizzle* is Checked
DQS0 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked
DQS1 Bit Swizzle			
MC's DQ<08,09,10,11,12,13,14,15> connects to DRAM DQ	8, 9, 10, 11, 12, 13, 14, 15	8/9/10/11/ 12/3/14/15	If *Enable Bit Swizzle* is Checked
DQS1 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked
DQS2 Bit Swizzle			
MC's DQ<16,17,18,19,20,21,22,23> connects to DRAM DQ	0, 1, 2, 3, 4, 5, 6, 7	0/1/2/3/ 4/5/6/7	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* >= 32
DQS2 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* >= 32
DQS3 Bit Swizzle			
MC's DQ<24,25,26,27,28,29,30,31> connects to DRAM DQ	8, 9, 10, 11, 12, 13, 14, 15	8/9/10/11/ 12/3/14/15	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* >= 32
DQS3 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* >= 32
DQS4 Bit Swizzle			
MC's DQ<32,33,34,35,36,37,38,39> connects to DRAM DQ	0, 1, 2, 3, 4, 5, 6, 7	0/1/2/3/ 4/5/6/7	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64
DQS4 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64

Attribute	Selectable Values	Default	Dependency on Other Attributes
DQS5 Bit Swizzle			
MC's DQ<40,41,42,43,44,45,46,47> connects to DRAM DQ	8, 9, 10, 11, 12, 13, 14, 15	8/9/10/11/ 12/3/14/15	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64
DQS5 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64
DQS6 Bit Swizzle			
MC's DQ<48,49,50,51,52,53,54,55> connects to DRAM DQ	0, 1, 2, 3, 4, 5, 6, 7	0/1/2/3/ 4/5/6/7	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64
DQS6 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64
DQS7 Bit Swizzle			
MC's DQ<56,57,58,59,60,61,62,63> connects to DRAM DQ	8, 9, 10, 11, 12, 13, 14, 15	8/9/10/11/ 12/3/14/15	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64
DQS7 DQ Bit Swizzle	Calculated	0x76543210	If *Enable Bit Swizzle* is Checked and *DDR Bus Width* == 64

Table 3.18. LPDDR4 Bit Swizzle Attribute Definitions

Attribute	Description
DQS<0,2,4,6> Bit Swizzle[1,2]	
MC's DQ* connects to DRAM DQ	Specifies how the DQ bits of the DQS groups 0, 2, 4, and 6 will be connected to the lower byte of the LPDDR4 DRAM channel on the board. You can swap around the bits within the DQS group (DQ byte).
DQS<0,2,4,6> DQ Bit Swizzle	This is the actual parameter used in MC's RTL. This is calculated based on the DQ connection settings.
DQS<1,3,5,7> Bit Swizzle[1,2]	
MC's DQ* connects to DRAM DQ	Specifies how the DQ bits of the DQS groups 0, 2, 4, and 6 will be connected to the upper byte of the LPDDR4 DRAM channel on the board. You can swap around the bits within the DQS group (DQ byte).
DQS<0,2,4,6> DQ Bit Swizzle	This is the actual parameter used in MC's RTL. This is calculated based on the DQ connection settings.

Note:

1. These DQS group pairs should be connected to the same DRAM channel: (DQS0, DQS1), (DQS2, DQS3), (DQS4, DQS5), and (DQS6, DQS7)
2. Swapping the DQS group with another DQS group is not yet supported.

4. Signal Description

The input and output signals of the DDRPHY are discussed in the following section.

4.1. Clock and Reset

Table 4.1. Clock and Reset Port Definitions

Port Name	I/O	Width	Description
pll_refclk_i	In	1	PLL reference clock input. It is recommended to use 100 MHz for better clock performance. Please refer to Design Rules and Guidelines section of the Avant High Speed IO and External Memory Interface User-Guide (FPGA-TN-02300) for more information.
pll_rst_n_i	In	1	PLL reset active low. The minimum reset pulse width is 5 µs. This will cause pll_lock_o to de-assert and sclk_o to stop. If you assert this signal, you should assert the main reset, rst_n_i as well. You can assert the rst_n_i at the same time as pll_rst_n_i or after pll_rst_n_i de-asserts.
pclk_i	In	1	Clock for APB interface, training CPU and control logic of the internal PLL. This clock is independent of sclk_o, since sclk_o stops during clock frequency changes. Supports 50 MHz to 150 MHz in simulation, but the upper limit for implementation may be less than 150 MHz, depending on the Radiant timing analysis report.
preset_n_i	In	1	Asynchronous active low reset for APB interface. This reset must be de-asserted synchronous to pclk_i.
pll_lock_o	Out	1	PLL lock output indicating when PLL is locked. Do not access the DDR Memory PHY Module in any bus I/F when the PLL is not locked.
sclk_o	Out	1	System clock. This is ¼ of the DDR clock frequency and is the main clock of the DDRPHY IP.
rst_i	In	1	Asynchronous active high reset. When asserted, output ports and registers are forced to their reset values. The DDRPHY IP implements logic to de-assert the internal reset synchronously to the internal clocks after rst_i de-asserts. The minimum pulse width is 2× the period of pclk_i. After rst_i deassertion, wait for a minimum of 5 pclk_i before accessing the registers. If you assert this reset signal, you need to perform the full initialization and training as described in the Calibration section.

4.2. Interrupts and Initialization/Training

Table 4.2. Interrupts and Initialization/Training Port Definitions

Port Name	I/O	Width	Description
irq_o	Out	1	Interrupt signal Reset value is 1'b0
turn_off_addr_ctrl_drv_i	In	1	Disables the output drive of the DDR CK, CS, and CA signals by setting to high-Z.
trn_done_o	Out	1	Indicates completion of initialization and training.
trn_err_o	Out	1	Indicates failure in training.

4.3. APB Register Interface

This section describes the configuration interface port in the DDRPHY IP. Refer to the AMBA APB Protocol Specification for a description of these signals.

Table 4.3. APB Interface Port Definitions

Port Name	I/O	Width	Description
apb_psel_i	In	1	APB Select signal Indicates that the subordinate device is selected, and a data transfer is required.
apb_paddr_i	In	12	APB Address signal
apb_pwdata_i	In	32	APB Write data signal Bits [31:8] are not used
apb_pwrite_i	In	1	APB Direction signal 1 = Write, 0 = Read
apb_penable_i	In	1	APB Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_pready_o	Out	1	APB Ready signal Indicates transfer completion. The subordinate uses this signal to extend an APB transfer. The reset value is 1'b0.
apb_pslverr_o	Out	1	APB Error signal Indicates a transfer failure. This signal is tied to 1'b0.
apb_prdata_o	Out	32	APB Read data signal

4.4. DFI 4.0 PHY Interface

This section describes the data interface port when the *Local Data Bus Type* attribute is set to AXI4 in the DDRPHY IP. These ports are available only when using IP Core v2.x.x. Refer to the DFI 4.0 Specification for a description of these signals.

Table 4.4. AXI4 Interface Port Definitions

Port Name	I/O	Width	Description
dfi_reset_n_i	In	1	Reset for DFI interface
dfi_ctrlupd_req_i	In	1	DFI MC-initiated update request signal
dfi_phyupd_ack_i	In	1	DFI PHY-initiated update acknowledge signal
dfi_cke_p<0,1,2,3>_i	In	CK_WIDTH	DFI clock enable signal
dfi_cs_p<0,1,2,3>_i	In	CS_WIDTH	DFI chip select (active low)
dfi_ca_p<0,1,2,3>_i	In	DFI_CA_WIDTH	DFI address bus
dfi_ba_p<0,1,2,3>_i	In	BA_WIDTH	DFI bank address
dfi_ras_n_p<0,1,2,3>_i	In	1	DFI row address strobe
dfi_cas_n_p<0,1,2,3>_i	In	1	DFI column address strobe
dfi_we_n_p<0,1,2,3>_i	In	1	DFI write enable
dfi_odt_p<0,1,2,3>_i	In	1	DFI on-die termination
dfi_wrdata_cs_p<0,1,2,3>_i	In	CS_WIDTH	DFI write data chip select (active low)
dfi_wrdata_en_p<0,2>_i	In	1	DFI write data and data mask enable
dfi_wrdata_i	In	BUS_WIDTH*8	DFI write data
dfi_wrdata_mask_i	In	BUS_WIDTH	DFI write data byte mask
dfi_rddata_cs_p<0,1,2,3>_i	In	CS_WIDTH	DFI read data chip select (active low)
dfi_rddata_en_p<0,2>_i	In	1	DFI read data enable
dfi_rddata_o	Out	BUS_WIDTH*8	DFI read data
dfi_rddata_dbi_o	Out	BUS_WIDTH	DFI read data bus inversion

Port Name	I/O	Width	Description
dfi_rddata_valid_p<0,2>_o	Out	BUS_WIDTH/8	DFI read data valid indicator. Each bit indicates read data valid for corresponding data lane.
dfi_ctrlupd_ack_o	Out	1	DFI MC-initiated update acknowledge signal
dfi_phyupd_req_o	Out	1	DFI PHY-initiated updated request signal
dfi_phyupd_type_o	Out	2	DFI PHY-initiated update select signal
dfi_init_complete_o	Out	1	DFI initialization complete signal

4.5. Memory Interface Signals

4.5.1. DDR4 Memory Interface

This section describes the interface ports for DDR4 SDRAM.

Table 4.5. DDR4 Interface Port Definitions

Port Name	I/O	Width	Description
ddr_ck_o[1,2]	Out	CK_WIDTH	DDR4 CK signal
ddr_cke_o[1,2]	Out	CK_WIDTH	DDR4 CKE signal
ddr_cs_o[1,2]	Out	CS_WIDTH	DDR4 CS signal
ddr_ca_o[2]	Out	CA_WIDTH	DDR4 CA signal
ddr_we_n_o[2]	Out	1	DDR4 WE signal
ddr_cas_n_o[2]	Out	1	DDR4 CAS signal
ddr_ras_n_o[2]	Out	1	DDR4 RAS signal
ddr_act_n_o[2]	Out	1	DDR4 ACT_n signal
ddr_ba_o[1,2]	Out	BANK_WIDTH	DDR4 BA signal
ddr_bg_o[1,2]	Out	BG_WIDTH	DDR4 BG signal
ddr_odt_o[1,2]	Out	ODT_WIDTH	DDR4 ODT signal
ddr_reset_n_o[2]	Out	1	Memory reset signal
ddr_dq_io[1]	In/Out	BUS_WIDTH	DDR4 DQ signal
ddr_dqs_io[1]	In/Out	DQS_WIDTH	DDR4 DQS signal
ddr_dmi_io[1]	In/Out	DQS_WIDTH	DDR4 DMI signal

Notes:

1. The bit width of SDRAM Memory Interface signals is defined based on the attributes listed in Table 3.1 and Table 3.3.
2. For component, terminate the command, address and control signals to VTT on the board. This is not needed for UDIMM because it already has the termination within the UDIMM.

4.5.2. LPDDR4 Memory Interface

This section describes the interface ports for LPDDR4 SDRAM.

Table 4.6. LPDDR4 Interface Port Definitions

Port Name	I/O	Width	Description
ddr_ck_o[1]	Out	CK_WIDTH	LPDDR4 CK signal
ddr_cke_o[1]	Out	CK_WIDTH	LPDDR4 CKE signal
ddr_cs_o[1]	Out	CS_WIDTH	LPDDR4 CS signal
ddr_ca_o	Out	6	LPDDR4 CA signal
ddr_reset_n_o	Out	1	Memory reset signal
ddr_dq_io[1]	In/Out	BUS_WIDTH	LPDDR4 DQ signal
ddr_dqs_io[1]	In/Out	DQS_WIDTH	LPDDR4 DQS signal
ddr_dmi_io[1]	In/Out	DQS_WIDTH	LPDDR4 DMI signal

Note:

1. The bit width of SDRAM Memory Interface signals is defined based on the attributes listed in Table 3.9 and Table 3.11.

5. Register Description

This section describes the user-accessible registers in the DDRPHY. Some registers are reserved for internal CPU usage and you should not write to them. Writing to these registers may cause failures during the initialization and training operations.

Table 5.1. Summary of DDRPHY Module Registers

Offset	Register Name	Access Type	Description
0x000 to 0x1FC	Reserved for DDRPHY Hard IP	—	Access is reserved for the Training CPU. Do not access this address from your APB interface.
0x200	FEATURE_CTRL_REG	RO	Feature Control Register
0x204	RESET_REG	RW	Reset Register
0x208	SETTINGS_REG	RW	Settings Register
0x20C	PHY_CLK_REG	RW	PHY Clock Control and Status Register Write access is reserved for the Training CPU. Do not access this address from your APB interface.
0x210	INT_STATUS_REG	WR1C	Interrupt Status Register
0x214	INT_ENABLE_REG	RW	Interrupt Enable Register
0x218	INT_SET_REG	WO	Interrupt Set Register
0x21C	INIT_CTRL_REG	WO	Reserved for use by the internal CPU. Writing to this register will cause unexpected behavior.
0x220	TRN_OP_REG	RW	Training Operation Register
0x224	STATUS_REG	RW	Training Status Register
0x228 to 0x22C	Reserved for DDRPHY Hard IP	—	Access is reserved for the Training CPU. Do not access this address from your APB interface.
0x230	MRW_CTRL_REG	WO	DDR Mode Register Write Control Register
0x234 to 0x23C	Reserved	RSVD	Reserved
0x240 to 0x244	Reserved for DDRPHY Hard IP Debug	RSVD	Access is reserved for the Training CPU debug information.
0x250	CK_ADRCTRL_TRIM	RW	Clock/Address/Control Trim Setting Register to specify delay.
0x254	ODT_SETTING	RW	ODT setting register to set ODT value.
0x258	Reserved	RSVD	Reserved
0x25C	DRAM_VREF_REG	RW	DRAM Vref Register Setting
0x260	PHY_VREF_0_3_REG	RW	PHY Vref setting for DQS Groups 0 to 3.
0x264	PHY_VREF_4_7_REG	RW	PHY Vref setting for DQS Groups 4 to 7.
0x268	PHY_VREF_8_REG	RW	PHY Vref setting for DQS Group 8.
0x26C to 0x2B0	Reserved for Training	RSVD	Access is reserved for the Training CPU. Do not access this address from your APB interface.
0x2B4 to 0x3FC	Reserved	RSVD	Reserved
0x400 to 0x46C	Reserved for PLL	—	Access is reserved for the Training CPU. Do not access this address from your APB interface.
0x470 to 0x7FC	Reserved	RSVD	Reserved

Note: The behavior of registers to write and read access is defined by its access type, which is defined in Table 5.2.

Table 5.2. Register Access Type Definitions

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value	Ignores write access
WO	Returns 0	Updates register value
RW	Returns register value	Updates register value
WR1C	Returns register value	Writing 1'b1 on register bit clears the bit to 1'b0 Writing 1'b0 on register bit is ignored
RSVD	Returns 0	Ignores write access

5.1. Feature Control Register (FEATURE_CTRL_REG) (0x200)

The Feature Control Register reflects the modes of operation specified by the attributes selected during IP configuration. These attributes are set during IP configuration and cannot be modified at runtime. The CPU reads this register to identify the modes of operation.

Table 5.3. Feature Control Register

Field	Name	Access	Width	Reset
[31:21]	reserved	RSVD	11	—
[20]	reset_init_by_phy	RO	1	1
[19:17]	reserved	RSVD	3	—
[16]	num_ranks	RO	1	*Number of Ranks*
[15:12]	ddr_width	RO	4	*DDR Bus Width*
[11:8]	ddr_type	RO	4	*DDR Interface Type*
[7:4]	reserved	RSVD	4	—
[3]	gear_ratio	RO	1	*Gearing Ratio*
[2]	reserved	RSVD	1	—
[1]	dbi_en	RO	1	*Enable DBI*
[0]	ecc_en	RO	1	*Enable SideBand ECC*

reset_init_by_phy

- Enables the logic and routine that drive the ddr_reset_n_o and ddr_cke_o signals during memory initialization, as well as the initial mode register writes and ZQ calibration right after the initialization. This is fixed to 1 for the first release.
- 0 – DDRPHY resets and initializes the memory
- 1 – PHY resets and initializes the memory

num_ranks

- The num_ranks specify the number of DDR ranks as follows:
  - 0 – Single rank
  - 1 – Dual rank

ddr_width

- The ddr_width specifies the bit width of the DDR data bus as follows:
  - 0 – *DDR Bus Width* = 8 bits
  - 1 – *DDR Bus Width* = 16 bits
  - 2 – reserved
  - 3 – *DDR Bus Width* = 32 bits or 40 bits
  - 4 – 4'h6: reserved
  - 7 – *DDR Bus Width* = 64 bits or 72 bits

ddr_type

- The ddr_type specifies the DDR standard implemented by the DDRPHY IP Core. This is based on the *Interface Type* attribute.
- 4 – *Interface Type* = DDR4
- 12 – *Interface Type* = LPDDR4

gear_ratio

- The gear_ratio specifies the ratio of clock frequency of DDR clock domain and system clock domain. This is based on the *Gearing Ratio* attribute.
- 0 – 4:1 gearing: ddr_ck_o frequency = 2 x sclk_o frequency
- 1 – 8:1 gearing: ddr_ck_o frequency = 4 x sclk_o frequency

dbi_en

- The dbi_en enables the data bus inversion function to reduce the toggling of DDR data signal in the board, thus improving the signal integrity and reducing dynamic power consumption. The DBI is only enabled on the read path and is always disabled on the write path to support masked write function. This mode is based on the *Enable Read DBI* attribute.

ecc_en

- The ecc_en enables the sideband ECC function. This mode is based on the *Enable Sideband ECC* attribute.

5.2. Reset Register (RESET_REG) (0x204)

The Reset Register controls the reset of the internal CPU and Training Engine, both of which reset at power-on. The host de-asserts the reset to the internal CPU and Training Engine to begin memory initialization and training. Upon training completion, the internal CPU sets the trn_eng_rst_n signal low (RESET_REG[0]=0) to place the Training Engine in reset to save power. This register does not reset the Configuration Set Registers (CSRs).

Table 5.4. Reset Register

Field	Name	Access	Width	Reset
[31:1]	reserved	RSVD	31	—
[0]	cpu_reset_n	RW	1	0

cpu_reset_n

- Reset input to the training CPU. This register is in a reset state at power-on. The host un-reset this register to start the memory initialization and training. Upon training completion, the internal CPU writes to this register to return the Memory Training Engine to reset state, thus saving power consumption. This register does not reset the CSR.

5.3. Settings Register (SETTINGS_REG) (0x208)

The Settings Register controls the DDR write and read latencies according to the attributes selected during IP configuration.

Table 5.5. Settings Register

Field	Name	Access	Width	Reset
[31:28]	reserved	RSVD	4	—
[27:16]	cmd_freq	RO	12	*DDR Memory Frequency*
[15:8]	read_latency	RW	8	*Read Latency*
[7:0]	write_latency	RW	8	*Write Latency*

cmd_freq

- The cmd_freq reflects the *DDR Memory Frequency* attribute value. The training routine uses this value to trim the initial delay settings of the DDR signals.

read_latency

- The read_latency specifies the number of DDR clock cycles from read command to the first read data.

write_latency

- The write_latency specifies the number of DDR clock cycles from write command to the first write data.

5.4. PHY Clock Register (PHY_CLOCK_REG) (0x20C)

The training CPU uses the PHY Clock Register shown in Table 5.6 during clock frequency changes. The host CPU reads this register to determine the clock frequency and lock status. You should not write to this register.

Table 5.6. PHY Clock Register

Field	Name	Access	Width	Reset
[31:16]	reserved	RSVD	16	—
[15:4]	pll_refclk	RO	12	*Reference Clock Frequency*
[3]	prim_rst_en_cfc	WO	1	—
[2]	pll_reset	WO	1	—
[1]	pll_lock	RO	1	—
[0]	disable_clkophy	WO	1	0

pll_refclk

- Returns the PLL reference clock frequency in MHz.

prim_rst_en_cfc

- Enables the reset of the DDR primitives during clock frequency change.

pll_reset

- Used by the Training CPU to reset the PLL during clock frequency change so that the PLL locks on the new frequency.

pll_lock

- Asserts when PLL is locked.

disable_clkophy

- Set to 1 to disable the PLL output clock going to the DDRPHY and ECLKSYNC hard IPs.

5.5. Interrupt Status Register (INT_STATUS_REG) (0x210)

Table 5.7 lists all the pending interrupts supported in the DDRPHY Module. When an interrupt bit asserts, it remains asserted until the host clears it by writing 1'b1 to the corresponding bit.

The interrupt status bits are independent of the interrupt enable bits. In other words, status bits may indicate pending interrupts, even though those interrupts are disabled in the Interrupt Enable Register. User logic that handles interrupts should mask (bitwise and logic) the contents of INT_STATUS_REG and INT_ENABLE_REG to determine which interrupts to service. The irq_o interrupt signal asserts whenever both an interrupt status bit and the corresponding interrupt enable bits are set.

Table 5.7. Interrupt Status Register

Field	Name	Access	Width	Reset
[31:2]	reserved	RSVD	30	—
[1]	trn_err_int	WR1C	1	0
[0]	trn_done_int	WR1C	1	0

trn_err_int

- Training Error Interrupt. This interrupt bit asserts when the Memory Training Engine encounters an error during training. Read the status register to determine the specific error.
- 0 – No interrupt
- 1 – Interrupt pending

trn_done_int

- Training Done Interrupt. This interrupt bit asserts when initialization and training is completed successfully.
- 0 – No interrupt
- 1 – Interrupt pending

5.6. Interrupt Enable Register (INT_ENABLE_REG) (0x214)

The Interrupt Enable Register lists all configurable interrupts within the DDRPHY.

Table 5.8. Interrupt Enable Register

Field	Name	Access	Width	Reset
[31:2]	reserved	RSVD	30	—
[1]	trn_err_en	RW	1	0
[0]	trn_done_en	RW	1	0

trn_err_en

- Training Error Interrupt Enable.
- 0 – Interrupt disabled
- 1 – Interrupt enabled

trn_done_en

- Training Done Interrupt Enable.
- 0 – Interrupt disabled
- 1 – Interrupt enabled

5.7. Interrupt Set Register (INT_SET_REG) (0x218)

Table 5.9 shows a summary of the Interrupt Set Register. Writing 1'b1 to a register bit in this register asserts the corresponding interrupt status bits in INT_STATUS_REG. Writing 1'b0 is ignored.

Table 5.9. Interrupt Set Register

Field	Name	Access	Width	Reset
[31:2]	reserved	RSVD	30	—
[1]	trn_err_set	WO	1	0
[0]	trn_done_set	WO	1	0

trn_err_set

- Training Error Interrupt Set.
- 0 – No action
- 1 – Asserts INT_STATUS_REG.trn_err_int

trn_done_set

- Training Done Interrupt Set.
- 0 – No action
- 1 – Asserts INT_STATUS_REG.trn_done_int

5.8. Training Operation Register (TRN_OP_REG) (0x220)

Table 5.10 summarizes the Training Operation Register, which controls the memory initialization and training. Set these register bits to 1'b0 during simulation to shorten the initialization and training procedure.

Table 5.10. Training Operation Register

Field	Name	Access	Width	Reset
[31:10]	reserved	RSVD	22	—
[9]	phy_2d_vref_en	RW	1	0
[8]	bit_lvl_trim_sweep_en	RW	1	0
[7]	mem_verf_training_en	RW	1	1
[6]	mc_vref_training_en	RW	1	1
[5]	ca_vref_training_en	RW	1	0
[4]	write_trn_en	RW	1	1
[3]	read_trn_en	RW	1	1
[2]	write_lvl_en	RW	1	1
[1]	cbt_en	RW	1	1
[0]	init_en	RW	1	1

phy_2d_vref_en

- The phy_2d_vref_en performs 2D VREF training to improve performance by addressing voltage variation both horizontally and vertically. This setting requires bit_lvl_trim_sweep_en = 1. Refer to the VREF Training and Bit-Level Trim Sweep sections of this user guide for more details.

bit_lvl_trim_sweep

- The bit_lvl_trim_sweep centers the DQ valid window to the DQS edge for each DQ bit. Refer to the Bit-Level Trim Sweep section of this user guide for more details.

mem_verf_training_en

- The mem_vref_trn_en enables the memory's DQ Vref training. When enabled, the DDRPHY performs write training across multiple memory Vref points and selects the optimal Vref value. Refer to the VREF Training section of this user guide for more details.

mc_vref_training_en

- The mc_vref_trn_en enables the DDRPHY's DQ Vref training. When enabled, the DDRPHY performs write training across multiple Vref points of the FPGA's I/O and selects the optimal Vref value. Refer to the VREF Training section of this user guide for more details.

ca_vref_trn_en

- The ca_vref_trn_en enables the memory's CA Vref training. When enabled, the DDRPHY performs CA training across multiple CA_Vref points and selects the optimal CA_Vref value. This bit is currently unused because we recommend setting the CA_Vref based on the SI/PI simulation for the target board design. Refer to the VREF Training section of this user guide for more details.

write_trn_en

- The write_trn_en enables the write DQ bit leveling. The write training optimizes the write DQ delay with respect to the write DQS to improve the data valid window for writes. Refer to the Write Training (Write Bit-Leveling) section of this user guide for more details.

read_trn_en

- The read_trn_en enables the read DQ bit leveling. This register optimizes the read DQ with respect to read DQS to improve the data valid window for read. Refer to the Read Training (Read Bit-Leveling) section of this user guide for more details.

write_lvl_en

- The write_lvl_en enables the write leveling during initialization and training. The write leveling compensates for CK-DQS timing skews. Refer to the Write Leveling section of this user guide for more details.

cbt_en

- The cbt_en enables the command bus during initialization and training. The command bus training performs CA_VREF programming and center aligns the CS/CA to CK for high frequency operation. See the Command Bus Training section for details. The command bus training is always performed as required by the LPDDR4 standard. This bit only disables the clock frequency change for faster simulation because this process requires long simulation time.
- 0 – The clock frequency change is not performed during CBT
- 1 – The clock frequency change is performed during CBT

init_en

- The init_en provides option to shorten the initialization for simulation purposes.
- 0 – Initialization is significantly reduced. For example, reset time and CKE low time is significantly shortened
- 1 – Initialization is complete according to the corresponding DDR standard

5.9. Training Status Register (TRN_STATUS_REG) (0x224)

Table 5.11 summarizes the Training Status Register. This register is written by the internal CPU to communicate the status to the system CPU.

Table 5.11. Training Status Register

Field	Name	Access	Width	Reset
[31:24]	reserved	RSVD	8	—
[23:20]	retraining_count	RW	4	0
[19:18]	reserved	RSVD	2	—
[17]	phy_2d_vref_done	RW	1	0
[16]	bit_lvl_trim_sweep_done	RW	1	0
[15:14]	err_on_rank	RW	2	0
[13]	blts_err	RW	1	0
[12]	scl_err	RW	1	0
[11]	write_training_err	RW	1	0
[10]	read_training_err	RW	1	0
[9]	write_lvl_err	RW	1	0
[8]	cbt_err	RW	1	0
[7]	rank1_done	RW	1	0
[6]	rank0_done	RW	1	0
[5]	scl_done	RW	1	0
[4]	write_training_done	RW	1	0
[3]	read_training_done	RW	1	0
[2]	write_lvl_done	RW	1	0
[1]	cbt_done	RW	1	0
[0]	init_done	RW	1	0

retraining_count

- In the event of a command bus training, write levelling, or read dq-bit leveling error, the Training CPU attempts to calibrate the DDR/LPDDR interface again with updated training settings. The retraining_count keeps track of the number of retries attempted by the Training CPU to successfully pass the DDR/LPDDR training routine, with a maximum of five retrains.

phy_2d_vref_done

- Asserts when 2D VREF training has completed.

bit_lvl_trim_sweep_done

- Asserts when bit-level trim sweep has completed.

err_on_rank

- Indicates which rank has encountered an error.
- 2'bx1: training error on rank 0
- 2'b1x: training error on rank 1

blts_err

- Asserts when a failure occurs during bit-level trim sweep.

scl_err

- Asserts when a failure occurs during self-calibrating logic.

write_trn_err

- Asserts when a failure occurs during write training.

read_trn_err

- Asserts when a failure occurs during read training at 533MHz or higher. This status bit does not assert for 350MHz and 450MHz.

write_lvl_err

- Asserts when a failure occurs during write leveling.

cbt_err

- Asserts when a failure occurs during command bus training.

rank1_done

- Asserts when training as completed for rank 1.

rank0_done

- Asserts when training as completed for rank 0.

scl_done

- Asserts when self-calibrating logic has completed.

write_training_done

- Asserts when write training has completed.

read_training_done

- Asserts when read training has completed.

write_lvl_done

- Asserts when write levelling has completed.

cbt_done

- Asserts when command bus training has completed.

init_done

- Asserts when PHY initialization has completed.

5.10. Mode Register Write Control Register (MRW_CTRL_REG) (0x230)

Table 5.12 summarizes the Mode Register Write Control Register. The training CPU writes to this register to perform mode register writes to the memory device. This register should not be used for normal operation. It may be used for debugging purposes when the DRAM is in an idle state. Note that setting an inappropriate mode register value will cause failure in operation.

Table 5.12. Mode Register Write Control Register

Field	Name	Access	Width[1, 2]	Reset
[31:OPW+8]	reserved	RSVD	24-OPW	—
[OPW+7:8]	mrw_op	WO	OPW	—
[7:MAW]	reserved	RSVD	8-MAW	—
[MAW-1:0]	mrw_ma	WO	MAW	—

Notes:

1. For DDR4: OPW = 14, MAW = 3
2. For LPDDR4: OPW = 8, MAW = 6

mrw_op

- Specifies the opcode for mode register write.

mrw_ma

- Specifies the mode register address to write to.

5.11. Clock/Address/Control Trim Register (CK_ADRCTRL_TRIM_REG) (0x250)

Table 5.13 summarizes the Clock/Address/Control Trim Settings Register. The reset value is set by the selected GUI attributes during IP generation. The training CPU reads this register and sets the corresponding DDR Hard IP registers. To try different settings on hardware, write to this register before releasing the reset of the training CPU. This method is useful for debugging command bus training and write leveling errors.

Table 5.13. Clock/Address/Control Trim Settings Register

Field	Name	Access	Width	Reset
[31:25]	reserved	RSVD	8	—
[23]	adrctrl_dly_val_inc	RW	1	*Address Control Delay Value Incr/Decr*
[22:16]	adrctrl_dly_val	RW	7	*Address Control Delay Value*
[15]	cs_dly_val_incr	RW	1	*CS Delay Value Incr/Decr*
[14:8]	cs_dly_val	RW	7	*CS Delay Value*
[7]	ck_dly_val_incr	RW	1	*DDR Clock Delay Value Incr/Decr*
[6:0]	ck_dly_val	RW	7	*DDR Clock Delay Value*

adrctrl_dly_val_inc

- Specifies whether the delay value is added or subtracted in relation to the address/control delay of the DDRPHY Hard IP.
- 0 – adrctrl_dly_val is subtracted from the address/control delay of the DDRPHY Hard IP.
- 1 – adrctrl_dly_val is added to the address/control delay of the DDRPHY Hard IP.

adrctrl_dly_val

- Specifies the delay (number of delay taps) to be added or subtracted in relation to the address/control delay of the DDRPHY Hard IP.

cs_dly_val_inc

- Specifies whether the delay value is added or subtracted in relation to the chip select delay of the DDRPHY Hard IP.
- 0 – cs_dly_val is subtracted from the chip select delay of the DDRPHY Hard IP.
- 1 – cs_dly_val is added to the chip select delay of the DDRPHY Hard IP.

cs_dly_val

- Specifies the delay (number of delay taps) to be added or subtracted in relation to the chip select delay of the DDRPHY Hard IP.

ck_dly_val_incr

- Specifies whether the delay value is added or subtracted in relation to the DRAM clock delay of the DDRPHY Hard IP.
- 0 – ck_dly_val is subtracted from the DRAM clock delay of the DDRPHY Hard IP.
- 1 – ck_dly_val is added to the DRAM clock delay of the DDRPHY Hard IP.

ck_dly_val

- Specifies the delay (number of delay taps) to be added or subtracted in relation to the DRAM clock delay of the DDRPHY Hard IP.

5.12. ODT Settings Register (ODT_SETTINGS_REG) (0x254)

The ODT Settings Register specifies the ODT settings to be written to the DRAM during initialization. The training CPU reads this register and sets the corresponding LPDDR4/DDR4 memory mode registers. The Table 5.14 shows the ODT Settings Register for LPDDR4, while Table 5.15 shows the ODT Settings Register for DDR4.

Table 5.14. ODT Settings Register for LPDDR4

Field	Name	Access	Width	Reset
[31:19]	reserved	RSVD	13	—
[18:16]	odtr_pdds	RW	3	*Pull-Down Drive Strength*
[15:14]	X8ODTD	RW	2	*ODT-CS/CA/CLK*
[13]	odtd_ca	RW	1	*CA_ODT Override Disable*
[12]	odte_cs	RW	1	*CS_ODT Override Enable*
[11]	odte_ck	RW	1	*CK_ODT Override Enable*
[10:8]	soc_odt_val	RW	3	*SoC ODT Value*
[7]	reserved	RSVD	1	—
[6:4]	ca_odt_val	RW	3	*CA_ODT Value*
[3]	reserved	RSVD	1	—
[2:0]	dq_odt_val	RW	3	*DQ_ODT Value*

odtr_pdds

- Specifies the pull-down drive strength settings to be written to LPDDR4 memory mode register 3 (MR3).

X8ODTD

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 22 (MR22).

odtd_ca

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 22 (MR22).

odte_cs

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 22 (MR22).

odte_ck

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 22 (MR22).

soc_odt_val

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 22 (MR22).

ca_odt_val

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 11 (MR11).

dq_odt_val

- Specifies the corresponding ODT settings to be written to LPDDR4 memory mode register 11 (MR11).

Table 5.15. ODT Settings Register for DDR4

Field	Name	Access	Width	Reset
[31:11]	reserved	RSVD	13	—
[10:8]	rtt_park_val	RW	3	*RTT_PARK Value*
[7]	reserved	RSVD	1	—
[6:4]	rtt_wr_val	RW	3	*RTT_WR Value*
[3]	reserved	RSVD	1	—
[2:0]	rtt_nom_val	RW	3	*RTT_NOM Value*

rtt_park_val

- Specifies the corresponding ODT settings to be written to DDR4 memory mode register 5 (MR5).

rtt_wr_val

- Specifies the corresponding ODT settings to be written to DDR4 memory mode register 2 (MR2).

rtt_nom_val

- Specifies the corresponding ODT settings to be written to DDR4 memory mode register 1 (MR1).

5.13. DRAM VREF Register (DRAM_VREF_REG) (0x25C)

The DRAM VREF Register specifies the Vref values written in the DRAM during initialization. When DRAM side Vref training is disabled, this register specifies the Vref settings. Table 5.16 shows the DRAM Vref Register.

Table 5.16. DRAM VREF Register

Field	Name	Access	Width	Reset
[31]	reserved	RSVD	1	—
[30:24]	dram_vref_ca_r1	RW	7	*Memory CA_Vref Value for Rank1*
[23]	reserved	RSVD	1	—
[22:16]	dram_vref_dq_r1	RW	7	*Memory DQ_Vref Value for Rank1*
[15]	reserved	RSVD	1	—
[14:8]	dram_vref_ca_r0	RW	7	*Memory CA_Vref Value for Rank0*
[7]	reserved	RSVD	1	—
[6:0]	dram_vref_dq_r0	RW	7	*Memory DQ_Vref Value for Rank0*

dram_vref_ca_r1

- Specifies the Vref value to be written to LPDDR4 Rank 1 MR12 VR(CA) and VREF(CA).
- This is not used in DDR4 mode.

dram_vref_dq_r1

- Specifies the Vref value to be written to:
  - When LPDDR4 mode: Rank 1 MR14 VR(DQ) and VREF(DQ).
  - When DDR4 mode: Rank 1 MR6 VrefDQ Training Range and Value.

dram_vref_ca_r0

- Specifies the Vref value to be written to LPDDR4 Rank 0 MR12 VR(CA) and VREF(CA).
- This is not used in DDR4 mode.

dram_vref_dq_r0

- Specifies the Vref value to be written to:
  - When LPDDR4 mode: Rank 0 MR14 VR(DQ) and VREF(DQ).
  - When DDR4 mode: Rank 0 MR6 VrefDQ Training Range and Value.

5.14. PHY VREF Register for DQS Groups 0-3 (PHY_VREF_0_3_REG) (0x260)

Table 5.17 displays the PHY VREF Register for DQS Groups 0 to 3. This register specifies the initial Vref values for DQS Groups 0 to 3. When PHY Vref Training is disabled (TRN_OP_REG.mc_vref_training_en=0), the value set in this register becomes the final Vref value.

Table 5.17. PHY VREF Register for DQS Groups 0-3

Field	Name	Access	Width	Reset
[31]	reserved	RSVD	1	—
[30:24]	phy_vref_dqs_grp3	RW	7	*MC DQS Grp3 Vref Value*
[23]	reserved	RSVD	1	—
[22:16]	phy_vref_dqs_grp2	RW	7	*MC DQS Grp2 Vref Value*
[15]	reserved	RSVD	1	—
[14:8]	phy_vref_dqs_grp1	RW	7	*MC DQS Grp1 Vref Value*
[7]	reserved	RSVD	1	—
[6:0]	phy_vref_dqs_grp0	RW	7	*MC DQS Grp0 Vref Value*

phy_vref_dqs_grp3

- Specifies the initial Vref value for DDRPHY DQS Group 3.

phy_vref_dqs_grp2

- Specifies the initial Vref value for DDRPHY DQS Group 2.

phy_vref_dqs_grp1

- Specifies the initial Vref value for DDRPHY DQS Group 1.

phy_vref_dqs_grp0

- Specifies the initial Vref value for DDRPHY DQS Group 0.

5.15. PHY VREF Register for DQS Groups 4-7 (PHY_VREF_4_7_REG) (0x264)

Table 5.18 displays the PHY VREF Register for DQS Groups 4 to 7. This register specifies the initial Vref values for DQS Groups 4 to 7. When PHY Vref Training is disabled (TRN_OP_REG.mc_vref_training_en=0), the value set in this register becomes the final Vref value.

Table 5.18. PHY VREF Register for DQS Groups 4-7

Field	Name	Access	Width	Reset
[31]	reserved	RSVD	1	—
[30:24]	phy_vref_dqs_grp7	RW	7	*MC DQS Grp7 Vref Value*
[23]	reserved	RSVD	1	—
[22:16]	phy_vref_dqs_grp6	RW	7	*MC DQS Grp6 Vref Value*
[15]	reserved	RSVD	1	—
[14:8]	phy_vref_dqs_grp5	RW	7	*MC DQS Grp5 Vref Value*
[7]	reserved	RSVD	1	—
[6:0]	phy_vref_dqs_grp4	RW	7	*MC DQS Grp4 Vref Value*

phy_vref_dqs_grp7

- Specifies the initial Vref value for DDRPHY DQS Group 7.

phy_vref_dqs_grp6

- Specifies the initial Vref value for DDRPHY DQS Group 6.

phy_vref_dqs_grp5

- Specifies the initial Vref value for DDRPHY DQS Group 5.

phy_vref_dqs_grp4

- Specifies the initial Vref value for DDRPHY DQS Group 4.

5.16. PHY VREF Register for DQS Group 8 (PHY_VREF_8_REG) (0x268)

Table 5.19 displays the PHY VREF Register for DQS Group 8. This register specifies the initial Vref values for DQS Group 8. When PHY Vref Training is disabled (TRN_OP_REG.mc_vref_training_en=0), the value set in this register becomes the final Vref value.

Table 5.19. PHY VREF Register for DQS Group 8

Field	Name	Access	Width	Reset
[31:7]	reserved	RSVD	25	—
[6:0]	phy_vref_dqs_grp8	RW	7	*MC DQS Grp8 Vref Value*

phy_vref_dqs_grp8

- Specifies the initial Vref value for DDRPHY DQS Group 8.

6. DDRPHY Example Design

This section describes the DDR Memory PHY Module Example Design, which is available to users for synthesis and simulation after successful IP generation. This example design does not support hardware evaluation. For hardware evaluation, refer to the DDR Memory Controller IP and DDR Memory Controller IP User Guide (FPGA-IPUG-02208). For steps on generating the DDRPHY IP Core, refer to the Designing and Simulating the IP section of this user guide.

6.1. Synthesis Example Design

After generating of the DDR Memory PHY, you have access to a synthesizable example design. This design allows you to run the Radiant flow to check resource utilization and Fmax for the selected DDR PHY Module IP configuration; it is not for hardware evaluation. For hardware evaluation, refer to the DDR Memory Controller IP and DDR Memory Controller IP User Guide (FPGA-IPUG-02208). Figure 6.1 shows a block diagram of the DDR Memory PHY Module Synthesis Example Design.

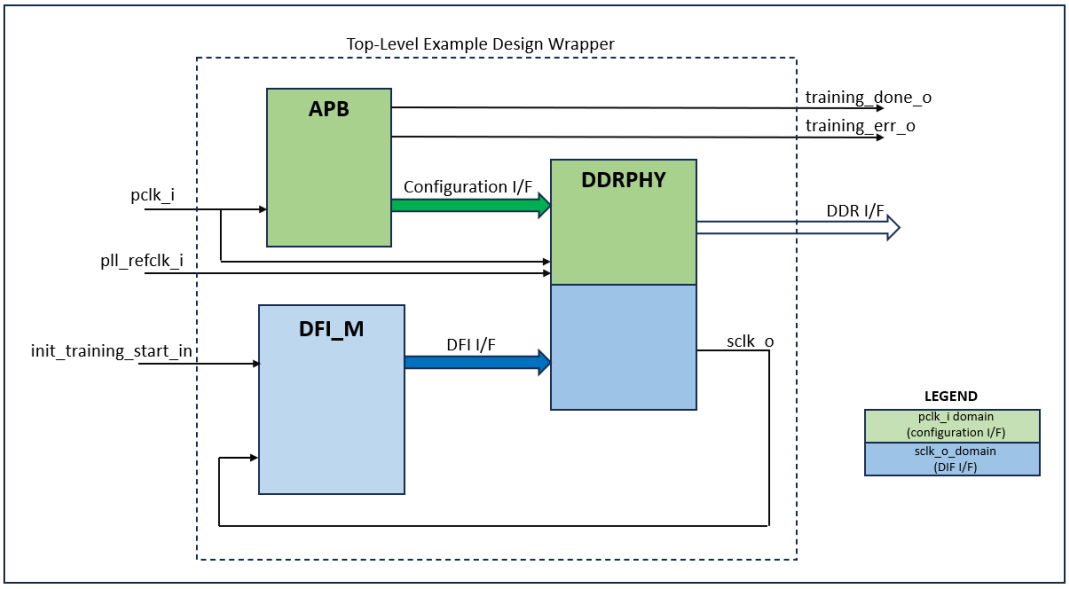

Figure 6.1. DDR Memory PHY Module Synthesis Example Design Diagram

The main blocks that make up the synthesizable example design include the following:

- Configuration interface (APB) block – This is an APB requestor to initiate training and is used for static timing analysis.
- DFI controller block – This drives the DFI interface. This block does not generate traffic data and is used only for testing the Radiant flow and static timing analysis.
- DDRPHY block – This is the DDR Memory PHY module.

The top-level example design wrapper file, eval_top.sv, provides ports for a PLL reference clock, a configuration interface clock (pclk_i), an APB block, a DFI_M block, and a DDRPHY block.

6.2. Simulation Example Design

The simulation example design is similar to the synthesizable example design, with the following changes:

- External DDR4/LPDDR4 memory is replaced with a DDR4/LPDDR4 memory model.

For instructions on simulating the DDR Memory PHY, including the example design, refer to the Designing and Simulating the IP section of this user guide.

7. Designing and Simulating the IP

This section describes the steps required within Lattice Radiant software to configure and generate the DDR Memory PHY Module. This section also provides information regarding design implementation and resource evaluation of the synthesizable example design. The screenshots provided in this section are for reference only and the details may vary depending on the version of the IP or software being used.

7.1. Generating the IP

This section describes the steps required to create, configure, and generate an instance of the DDR Memory PHY Module.

7.1.1. Creating a Radiant Project

In order to generate an instance of the DDRPHY IP, a Lattice Radiant project must first be created.

1. Launch the Lattice Radiant software and select **File > New > Project**. This will open the **New Project** dialog box. Click **Next**.

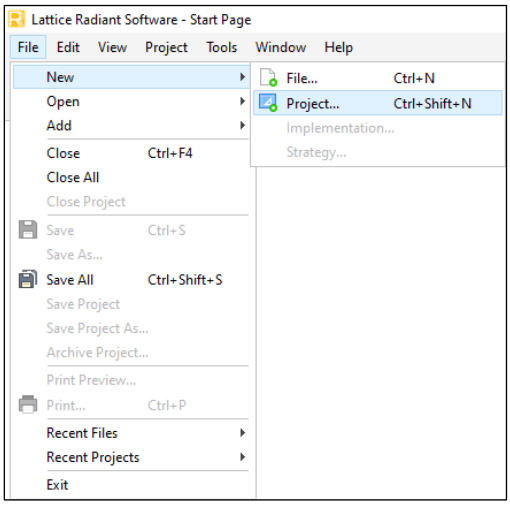

Figure 7.1. Creating a New Radiant Project

2. Specify a name (<project_name>) for the Lattice Radiant project, a directory (<project_directory>) to store the project files, and a top-level design implementation name (<top_level_instance_name>). Click **Next** two times.

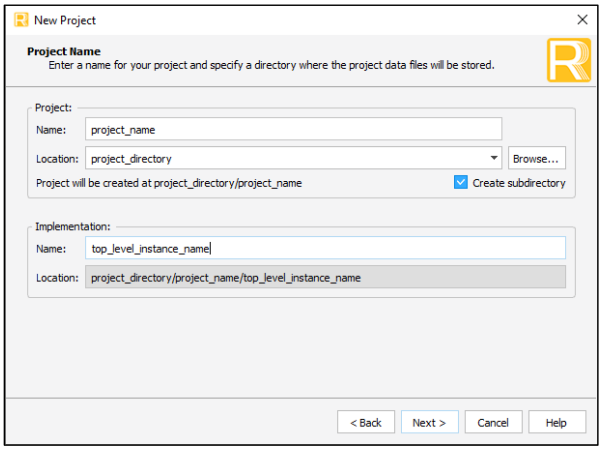

Figure 7.2. New Project Settings

3. Under **Family**, select Avant or Certus-N2. Under **Device, Package, Operating Condition, and Performance Grade**, make the appropriate selections representative of the selected device part number. Click **Next**.

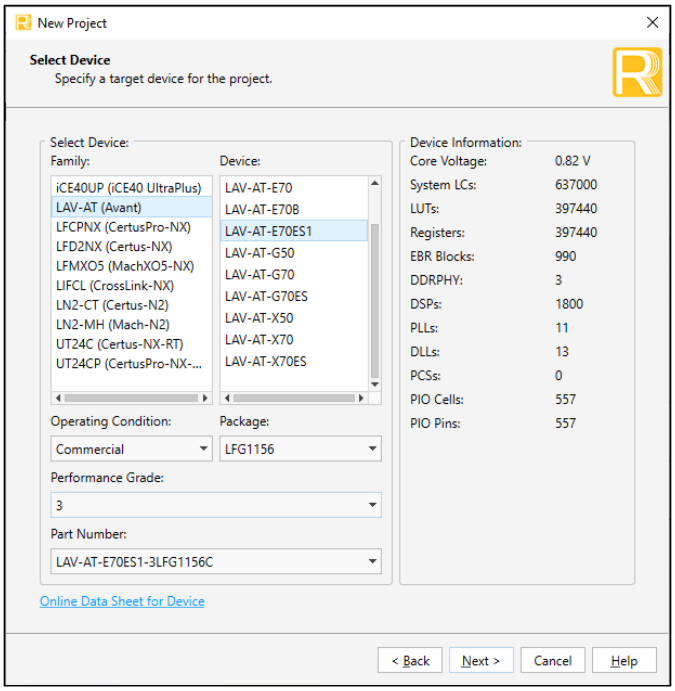

Figure 7.3. Project Device Settings

4. Specify the desired synthesis tool for implementation of the Lattice Radiant project. Click **Next** and **Finish**.

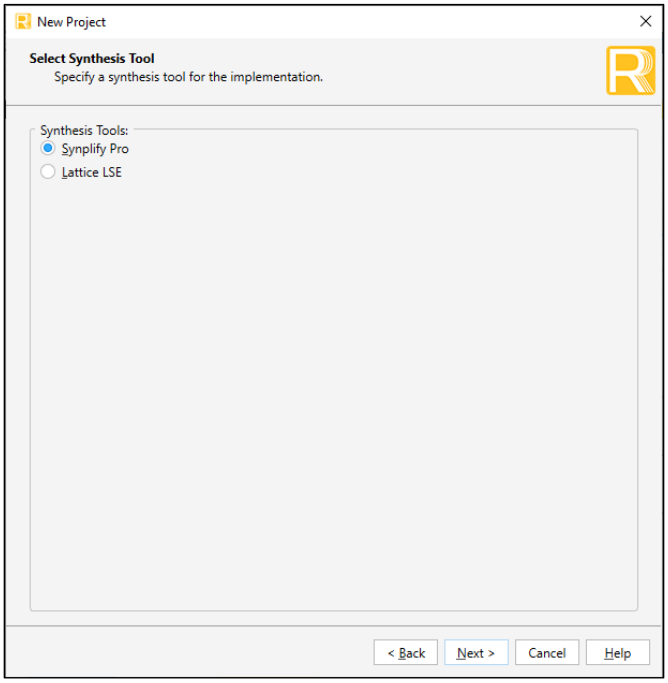

Figure 7.4. Project Synthesis Tool Selection

7.1.2. Configuring and Generating the IP

The following steps shows how to generate the DDR Memory PHY IP Core in Lattice Radiant software.

1. Under the **IP Catalog** (Tools > IP Catalog), locate and double-click on the desired DDRPHY IP listed under **Module > Architecture_Modules > IO**.
2. The **Module/IP Block Wizard** dialog box will open. Provide a name (<instance_name>) and directory (<instance_directory>) for the DDRPHY IP, where the default directory is set to project_directory>/<project_name>. Click **Next**.

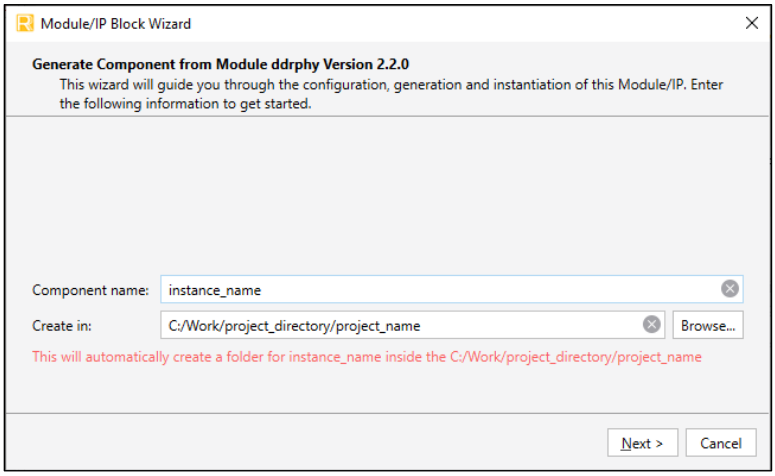

Figure 7.5. IP Instance Settings

3. The DDRPHY IP editor contains multiple tabs that need to be configured according to the desired DDR4/LPDDR4 memory interface implementation. For detailed information on the individual attributes, refer to the IP Parameter Description section of this user guide.
4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 7.6. Click **Finish**.

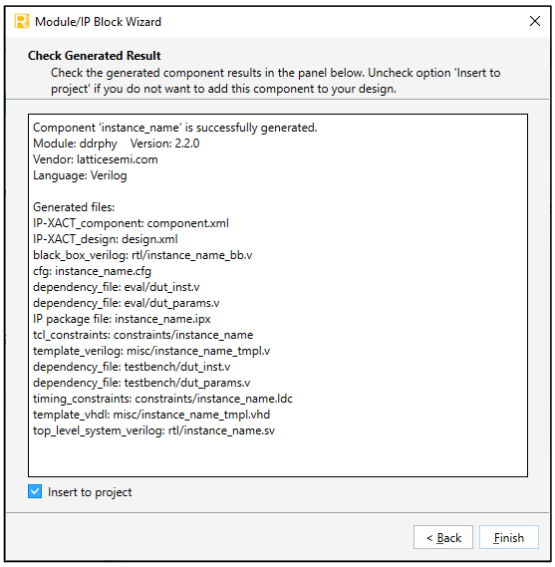

Figure 7.6. IP Generation Result

5. All the generated files are placed under the <instance_directory>/<instance_name> directory path. The generated files in this directory <instance_directory>/<instance_name> are listed in Table 7.1. Generated File List

Table 7.1. Generated File List

File Name	Description
component.xml	Contains the ipxact_component information of the IP.
design.xml	Lists the set parameters of the IP in IP-XACT 2014 format.
<instance_name>.cfg	Lists only the configured/changed parameter values set during IP configuration.
<instance_name>.ipx	Lists the files associated with IP generation.
constraints/<instance_name>.ldc	Defines the I/O standard for LPDDR4 memory interface signals.
eval/apb_m_init_trn.sv	Implements handshaking between APB accesses and internal RISC-V CPU for initialization of DDR4/LPDDR4 memory in DDR Memory PHY Module Example Design.
eval/clock_constraint.sdc	Pre-synthesis constraint for setting the PLL reference clock frequency of the DDR Memory PHY Module Example Design.
eval/constraint.pdc	Post-synthesis constraints for the DDRPHY Example Design.
eval/dut_inst.v	Instantiation of generated IP core in eval_top.sv for DDR Memory PHY Module Example Design.
eval/dut_params.v	Defines local parameters for eval_top based on parameter values set during IP configuration for DDR Memory PHY Module Example Design.
eval/eval_top.sv	Top-level RTL file for the DDR Memory PHY Module Example Design.
eval/lscc_dfi_m_model_dummy.sv	Drives the DFI I/F with random values this is only used for static timing analysis and should not be used for functional simulation of the DFI I/F.
eval/lscc_dummy_model_lfsr.sv	Used inside lscc_dfi_m_model_dummy.
eval/select_protocol.py	Script that defines LPDDR4 protocol for eval_top and tb_top files in DDR Memory PHY Module Example Design.
misc/<instance_name>_tmpl.v misc/<instance_name>_tmpl.vhd	These files provide instance templates for the IP core.
rtl/<instance_name>.sv	Example RTL top-level file that instantiates the IP core.
rtl/<instance_name>_bb.v	Example synthesizable RTL black box file that instantiates the IP core.
testbench/debug_c_code.sv	For internal use only.
testbench/dq_bit_swizzle.vh	Specifies the MC to DRAM connection based on the Bit Swizzle settings.
testbench/dut_inst.v	Template instance files.
testbench/dut_params.v	List of parameters based on user IP configurations.
testbench/tb_top.sv	Top level testbench file.
testbench/ddr4/ testbench/lpddr4/	Contains DDR4/LPDDR4 memory model and instances for simulation.

7.2. Design Implementation

A memory controller is required to run the DDR Memory PHY Module Example Design on hardware. For hardware evaluation, please refer to the DDR Memory Controller IP and DDR Memory Controller IP User Guide (FPGA-IPUG-02208).

7.2.1. Pin Placement

In the Lattice Avant and Lattice Nexus 2 FPGA devices, external memory interfaces are supported in the DDRPHY, which is composed of three High Performance I/O (HPIO) banks. These banks are labeled as HIGHSPEED in the device pinout tables. Since Avant and Nexus 2 leverage a hardened PHY, the external memory interface pinouts are in fixed locations, where each pin location is specified under DDRPHY in the device pinout tables. Dedicated clock routing within HPIO banks is represented as PLL or PCLK, and dedicated reference voltage pins are represented as VREF, in the device pinout tables. For more information refer to the High-Speed I/O User Guide and Pinout files located on the Avant-E/G/X and Certus-N2 web pages.

Observe the following guidelines when placing pins for external memory interfaces:

- Ensure that pins for external memory interfaces reside within a DDRPHY.
- The input reference clock to the PLL must be assigned to use dedicated clock routing (GPLL). It is recommended to place the input reference clock on a dedicated PLL pin (GPLL) within the HPIO bank to improve performance and minimize jitter and routing.

Always test proposed pinouts in Lattice Radiant software with correct I/O standards before finalizing. Note that unused pins within a DDRPHY can be used as general-purpose I/O under certain conditions. Refer to the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) more details.

7.2.2. Constraints

To ensure proper design coverage and hardware functionality, you must include the necessary constraints from Table 7.2 in their DDRPHY IP project.

Table 7.2. Project Constraints

File Name	Description	Action Required
DDRPHY IP LDC file: constraints.sdc/<instance_name>.ldc	Sets the I/O type for each of the ports necessary to interface with DDR4/LPDDR4 SDRAM.	No – these constraints are automatically propagated.
Clock Constraint SDC file: eval/clock_constraint.sdc	Contains an example constraint for the input PLL reference clock.	Yes – user needs to include a create_clock constraint based on the frequency for the input PLL reference clock. This can be placed in a user-created SDC or PDC file.
Example Design PDC file: eval/constraint.pdc	Contains generated constraints based on IP configuration.	Yes – user needs to copy example design constraints to run the DDRPHY Example Design.

7.2.2.1. Reference Clock SDC

The provided clock_constraint.sdc file contains a single create_clock constraint for the PLL reference clock (pll_refclk_i). This constraint is necessary for the PLL to generate the constraint for its output clock. You should copy this constraint into the Radiant Project SDC file (not in PDC file) to allow the synthesis tool to optimize the logic for the target clock.

7.2.2.2. Example Design PDC

The provided constraint.pdc file contains eval constraints – specific to the DDRPHY Example Design.

The eval constraints include set_false_path, set_max_delay, and ldc_create_group constraints and should only be copied if running the provided DDRPHY Example Design. Refer to the Lattice Radiant Timing Constraints Methodology User Guide (FPFA-AN-02059) for details regarding the implementation of constraints.

7.3. Example Design Simulation

After configuring and generating the DDRPHY IP Core, you can use the included example design to simulate the DDR4/LPDDR4 memory interface. All associated simulation files are located in the testbench directory. Refer to Table 7.2 for more details.

The following steps illustrate how to prepare the DDRPHY Example Design project for simulation.

1. After generating the DDR Memory PHY IP Core, the Radiant project should include the <instance_name>.ipx under the project's input files. If it is not included, right-click on **Input Files** and select **Add > Existing File** under the **File List** tab in the lower-left corner of the Radiant window. This action opens an **Add Existing File** dialog box. Navigate to the <instance_directory>/<instance_name> directory and select the <instance_name>.ipx file. Ensure the **Copy file to directory** option is unchecked. Click **Add**.
2. To add the top-level example design file to the project, right-click on **Input Files** and select **Add > Existing File**. This action opens an **Add Existing File** dialog box. Navigate to the eval directory and select the eval_top.sv file. Ensure the **Copy file to directory** option is unchecked. Click **Add**.

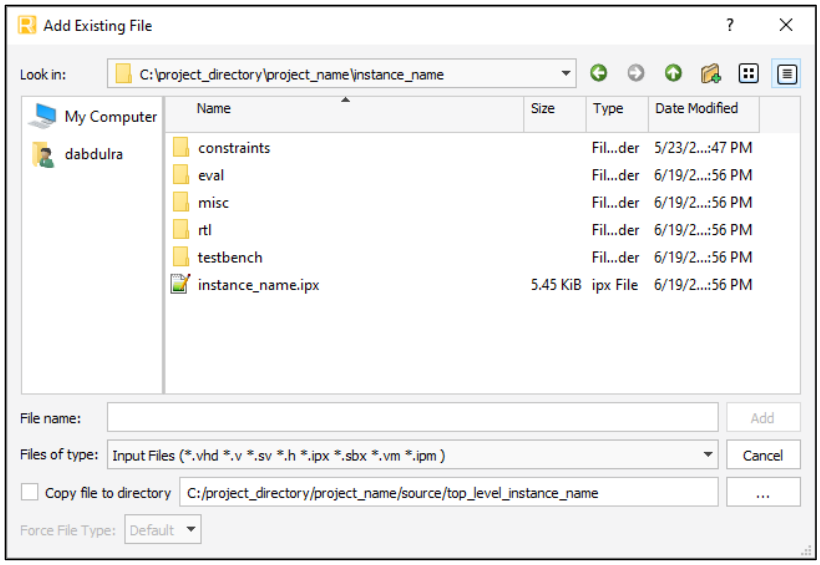

Figure 7.7. Add Existing File Dialog Box

3. To add the top-level testbench file to the project, select **File > Add > Existing Simulation File**. This action opens an **Add Existing Simulation File** dialog box. Navigate to the testbench directory and select the tb_top.sv file. In the **Add Existing File** dialog box, ensure the **Copy file to directory** option is unchecked. Click **Add**.
4. Before creating the simulation environment, set the SIM parameter in eval_top.sv to 1. This parameter shortens the initialization sequence of the DDR4/LPDDR4 interface.

When SIM is set to 1, it programs 0x01C to the Training Operation Register (TRN_OP_REG) to speed up the simulation runtime by reducing the reset and CKE initialization time. You can configure the simulation of reset, initialization, and training sequences by forcing the value of TRN_OP_REG, as indicated by locating the following comment in tb_top.sv:

```
// This force shortens the initialization, vref trainings are also skipped
// force
tb_top.u_eval_top.u_lp4mc_0.lscc_lpddr4_mc_inst.u_trn_eng.i_csr.trn_operation_reg =
10'h01C;
```

It is also recommended to skip the training sequences by writing 10’h01C to TRN_OP_REG/trn_opr_i. This action reduces simulation time by programming the verified trained values to the PHY.

To create the simulation environment for the DDR Memory PHY Module Example Design, the follow these steps:

1. Launch the simulation wizard in Radiant by selecting **Tools > Simulation Wizard**. This action opens the **Simulation Wizard** dialog box. Click **Next** and provide a name (<sim_name>) and directory (<sim_directory>) for the simulation project. The default directory is set to <project_directory>/<project_name>. Click **Next**.

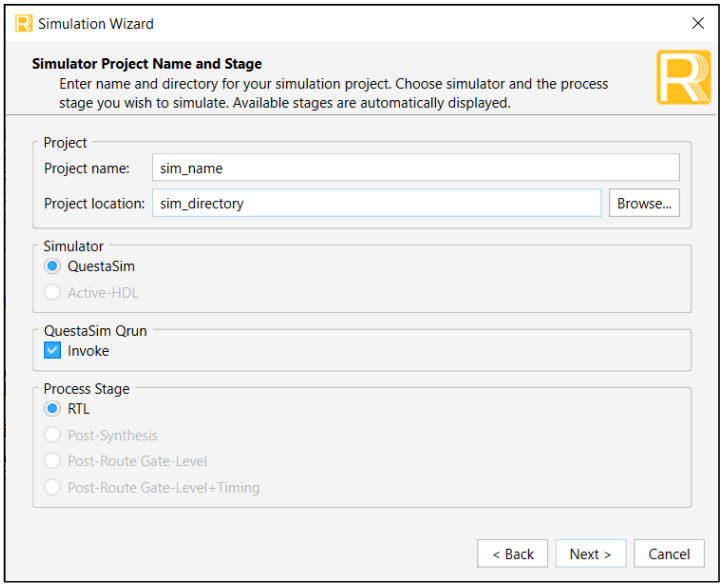

Figure 7.8. Simulation Wizard

2. In the **Add and Reorder Source** window, note that the **Source Files** only contain the top-level evaluation (eval_top.sv) and top-level testbench (tb_top.sv) files. Click **Next**.

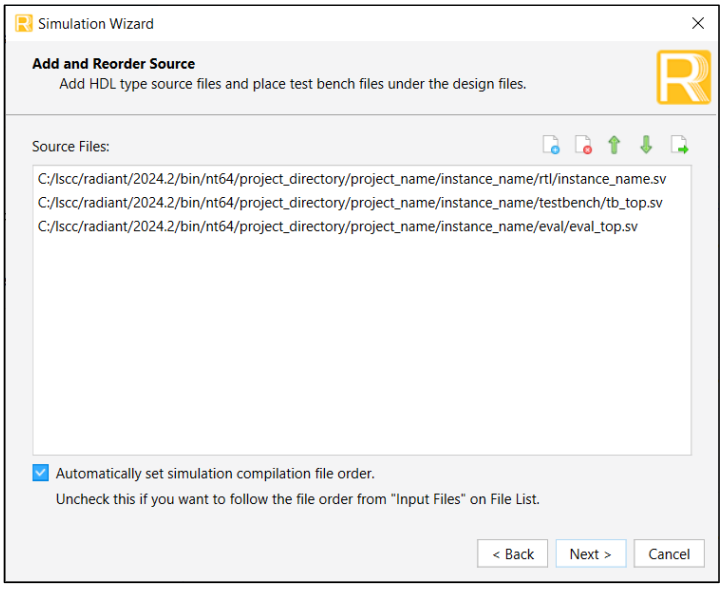

Figure 7.9. Adding and Reordering Simulation Source Files

3. In the **Parse HDL files for simulation** window, note that the **Simulation Top Module** is set to tb_top. Click **Next**.

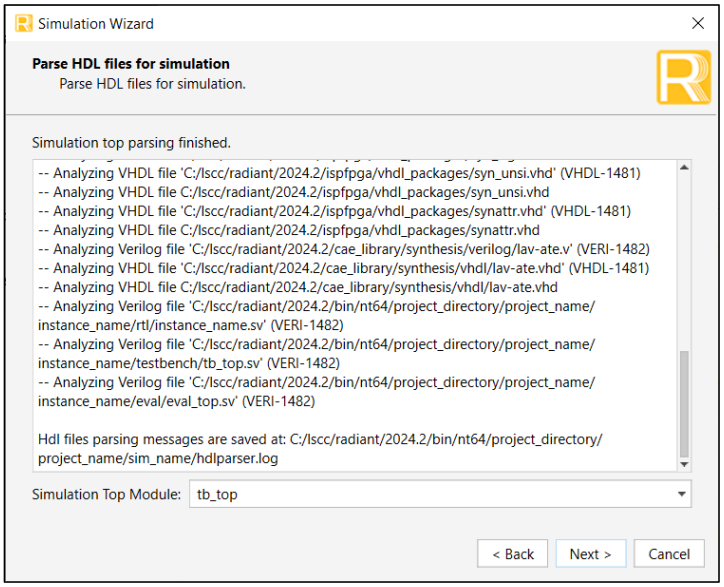

Figure 7.10. Parsing Simulation HDL Files

The following error message is expected during the parsing of the HDL files using the Simulation Wizard. This message is due to the DDR4 simulation model being encrypted. They will not affect the simulation behavior since Questasim can decrypt the DDR4 memory model:

```
ERROR <1009990> - key keyowners are not support. Must have “Lattice Semiconductor”.
```

4. This action opens the **Summary** window. By default, the simulation will run for 100 ns, allowing you to configure the waveform to log signals of interest in the Questasim simulator before continuing. You can then enter the following TCL command in Questasim to run the simulation until completion: run -all. Alternatively, if you wish to run the simulation with the default top-level signals, you can change the 100 ns value to 0 µs to execute the simulation completely.

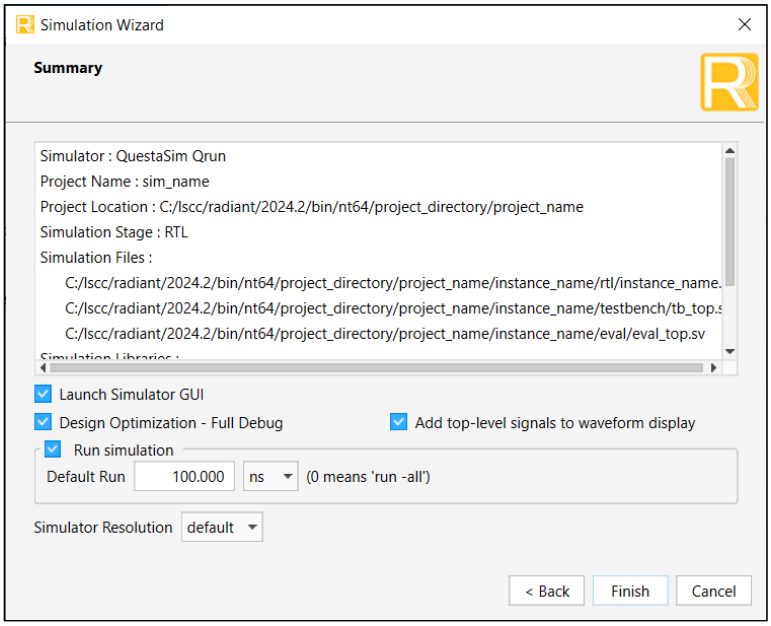

Figure 7.11. Simulation Summary

The results of the DDRPHY simulation design are shown in Figure 7.12.

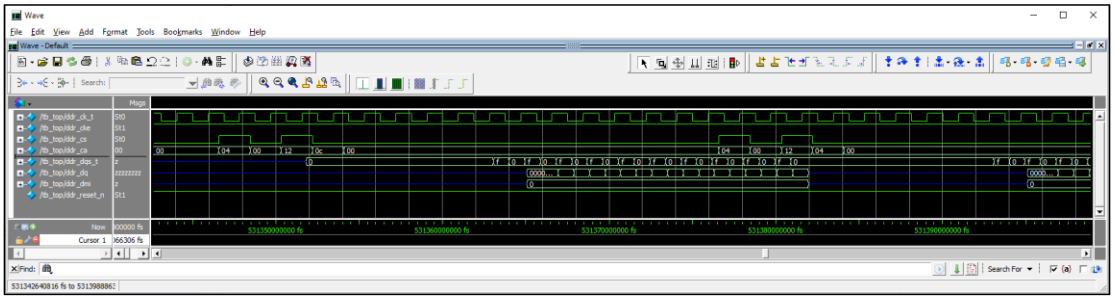

Figure 7.12. Simulation Result Waveform

The Questasim simulation log expects the following error messages and disregard them. These messages violate the timing requirements of the LPDDR4 simulation model due to the shortened reset and CKE initialization:

```
# tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected> 26083125000 : ###  lpddr4_debug
RESET_n high input
# tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected> 26083125000 : ###  lpddr4_debug
RESET_n high input
# Error: tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected>.<protected> 26083125000  tINIT1
Error.
# Error: tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected>.<protected> 26083125000  tINIT1
Error.
# tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected> 32804075000 : ###  lpddr4_debug CKE
high input
# tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected> 32804075000 : ###  lpddr4_debug CKE
high input
# Error: tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected>.<protected> 32804075000  tINIT3
Error.
# Error: tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected>.<protected> 32804075000  tINIT3
Error.
```

Appendix A. Resource Utilization

Table A.1 and Table A.2 display the configuration and resource utilization for IP Core v2.5.0 implemented for LAV-AT-X70 using Synplify Pro of Lattice Radiant software 2025.2.

Table A.1. DDR4 Resource Utilization for IP Core v2.5.0

Configuration	sclk_o Fmax[1] (MHz)	Registers	LUTs	EBR	DSP
Interface Type = DDR4, DDR Bus Width = 16, Clock Frequency = 1200, Others = Default	300	1,488	2,238	16	0
Interface Type = DDR4, DDR Bus Width = 32, Clock Frequency = 1200, Others = Default	300	1,487	2,133	16	0
Interface Type = DDR4, DDR Bus Width = 64, Clock Frequency = 1200, Others = Default	300	1,488	2,146	16	0
Interface Type = DDR4, DDR Bus Width = 40, Side Band ECC Enable = Checked, Clock Frequency = 1200, Others = Default	300	1,515	2,156	16	0
Interface Type = DDR4, DDR Bus Width = 72, Side Band ECC Enable = Checked, Clock Frequency = 1200, Others = Default	300	1,516	2,167	16	0

Note:

1. The sclk_o Fmax is generated using the top-level example design wrapper file, eval_top.sv, that is described in the Synthesis Example Design section of this User Guide. These values may increase when the IP Core is used with the user logic.

Table A.2. LPDDR4 Resource Utilization for IP Core v2.5.0

Configuration	sclk_o Fmax[1] (MHz)	Registers	LUTs	EBR	DSP
Interface Type = LPDDR4, DDR Bus Width = 16, Clock Frequency = 1200, Others = Default	300	1,688	2,225	16	0
Default	300	1,689	2,219	16	0
Interface Type = LPDDR4, DDR Bus Width = 64, Clock Frequency = 1200, Others = Default	300	1,689	2,229	16	0

Note:

1. The sclk_o Fmax is generated using the top-level example design wrapper file, eval_top.sv, that is described in the Synthesis Example Design section of this User Guide. These values may increase when the IP Core is used with the user logic.

Appendix B. Known Issues

1. Some DQ swizzle settings on DQS group 1 may encounter a CBT error due to the initialization values of the DDRPHY Hard IP's input DQ, making it appear that the CBT pattern is already matching at the very start of CBT. This issue will only occur in simulation and will not occur on hardware since the real default input DQ value in silicon will be zero, due to the DQ signal being in high-impedance state, and the termination pulling it down to zero. The simulation model issue occurs when using Lattice Radiant 2025.2 or earlier.

References

For more information refer to:

- DDR Memory PHY IP Release Notes (FPGA-RN-02072)
- Lattice Radiant Timing Constraints Methodology User Guide (FPGA-AN-02059)
- Debugging with Reveal Usage Guidelines and Tips Application Note (FPGA-AN-02060)
- Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Lattice Radiant FPGA design software
- AMBA APB Protocol Specification
- DFI 4.0 Specification
- DDR4 JEDEC Standard
- LPDDR4 JEDEC Standard
- Lattice Sales Office for more information about pricing and availability of the DDRPHY IP
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.4, IP v2.5.0, December 2025

Section	Change Summary
All	Updated IP version from *2.4.0* to *2.5.0*.
Introduction	• Added table notes *1* and *2* in Table 1.1. Quick Facts. • Added *Bit Swizzle* and 2-D Vref Training features in Table 1.2. DDR4 Features Overview, LPDDR4 Features section, and Table 1.3. LPDDR4 Features Overview.
Functional Description	• Added Read Training Limitation for LPDDR4 at 350MHz and 400MHz section. • Enabled *BLTS for 800 MHz/1,600 Mbps* in Calibration section. • Updated Bit-Level Trim Sweep (BLTS) section. • Added 2-D Vref Training section. • Added Bit Swizzle section.
IP Parameter Description	• Added *Enable Bit Swizzle* option in Table 3.9. LPDDR4 General Attributes. • Added Bit Swizzle Settings section.
Signal Description	Updated the description of *pll_refclk_i*, *pll_rst_n_i*, *pll_lock_o*, and *rst_i* signals in Table 4.1. Clock and Reset Port Definitions.
Register Description	• Updated the *register offset range* for registers that are reserved for the Training CPU in Table 5.1. Summary of DDRPHY Module Registers. • Updated the description of *read_trn_err bit* of Training Operation Register.
Designing and Simulating the IP	Updated the *generated file list* in Table 7.1. Generated File List.
Appendix A	Updated resource utilization.
Appendix B	Added this section.
Revision History	Added a note, *In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates* in this section.

Revision 1.3, IP v2.4.0, June 2025

Section	Change Summary
All	• Minor editorial fixes. • Updated IP version from *2.3.0* to *2.4.0*.

Introduction	• Updated Supported Devices and removed Target Devices in Table 1.1.
	• Updated DDR4 Features:
	  • x8 and x16 DDR4 device support (8:1 DQ:DQS ratio)
	  • Configurable CAS latencies for Reads and Writes based on target interface speed
	  • Supports component (DRAM soldered on the board) and UDIMM.
	• Added CS Training, updated Bit-Level Trim Sweep and Data Bus Inversion in Table 1.2.
	• Updated Automatic VREF Training to *Not yet supported* in Table 1.2.

IP Parameter Description	• Removed Enable DBI, and updated *Read Latency* and *Write Latency* in Table 3.1. • Updated *I/O Buffer Type*, *Read Latency* and *Write Latency* description in Table 3.4. • Updated DDR4 training settings in Table 3.5. • Added DDR4 training settings: Table 3.6 and Table 3.7. • Updated DDR4 training settings description in Table 3.8. • Change parameter name from Enable DBI to Enable Read DBI in Table 3.9. • Updated LPDDR4 training settings in Table 3.13. • Added LPDDR4 training settings: Table 3.14 and Table 3.15. • Updated LPDDR4 training settings description in Table 3.16.

Section	Change Summary
Signal Description	• Updated descriptions of pll_refclk_i, pclk_i, rst_i in Table 4.1. • Added note 2 in Table 4.5.
Register Description	• Updated description for INIT_CTRL_REG and added Vref registers in Table 5.1. • Removed phy_reset in Reset Register section. • Removed Initialization Control Register section. • Modified Mode Register Write Control Register section. • Added CS delay in Clock/Address/Control Trim Register section. • Added DDR4 mode in ODT Settings Register section. • Added Vref setting sections: DRAM VREF Register, PHY VREF Register for DQS Groups 0-3, PHY VREF Register for DQS Groups, and PHY VREF Register for DQS Group 8.

Revision 1.2, IP v2.3.0, March 2025

Section	Change Summary
All	• Changed the document title from *DDR Memory PHY Module for Avant Devices* to *DDR Memory PHY Module*. • Reworked document content and structure for clarity. • Removed *DDR3L support*. • Added *IP version 2.3.0* in the cover page.
Abbreviations in This Document	• Replaced *Acronyms* with *Abbreviations*. • Reworked section contents.
Introduction	• Reworked section contents. • Added IP Validation Summary, Licensing and Ordering Information, and Minimum Device Requirements subsections. • Reworked *1.3 Conventions* section and renamed to subsection 1.6 Naming Conventions.
Functional Description	• Reworked subsection *2.1. Overview* and renamed to subsection 2.1 IP Architecture. • Added Clocking, Reset and User Interfaces subsections. • Reworked subsection *2.5. Initialization and Training* and renamed to subsection 2.5 Calibration. • Reworked *subsection 2.2.1 DFI Signals Consideration* and moved under *subsection* 2.6 Operations Descriptions.
IP Parameter Description	Reworked subsection *2.3 Attributes Summary* and moved this under the IP Parameter Description section.
Signal Description	Reworked subsection *2.2 Signal Description* and converted it to Signal Description section.
Register Description	Reworked subsection *2.4 Register Description* and converted it to Register Description section.
DDRPHY Example Design	Added this section.
Designing and Simulating the IP	Reworked the *IP Generation, Simulation, and Validation section* and converted it to Designing and Simulating the IP section.
Appendix A. Resource Utilization	Reworked section contents.
References	Reworked section contents.

Revision 1.1, December 2023

Section	Change Summary
Disclaimers	Updated disclaimers.
Inclusive Language	Added inclusive language boilerplate.
Acronyms in This Document	Added acronyms definition.
Introduction	• Added supported interfaces for DDR4 and DDR3L in the Introduction section. • Added support for LAV-AT-G70 and LAV-AT-X70 devices in Table 1.1 Quick Facts. • Updated supported frequencies, DDR widths, and training and initialization support in

Section	Change Summary
	the Features section.

Functional Description	• Updated the Overview section.
	• Updated the following tables:
	  • Table 2.1. DDR Memory PHY Module Signal Description
	  • Table 2.2. Attribute Table
	  • Table 2.3. Attribute Description
	  • Table 2.4. Summary of DDRPHY Module Registers
	• Updated the following registers in the Registers Description section:
	  • Feature Control Register (FEATURE_CTRL_REG)
	  • Reset Register (RESET_REG)
	  • PHY Clock Register (PHY_CLOCK_REG)
	  • Interrupt Status Register (INT_STATUS_REG)
	  • Interrupt Enable Register (INT_ENABLE_REG)
	  • Interrupt Set Register (INT_SET_REG)
	  • Initialization Control Register (INIT_CTRL_REG)
	  • Training Operation Register (TRN_OP_REG)
	  • Training Status Register (TRN_STATUS_REG)
	• Added the following registers in the Register Description section:
	  • Time Out Register (TIMEOUT_REG)
	  • Time Reload Register (TIMER_RELOAD_REG)
	  • Mode Register Write Control Register (MRW_CTRL_REG)
	  • Trim Settings 1 Register (TRIM_SETTINGS_1_REG)
	  • ODT Settings Register (ODT_SETTINGS_REG)
	• Updated the Initialization and Training section.
	• Added the Bit-Level Trimp Sweep section.

IP Generation, Simulation, and Validation	• Updated Figure 3.1, Figure 3.2, Figure 3.3, and Table 3.1 in the Configuring and Generating the IP section. • Updated Running Functional Simulation section. • Added a reference to the Lattice Radiant Timing Constraints Methodology in the Constraining the IP section.
Resource Utilization	Updated the Resources Utilization section.
References	Added references.
Technical Support Assistance	Added link to the Lattice Answer Database.

Revision 1.0, November 2022

Section	Change Summary
Introduction	• Updated device name, software version and resource utilization in Table 1.1. • Updated Features section to add DDR4 Support and Self-Calibrating Logic, and updated the supported frequencies and DDR data widths.
Functional Description	• Updated Table 2.1 to add DDR4-specific signals • Updated Table 2.2 and Table 2.3 to add DDR4-related attributes. • Updated Table 2.4 with additional registers • Updated ddr_type and addr_translation fields of Feature Control Register section. • Added pll_ref_clk field in PHY Clock Register section. • Added ddr_ck_dis and updated dfi_cke in Initialization Control Register section. • Added mem_verf_training_en and mc_vref_training_en in Training Operation Register section. • Added Scratch Registers in Table 2.4 and added section 2.4.15 for these registers. Removed Read Gate Leveling section and added Self-Calibrating Logic section.

Section	Change Summary
IP Generation, Simulation, and Validation	• Updated section name. • Updated Figure 3.1, Figure 3.2, and Figure 3.3 in Configuring and Generating the IP section. • Updated Running Functional Simulation section. Added Constraining the IP section.
Appendix A. Resource Utilization	Added Resource Utilization section.
References	Added web page references of Avant and JEDEC.

Revision 0.8, May 2022

Section	Change Summary
All	Preliminary Release

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