Lattice Avant OSC Module

User Guide

FPGA-IPUG-02184-1.2

December 2023

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
LSE	Lattice Synthesis Engine

1. Introduction

The Lattice Semiconductor OSC Module is designed to generate a clock signal that can be used for FPGA clock tree and any Lattice Avant™ IP that needs a non-PLL based clock source. It has dynamically selectable clock frequency between 400 MHz or 320 MHz clock depending on the selected device with 1–256 programmable divider options.

1.1. Features

The key feature of this module is selectable 400 MHz or 320 MHz clock with 1–256 programmable divider for global clock tree.

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals

1.2.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

The Lattice Avant OSC Module generates a clock with maximum frequency of 400 MHz. Figure 2.1 shows the top-level block diagram of the OSC wherein the clk_out_o is selectable between 400 MHz and 320 MHz using the input port clk_sel_i and has programmable feature.

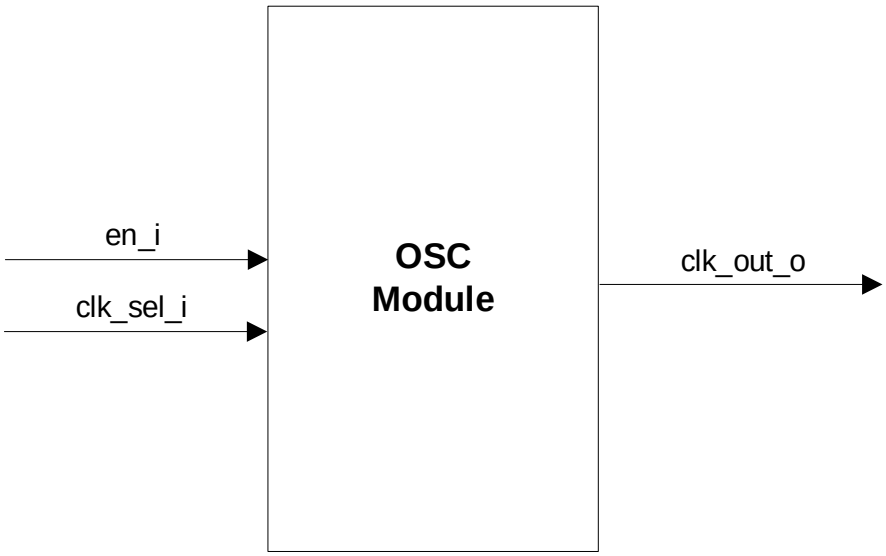

Figure 2.1. OSC Module Block Diagram

2.1. Signal Descriptions

Table 2.1. OSC Module Signal Description

Port Name	I/O	Width	Description
Clock ports			
clk_sel_i	In	1	Control signal to dynamically switch between 400 MHz and 320 MHz. • 1'b1 – 320 MHz • 1'b0 – 400 MHz
clk_out_o	Out	1	Programmable clock output.
Enable Ports			
en_i	In	1	Control signal to enable user clock.

2.2. Attribute Summary

The configurable attributes of the OSC Module are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant™ software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
Oscillator Clock (MHz)	400, 320	400	—
CLK Divider	Calculated	1	*Oscillator Clock/Result Frequency*
Output Clock			
Frequency (MHz): clk_sel_i = 0	1.5625 – 400.0	400	Active if *Oscillator Clock = 400*
Frequency (MHz): clk_sel_i = 1	1.25 – 320	320	Active if *Oscillator Clock = 320*

Table 2.3. Attributes Descriptions

Attribute	Description
General	
Oscillator Clock (MHz)	Displays the target maximum clk_out_o frequency.
CLK Divider	Displays the calculated divider of the user clock.
Result	
Frequency (MHz): clk_sel_i = 0	Displays the selectable desired frequency when control signal clk_sel_i is low.
Frequency (MHz): clk_sel_i = 1	Displays the selectable desired frequency when control signal clk_sel_i is high.

3. IP Generation, Simulation, and Validation

This section provides information on how to generate and synthesize this module using the Lattice Radiant software. For more on the Lattice Radiant software, refer to the Lattice Radiant software user guide and relevant tutorials.

3.1. Generating the IP

The Lattice Radiant software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the OSC Module in Lattice Radiant software is described below.

To generate the OSC Module:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **OSC** under **Module, Architecture_Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

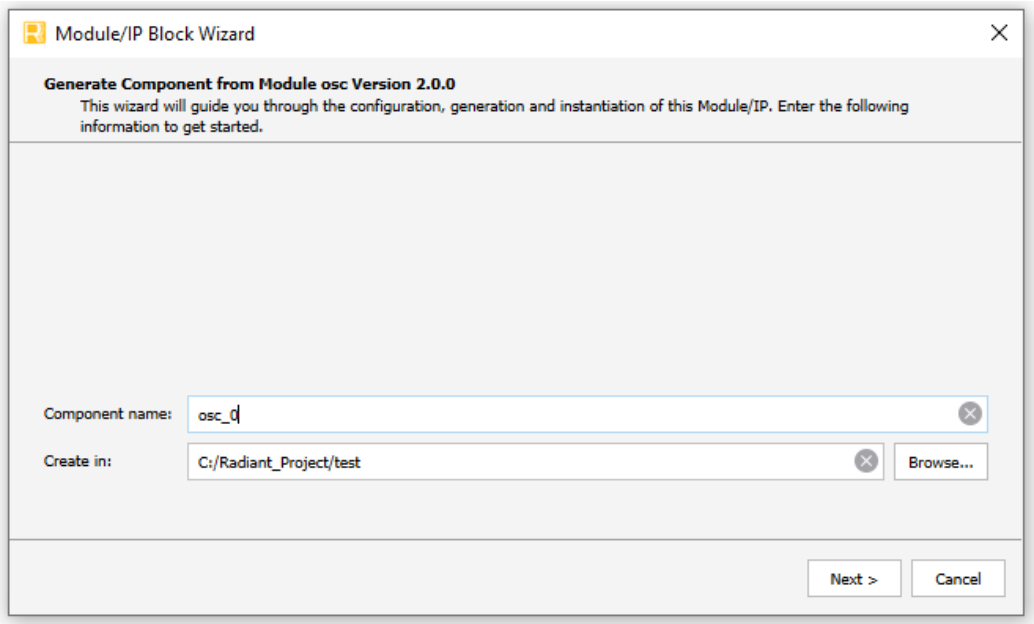

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected OSC Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

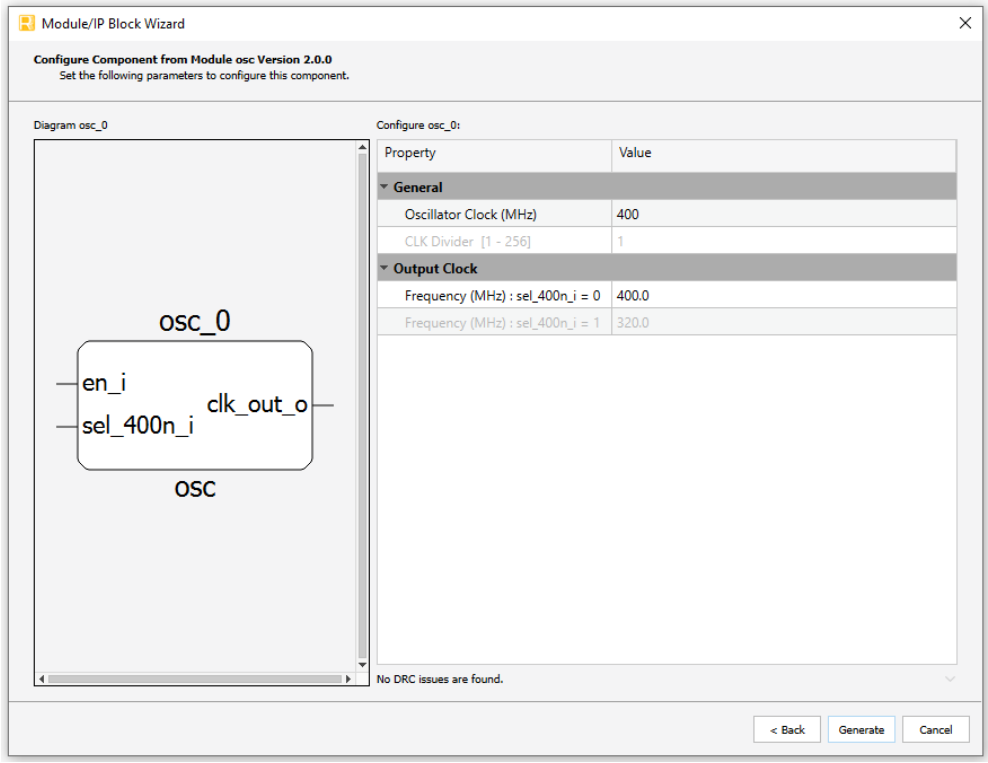

Figure 3.2. Configure User Interface of OSC Module

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

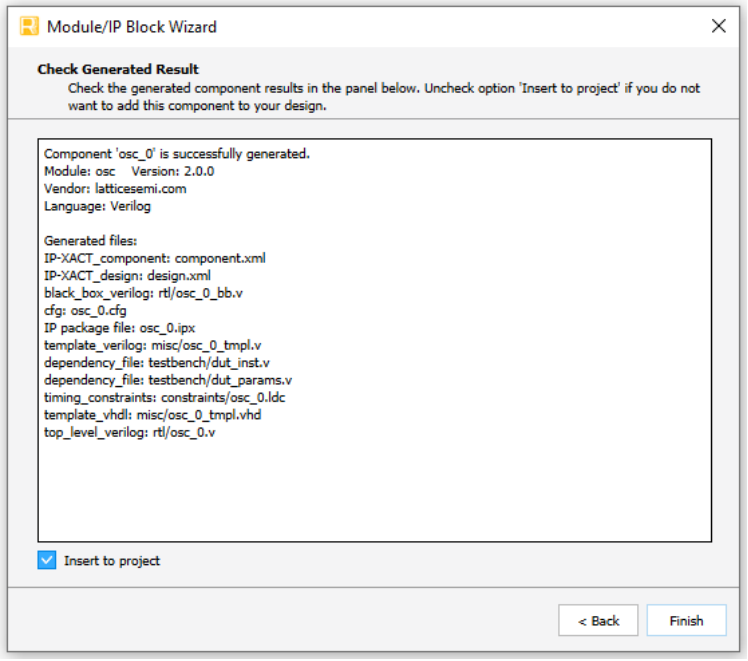

Figure 3.3. Check Generating Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated OSC Module package includes the black box (<Component Name>_bb.v) and component templates (<Component Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Component Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Component Name>.ipx	This file contains the information on the files associated to the generated IP.
<Component Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Component Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/< Component Name>_bb.v	This file provides the synthesis black box.
misc/< Component Name>_tmpl.v misc /< Component Name>_tmpl.vhd	These files provide component templates for the module.
testbench/dut_inst.v	Instantiated version of the <Component Name>.v file for simulation use.
testbench/dut_params.v	Top Level parameters of the generated RTL file.
testbench/tb_top.v	Testbench template, you can modify this to match your specific needs.

3.2. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run Verilog simulation:

1. Click the  button located on the Toolbar to initiate the Simulation Wizard shown in Figure 3.4.

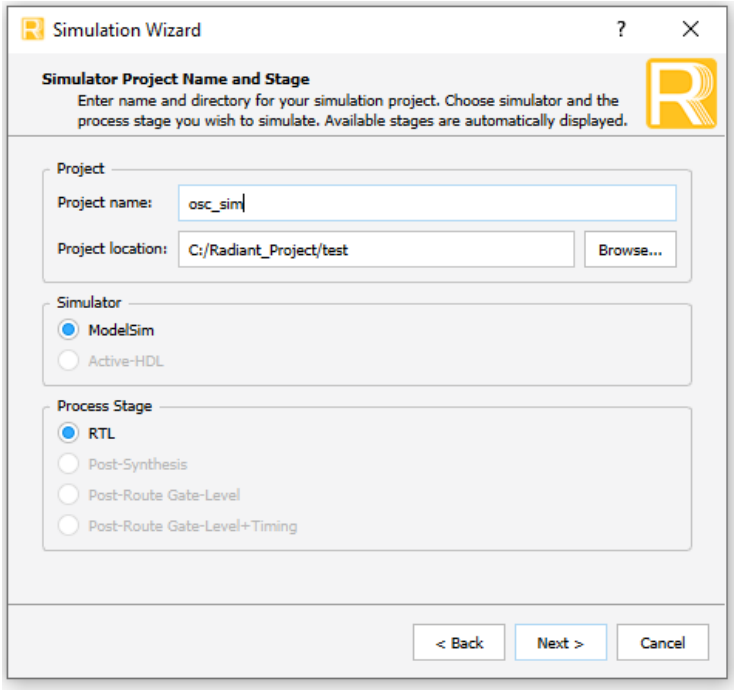

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

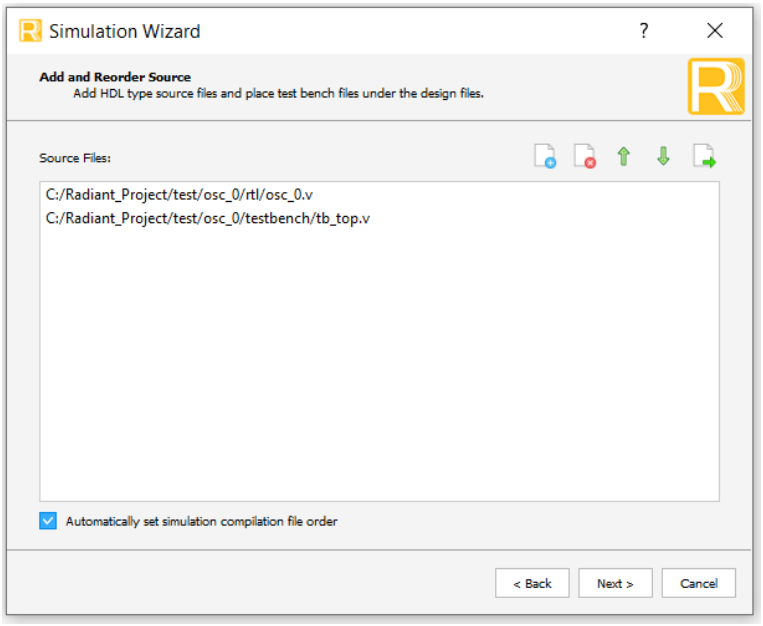

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

An example of the simulation results is shown in Figure 3.6.

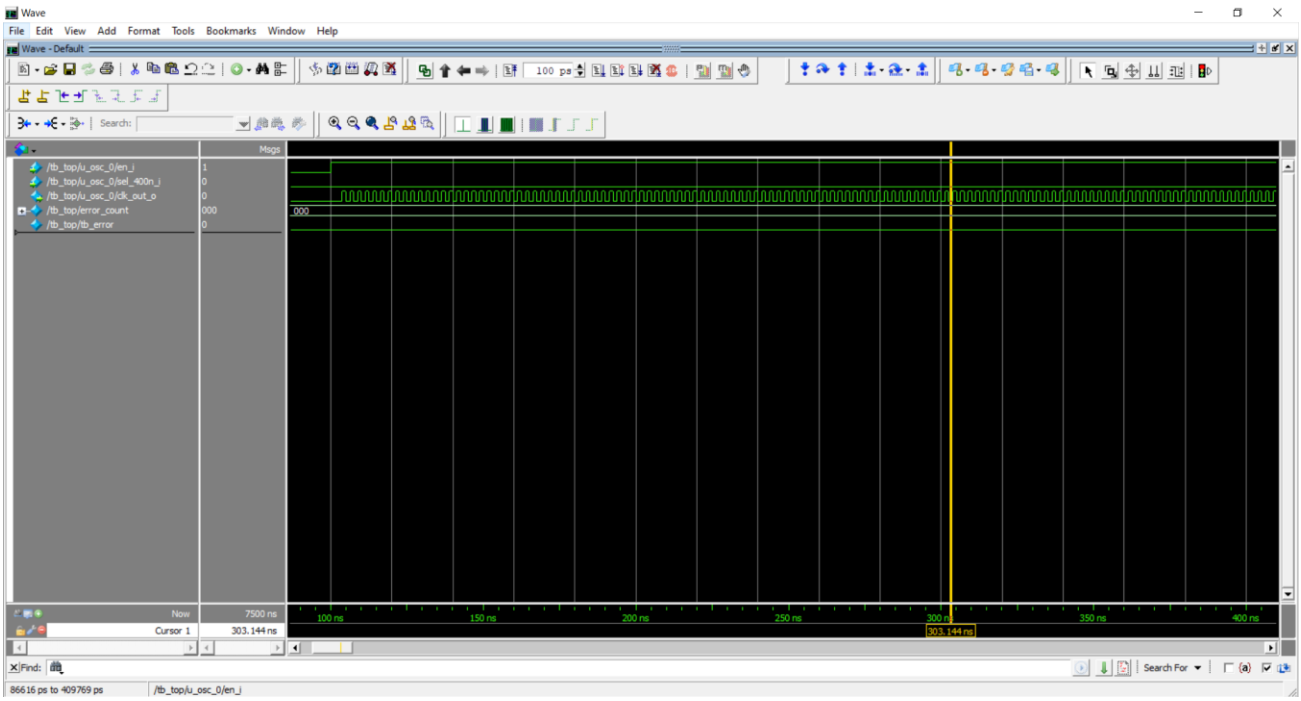

Figure 3.6. Simulation Waveform

3.3. Constraining the IP

You need to provide proper timing and physical design constraints to ensure that the design meets the desired performance goals on the FPGA. Add the content of the following IP constraint file to your design constraints: *<Instance_Path>/<Instance_Name>/constraints/<Instance_Name>.ldc*

The constraint file has been verified with the IP instantiated directly in the top-level module. You can modify the constraint in this file with a complete understanding of the effect of the constraint.

To use this constraint file, copy the content of the <Instance_Name>.ldc to the top-level design constraint for post-synthesis.

Refer to Lattice Radiant Timing Contraints Methodology for details on how to constraint the design.

References

- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.2, December 2023

Section	Change Summary
Disclaimers	Updated disclaimers.
Inclusive Language	Added inclusive language boilerplate.
Introduction	Removed information on clock frequencies 360 MHz and 450 MHz in the following: • Section 1 Introduction • Section 1.1 Features
Functional Description	Removed information on clock frequencies 360 MHz and 450 MHz in the following: • Section 2 Functional Description • Table 2.1. OSC Module Signal Description • Table 2.2. Attributes Table
IP Generation, Simulation, and Validation	Added section 3.3 Constraining the IP.
References	Added this section.

Revision 1.1.1, June 2023

Section	Change Summary
Introduction	Updated dynamically selectable clock frequency from 'between 400 or 320 MHz clock' to 'between 400/450 or 320/360 MHz clock depending on the selected device'.
Functional Description	• Updated maximum clock frequency from '400MHz' to '400MHz or 450MHz depending on the device selected'. • Updated clk_out_o is selectable from 'between 400MHz and 320 MHz' to 'between 400MHz or 450MHz and 320MHz or 360MHz'. • Updated Table 2.1. OSC Module Signal Description to revise the Descriptions of the Clock Port 'iclk_sel_i'. • Updated Table 2.2. Attributes Table to revise the Dependency on Other Attributes of Oscillator Clock (MHz).

Revision 1.1, June 2023

Section	Change Summary
All	• Document title changed from 'Avant OSC Module User Guide' to 'Lattice Avant OSC Module User Guide'. • Changed ‘Avant’ to ‘Lattice Avant’ throughout the entire document.
Functional Description	Changed ‘sel_400n_i’ to ‘clk_sel_i’.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Revision 1.0, October 2022

Section	Change Summary
All	Initial release.

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