LVDS Tunneling Protocol and Interface (LTPI) User Guide

Reference Design

FPGA-RD-02247-1.5

September 2025

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
AC	Alternating Current
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CDC	Clock Domain Crossing
CRC	Cycle Redundancy Check
CSR	Control and Status Register
DC-SCI	Datacenter-ready Secure Control Interface
DC-SCM	Datacenter-ready Secure Control Module
DDR	Double Data Rate
EFB	Embedded Function Block
FPGA	Field Programmable Gate Array
GDDR	Graphics Double Data Rate
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HDL	Hardware Description Language
HPM	Host Processor Module
I/O	Input/Output
I2C	Inter-Integrated Circuit
IP	Intellectual Property
IPK	Intellectual Property Kit
LED	Light-Emitting Diode
LLGPIO	Low Latency General Purpose Input/Output
LTPI	LVDS Tunneling Protocol and Interface
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
MCSI	Multi-Channel Serial Interface
MCTP	Management Component Transport Protocol
N/A	Not Applicable
NLGPIO	Normal Latency General Purpose Input/Output
OCP	Open Compute Project
OEM	Original Equipment Manufacturer
PFU	Programmable Functional Unit
PLL	Phase-Locked Loop
RTL	Register Transfer Level
Rx	Receiver
SCM	Secure Control Module
SDR	Single Data Rate
Tx	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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1. Introduction

The DC-SCM 2.0 LTPI Reference Design offers multiple solution templates utilizing the current LVDS Tunneling Protocol Interface (LTPI) IP. This IP complies with Datacenter-ready Secure Control Module (DC-SCM) 2.0 LTPI specifications and features a standardized Datacenter-ready Secure Control Interface (DC-SCI). It aggregates multiple data channels, including I2C, GPIO, and UART to enhance flexibility in a customer's system and board design.

This reference design is OCP Ready™.

1.1. Quick Facts

You can download the reference design files in the LVDS Tunneling Protocol and Interface Reference Design web page.

Table 1.1. Summary of the Reference Design

General	Supported Devices	MachXO3™, MachXO3D™, and MachXO5-NX™
	Source code format	Verilog
Simulation	Functional simulation	Performed
	Timing simulation	Not performed
	Test bench	Available
	Test bench format	Verilog
Software Requirements	Software tool and version	Lattice Diamond™ version 3.14 for the MachXO3, MachXO3D devices Lattice Radiant™ version 2025.1 for the MachXO5-NX devices Lattice Propel™ version 2025.1 Synplify Pro® Questa Lattice OEM Edition-64 2024.2
	IP version (if applicable)	DC-SCM LTPI 2.0.0 I2C-to-APB Bridge Reference Design 1.2.1
Hardware Requirements	Board	MachXO3LF Starter Kit MachXO3D Breakout Board MachXO5-NX Development Board
	Cable	USB Mini-B to USB-A cable (provided for all boards except the LTPI board)

1.2. Features

Key features of the LTPI reference design include:

- Support for DC-SCM 2.0 LTPI version 1.1 (Oct 2023)
- Link initialization, discovery, and negotiation
- Support for multi-channel serial interface
- Support for LVDS
- Aggregation/disaggregation of up to five channels in total
- Support for GPIO, I2C, UART, OEM, and data channel aggregation
- Configurable I2C interface as single-node (controller or target only) or multi-node (supports both external controller and target)
- Each multi-node I2C bus uses 1 payload byte, equivalent to two single-node I2C buses
- Support for up to 1,200 Mbps LVDS data rate (up to 800 Mbps on the MachXO3 and MachXO3D devices; up to 1,200 Mbps on the MachXO5-NX devices)
- Support for AMBA 3 APB Protocol version 1.0 for register access of the soft IP and data channel:
  - PREADY signal indicates completion of an APB transfer
  - PSLVERR signal indicates failure of a transfer, supported only in data channel-related access

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1.3. Naming Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that have:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

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2. Directory Structure and Files

Figure 2.1 shows the directory structure.

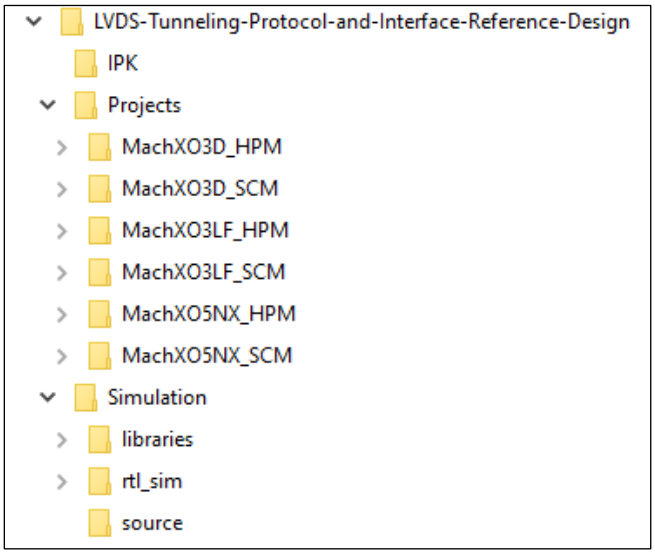

Figure 2.1. Directory Structure

Table 2.1 shows the list of files included in the reference design package.

Table 2.1. File List

Subfolder	Description
IPK	This subfolder contains the IPK used in the project.
Projects	This subfolder contains pre-built projects, subcategorized by the function and the Lattice FPGA used. • MachXO3D_HPM • MachXO3D_SCM • MachXO3LF_HPM • MachXO3LF_SCM • MachXO5NX_HPM • MachXO5NX_SCM Each project has been tested through simulation and on hardware.
Simulation	This subfolder contains the simulation files used for functional simulation. • Libraries: pre-built simulation libraries for the Lattice FPGA devices • Source: contains the test bench RTL and other submodules needed for simulation Additionally, this subfolder *.do files used to run preset functional simulations. These files are named in this format: *SCM_<device_used_for_SCM>_HPM_<device_used_for_HPM>.do* • SCM_XO3D_HPM_XO3D.do • SCM_XO3D_HPM_XO3LF.do • SCM_XO3D_HPM_XO5.do • SCM_XO3LF_HPM_XO3D.do • SCM_XO3LF_HPM_XO3LF.do • SCM_XO3LF_HPM_XO5.do • SCM_XO5_HPM_XO3D.do • SCM_XO5_HPM_XO3LF.do • SCM_XO5_HPM_XO5.do • wave.do – this is invoked by the other *.do files to add preset signals on the Wave view of the simulator

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3. Functional Description

The reference design provides you with a ready-to-use LTPI template for both SCM and HPM. The design manages all initialization requirements for SCM and HPM to establish a working link, following the LTPI state flow internally, as shown in Figure 3.1. It also provides access to the LTPI IP's Control and Status Registers through the I2C interface.

Figure 3.2 and Figure 3.3 illustrate the implementation of the DC-SCM LTPI IP within the reference design. Some modules differ between the HPM and SCM implementations based on their intended usage. Additionally, because the design supports multiple target devices, some modules vary for each device. These differences will be discussed in the subsection of each block.

The reset from the Reset Timer is also used as the primary reset net unless specified otherwise.

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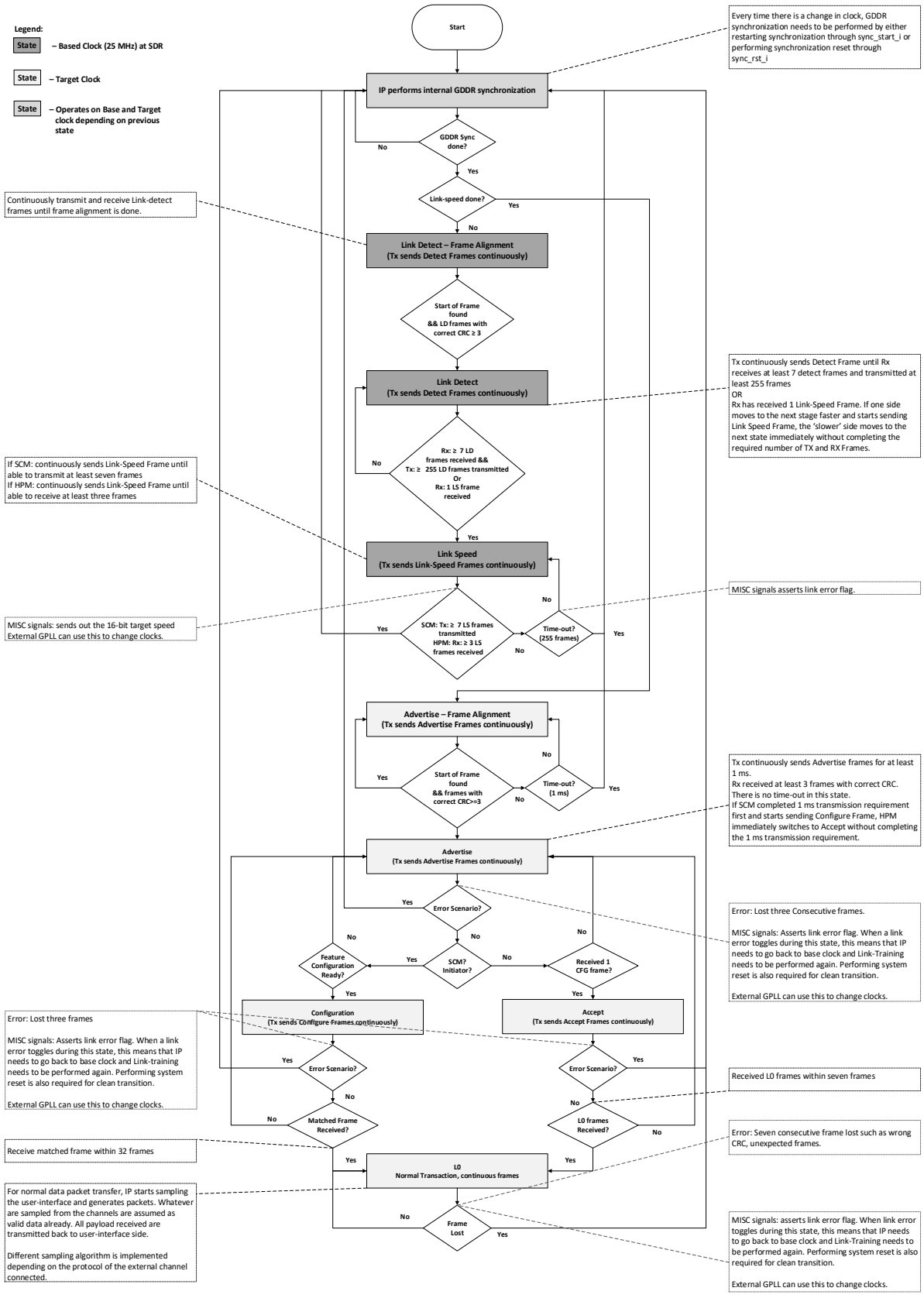

Figure 3.1. LTPI State Flow

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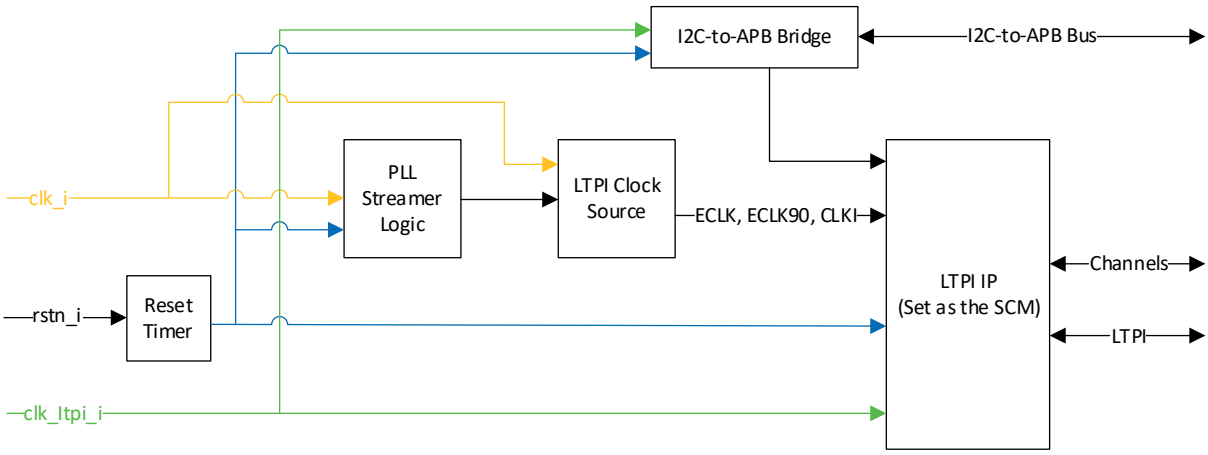

Figure 3.2. SCM Block Diagram

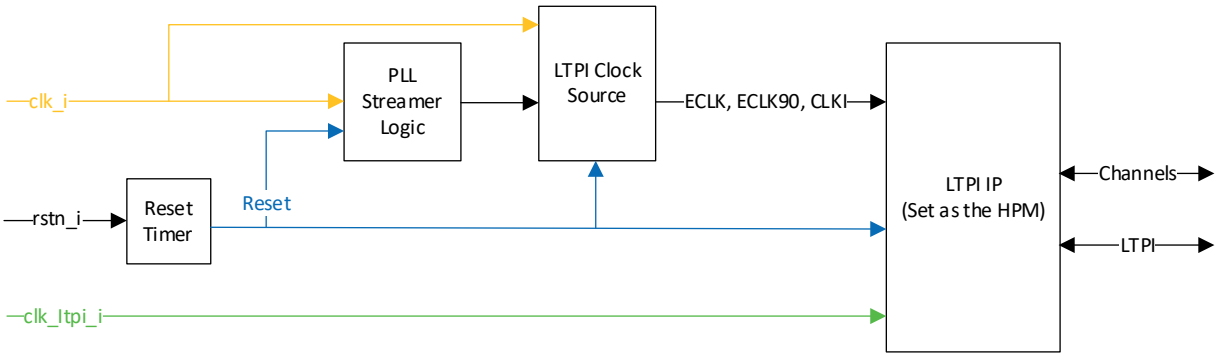

Figure 3.3. HPM Block Diagram

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3.1. Design Components

This section outlines the module components of the top-level module in the reference design. For the signal description of the top-level module, refer to the Signal Description section.

3.1.1. LTPI

This module utilizes the DC-SCM LTPI IP from Lattice Propel. Depending on the configuration, it can be either an SCM or HPM instance.

Module Name: scm0 (for SCM instance) or hpm0 (for HPM instance).

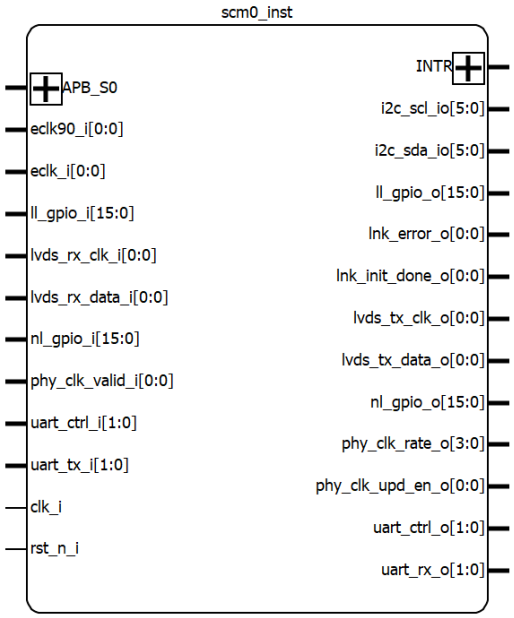

Figure 3.4. LTPI (SCM) Block Diagram

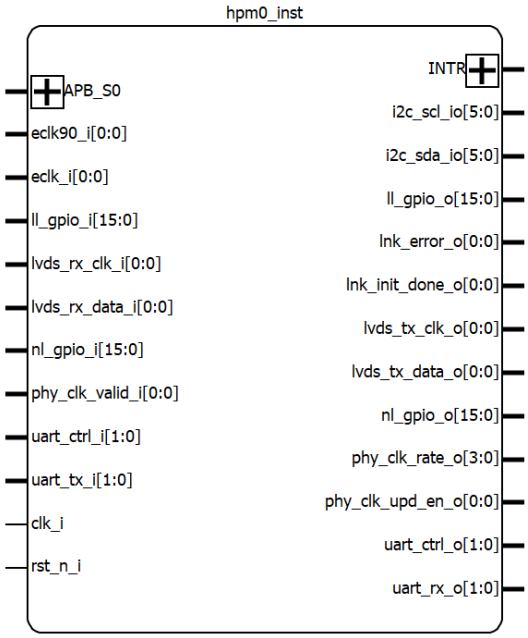

Figure 3.5. LTPI (HPM) Block Diagram

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Table 3.1. LTPI Clock Source Signals

Port Name	Input/Output	Width	Default Value	Description
System Signals				
clk_i	Input	1	N/A	The LTPI main clock connects to either CLKOS2 of LTPI clock source or sys_clk_o of clock generator.
reset_n_i	Input	1	N/A	Active low reset.
soft_reset_i	Input	1	1'b0	LTPI active high soft reset.
eclk_i	Input	1	N/A	The ECLK input connects to either CLKOP or clkop_o of the LTPI clock source.
eclk90_i	Input	1	N/A	The ECLK90 input connects to either CLKOS or clkos_o of the LTPI clock source.
INTR	Interrupt	N/A	N/A	Interrupt interface. Unused.
LTPI Signals				
lvds_rx_clk_i	Input	1	N/A	LVDS Receive Clock. Connects to scm0_inst_lvds_rx_clk_i_port or hpm0_inst_lvds_rx_clk_i_port (Top Module).
lvds_rx_data_i	Input	1	N/A	LVDS Receive Data. Connects to scm0_inst_lvds_rx_data_i_port or hpm0_inst_lvds_rx_data_i_port (Top Module).
lvds_tx_clk_o	Output	1	N/A	LVDS Transmit Clock. Connects to scm0_inst_lvds_tx_clk_o_port or hpm0_inst_lvds_tx_clk_o_port (Top Module).
lvds_tx_data_o	Output	1	N/A	LVDS Transmit Data. Connects to scm0_inst_lvds_tx_data_o_port or hpm0_inst_lvds_tx_data_o_port (Top Module).
Low Latency GPIO Channel				
ll_gpio_i	Input	4	N/A	Low Latency Input. Connects to scm0_inst_ll_gpio_i_portbus or hpm0_inst_ll_gpio_i_portbus (Top Module).
ll_gpio_o	Output	4	N/A	Low Latency Output. Connects to scm0_inst_ll_gpio_o_portbus or hpm0_inst_ll_gpio_o_portbus (Top Module).
Normal Latency GPIO Channel				
nl_gpio_i	Input	4	N/A	Low Latency Input. Connects to scm0_inst_nl_gpio_i_portbus or hpm0_inst_nl_gpio_i_portbus (Top Module).
nl_gpio_o	Output	4	N/A	Low Latency Output. Connects to scm0_inst_nl_gpio_o_portbus or hpm0_inst_nl_gpio_o_portbus (Top Module).
UART Channel				
uart_tx_i	Input	1	N/A	UART Tx pin. Connects to scm0_inst_uart_tx_i_portbus or hpm0_inst_uart_tx_i_portbus.
uart_rx_o	Output	1	N/A	UART Rx pin. Connects to scm0_inst_uart_rx_o_portbus or hpm0_inst_uart_rx_o_portbus (Top Module).
I2C Channel				
i2c_scl_io	Inout	1	N/A	I2C Clock pin. Connects to scm0_inst_i2c_scl_io_portbus or hpm0_inst_i2c_scl_io_portbus (Top Module).
i2c_sda_io	Inout	1	N/A	I2C Data pin. Connects to scm0_inst_i2c_sda_io_portbus or hpm0_inst_i2c_sda_io_portbus (Top Module).
Data Channel				
data_ch_i	Input	8	8'h00	Data channel input tag. Unused.
data_ch_o	Output	8	8'h00	Data channel output tag. Unused.
APB_M0	APB IF	N/A	N/A	Data Channel APB Requester Interface. Connects to the APB_S0 interface of LTPI.

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Port Name	Input/Output	Width	Default Value	Description
APB Interface				
apb_pclk_i	Input	1	N/A	APB interface clock. 25 MHz clock input.
apb_reset_n_i	Input	1	N/A	Active-low reset.
APB_S0	APB IF	N/A	N/A	CSR APB Completer Interface. Connects to APB_M0 of the I2C-to-APB Bridge module (SCM only).
Miscellaneous Signals				
lnk_init_done_o	Output	1	N/A	Link Established Flag.
lnk_error_o	Output	1	N/A	Link Error Flag. Indicates that the link between SCM and HPM is lost.

3.1.2. Reset Timer

This module uses the output of an internal watchdog timer to generate the system's reset net. If the timer is disabled (timeout_en_i = 0), the output reset source matches the input reset.

Module Name: reset_timeout

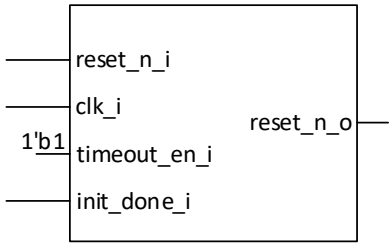

Figure 3.6. Reset Timer Block Diagram

Table 3.2. Reset Timer Signals

Port Name	Input/Output	Width	Default Value	Description
reset_n_i	Input	1	N/A	Active-low reset.
clk_i	Input	1	N/A	25 MHz clock input.
timeout_en_i	Input	1	1'b1	Enables the timeout timer. The timer is active when timeout_en_i = 1 and init_done_i = 0.
init_done_i	Input	1	N/A	Connects to init_done_o of LTPI. The timer is active when timeout_en_i = 1 and init_done_i = 0.
reset_n_o	Output	1	1'b0	System reset source.

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3.1.3. PLL Streamer Logic

This module manages the process of changing the LTPI Clock Source frequency from Base Speed to Target Speed and vice versa. Table 3.4 outlines the difference in implementation for the three devices.

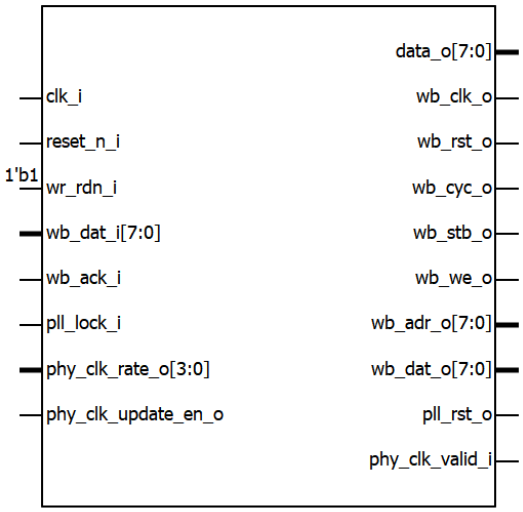

Figure 3.7. PLL Streamer Logic (Wishbone) Block Diagram

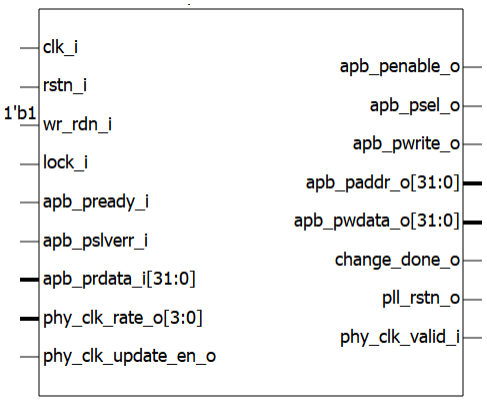

Figure 3.8. PLL Streamer Logic (APB) Block Diagram

Table 3.3. PLL Streamer Logic Implementation

Target Device	Module Name
MachXO3	wishbone_streamer
MachXO3D	wishbone_streamer
MachXO5-NX	apb_streamer

Table 3.4. PLL Streamer Logic Signals

Port Name	Input/Output	Width	Default Value	Description
Wishbone				
clk_i	Input	1	N/A	25 MHz clock input.
reset_n_i	Input	1	N/A	Active-low reset.
wr_rdn_i	Input	1	1’b1	Write (High) / Read (Low) Enable. **DO NOT CHANGE.**
wb_dat_i	Input	8	N/A	Wishbone Data In. Connects to wb_dat_o of EFB.
wb_ack_i	Input	1	N/A	Wishbone Ack Bit. Connects to wb_ack_o of EFB.

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Port Name	Input/Output	Width	Default Value	Description
pll_lock_i	Input	1	N/A	PLL lock status signal. Connects to lock_o of PLL Wrapper.
phy_clk_rate_o	Output	4	N/A	Indicates the requested clock frequency rate of eclk_i and eclk90_i: 4'd0 – 25 MHz (default) 4'd1 – 50 MHz 4'd2 – 75 MHz 4'd3 – 100 MHz 4'd4 – 150 MHz 4'd5 – 200 MHz 4'd6 – 250 MHz 4'd7 – 300 MHz 4'd8 – 400 MHz 4'd9 – 600 MHz Other values – reserved
phy_clk_update_en_o	Output	1	N/A	Indicates a request to update the clock frequency of eclk_i and eclk90_i to the rate specified by phy_clk_rate_o. Connects to phy_clk_update_en_o of LTPI.
data_o	Output	8	8'h00	Module debug port. Unused.
wb_clk_o	Output	1	1'b0	Wishbone Clock. Connects to wb_clk_i of EFB.
wb_rst_o	Output	1	1'b0	Wishbone Reset. Connects to wb_rst_i of EFB.
wb_cyc_o	Output	1	1'b0	Wishbone Cycle. Connects to wb_cyc_i of EFB.
wb_stb_o	Output	1	1'b0	Wishbone Strobe. Connects to wb_stb_i of EFB.
wb_we_o	Output	1	1'b0	Wishbone Write Enable. Connects to wb_we_i of EFB.
wb_adr_o	Output	8	8'h00	Wishbone Address. Connects to wb_adr_i of EFB.
wb_dat_o	Output	8	8'h00	Wishbone Data Out. Connects to wb_dat_i of EFB.
pll_rst_o	Output	1	1'b0	Dynamic PLL Reset Source. Connects to RST of LTPI Clock Source.
phy_clk_valid_i	Input	1	N/A	Indicates that the input clocks eclk_i and eclk90_i are valid and stable. Connects to phy_clk_rate_i of LTPI.
APB				
clk_i	Input	1	N/A	25 MHz clock input.
rstn_i	Input	1	N/A	Active-low reset.
wr_rdn_i	Input	1	1'b1	Write (High) / Read (Low) Enable. **DO NOT CHANGE.**
lock_i	Input	1	N/A	Dynamic PLL Lock. Connects to lock_o of LTPI Clock Source.
apb_pready_i	Input	1	N/A	APB Ready. Connects to apb_pready_o of LTPI Clock Source.
apb_pslverr_i	Input	1	N/A	APB Completer Error. Connects to apb_pslverr_o of LTPI Clock Source.
apb_prdata_i	Input	32	N/A	APB Read Data. Connects to apb_prdata_o of LTPI Clock Source.

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Port Name	Input/Output	Width	Default Value	Description
phy_clk_rate_o	Output	4	N/A	Indicates the requested clock frequency rate of eclk_i and eclk90_i: 4'd0 – 25 MHz (default) 4'd1 – 50 MHz 4'd2 – 75 MHz 4'd3 – 100 MHz 4'd4 – 150 MHz 4'd5 – 200 MHz 4'd6 – 250 MHz 4'd7 – 300 MHz 4'd8 – 400 MHz 4'd9 – 600 MHz Other values – reserved
phy_clk_update_en_o	Output	1	N/A	Indicates a request to update the clock frequency of eclk_i and eclk90_i to the rate specified by phy_clk_rate_o. Connects to phy_clk_update_en_o of LTPI.
apb_penable_o	Output	1	1'b0	APB Enable. Connects to apb_penable_i of LTPI Clock Source.
apb_psel_o	Output	1	1'b0	APB Select. Connects to apb_psel_i of LTPI Clock Source.
apb_pwrite_o	Output	1	1'b0	APB Write Enable. Connects to apb_pwrite_i of LTPI Clock Source.
apb_paddr_o	Output	32	32'h00000000	APB Address. Connects to apb_paddr_i of LTPI Clock Source.
apb_pwdata_o	Output	32	32'h00000000	APB Write Data. Connects to apb_pwdata_i of LTPI Clock Source.
change_done_o	Output	1	1'b0	Frequency Change Done Flag. Connects to change_done_i of Clock Generator.
pll_rstn_o	Output	1	1'b1	Dynamic PLL Reset Source. Connects to rstn_i of LTPI Clock Source.
phy_clk_valid_i	Input	1	N/A	Indicates that the input clocks eclk_i and eclk90_i are valid and stable. Connects to phy_clk_rate_i of LTPI

3.1.4. EFB

This module serves as a wrapper for an EFB instance, providing access to the Wishbone interface of the LTPI Clock Source PLL. This module is used exclusively for MachXO3 and MachXO3D devices.

Module Name: wb_pll

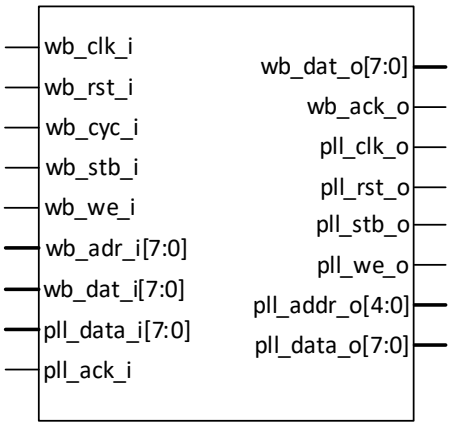

Figure 3.9. EFB Block Diagram

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Table 3.5. EFB Signals

Port Name	Input/Output	Width	Default Value	Description
wb_clk_i	Input	1	N/A	Wishbone Clock. Connects to wb_clk_o of PLL Streamer Logic.
wb_rst_i	Input	1	N/A	Wishbone Reset. Connects to wb_rst_o of PLL Streamer Logic.
wb_cyc_i	Input	1	N/A	Wishbone Cycle. Connects to wb_cyc_o of PLL Streamer Logic.
wb_stb_i	Input	1	N/A	Wishbone Strobe. Connects to wb_stb_o of PLL Streamer Logic.
wb_we_i	Input	1	N/A	Wishbone Write Enable. Connects to wb_we_o of PLL Streamer Logic.
wb_adr_i	Input	8	N/A	Wishbone Address. Connects to wb_adr_o of PLL Streamer Logic.
wb_dat_i	Input	8	N/A	Wishbone Data In. Connects to wb_dat_o of PLL Streamer Logic.
pll_dat_i	Input	8	N/A	PLL Wishbone Data In. Connects to PLLDATO of LTPI Clock Source.
pll_ack_i	Input	1	N/A	PLL Wishbone Ack Bit. Connects to PLLACK of LTPI Clock Source.
wb_dat_o	Output	8	8'h00	Wishbone Data Out. Connects to wb_dat_i of PLL Streamer Logic.
wb_ack_o	Output	1	1'b0	Wishbone Ack Bit. Connects to wb_ack_i of PLL Streamer Logic.
pll_clk_o	Output	1	N/A	PLL Wishbone Clock. Connects to PLLCLK of LTPI Clock Source.
pll_rst_o	Output	1	1'b0	PLL Wishbone Reset. Connects to PLLRST of LTPI Clock Source.
pll_stb_o	Output	1	1'b0	PLL Wishbone Strobe. Connects to PLLSTB of LTPI Clock Source.
pll_we_o	Output	1	1'b0	PLL Wishbone Write Enable. Connects to PLLWE of LTPI Clock Source.
pll_addr_o	Output	5	5'h00	PLL Wishbone Address. Connects to PLLADDR of LTPI Clock Source.
pll_data_o	Output	8	8'h00	PLL Wishbone Data Out. Connects to PLLDATI of LTPI Clock Source.

3.1.5. LTPI Clock Source

This module serves as a wrapper for a PLL instance, providing the necessary clocks for the LTPI.

Module name: dynamic_pll

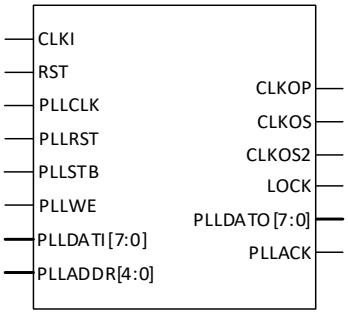

Figure 3.10. LTPI Clock Source (MachXO3/MachXO3D) Block Diagram

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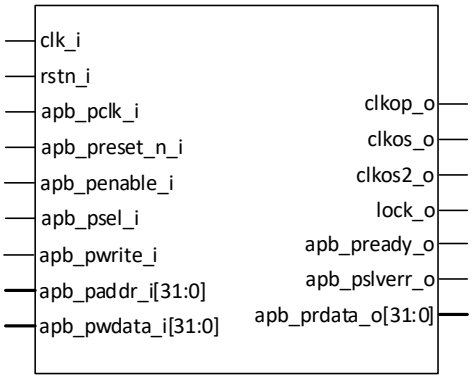

Figure 3.11. LTPI Clock Source (MachXO5-NX) Block Diagram

Table 3.6. LTPI Clock Source Signals

Port Name	Input/Output	Width	Default Value	Description
MachXO3/MachXO3D				
CLKI	Input	1	N/A	25 MHz clock input.
RST	Input	1	N/A	Active-high reset. Connects to pll_rst_o of PLL Streamer Logic.
PLLCLK	Input	1	N/A	PLL Wishbone Clock. Connects to pll_clk_o of LTPI Clock Source.
PLLRST	Input	1	N/A	PLL Wishbone Reset. Connects to pll_rst_o of LTPI Clock Source.
PLLSTB	Input	1	N/A	PLL Wishbone Strobe. Connects to pll_stb_o of LTPI Clock Source.
PLLWE	Input	1	N/A	PLL Wishbone Write Enable. Connects to pll_we_o of LTPI Clock Source.
PLLDATI	Input	8	N/A	PLL Wishbone Data In. Connects to pll_data _o of LTPI Clock Source.
PLLADDR	Input	5	N/A	PLL Wishbone Address. Connects to pll_addr_o of LTPI Clock Source.
CLKOP	Output	1	N/A	LTPI ECLK source. Connects to eclk_i of LTPI.
CLKOS	Output	1	N/A	LTPI ECLK 90 source. Connects to eclk90_i of LTPI.
CLKOS2	Output	1	N/A	LTPI main clock source. Connects to clk_i of LTPI.
LOCK	Output	1	1'b0	Dynamic PLL Lock. Connects to lock_i of Initialization Logic.
PLLDATO	Output	8	8'h00	PLL Wishbone Data Out. Connects to pll_dat_i of EFB.
PLLACK	Output	1	1'b0	PLL Wishbone Ack Bit. Connects to pll_ack_i of EFB.
MachXO5-NX				
clk_i	Input	1	N/A	25 MHz clock input.
rstn_i	Input	1	N/A	Active-low reset. Connects to pll_rstn_o of PLL Streamer Logic.
apb_pclk_i	Input	1	N/A	25 MHz clock input.
apb_preset_n_i	Input	1	N/A	Active-low reset.
apb_penable_i	Input	1	N/A	APB Enable. Connects to apb_penable_o of PLL Streamer Logic.
apb_psel_i	Input	1	N/A	APB Select. Connects to apb_psel_o of PLL Streamer Logic.
apb_pwrite_i	Input	1	N/A	APB Write Enable. Connects to apb_pwrite_o of PLL Streamer Logic.
apb_paddr_i	Input	32	N/A	APB Address. Connects to apb_paddr_o of PLL Streamer Logic.

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Port Name	Input/Output	Width	Default Value	Description
apb_pwdata_i	Input	32	N/A	APB Write Data. Connects to apb_pwdata_o of PLL Streamer Logic.
clkop_o	Output	1	N/A	LTPI ECLK source. Connects to eclk_i of LTPI.
clkos_o	Output	1	N/A	LTPI ECLK 90 source. Connects to eclk90_i of LTPI.
clkos2_o	Output	1	N/A	LTPI Target Speed System Clock. Connects to clk_systarget_i of Clock Generator.
lock_o	Output	1	1'b0	Dynamic PLL Lock. Connects to lock_i of Initialization Logic and lock_i of Clock Generator.
apb_pready_o	Output	1	1'b0	APB Ready. Connects to apb_pready_i of PLL Streamer Logic.
apb_pslverr_o	Output	1	1'b0	APB Completer Error. Connects to apb_pslverr_i of PLL Streamer Logic.
apb_prdata_o	Output	32	32'h00000000	APB Read Data. Connects to apb_prdata_i of PLL Streamer Logic.

Table 3.7. LTPI Clock Source Implementation

Target Device	Module Name	PLL Instance
MachXO3	dynamic_pll	dpll
MachXO3D	dynamic_pll	dpll
MachXO5-NX	dynamic_pll_xo5	dpll_xo5

3.1.6. I2C-to-APB Bridge (SCM Only)

This module utilizes the I2C-to-APB Bridge Reference Design from Lattice Propel. It converts external I2C commands into APB commands.

Module name: i2c2apb0

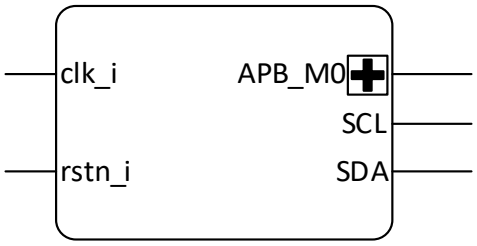

Figure 3.12. I2C-to-APB Bridge Block Diagram

Table 3.8. I2C-to-APB Bridge Signals

Port Name	Input/Output	Width	Default Value	Description
clk_i	Input	1	N/A	25 MHz clock input.
rstn_i	Input	1	N/A	Active-low reset.
APB_M0	APB IF	N/A	N/A	APB Requester Interface 0. Connects to APB_S00 of APB Interconnect.
SCL	Inout	1	Tri-state	I2C Clock port. Connects to i2c2apb0_inst_SCL_port (Top Module).
SDA	Inout	1	Tri-state	I2C Data port. Connects to i2c2apb0_inst_SDA_port (Top Module).

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3.2. Clocking Scheme

The reference design employs two input clocks, clk_i and clk_ltpi_i. The clk_i signal serves as the primary system clock and is fixed at 25 MHz. This 25 MHz source is essential for generating the derived clocks required by the DC-SCM LTPI IP, specifically, ECLK, ECLK90, and CLK. This configuration enables a single set of computed parameters to produce LTPI-compliant operating frequencies as defined by the specification – up to 400 MHz for MachXO3 and MachXO3D devices, and up to 600 MHz for MachXO5-NX devices.

In contrast, the clk_ltpi_i signal is directly connected to the LTPI IP core, and its frequency is determined by the system clock range specified in the LTPI IP specifications.

3.3. Reset Scheme

The reference design uses the Reset Timer module to generate the system's reset net.

Note that the LTPI Clock Source module does not use the system reset. Its reset is provided by the PLL streamer logic, allowing the module to toggle the PLL's output when changing from Base Speed to Target Speed and vice versa.

3.4. DC-SCM LTPI IP Control and Status Registers

Refer to the DC-SCM LTPI IP User Guide (FPGA-IPUG-02200) for the DC-SCM LTPI IP register description information.

3.5. GPIO Latency

The latency for the LL GPIO is at best case 700 ns (at 800 Mbps for MachXO3 and MachXO3D) and 425 ns (at 1200 Mbps for MachXO5-NX). We measure this from the time the transmitting module system clock samples the data on the LL Input Interface to the time the LL Output Interface of the receiver module reflects the data.

The latency for the NL GPIO depends on the ratio of the number of NL GPIO and the number of NL GPIO per frame (rounded up). This pertains to how many frames we need to send before the next frame contains an update to the same NL GPIO bits. Below is a sample computation:

Number of NL GPIO : 130

Number of NL GPIO per Frame: 16

Target Device: MachXO3

Total Delay (Best Case) = 700 ns × ceiling(130/16) = 6300 ns

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4. Signal Description

This section describes the top module signals of the reference design, which are shown in Table 4.1 for SCM and Table 4.2 for HPM.

Table 4.1. SCM Top Module Signals

Port Name	Input/Output	Width	Default Value	Description
System				
clk_i	Input	1	25 MHz	External clock input, fixed at 25 MHz.
clk_ltpi_i	Input	1	N/A	LTPI IP input clock which value depends on the system clock range defined by the LTPI IP specifications.
rstn_i	Input	1	N/A	Active-low reset.
LVDS Interface				
scm0_inst_lvds_tx_clk_o_port	Output	1	N/A	LVDS Tx PHY clock
scm0_inst_lvds_tx_data_o_port	Output	1	N/A	LVDS Tx PHY data
scm0_inst_lvds_rx_clk_i_port	Input	1	N/A	LVDS Rx PHY clock
scm0_inst_lvds_rx_data_i_port	Input	1	N/A	LVDS Rx PHY data
Low Latency GPIO Channel Interface				
scm0_inst_ll_gpio_i_portbus	Input	16	N/A	Low latency input pins
scm0_inst_ll_gpio_o_portbus	Output	16	N/A	Low latency output pins
Normal Latency GPIO Channel Interface				
scm0_inst_nl_gpio_i_portbus	Input	16	N/A	Normal latency input pins
scm0_inst_nl_gpio_o_portbus	Output	16	N/A	Normal latency output pins
UART Channel Interface				
scm0_inst_uart_tx_i_portbus	Input	2	N/A	UART Tx pin
scm0_inst_uart_rx_o_portbus	Output	2	N/A	UART Rx pin
I2C Channel Interface				
scm0_inst_i2c_scl_io_portbus	Inout	6	Tri-state	I2C clock pin. Requires external pull-up.
scm0_inst_i2c_sda_io_portbus	Inout	6	Tri-state	I2C data pin. Requires external pull-up.
I2C-to-APB Interface				
i2c2apb0_inst_SCL_port	Inout	1	Tri-state	I2C-to-APB clock pin. Requires external pull-up.
i2c2apb0_inst_SDA_port	Inout	1	Tri-state	I2C-to-APB data pin. Requires external pull-up.
OEM Channel Interface				
scm0_inst_oem_oe_i_portbus	Input	32	N/A	OEM input pins
scm0_inst_oem_io_portbus	Output	32	N/A	OEM output pins
Protocol Information				
concat_module_inst_status_display_portbus	Output	2	1	Status Flags from LTPI: Bit 0: init_done Bit 1: link_err
scm0_inst_lnk_error_o_portbus	Output	1	1	LTPI status flag: Link Error
scm0_inst_lnk_init_done_o_portbus	Output	1	1	LTPI status flag: Link Init Done

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Table 4.2. HPM Top Module Signals

Port Name	Input/Output	Width	Default Value	Description
System				
clk_i	Input	1	25 MHz	External clock input, fixed at 25 MHz.
clk_ltpi_i	Input	1	N/A	LTPI IP input clock which value depends on the system clock range defined by the LTPI IP specifications.
rstn_i	Input	1	N/A	Active-low reset.
LVDS Interface				
hpm0_inst_lvds_tx_clk_o_port	Output	1	N/A	LVDS Tx PHY clock
hpm0_inst_lvds_tx_data_o_port	Output	1	N/A	LVDS Tx PHY data
hpm0_inst_lvds_rx_clk_i_port	Input	1	N/A	LVDS Rx PHY clock
hpm0_inst_lvds_rx_data_i_port	Input	1	N/A	LVDS Rx PHY data
Low Latency GPIO Channel Interface				
hpm0_inst_ll_gpio_i_portbus	Input	16	N/A	Low latency GPIO input pins
hpm0_inst_ll_gpio_o_portbus	Output	16	N/A	Low latency GPIO output pins
Normal Latency GPIO Channel Interface				
hpm0_inst_nl_gpio_i_portbus	Input	16	N/A	Normal latency GPIO input pins
hpm0_inst_nl_gpio_o_portbus	Output	16	N/A	Normal latency GPIO output pins
UART Channel Interface				
hpm0_inst_uart_tx_i_portbus	Input	2	N/A	UART Tx pin
hpm0_inst_uart_rx_o_portbus	Output	2	N/A	UART Rx pin
I2C Channel Interface				
hpm0_inst_i2c_scl_io_portbus	Inout	1	N/A	I2C Clock pin. Requires external pull-up.
hpm0_inst_i2c_sda_io_portbus	Inout	1	N/A	I2C Data pin. Requires external pull-up.
OEM Channel Interface				
hpm0_inst_oem_oe_i_portbus	Input	32	N/A	OEM input pins
hpm0_inst_oem_io_portbus	Output	32	N/A	OEM output pins
Protocol Information				
hpm0_inst_lnk_error_o_portbus	Output	1	1	LTPI status flag: Link Error
hpm0_inst_lnk_init_done_o_portbus	Output	1	1	LTPI status flag: Link Init Done

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5. Timing Constraints

For timing constraint guidelines, refer to the Timing Analysis for High-Speed GDDR Interfaces in the following documents:

- Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057) for MachXO3 devices.
- Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065) for MachXO3D devices.
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286) for MachXO5-NX devices.

5.1. Clock Definitions

The following clock frequencies are set either manually (preset by the reference design) or automatically (preset by the software). All are referenced to input or internal clocks of the DC-SCM LTPI IP.

- clk_i: Clock supplied to the LTPI Clock Source PLL as well as the system clock of all other modules in the reference design except for the LTPI IP and I2C-to-APB Bridge module. This clock **must** be set to 25 MHz and is constrained by the reference design to 25 MHz.
- clk_ltpi_i: Clock used as system clock for the LTPI IP and I2C-to-APB Bridge module. This clock **must** match the *Actual System Clock Frequency (MHz)* setting of the LTPI IP. This clock is constrained by the reference design to:
  - 100 MHz for MachXO3 and MachXO3D devices.
  - 125 MHz for MachXO5-NX devices.
- eclk_i: Clock supplied as the ECLK of the LTPI IP. This clock is constrained based on the LTPI Clock Source PLL setting (software-defined). This clock varies from 25 MHz (during Base Speed states) up to:
  - 400 MHz for MachXO3 and MachXO3D devices.
  - 600 MHz for MachXO5-NX devices.
- eclk90_i: Clock supplied as the ECLK90 of the LTPI IP and is 90 degrees out of phase with eclk_i. This clock is constrained based on the LTPI Clock Source PLL setting (software-defined). This clock varies from 25 MHz (during Base Speed states) up to:
  - 400 MHz for MachXO3 and MachXO3D devices.
  - 600 MHz for MachXO5-NX devices.
- lvds_rx_clk_i_portbus[0]: Expected LVDS RX Clock frequency. This clock is constrained by the reference design to:
  - 400 MHz for MachXO3 and MachXO3D devices.
  - 600 MHz for MachXO5-NX devices.
- tx_sclk_o: Generated SCLK by the Tx PHY module. This clock is:
  - 1/4 of the ECLK and constrained by the reference design to 100 MHz for MachXO3 and MachXO3D devices.
  - 1/5 of the ECLK and constrained by the reference design to 120 MHz for MachXO5-NX devices.
- rx_sclk_o: Generated SCLK by the Rx PHY module. This clock is:
  - 1/4 of the ECLK and constrained by the reference design to 100 MHz for MachXO3 and MachXO3D devices.
  - 1/5 of the ECLK and constrained by the reference design to 120 MHz for MachXO5-NX devices.

5.2. Clocks, Resets, and False Paths

All reset paths are asynchronous and can be set as false paths. Data transfers and clock domain crossings are already handled in the reference design. All clocks defined in the Clock Definitions section can also be set as false paths.

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6. Modifying the Reference Design

The reference design is pre-compiled and ready to use upon download. If the intent is to run the default design on hardware for evaluation purposes, proceed to the Hardware Implementation section.

This section discusses the software design flow if changes to the reference design need to be made.

IMPORTANT: Ensure that the linked project for Lattice Diamond or Lattice Radiant is not open when making any modifications in the Lattice Propel project, and vice versa.

6.1. Lattice Propel

This section discusses changes that the user can make to the reference design using Lattice Propel.

For more information on Lattice Propel usage, refer to the Lattice Propel 2024.2 Builder User Guide (FPGA-UG-02219).

6.1.1. Opening the Lattice Propel Project

1. Unzip the reference design ZIP file.
2. Open Lattice Propel 2024.2. Note that the reference design is tested using this version and does not guarantee backward compatibility with previous Lattice Propel versions.
3. Click the Open Design button or go to **File** > **Open Design**.

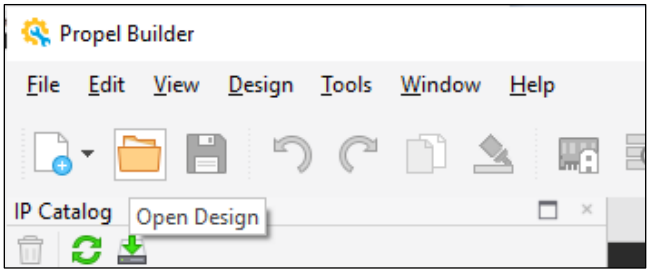

Figure 6.1. Open Design Button

4. Select the project file (*.sbx) found in *<Reference_Design_Folder>/Projects/<Design_Folder>/<Design_Folder>*. In this section, the design used as an example is **MachXO3D_SCM**.

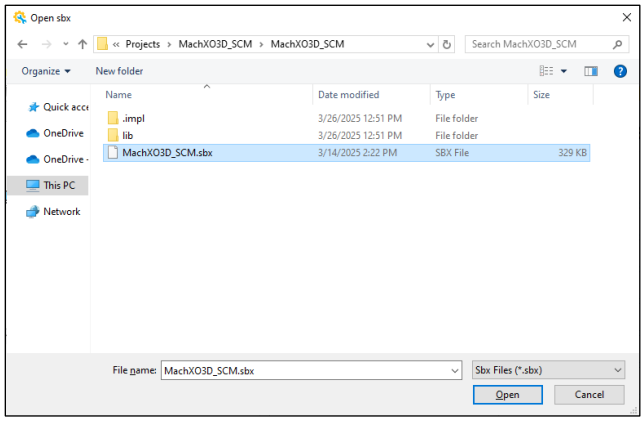

Figure 6.2. Selecting the Lattice Propel Project

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6.1.2. Add/Remove Top-Level Module Ports

All module ports that are connected to an external port (input , output or inout) will be part of the top-level module port list.

- To remove a top-level port, do any of the following:
  - Right-click the external port and select Disconnect.
  - Click the external port and press Delete.
- To add a top-level port to an unconnected module port, right-click.
- To add a top-level port to connected module port(s) or net(s), do the following:
  - Right-click on any blank space in the Schematic Window and select Create Port.
  - Configure the external port.
  - Connect to the module port or net.

Click **Save** after making changes.

6.1.3. Changing the DC-SCM LTPI IP Settings

This section provides an overview of what users can change in the IP GUI. All figures in this section show the default IP settings, not the SCM or HPM project settings. Each subsection describes the settings made for each tab (if applicable) and other changes that can be made to customize the reference design.

For more information on the IP's function, refer to the DC-SCM LTPI IP User Guide (FPGA-IPUG-02200).

After making changes to the IP:

1. Click **Generate**.
2. Review the generated result.
3. Check or Uncheck the **Insert to project** option, depending on your needs.
4. Click **Finish**.
5. Create top-level ports, if necessary.
6. Click **Save**.

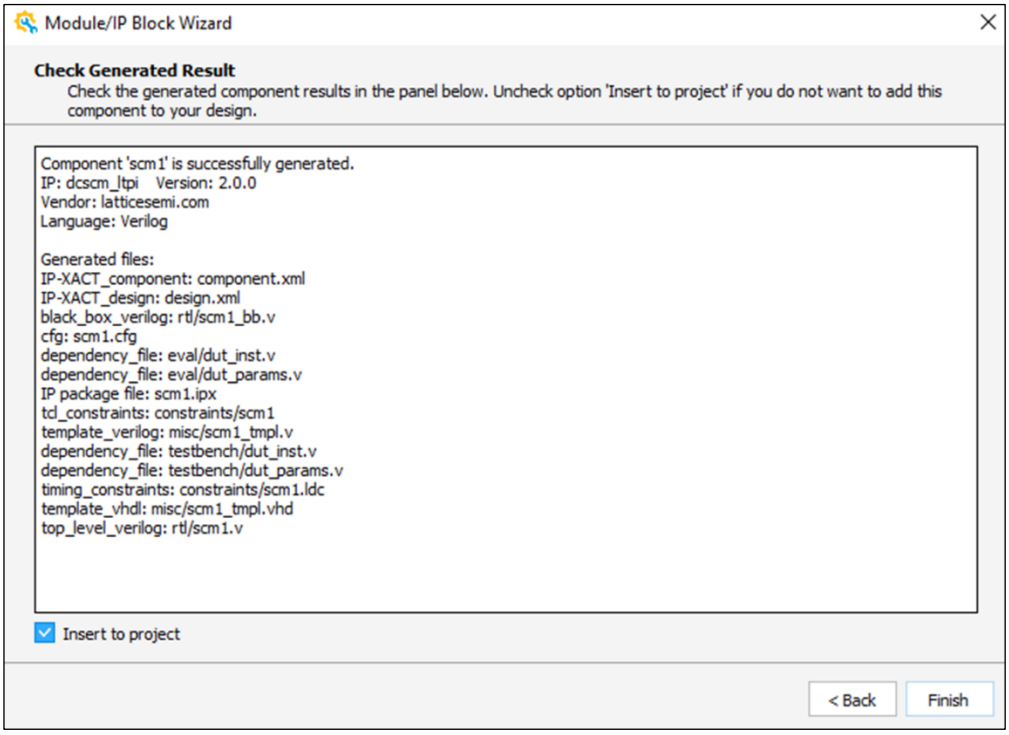

Figure 6.3. Check Generated Result Window

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6.1.3.1. General Tab

This section provides descriptions of the parameters in the General tab.

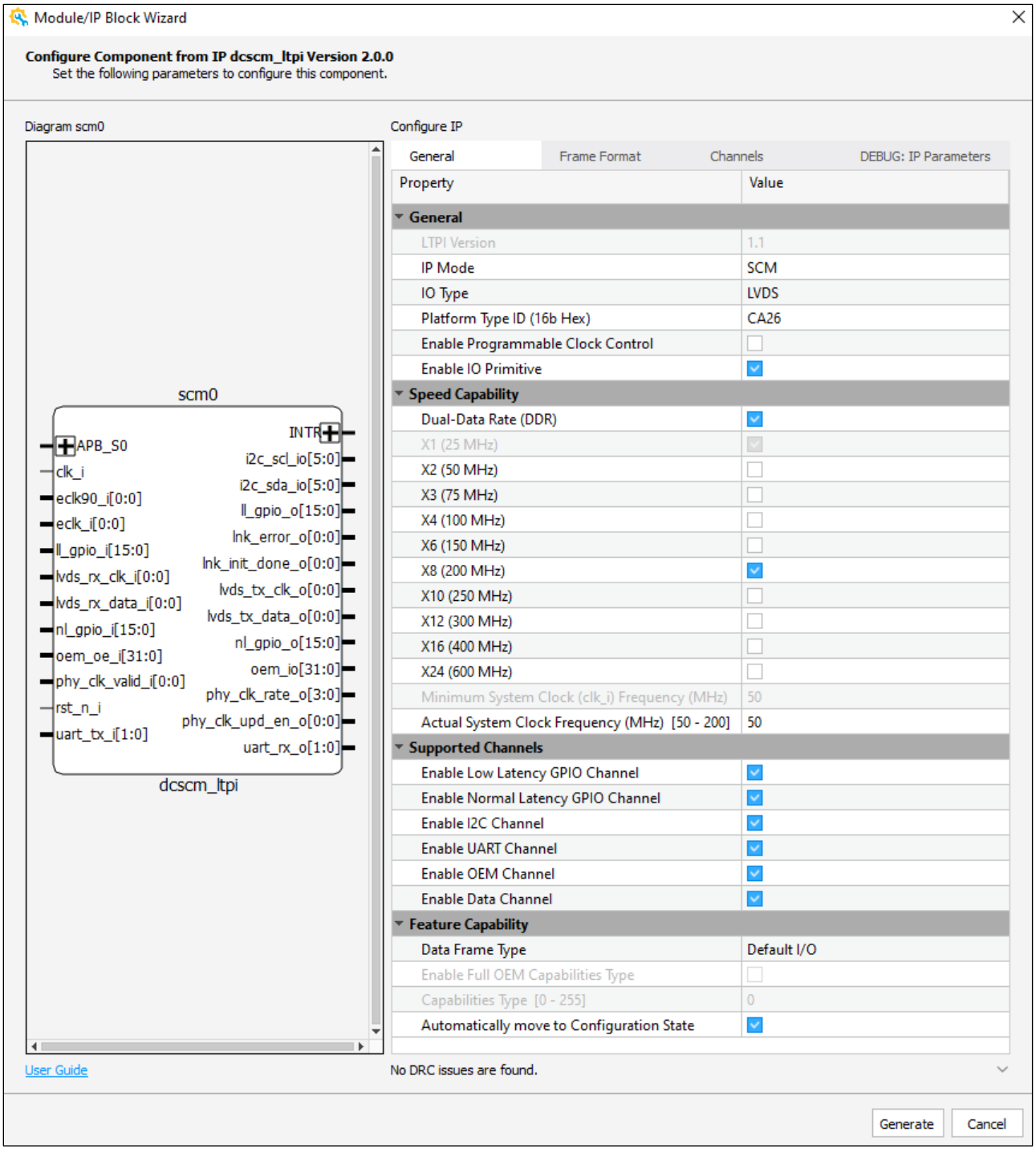

Figure 6.4. General Tab

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Table 6.1. General Tab Parameter Descriptions

Parameter	Description
General	
LTPI Version	Set by default and specifies the LTPI version supported by the IP core.
IP Mode	Determines the function of the IP. When modifying the reference design, do not change the value unless necessary.
IO Type	A placeholder option intended for future support of additional IO types in upcoming LTPI versions. Do not modify.
ID Number in Hex (0x0000)	Set to 0xCA26 for SCM and 0xBF17 for HPM. It is used to differentiate the contents of the SCM and HPM CSR, which is then used to validate CSR access. This option can be removed or modified as needed. Any changes to this value are written at offset 0x00 of the CSR (ID).
Enable Programmable Clock Control	Disabled by default. When enabled, the signals used for requesting clock update are not present and are instead converted to equivalent programmable registers.
Enable IO Primitive	Enabled by default. When enabled, the I2C and OEM signals appear as bidirectional ports. Otherwise, the internal tri-state I/O signals are brought out as ports.
Speed Capability[1]	
Dual-Data Rate (DDR)	SPEED_CAP[15] = 1 when enabled. SPEED_CAP[15] = 0 when disabled. This setting is enabled in the reference design.
X1 (25 MHz)	This setting is always enabled. Mapped to SPEED_CAP[0].
X2 (50 MHz)	SPEED_CAP[1] = 1 when enabled. SPEED_CAP[1] = 0 when disabled. This setting is disabled in the reference design.
X3 (50 MHz)	SPEED_CAP[2] = 1 when enabled. SPEED_CAP[2] = 0 when disabled. This setting is disabled in the reference design.
X4 (100 MHz)	SPEED_CAP[3] = 1 when enabled. SPEED_CAP[3] = 0 when disabled. This setting is disabled in the reference design.
X6 (150 MHz)	SPEED_CAP[4] = 1 when enabled. SPEED_CAP[4] = 0 when disabled. This setting is disabled in the reference design.
X8 (200 MHz)	SPEED_CAP[5] = 1 when enabled. SPEED_CAP[5] = 0 when disabled. This setting is enabled in the reference design.
X10 (250 MHz)	SPEED_CAP[6] = 1 when enabled. SPEED_CAP[6] = 0 when disabled. This setting is disabled in the reference design.
X12 (300 MHz)	SPEED_CAP[7] = 1 when enabled. SPEED_CAP[7] = 0 when disabled. This setting is disabled in the reference design.
X16 (400 MHz)	SPEED_CAP[7] = 1 when enabled. SPEED_CAP[7] = 0 when disabled. This setting is disabled in the reference design.
X24 (600 MHz)	SPEED_CAP[9] = 1 when enabled. SPEED_CAP[9] = 0 when disabled. This setting is disabled in the reference design. This setting is not accessible for MachXO3 and MachXO3D (grayed out).
Minimum System Clock (clk_i) Frequency (MHz)	Shows the recommended minimum system clock frequency.
Actual System Clock Frequency (MHz)	You must indicate the actual clk_i frequency that is used. This serves as the basis for calculating the necessary values in timer counters.
Supported Channels	
Enable Low Latency GPIO Channel	Enables or disables the low latency GPIO channel. This option is enabled in the reference design. When disabled, this option removes the LL GPIO ports from the IP and the top-level module.
Enable Normal Latency GPIO Channel	Enables or disables the low latency GPIO channel. This option is enabled in the reference design. When disabled, this option removes the LL GPIO ports from the IP and the top-level module.
Enable I2C Channel	Enables or disables the low latency GPIO channel. This option is enabled in the reference design. When disabled, this option removes the LL GPIO ports from the IP and the top-level module.
Enable UART Channel	Enables or disables the UART Channel. This option is enabled in the reference design. When disabled, this option removes the LL GPIO ports from the IP and the top-level module.

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Parameter	Description
Enable OEM Channel	Enables or disables the OEM Channel. This option is enabled in the reference design.
Enable Data Channel	Enables or disables the Data Channel. This option is enabled in the reference design. When disabled, this option removes the APB_S1 interface (SCM) or APB_M0 interface (HPM). This effectively disconnects the HPM CSR from access through the I2C-to-APB Bridge module. Disabling this option also removes data_ch_i and data_ch_o from the IP ports. However, these are already unused in the reference design.
Feature Capability	
Data Frame Type	Specifies the frame type for data frames. This option sets **Default I/O** by default, which is a predefined frame based on the DC-SCM LTPI 1.1 specification. You can also choose **Custom** to customize the data I/O frames.
Enable Full OEM Capabilities Type	This option can only be enabled when **Data Frame Type** is set to **Custom**. It enables customized value for **Capabilities Type** that is used in Advertise Frame, allowing the use for non-default and non-IP predefined capabilities.
Capabilities Type	Indicates if Advertise Frame mapping follows default, IP predefined, or user-customized capabilities mapping. Refer to the DC-SCM LTPI IP User Guide (FPGA-IPUG-02200) for more information on capabilities type details.
Custom OEM Capability (64b Hex)	Indicates the OEM feature capability of the IP. This information is used in Advertise Frame if Full OEM Capabilities Type ==Checked. Refer to the Advertise Frame details in the DC-SCM LTPI IP User Guide (FPGA-IPUG-02200) for more information.
Automatically Move to Configuration State	Specifies that when IP Mode == SCM, the IP automatically goes to configuration state after completing the required frame transmission for Advertise State. When unchecked, you must perform manual feature request related programming. Refer to the request features details in the DC-SCM LTPI IP User Guide (FPGA-IPUG-02200) for more information.

Note:

1. Changes to the options in this section are recorded at offset 0x08 of the CSR (SPEED_CAP). Multiple options can be enabled simultaneously.

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6.1.3.2. Frame Format Tab

This section provides descriptions of the parameters in the Frame Format tab. By default, the parameters are not editable. They can only be modified by setting **Data Frame Type** to **Custom**. The default setting adheres to the default I/O frame format as defined in the LTPI specification.

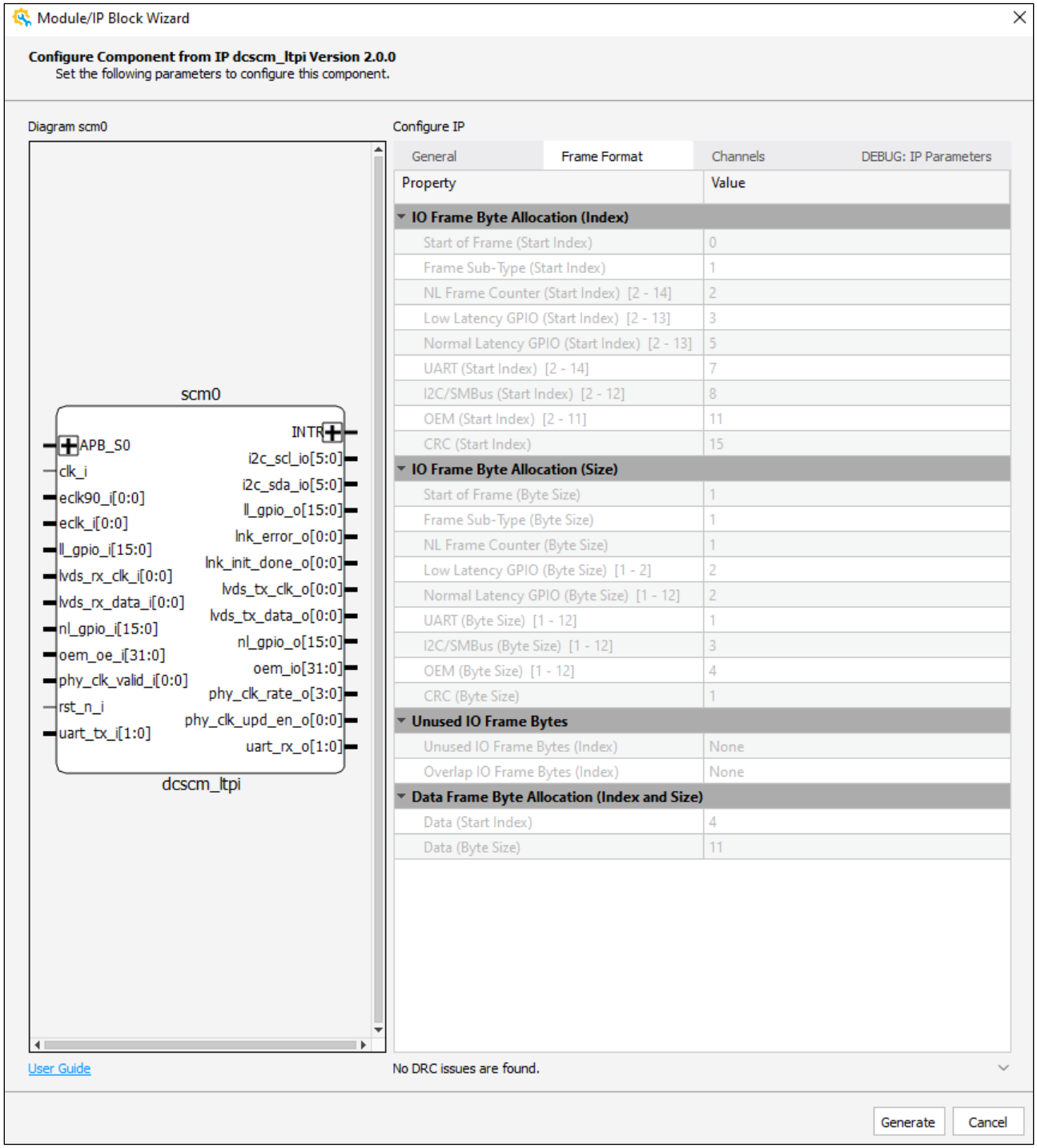

Figure 6.5. Frame Format Tab

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6.1.3.3. Channels Tab

This section provides descriptions of the parameters in the Channels tab.

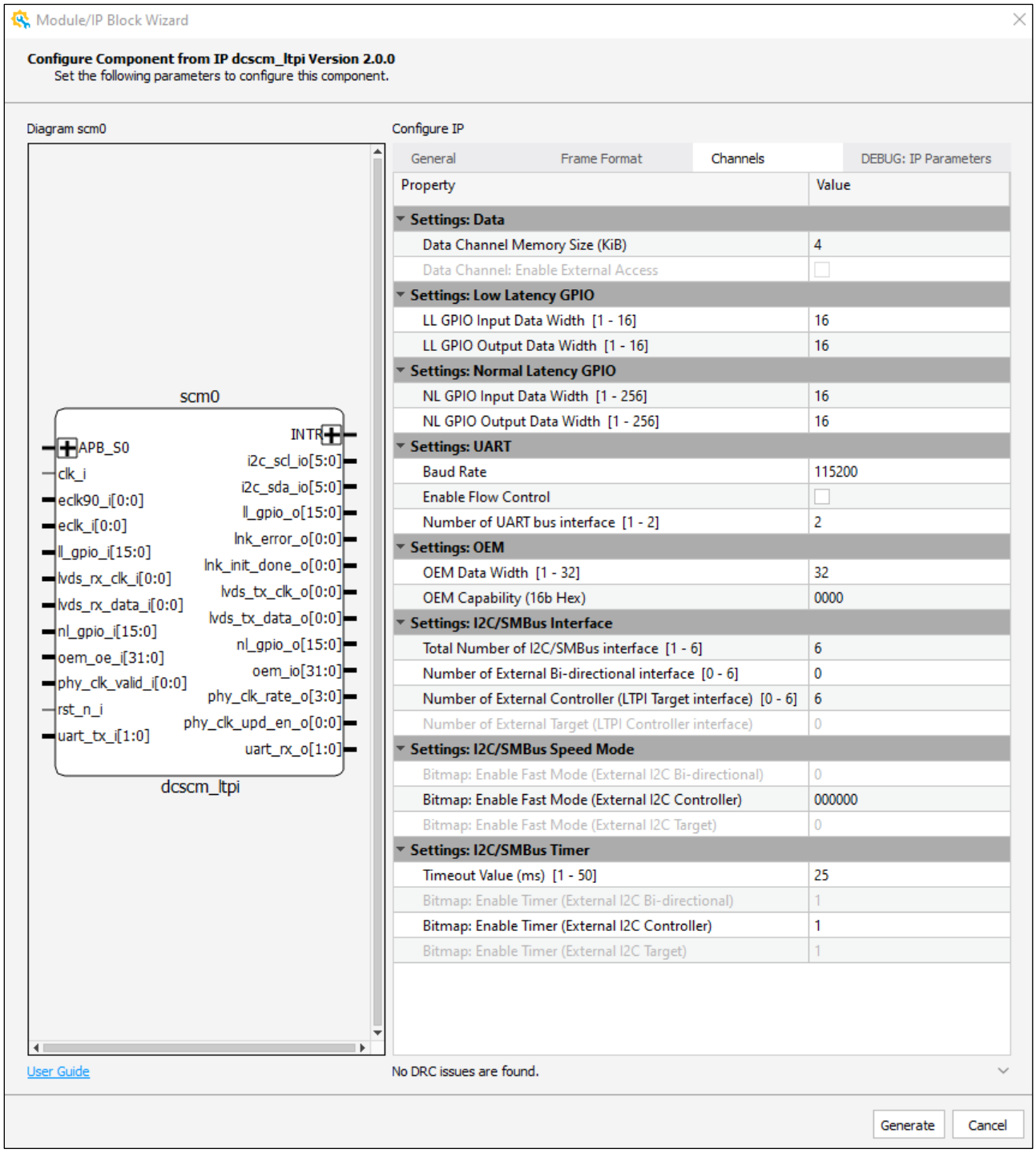

Figure 6.6. Channels Tab

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Table 6.2. Channels Tab Parameter Descriptions

Parameter	Description
Low Latency GPIO Settings	
LL GPIO Input Data Width	Determines the size of the Low Latency inputs. In the reference design, this option is set to *8* and can be configured for up to 16 bits.
LL GPIO Output Data Width	Determines the size of the Low Latency outputs. In the reference design, this option is set to *8* and can be configured for up to 16 bits.
Normal Latency GPIO Settings	
NL GPIO Input Data Width	Determines the size of the Normal Latency inputs. In the reference design, this option is set to *8*. Unlike LL GPIO, it can be configured to its maximum size of 256 bits. This is possible because NL GPIO bits are transmitted through the frame using a round-robin sequence, based on the size of the NL GPIO Payload Width per Frame. **Note:** Setting this option beyond the size of the NL GPIO Payload Width per Frame causes delays in I/O updates.
NL GPIO Output Data Width	Determines the size of the Normal Latency outputs. In the reference design, this option is set to *8* and can be configured to its maximum size of 256 bits. **Note:** Setting this option beyond the size of the NL GPIO Payload Width per Frame causes delays in I/O updates.
UART Settings	
Baud Rate	Determines the maximum baud rate that can be supported. In the reference design, this option is set to 115,200.
Enable Flow Control	Enables or disables the flow control signals, which are used to support multiple full-duplex UART interfaces tunneling. In the reference design, this option is disabled.
Number of UART bus Interface	Determines the number of UART buses enabled by the IP. In the reference design, this option is set to *1*.
I2C/SMBus Interface Settings	
Total Number of I2C/SMBus Interface	Determines the number of I2C buses enabled by the IP. Each number generates a new Bus X section in the GUI.
Number of External Bi-directional Interface	Specifies the number of I2C interface with bidirectional (both target and controller) functions.
Number of External Controller (LTPI Target Interface)	Specifies the number of I2C interface with target function only. This interface is connected to an external I2C Controller.
Number of External Target (LTPI Controller Interface)	Specifies the number of I2C interface with controller function only. This interface is connected to an external I2C Target.
I2C/SMBus Speed Settings	
Bitmap: Enable Fast Mode (I2C Bi-directional/Target/Controller)	Can be enabled to support fast mode I2C (400 kHz) or disabled to support standard mode I2C (100 kHz). Each bit represents a setting for each I2C interface. In the reference design, this option is disabled. **Note:** This option affects how the IP regenerates the I2C transaction. While a bus with Fast Mode enabled supports a 100 kHz transaction, the IP regenerates it at 400 kHz on the Target side.
I2C/SMBus Timer Settings	
Bitmap: Timeout Value (ms)	Specifies the timeout value in milliseconds. Each bit represents a setting for each I2C interface. **Note:** The timer counter requires the clock period, which is calculated based on the setting in Actual System Clock Frequency (MHz).
Bitmap: Enable Timer (I2C Bi-directional/Target/Controller)	Enables the built-in timer in each available I2C bus. Each bus has its own timer logic. This option is enabled by default.

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6.1.3.4. Debug: IP Parameters

This tab displays the parameter configurations applied to the project, reflecting the actual values implemented in the generated RTL. The configurations are intended for comparison and debugging purposes only.

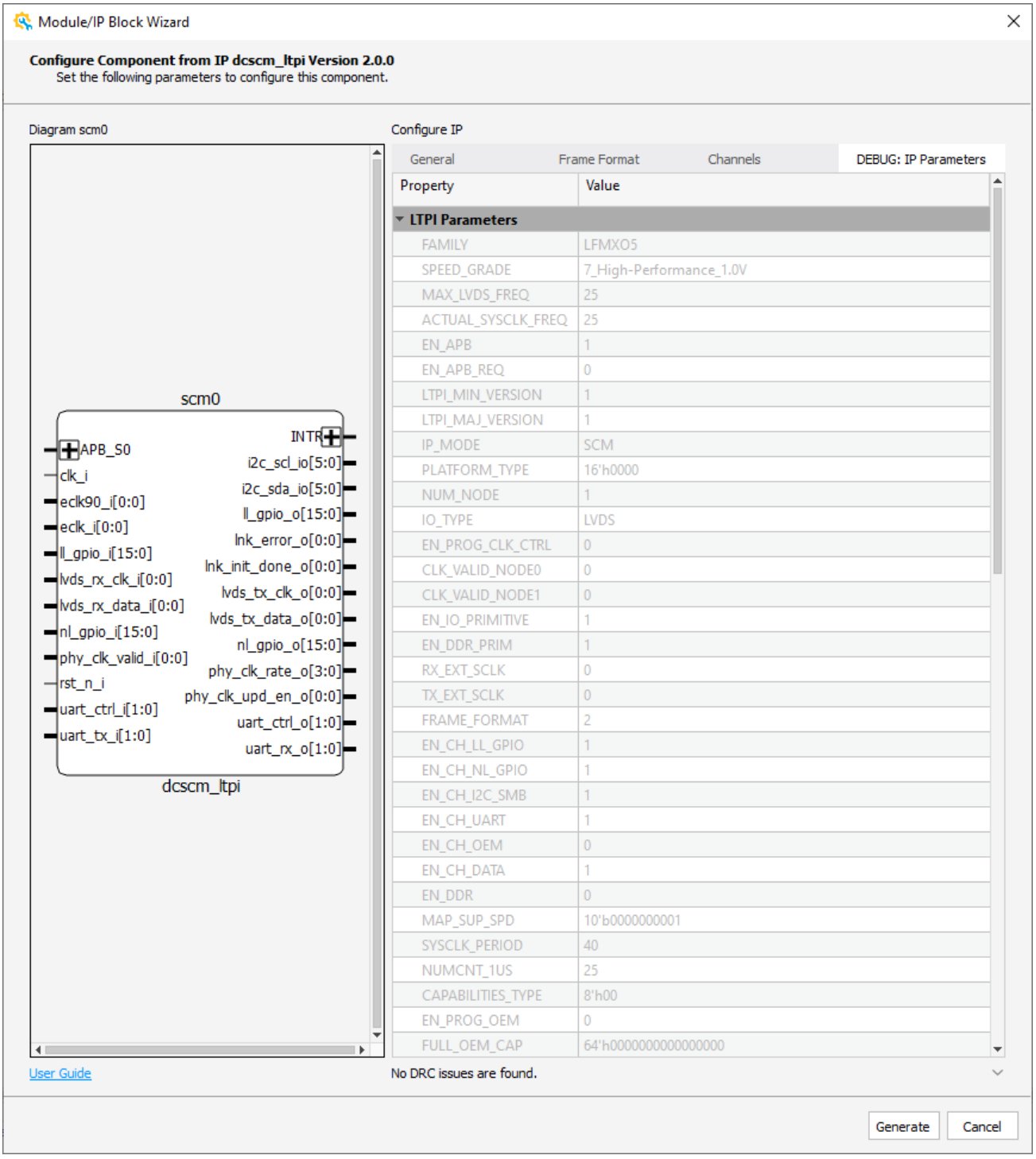

Figure 6.7. Debug: IP Parameters Tab

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Table 6.3. Debug: IP Parameters Tab Descriptions

Parameter	Description
LTPI Parameters	
FAMILY	Displays the device family selected during the creation of the Propel Builder project.
SPEED GRADE	Displays the performance grade selected during creation of the Propel Builder project.
MAX_LVDC_FREQ	Displays the maximum LTPI speed capability parameter as configured under the General settings in the General tab.
ACTUAL_SYSCLK_FREQ	Displays the actual LTPI system clock frequency as configured under the General settings in the General tab.
EN_APB	Indicates whether Data Channel is enabled or disabled as configured under the General settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_APB_REQ	Indicates whether an external access on Data Channel is enabled. When enabled, it provides an APB requester interface: • 0 – Disabled • 1 – Enabled
LTPI_MIN_VERSION	Displays the LTPI minor version. This setting is fixed and set by default.
LTPI_MAJ_VERSION	Displays the LTPI major version. This setting is fixed and set by default.
IP_MODE	Displays the IP mode, either SCM or HPM, as configured under the General settings in the General tab.
PLATFORM_TYPE	Displays the address as configured under the General settings in the General tab.
NUM_NODE	Indicates the number of nodes set on the IP.
IO_TYPE	Displays the I/O type (LVDS) as configured under the General settings in the General tab.
EN_PROG_CLK_CTRL	Indicates whether the program clock control is enabled or disabled as configured under the General settings in the General tab: • 0 – Disabled • 1 – Enabled
CLK_VALID_NODE0	Default value of the Clock Valid register, indicating that the clock is valid at Node 0.
CLK_VALID_NODE1	Default value of the Clock Valid register, indicating that the clock is valid at Node 1.
EN_IO_PRIMITIVE	Indicates whether the I/O primitive is enabled or disabled as configured under the General settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_DDR_PRIM	Default value is 1, which instantiates the DDR primitive.
FRAME_FORMAT	Indicates whether the frame format is set to Custom or Default as configured under the General settings in the General tab: • 1 – Custom • 2 – Default
EN_CH_LL_GPIO	Indicates whether the LL GPIO channel is enabled or disabled as configured under the General settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_CH_NL_GPIO	Indicates whether the NL GPIO channel is enabled or disabled as configured under the Supported Channels settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_CH_I2C_SMB	Indicates whether the I2C channel is enabled or disabled as configured under the Supported Channels settings in the General tab: • 0 – Disabled • 1 – Enabled

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Parameter	Description
EN_CH_UART	Indicates whether the UART channel is enabled or disabled as configured under the Supported Channels settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_CH_OEM	Indicates whether the OEM channel is enabled or disabled as configured under the Supported Channels settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_CH_DATA	Indicates whether the Data channel is enabled or disabled as configured under the Supported Channels settings in the General tab: • 0 – Disabled • 1 – Enabled
EN_DDR	Indicates whether the DDR is enabled or disabled as configured under the Speed Capability settings in the General tab: • 0 – Disabled • 1 – Enabled
MAP_SUP_SPD	Indicates the bit mapping of supported LTPI speeds.
SYSCLK_PERIOD	Displays the computed system clock period as configured under the LTPI speed capability settings in the General tab.
NUMCNT_1US	Indicates the number of clock cycles.
CAPABILITIES_TYPE	Displays the capabilities type as configured under Feature Capability settings in the General tab.
EN_PROG_OEM	Indicates whether the program OEM is enabled or disabled as configured under the Feature Capability settings (when Custom Data Frame is selected) in the General tab: • 0 – Disabled • 1 – Enabled
FULL_OEM_CAP	Indicates the default value of the Capability settings.
SCM_AUTO_CFG	Indicates whether the SCM automatic configuration state is enabled under the Feature Capability settings in the General tab: • 0 – Disabled • 1 – Enabled
LLGPIO_IDX	Displays the LL GPIO index as configured under the IO Frame Byte Allocation (Index) settings in the Frame Format tab.
LLGPIO_SIZE	Displays the LL GPIO byte size as configured under the IO Frame Byte Allocation (Size) settings in the Frame Format tab.
NLGPIO_IDX	Displays the NL GPIO index as configured under the IO Frame Byte Allocation (Index) settings in the Frame Format tab.
NLGPIO_SIZE	Displays the NL GPIO byte size as configured under the IO Frame Byte Allocation (Size) settings in the Frame Format tab.
NLCNTR_IDX	Displays the NL Frame Counter index as configured under the IO Frame Byte Allocation (Index) settings in the Frame Format tab.
NLCNTR_SIZE	Displays the NL Frame Counter byte size as configured under the IO Frame Byte Allocation (Size) settings in the Frame Format tab.
UART_IDX	Displays the UART index as configured under the IO Frame Byte Allocation (Index) settings in the Frame Format tab.
UART_SIZE	Displays the UART byte size as configured under the IO Frame Byte Allocation (Size) settings in the Frame Format tab.
I2CSMB_IDX	Displays the I2C/SMBus index as configured under the IO Frame Byte Allocation (Index) settings in the Frame Format tab.
I2CSMB_SIZE	Displays the I2C/SMBus byte size as configured under the IO Frame Byte Allocation (Size) settings in the Frame Format tab.
OEM_IDX	Displays the OEM Index as configured under the IO Frame Byte Allocation (Index) settings in the Frame Format tab.

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Parameter	Description
OEM_SIZE	Displays the OEM byte size as configured under the IO Frame Byte Allocation (Size) settings in the Frame Format tab.
DATA_IDX	Displays the data index as configured under the Unused IO Frame Bytes settings in the Frame Format tab.
DATA_SIZE	Displays the data size as configured under the Unused IO Frame Bytes settings in the Frame Format tab.
DATA_SPACE_AWID	Indicates the Data Channel address space multiplier with a constant value of 4 kB.
LL_IWID	Displays the LL GPIO input data width as configured under the LL GPIO Settings in the Channels tab.
LL_OWID	Displays the LL GPIO output data width as configured under the LL GPIO Settings in the Channels tab.
NL_IWID	Displays the NL GPIO input data width as configured under the NL GPIO Settings in the Channels tab.
NL_OWID	Displays the NL GPIO output data width as configured under the NL GPIO Settings in the Channels tab.
UART_MAX_BAUD	Displays the baud rate as configured under the UART settings in the Channels tab.
NUM_UART	Displays the number of UART channels as configured under the UART settings in the Channels tab.
UART_DWID	Indicates the number of UART channels that are enabled.
UART_FLOW_CTL_EN	Indicates whether UART flow control is enabled as configured under the UART settings in the Channels tab: • 0 – Disabled • 1 – Enabled
OEM_DWID	Displays the OEM data width as configured under the OEM settings in the Channels tab.
OEM_DEFAULT_CAP	Displays the OEM data width as configured under the OEM Capability settings in the Channels tab.
I2C_DWID	Displays the I2C/SMBus data width as configured under the OEM Capability settings in the Channels tab.
NUM_I2C_SMB	Displays the number of I2C/SMB interface as configured under the I2C/SMBus Interface settings in the Channels tab.
NUM_I2C_TGT	Displays the number of I2C/SMB target interface as configured under the I2C/SMBus Interface settings in the Channels tab.
NUM_I2C_CTL	Displays the number of I2C/SMB control interface as configured under the I2C/SMBus Interface settings in the Channels tab.
I2C_SMB_SPD	Displays the I2C speed as configured under the I2C/SMBus Interface settings in the Channels tab.
I2C_SMB_TIMEOUT	Displays the timeout value set for I2C as configured under the I2C/SMBus Interface settings in the Channels tab.
I2C_SMB_TIMER	Displays the I2C timer as configured under the I2C/SMBus Interface settings in the Channels tab.

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6.1.4. Adding a Custom RTL Module

This step can be used to add any of the following options:

- A placeholder RTL Module (only declarations of inputs and outputs).
- A wrapper module for RTL modules that will be added through Lattice Diamond or Lattice Radiant.
- An existing RTL module.

1. Double-click or drag the **rtl** glue logic from the IP Catalog to the Schematic window.

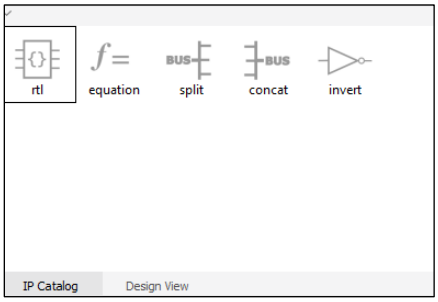

Figure 6.8. RTL Glue Logic

2. The user can either place the RTL code in the **Rtl** box of the Glue Logic window and then click **OK,** or

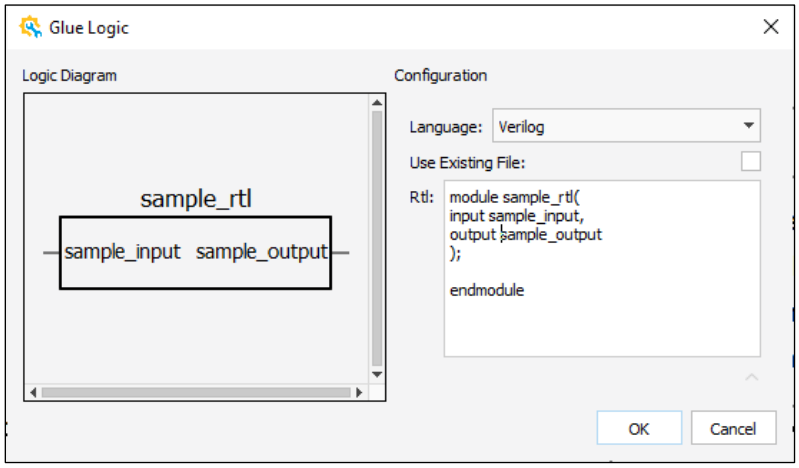

Figure 6.9. Using the RTL Box

3. Check the **Use Existing File** checkbox, link the file in **Path** field, and then click **OK**.

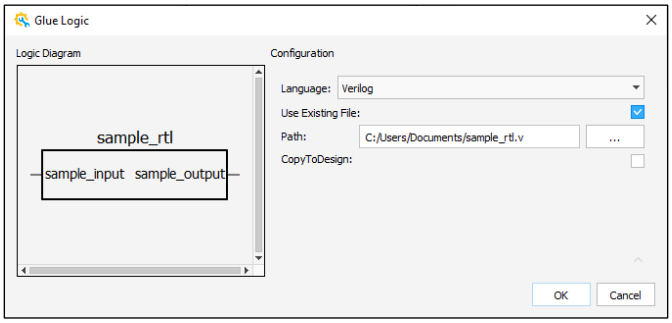

Figure 6.10. Using an Existing RTL File

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4. The user can either connect the module to existing modules, or connect it to a top-level module port. See the Add/Remove Top-Level Module Ports section for more details.

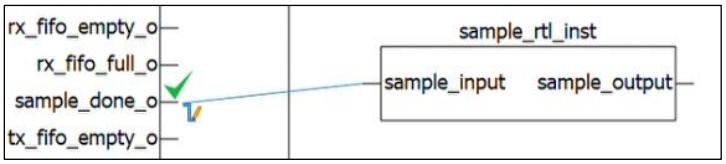

Figure 6.11. Connecting to Existing Modules

5. Click **Save**.

6.2. Lattice Diamond

This section discusses the changes that users can make to the reference design using Lattice Diamond. This section is only applicable to projects that use either MachXO3 or MachXO3D. For more information on using Lattice Diamond, refer to the Lattice Diamond software user guide.

6.2.1. Opening the Lattice Diamond Project

1. Unzip the reference design zip file.
2. Open Lattice Diamond 3.14. Note that the reference design has been tested using this version and does not guarantee backwards compatibility with previous Lattice Diamond versions.
3. Go to **File** > **Open** > **Project**.
4. Select the project file (*.ldf) found in *<Reference_Design_Folder>/Projects/<Design_Folder>*. In this section, the design used as an example is MachXO3D_SCM.

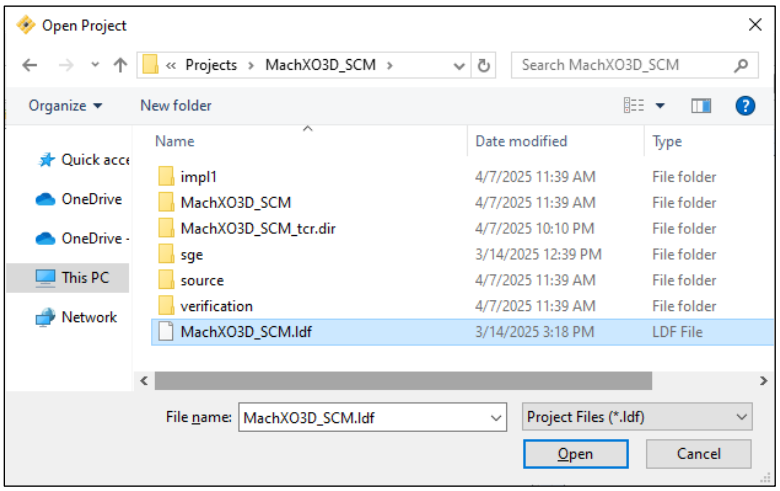

Figure 6.12. Selecting the Lattice Diamond Project

6.2.2. Changing the Target Device

This section explains how to change the project's target device. While it is possible to change to other device families using these steps, it is recommended to use the project dedicated to that device family and then use these steps to adjust the specifications for that device.

Note that changing to other device families may result in incompatibility with some modules in the design.

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1. Double-click the current target device or right-click then select Edit.

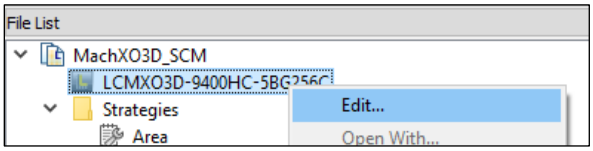

Figure 6.13. Selecting the Lattice Diamond Project

2. Choose the new target device.

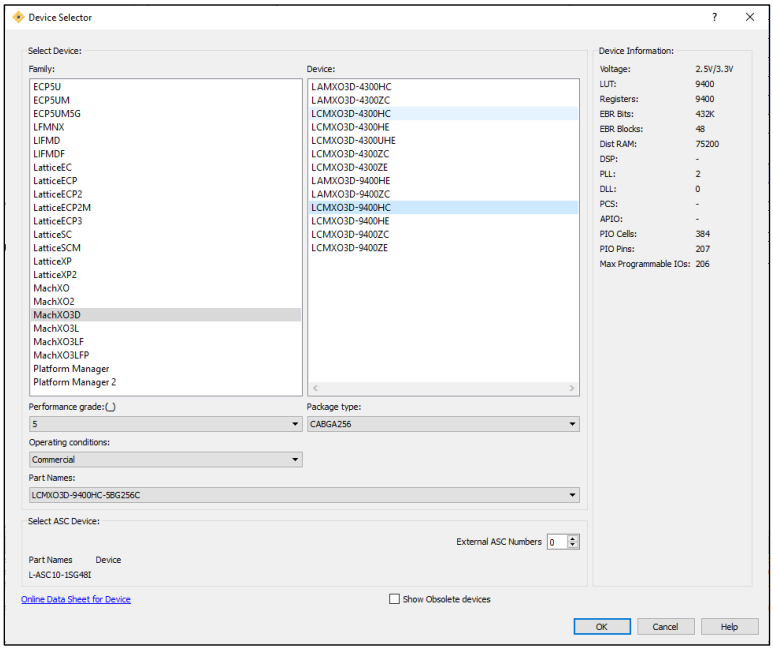

Figure 6.14. Device Selector Window

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6.2.3. Adding Modules to the Design

Below are the steps for adding a new module to the design.

1. Drag the file from Windows Explorer to the File List Window or,

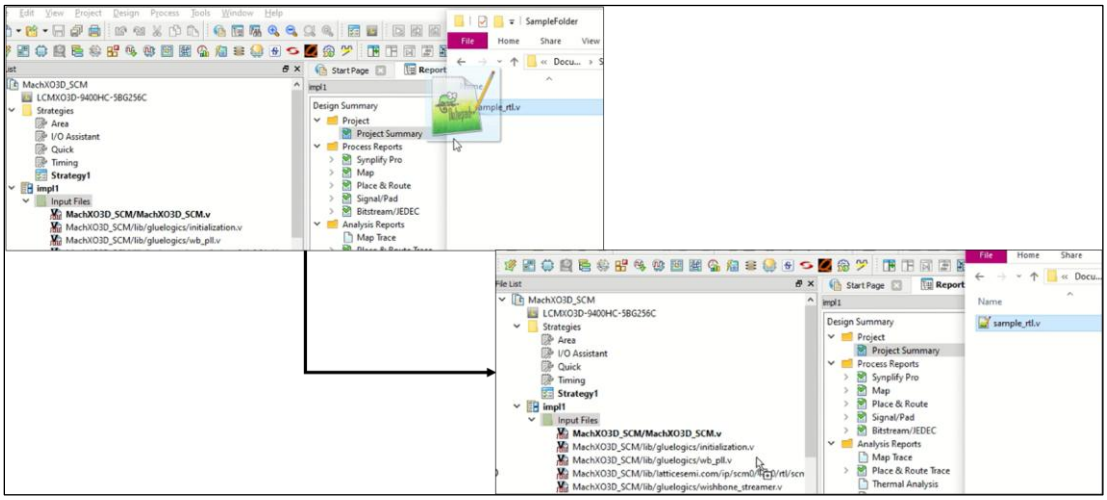

Figure 6.15. Adding a Module through Drag and Drop

2. Right-click the Input Files folder under the implementation, and select **Add** > **Existing File**.

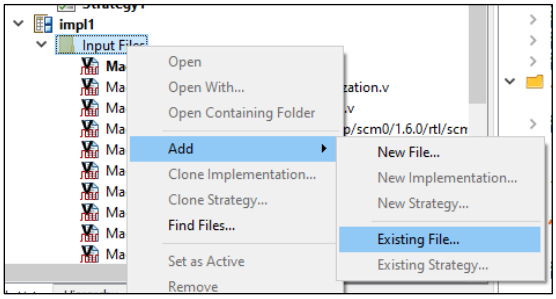

Figure 6.16. Selecting the Lattice Diamond Project

3. Select the file to be added and click **Add**.

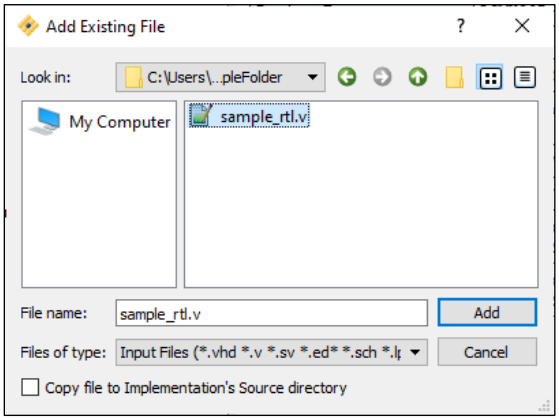

Figure 6.17. Add Existing File Window

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Note that for these modules to be used in the design, any of the following must be met:

- The added module is instantiated by one of the existing modules. This is especially useful for modules that are instantiated by wrapper modules in the Lattice Propel project. This is the recommended method of adding modules. See Adding a Custom RTL Module section for instructions on how to add wrapper modules.
- The added module is manually instantiated into one of the existing modules. This requires modification of the existing modules. This method is not recommended as any changes to the top-level module may be overwritten by changes to the Lattice Propel project.

6.2.4. Updating the Pin Assignments

There are two ways to change the pin assignment:

- Changing the constraint file (*.lpf)
- Using spreadsheet view

6.2.4.1. Updating Using Constraint File

1. Open the LPF file found under LPF constraint files.

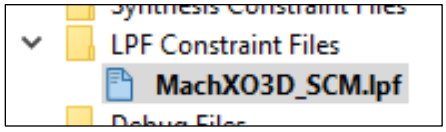

Figure 6.18. Constraint File (*.lpf)

2. Define or modify the I/O properties of the port.

```
IOBUF PORT "clk_i" IO_TYPE=LVCMOS33 PULLMODE=NONE ;
```

Figure 6.19. I/O Properties Example

3. Define or modify the location (pin assignment) of the port. For specific pin assignment requirements, refer to the Lattice FPGA Requirements section.

```
LOCATE COMP "clk_i" SITE "C8" ;
```

Figure 6.20. I/O Location Example

4. Save the file.

6.2.4.2. Updating Using Spreadsheet View

1. Run synthesis.

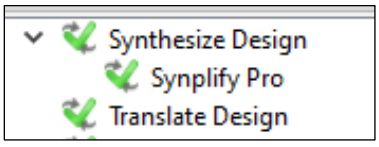

Figure 6.21. Lattice Diamond Synthesis

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2. Open the spreadsheet view by clicking the **Spreadsheet View** icon or by clicking **Tools** > **Spreadsheet View**.

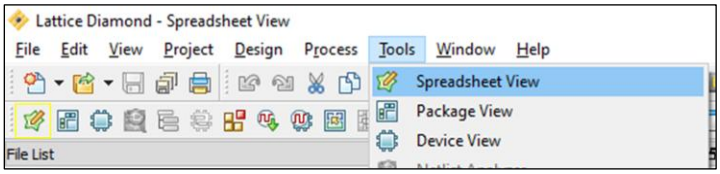

Figure 6.22. Open Spreadsheet View

3. Update the necessary properties. For specific pin assignment requirements, refer to the Lattice FPGA Requirements section.

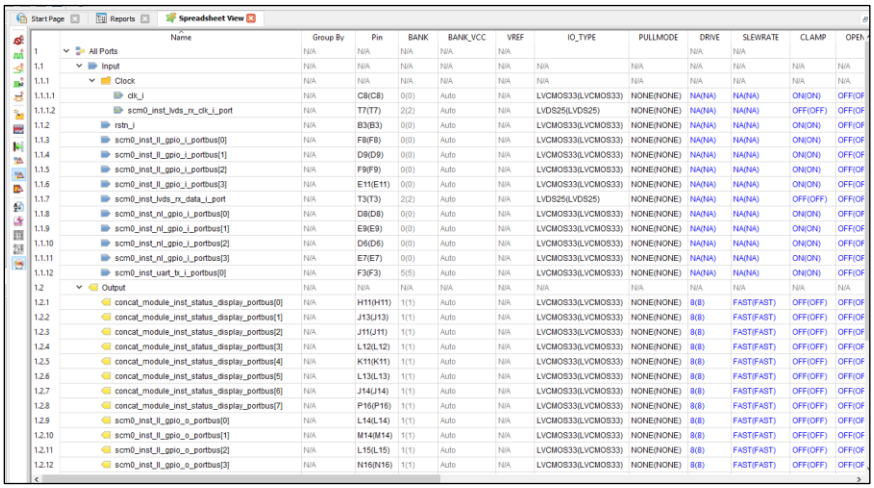

Figure 6.23. Spreadsheet View

4. Save the changes.

6.3. Lattice Radiant

This section discusses changes the user can make to the reference design using Lattice Radiant. This section is only applicable for the projects that use MachXO5-NX.

For more information on Lattice Radiant usage, refer to the Lattice Radiant software user guide.

6.3.1. Opening the Lattice Radiant Project

1. Unzip the reference design zip file.
2. Open Lattice Radiant 2024.2. Note that the reference design is tested using this version and does not guarantee backward compatibility with previous Lattice Radiant versions.
3. Go to **File** > **Open** > **Project**.
4. Select the project file (*.rdf) found in *<Reference_Design_Folder>/Projects/<Design_Folder>.* In this section, the design used as an example is **MachXO5NX_SCM**.

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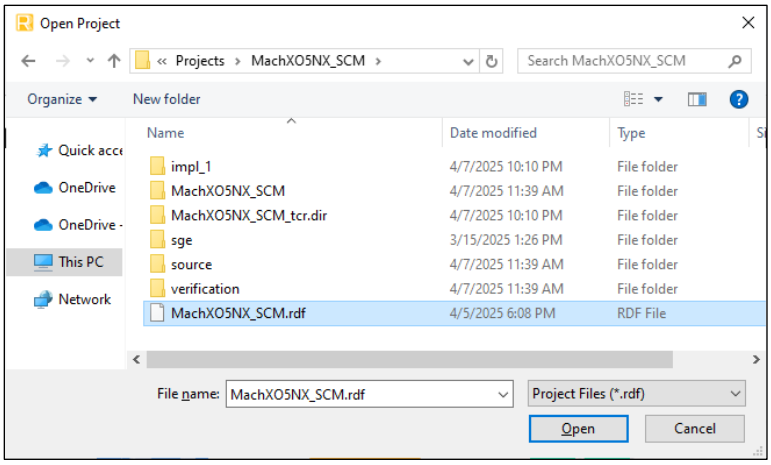

Figure 6.24. Selecting the Lattice Radiant Project

6.3.2. Adding Modules to the Design

Below are the steps for adding a new module to the design:

1. Drag the file from Windows Explorer to the File List window or,

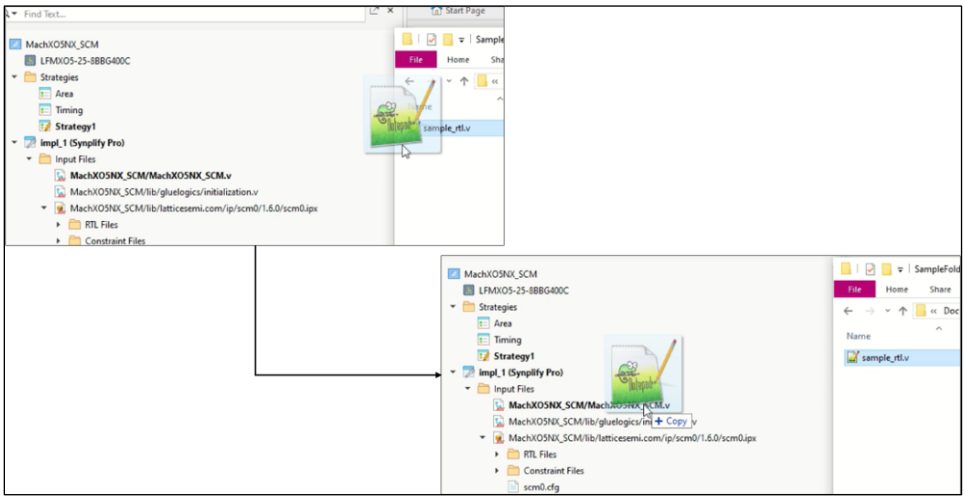

Figure 6.25. Adding a Module through Drag and Drop

2. Right-click the input files folder under the implementation, and select **Add** > **Existing File**.

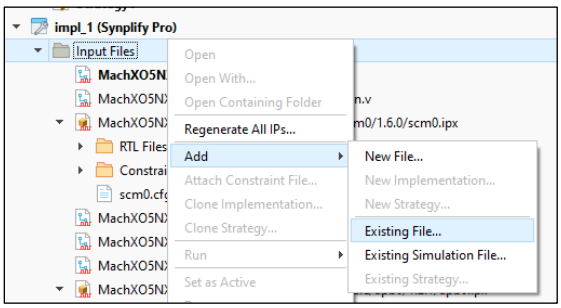

Figure 6.26. Selecting the Lattice Diamond Project

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3. Select the file to be added and click **Add**.

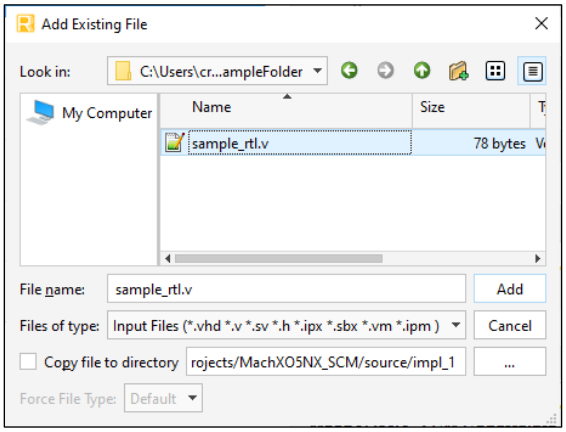

Figure 6.27. Add Existing File Window

Note that for these modules to be used in the design, any of the following conditions must be met:

- The added module is instantiated by one of the existing modules. This is especially useful for modules that are instantiated by wrapper modules in the Lattice Propel project. This is the recommended method of adding modules. See the Adding a Custom RTL Module section on how to add wrapper modules.
- The added module is manually instantiated into one of the existing modules. This requires modification of the existing modules. This method is not recommended as any changes to the top-level module may be overwritten by changes to the Lattice Propel project.

6.3.3. Updating the Pin Assignments

There are two ways to change the pin assignment:

- Changing the constraint file (*.pdc)
- Using the device constraint editor

6.3.3.1. Updating Using Constraint File

1. Open the *.pdc file found under **Post-Synthesis Constraint Files**.

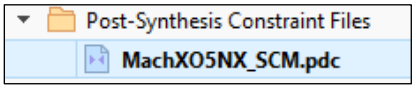

Figure 6.28. Lattice Radiant Constraint File (*.pdc)

2. Define or modify the I/O properties of the port.

```
ldc_set_port -iobuf {IO_TYPE=LVCMOS33 PULLMODE=NONE} [get_ports clk_i]
```

Figure 6.29. Lattice Radiant I/O Properties Example

3. Define or modify the location (pin assignment) of the port. For specific pin assignment requirements, refer to the Lattice FPGA Requirements section.

```
ldc_set_location -site {V1} [get_ports clk_i]
```

Figure 6.30. Lattice Radiant I/O Location Example

4. Save the file.

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6.3.3.2. Updating Using the Device Constraint Editor

1. Run synthesis.

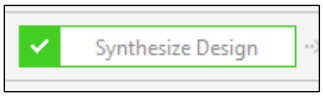

Figure 6.31. Lattice Radiant Synthesis

2. Open the device constraint editor by clicking the **Device Constraint Editor** icon or by clicking **Tools** > **Device Constraint Editor**.

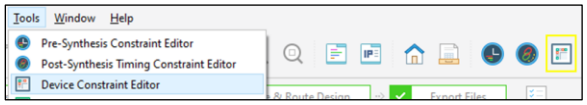

Figure 6.32. Open Device Constraint Editor

3. Update the necessary properties. For specific pin assignment requirements, refer to the Lattice FPGA Requirements section.

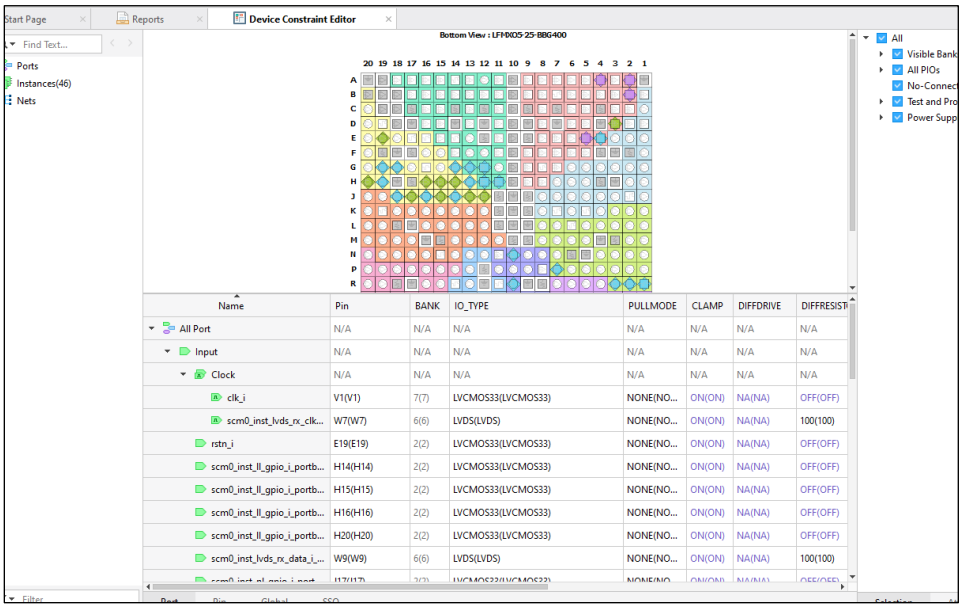

Figure 6.33. Device Constraint Editor

4. Save the changes.

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7. Simulating the Reference Design

7.1. Setting Up the Simulation

To simulate using the default configurations of the designs, perform the following steps:

1. Unzip the reference design zip file.
2. Open the simulation **do** file to be used. For this walkthrough, **SCM_XO3D_HPM_XO3D.do** will be used. Note that the succeeding steps apply regardless of the chosen **do** file.
3. On line 2 of the **do** file, replace the default path with the simulation folder path.

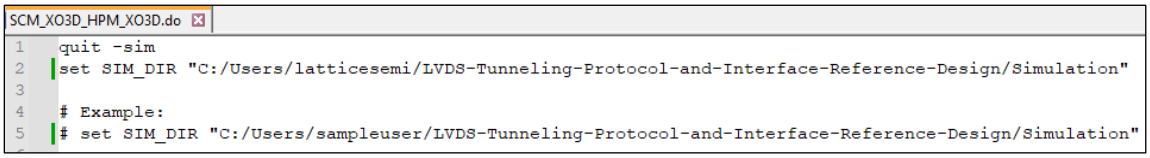

Figure 7.1. Simulation Do File

4. Click **Save**.
5. Open the simulator tool. For this walkthrough, **Questa Lattice OEM Edition-64 2024.2** will be used.
6. Go to **Tools** > **Td** > **Execute Macro**.

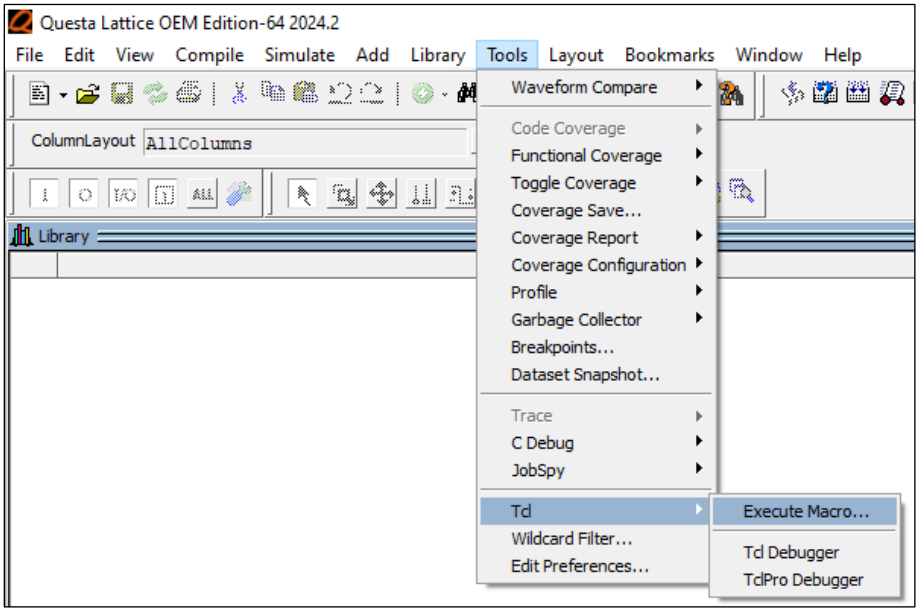

Figure 7.2. Execute Macro

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7. Open the simulation **do** file. Close and overwrite any existing projects when prompted.

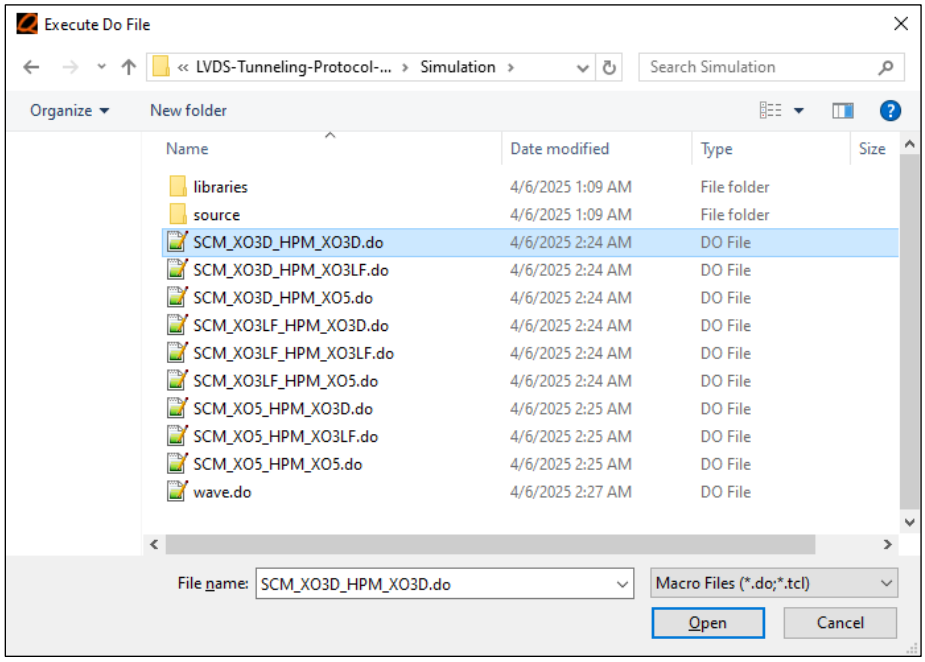

Figure 7.3. Execute Macro

7.2. Simulation Details and Results

The simulation is executed in six parts: Link Training, GPIO Test, OEM Test, UART Test, I2C Test, and CSR Test.

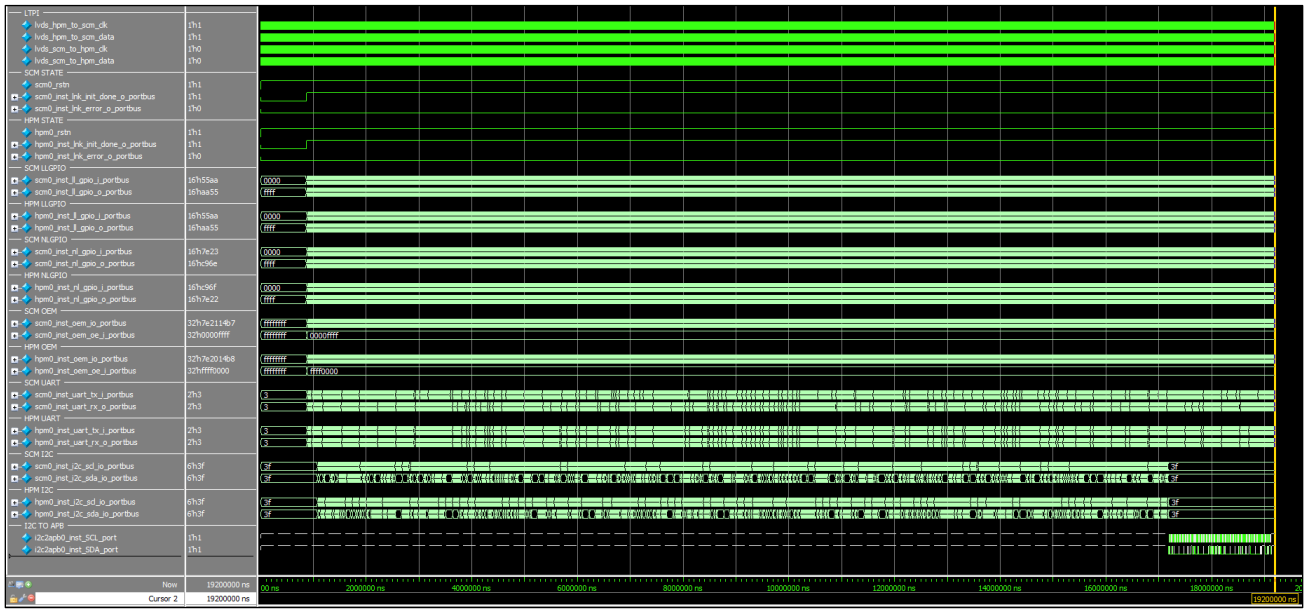

Figure 7.4. Simulation Wave View

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7.2.1. Link Training

1. After the reset is released at 100 ns, the LTPI connection between the SCM and the HPM starts transmitting data at 25 MHz SDR (LTPI Base Speed).

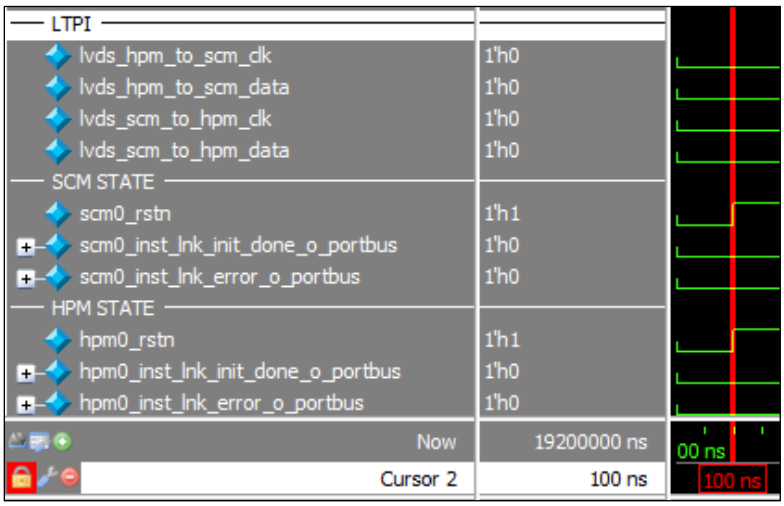

Figure 7.5. Reset Release

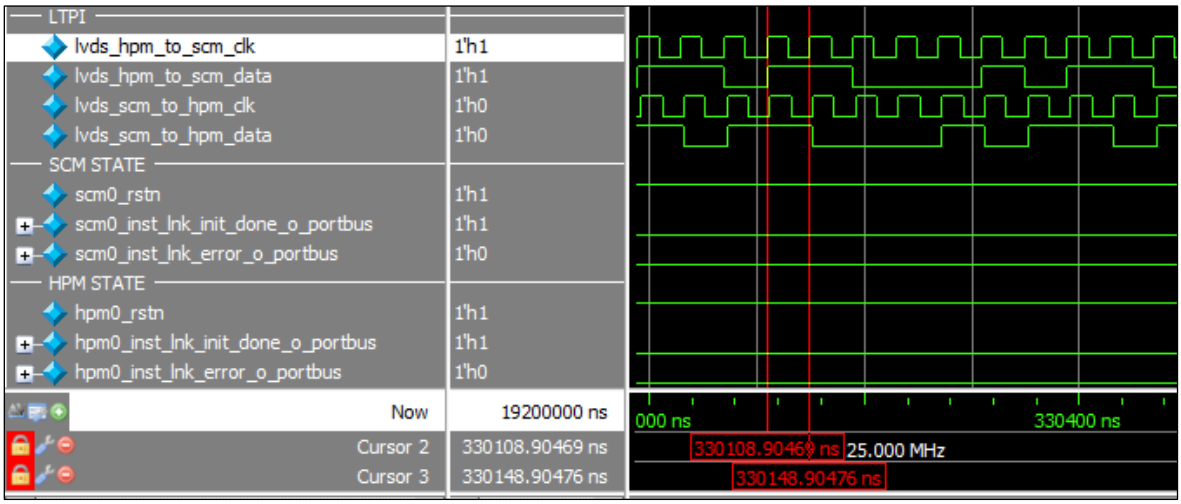

Figure 7.6. LTPI Base Speed

2. Once the Base Speed clock is stable, the system enters the Link Detect state. The transitions between the internal states are not explicitly shown in the simulation and are only observable through CSR access.
3. The transition between Base Speed and Target Speed is observable in the simulation. The default Target Speed of the reference design is 200 MHz DDR.

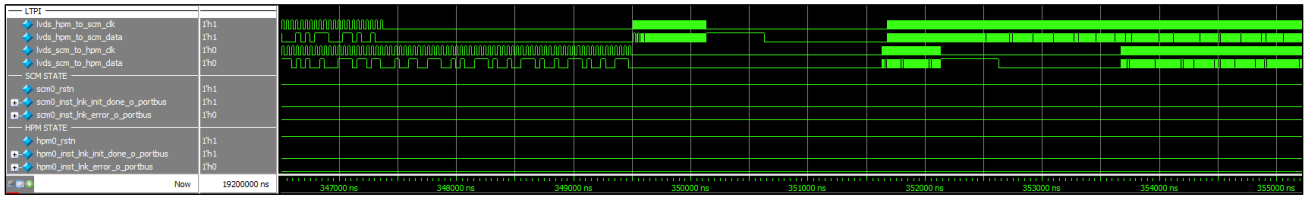

Figure 7.7. Base Speed to Target Speed Transition

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4. Both SCM and HPM realign their PHY using the new clock frequency and go through the Advertise, Configuration (SCM only), Accept (HPM only) and Active states.
5. A message is printed on the simulator console once the link is established (scm0_inst_lnk_init_done_o_portbus= 1 and hpm0_inst_lnk_init_done_o_portbus = 1).

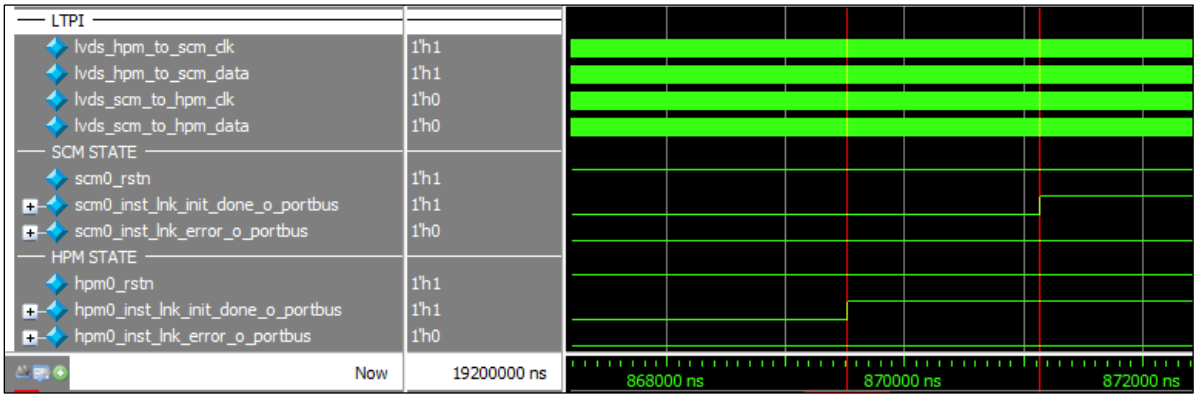

Figure 7.8. Link Training Done

```
2905295ns  : ########## Link Established ##########
```

Figure 7.9. Link Established Message

7.2.2. GPIO Test

This test evaluates both Low Latency GPIO and Normal Latency GPIO, in the following order:

1. The Low Latency Input of SCM is set to 0xAA55.
2. The test bench checks for changes in the Low Latency Output of HPM. If the change matches the set value of 0xAA55, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
3. The Low Latency Input of HPM is set to 0x55AA.
4. The test bench checks for changes in the Low Latency Output of SCM. If the change matches the set value of 0x55AA, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
5. The Normal Latency Input of SCM is set to 0x5A5A.
6. The test bench checks for changes in the Normal Latency Output of HPM. If the change matches the set value of 0x5A5A, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
7. The Normal Latency Input of HPM is set to 0xA5A5.
8. The test bench checks for changes in the Normal Latency Output of SCM. If the change matches the set value of 0xA5A5, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.

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After step 8, a message is printed to indicate that the GPIO test is complete. The test bench continues to stimulate all Low Latency and Normal Latency inputs by inversion and increments of one, respectively. However, all outputs are no longer checked by the test bench. This continuous activity helps simulate active LLGPIO and NLGPIO channels while the next channels are being tested.

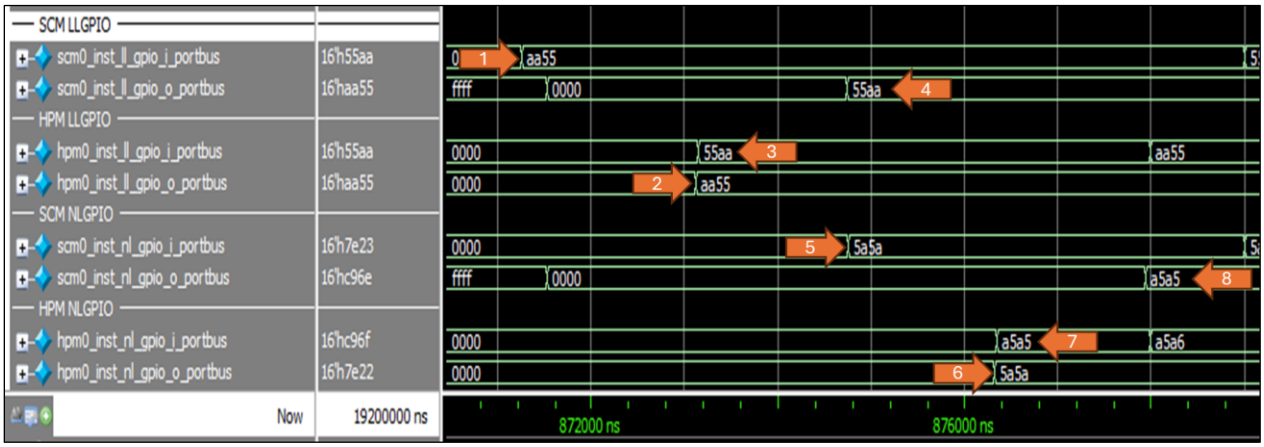

Figure 7.10. GPIO Test Flow

```
871243ns  : <<<<<GPIO Test - START>>>>>


871253ns  : SCM to HPM LLGPIO Test - START
871258ns  : Setting SCM LLGPIO Input to 0xAA55
873135ns  : HPM LLGPIO Output received 0xaa55
873140ns  : SCM to HPM LLGPIO Test - Passed
873140ns  : SCM to HPM LLGPIO Test - END


873150ns  : HPM to SCM LLGPIO Test - START
873155ns  : Setting SCM LLGPIO Input to 0x55AA
874743ns  : SCM LLGPIO Output received 0x55aa
874748ns  : HPM to SCM LLGPIO Test - Passed
874748ns  : HPM to SCM LLGPIO Test - END


874758ns  : SCM to HPM NLGPIO Test - START
874763ns  : Setting SCM NLGPIO Input to 0x5A5A
876335ns  : HPM NLGPIO Output received 0x5a5a
876340ns  : SCM to HPM NLGPIO Test - Passed
876340ns  : SCM to HPM NLGPIO Test - END


876350ns  : HPM to SCM NLGPIO Test - START
876355ns  : Setting SCM NLGPIO Input to 0xA5A5
877943ns  : SCM NLGPIO Output received 0xa5a5
877948ns  : HPM to SCM NLGPIO Test - Passed
877948ns  : HPM to SCM NLGPIO Test - END


877958ns  : GPIO Test - Passed
```

Figure 7.11. GPIO Test Console Messages

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7.2.3. OEM Test

This test evaluates the OEM channel in the following order:

1. SCM is set as input and HPM as output.
2. Fixed data (0x5A5A0F0F) is transmitted through SCM OEM.
3. The test bench checks for changes in HPM OEM. If the change matches the set value of 0x5A5A0F0F, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
4. HPM is set as input and SCM as output.
5. Fixed data (0xA5A5F0F0) is transmitted through HPM OEM.
6. The test bench checks for changes in SCM OEM. If the change matches the set value of 0xA5A5F0F0, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.

After step 6, a message is printed to indicate that the GPIO test is complete. The test bench continues to stimulate the upper 16 bits of SCM OEM and lower 16 bits of HPM OEM by increments of one. However, all outputs are no longer checked by the test bench. This continuous activity helps simulate an active OEM channel while the next channels are being tested.

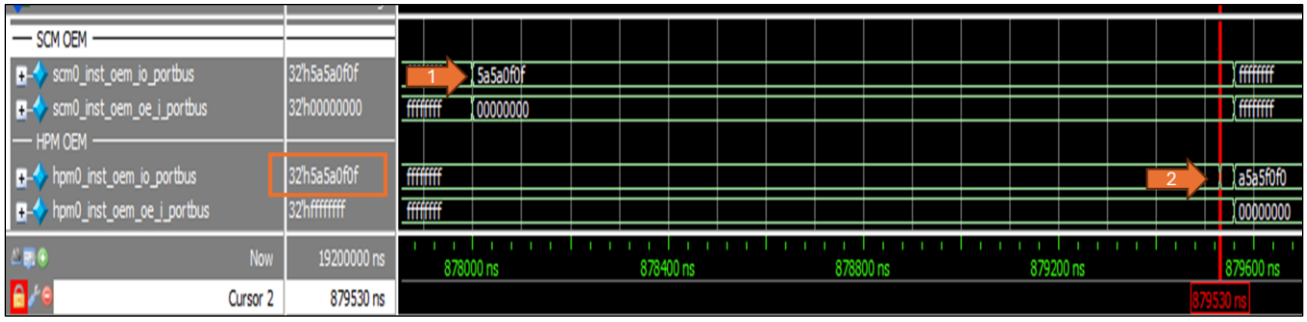

Figure 7.12. OEM Test Flow (SCM to HPM)

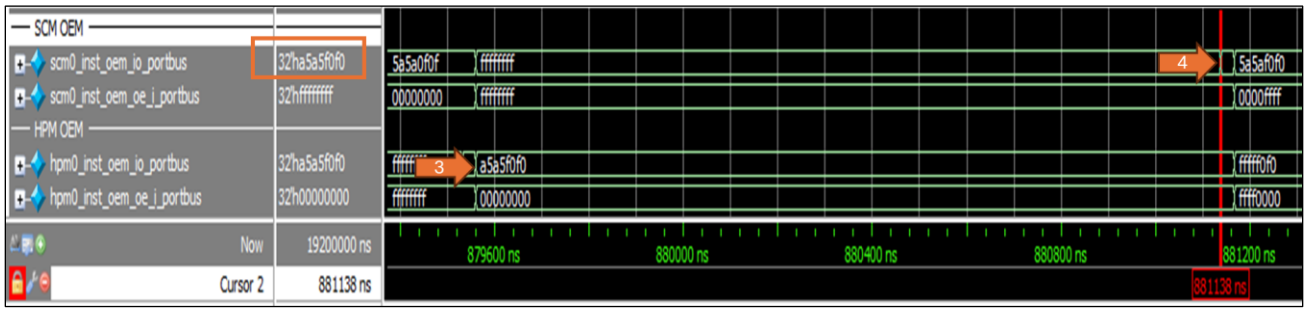

Figure 7.13. OEM Test Flow (SCM to HPM)

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```
877978ns  : <<<<<OEM Test - START>>>>>


877988ns  : SCM to HPM OEM Test - START
877993ns  : Setting SCM OEM as input and HPM OEM as output
877998ns  : Transmitting 0x5a5a0f0f
879535ns  : HPM OEM received 0x5a5a0f0f
879540ns  : SCM to HPM OEM Test - Passed
879540ns  : SCM to HPM OEM Test - END


879550ns  : HPM to SCM OEM Test - START
879555ns  : Setting HPM OEM as input and SCM OEM as output
879560ns  : Transmitting 0xa5a5f0f0
881143ns  : SCM OEM received 0xa5a5f0f0
881148ns  : HPM to SCM OEM Test - Passed
881148ns  : HPM to SCM OEM Test - END


881158ns  : OEM Test - Passed


881168ns  : <<<<<OEM Test - END>>>>>
```

Figure 7.14. OEM Test Console Messages

7.2.4. UART Test

This test evaluates the UART channel at a baud rate of 115,200.

1. Fixed data (0xA5) is sent through the Tx port of SCM Bus 0.
2. On the HPM side, the Tx and Rx are tied together, transmitting the exact data received from SCM back to the source.
3. Data is checked at the Rx port of SCM Bus 0. If the received data matches the transmitted data, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
4. Steps 1–3 are repeated for Bus 1, sending 0x5A instead.

After completion, a message is printed to indicate that the UART test is complete. The test bench continues to stimulate the Tx ports of SCM Bus 0 and Bus 1 by increments of one. However, the Rx ports of SCM Bus 0 and Bus 1 are no longer checked by the test bench. This continuous activity helps simulate an active UART channel while the next channel is being tested.

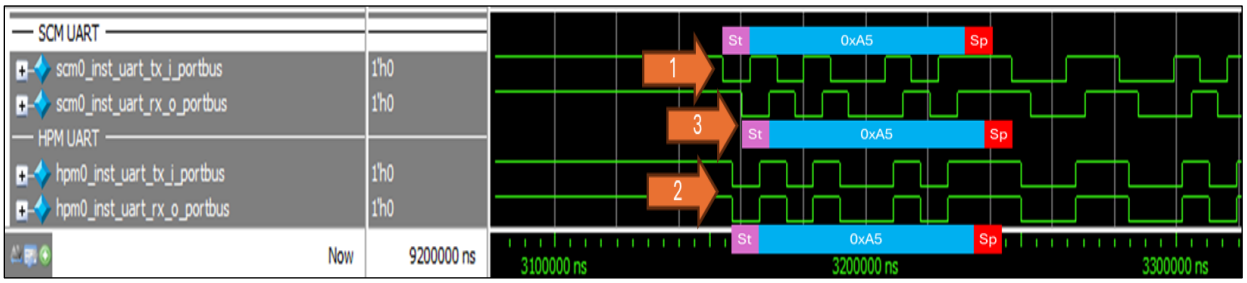

Figure 7.15. UART Test Flow

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```
 881178ns  : <<<<<UART Test - START>>>>>


 881188ns  : Sending 0xA5 on Bus 0
 971930ns  : SCM UART Bus 0 RX received 0xa5
 971935ns  : UART Bus 0 Test - Passed


 971945ns  : Sending 0x5A on Bus 1
1062580ns  : SCM UART Bus 1 RX received 0x5a
1062585ns  : UART Bus 1 Test - Passed


1062595ns  : UART Test - Passed
```

Figure 7.16. UART Test Console Messages

7.2.5. I2C Test

This test evaluates the I2C channel in standard mode (100 kHz). The channels are configured such that an external I2C controller is connected to SCM, while an external I2C target is connected to HPM. The external I2C target has a memory block for simulating the writing and reading of internal registers through I2C.

1. The external controller sends an initial 32-bit read command to address 0x00. The contents of this address are irrelevant and this step is performed only to show the initial status of the target register.
2. The external controller sends a 32-bit write command to address 0x00 with a fixed data.
3. To check if the write was successful, another 32-bit read command is sent to address 0x00. If the read data matches the written data, a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
4. Steps 1–3 are repeated for Bus 1 through Bus 5. Each previously tested I2C bus is idle.

After step 4, a message is printed to indicate that the I2C test is complete. The I2C channels are no longer stimulated by the test bench and remain in a pull-up state.

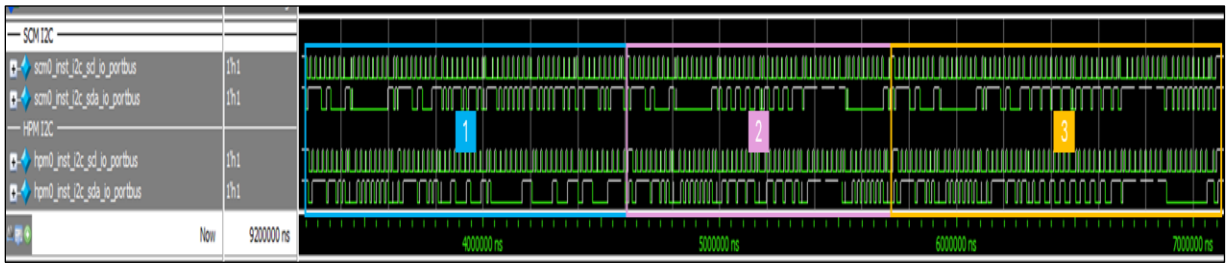

Figure 7.17. I2C Test Flow

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```
 1062615ns  : <<<<<I2C Test - START>>>>>


 1062625ns  : I2C Bus 0 Initial 32-bit Data Read from Address 0x00
 2012453ns  : I2C Bus 0 Received Data is 0x24810963
 2012458ns  : I2C Bus 0 Write Data 0xAA55FF00 to Address 0x00
 2826055ns  : I2C Bus 0 Read Data from Address 0x00
 3776453ns  : I2C Bus 0 Received Data is 0xaa55ff00
 3776458ns  : I2C Bus 0 Test - Passed


 3776468ns  : I2C Bus 1 Initial 32-bit Data Read from Address 0x00
 4722453ns  : I2C Bus 1 Received Data is 0x88ae9b92
 4722458ns  : I2C Bus 1 Write Data 0x55FF00AA to Address 0x00
 5536055ns  : I2C Bus 1 Read Data from Address 0x00
 6486453ns  : I2C Bus 1 Received Data is 0x55ff00aa
 6486458ns  : I2C Bus 1 Test - Passed


 6486468ns  : I2C Bus 2 Initial 32-bit Data Read from Address 0x00
 7416453ns  : I2C Bus 2 Received Data is 0x4ab91313
 7416458ns  : I2C Bus 2 Write Data 0xFF00AA55 to Address 0x00
 8226055ns  : I2C Bus 2 Read Data from Address 0x00
 9160453ns  : I2C Bus 2 Received Data is 0xff00aa55
 9160458ns  : I2C Bus 2 Test - Passed


 9160468ns  : I2C Bus 3 Initial 32-bit Data Read from Address 0x00
10086453ns  : I2C Bus 3 Received Data is 0xc782cec7
10086458ns  : I2C Bus 3 Write Data 0x00AA55FF to Address 0x00
10896055ns  : I2C Bus 3 Read Data from Address 0x00
11830453ns  : I2C Bus 3 Received Data is 0x00aa55ff
11830458ns  : I2C Bus 3 Test - Passed


11830468ns  : I2C Bus 4 Initial 32-bit Data Read from Address 0x00
12756453ns  : I2C Bus 4 Received Data is 0x62e92e8d
12756458ns  : I2C Bus 4 Write Data 0x55AA00FF to Address 0x00
13566055ns  : I2C Bus 4 Read Data from Address 0x00
14500453ns  : I2C Bus 4 Received Data is 0x55aa00ff
14500458ns  : I2C Bus 4 Test - Passed


14500468ns  : I2C Bus 5 Initial 32-bit Data Read from Address 0x00
15426453ns  : I2C Bus 5 Received Data is 0x79cd9245
15426458ns  : I2C Bus 5 Write Data 0x00FF55AA to Address 0x00
16236055ns  : I2C Bus 5 Read Data from Address 0x00
17170453ns  : I2C Bus 5 Received Data is 0x00ff55aa
17170458ns  : I2C Bus 5 Test - Passed


17170468ns  : I2C Test - Passed


17170478ns  : <<<<<I2C Test - END>>>>>
```

Figure 7.18. I2C Test Console Messages

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7.2.6. CSR Test

This test evaluates the integrated I2C-to-APB module's capability to access both SCM and HPM CSR. It also serves as a test of the data channel, which is the method by which the module can access the HPM CSR. An external I2C controller is connected to the module to execute the testing.

Note that by default, all HPM IDs were set to 0xBF17 and all SCM IDs were set to 0xCA26 during IP generation. This is arbitrary and can be removed or changed as necessary. These IDs were set to help differentiate the SCM and HPM CSR.

1. The external controller sends a 32-bit read command to address 0x0000020C, effectively reading offset 0x0C (Platform ID Local) of SCM CSR (mapped to 0x200-0x2FF by default).
2. If the read data matches the expected SCM ID (0x0000CA26), a message is printed indicating the test passed. Otherwise, the message indicates the test failed.
3. The external controller sends a 32-bit read command to address 0x0000120C, effectively reading offset 0x00 (Platform ID Local) of HPM CSR (mapped to 0x200-0x2FF by default, accessed through Data Channel).
4. If the read data matches the expected HPM ID (0x0000BF17), a message is printed indicating the test passed. Otherwise, the message indicates the test failed.

After step 4, a message is printed to indicate that the CSR test is complete. At this point, the simulation is finished.

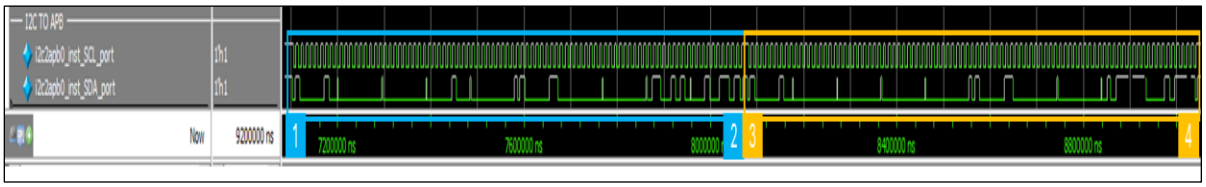

Figure 7.19. CSR Test Flow

```
17170488ns  : <<<<<CSR Access via I2C Test - START>>>>>


17170498ns  : SCM CSR Test - START
17170503ns  : Read Unique ID for SCM (Offset = 0x0000020C), expecting 0x0000CA26
18148555ns  : Received Data is 0x0000ca26
18148560ns  : SCM CSR Test - Passed
18148565ns  : SCM CSR Test - END
18148570ns  : HPM CSR Test - START
18148575ns  : Read Unique ID for HPM (Offset = 0x0000120C), expecting 0x0000BF17
19124555ns  : Received Data is 0x0000bf17
19124560ns  : HPM CSR Test - Passed
19124565ns  : HPM CSR Test - END


19124575ns  : <<<<<CSR Access via I2C Test - END>>>>>
```

Figure 7.20. CSR Test Console Messages

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8. Hardware Implementation

8.1. Requirements

8.1.1. DC-SCM 2.0 Requirements

This section discusses the hardware requirements as defined by the DC-SCM 2.0 Specification.

It defines the LVDS link as AC-coupled. As such, the following components are required on the hardware:

- DC Blocking Capacitor – placed on SCM only.
- Voltage Bias Circuit – placed close to the LVDS RX I/O Buffer.

To ensure that these specifications are met within the board design, it is highly recommended that both DC blocking capacitors and the voltage bias circuit be added externally on any user board design.

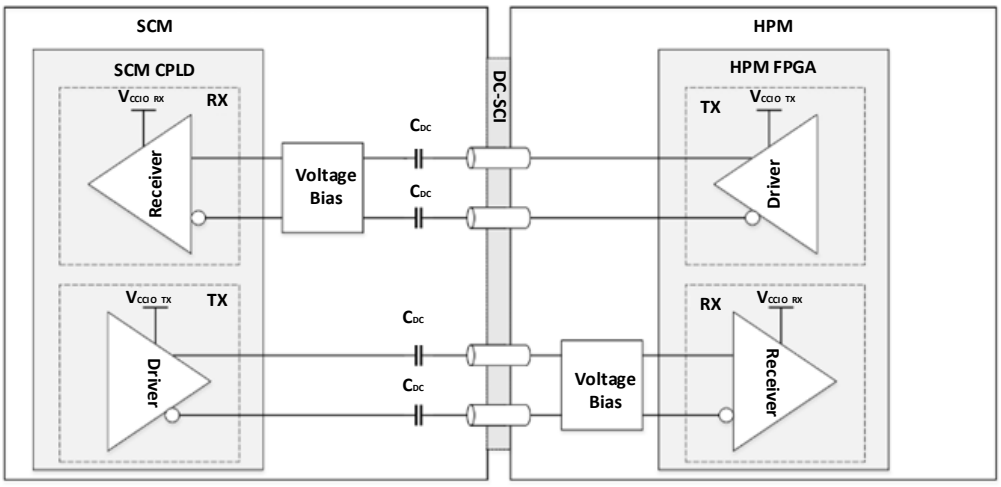

Figure 8.1. LVDS Link

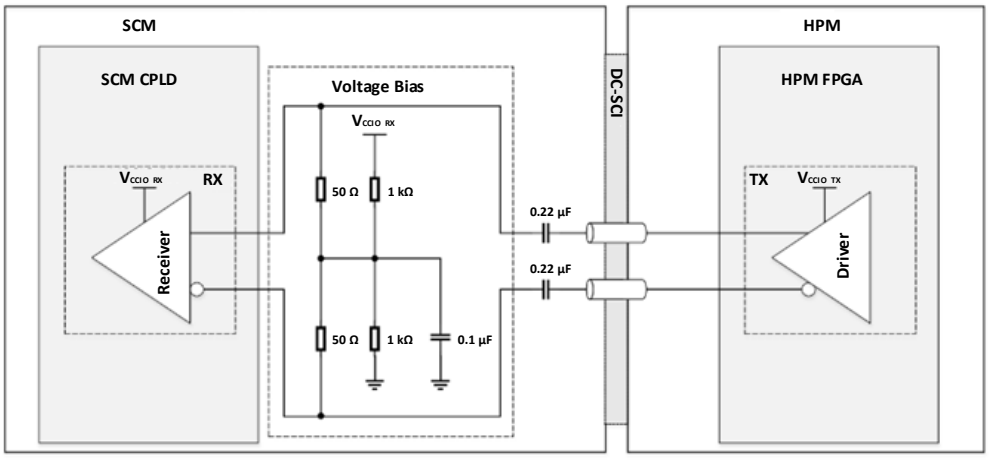

Figure 8.2. LVDS Link

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Table 8.1. LVDS Electrical Requirements

Parameter	Min	Max	Description
V_{OD}	100 mV	800 mV	Output Differential Voltage Swing.
V_{ID}	100 mV	800 mV	Input Differential Voltage Swing.
$V_{CCIO\ RX/TX}$	2.5 V	3.3 V	LVDS VCCIO Voltage (Refer to MachXO3/MachXO3D/Mach-NX documentation).
V_{ICM}	N/A	($V_{CCIO\ RX}$ / 2) + 20%	Input common mode voltage on LVDS I/O pins.
C_{DC}	0.22 µF	N/A	DC blocking capacitor.
R_{TT}	100 Ω – 5%	100 Ω + 5%	LVDS Termination Resistor (can be set internally on the device).

8.1.2. Lattice FPGA Requirements

This section describes the device-specific requirements for implementing the reference design on hardware. Note that by default, these requirements are already covered by the reference design.

Below is the guidance for the pin assignments of input and output LVDS for MachXO3 and MachXO3D:

- Input LVDS: These signals can only be assigned to A/B pairs (PBxxA/PBxxB) on Bank 2. In addition, the LVDS clock should be assigned to a PCLK pin (PCLKT2_x /PCLKC2_x).
- Output LVDS: These signals can only be assigned to A/B pairs (PTxxA/PTxxB) on Bank 0.

For MachXO5-NX, the LVDS pairs (both input and output) should be mapped to high-performance I/O banks (bottom banks).

Disclaimer: This is not a comprehensive list of requirements for each device. For more information, refer to the supporting documents for each device available on the following web pages:

- MachXO3 web page
- MachXO3D web page
- MachXO5-NX web page

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9. Resource Utilization

The resource utilization depends on the DC-SCM LTPI IP configuration. The following tables show the resource utilization of the reference design based on device family.

Note: Resource utilization values may vary depending on whether additional or fewer channel buses are used.

Table 9.1. MachXO3 Device Resource Utilization for Demo Designs

Configuration	LUT4	PFU Register	EBR	Slice
DC-SCM LTPI IP – SCM				
LTPI Reference Design	2447	1708	2	1296
LTPI IP (Default I/O Setting): LLGPIO: 16-bit NLGPIO: 16-bit I2C/SMBus: 6 bus UART : 2 channels OEM : 32-bit	2087.5	1402	2	1098.05
Miscellaneous LTPI Module Examples include: APB Streamer, Timeout, I2C-to-APB Bridge modules.	359.5	306	0	197.95
DC-SCM LTPI IP – HPM				
LTPI Reference Design	2916	1671	2	1527
LTPI IP (Default I/O Setting): LLGPIO: 16-bit NLGPIO: 16-bit I2C/SMBus: 6 bus UART : 2 channels OEM : 32-bit	2822.5	1576	2	1465.48
Miscellaneous LTPI Modules Examples include: APB Streamer, Timeout, I2C-to-APB Bridge modules.	93.5	95	0	61.52

Table 9.2. MachXO3D Device Resource Utilization for Demo Designs

Configuration	LUT4	PFU Register	EBR	Slice
DC-SCM LTPI IP – SCM				
LTPI Reference Design	2535	1805	2	1349
LTPI IP (Default I/O Setting): LLGPIO: 16-bit NLGPIO: 16-bit I2C/SMBus: 6 bus UART : 2 channels OEM : 32-bit	2174.5	1499	2	1155.82
Miscellaneous LTPI Module Examples include: APB Streamer, Timeout, I2C-to-APB Bridge modules.	360.5	306	0	193.18
DC-SCM LTPI IP – HPM				
LTPI Reference Design	2916	1671	2	1527
LTPI IP (Default I/O Setting): LLGPIO: 16-bit NLGPIO: 16-bit I2C/SMBus: 6 bus UART : 2 channels OEM : 32-bit	2822.5	1576	2	1465.48

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Configuration	LUT4	PFU Register	EBR	Slice
Miscellaneous LTPI Modules Examples include: APB Streamer, Timeout, I2C-to-APB Bridge modules.	93.5	95	0	61.52

Table 9.3. MachXO5-NX Device Resource Utilization for Demo Designs

Configuration	LUT4	PFU Register	EBR	Slice
DC-SCM LTPI IP – SCM				
LTPI Reference Design	2702	1812	2	3326
LTPI IP (Default I/O Setting): LLGPIO: 16-bit NLGPIO: 16-bit I2C/SMBus: 6 bus UART : 2 channels OEM : 32-bit	2343	1533	2	—
Miscellaneous LTPI Module Examples include: APB Streamer, Timeout, I2C-to-APB Bridge modules.	364	276	0	—
DC-SCM LTPI IP – HPM				
LTPI Reference Design	2936	1651	2	3531
LTPI IP (Default I/O Setting): LLGPIO: 16-bit NLGPIO: 16-bit I2C/SMBus: 6 bus UART : 2 channels OEM : 32-bit	2803	1586	2	—
Miscellaneous LTPI Modules Examples include: APB Streamer, Timeout, I2C-to-APB Bridge modules.	132	65	0	—

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10. Common Issues and Troubleshooting

10.1. Link Not Reaching Active State

The most common issue observed in the design is that the LTPI does not reach the Active State (status_display[0] = 0). This can be caused by any of the following:

1. IP Feature Capability Mismatch
   - This occurs when the feature capability of HPM and SCM does not match, meaning that one or more of the enabled or disabled interfaces do not match. This can be checked using the **Capabilities** tab of the IP (as shown in Figure 10.1).

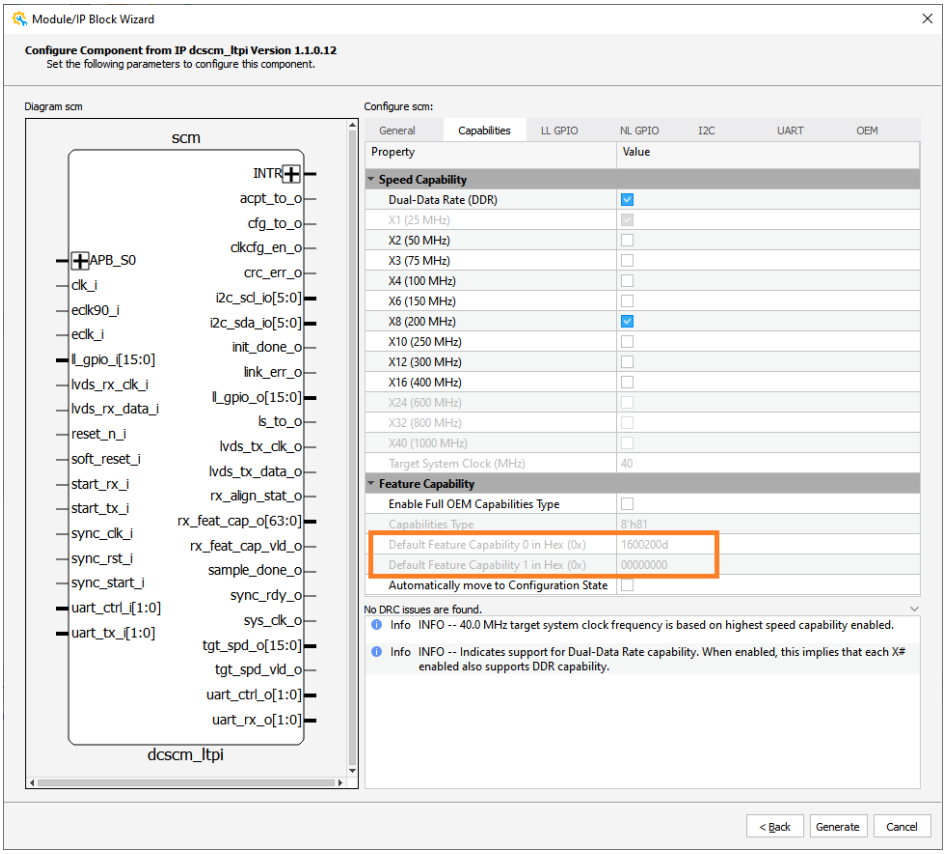

Figure 10.1. Feature Capabilities

2. Floating Inputs
   - This issue occurs when interface inputs, LL inputs, NL inputs, I2C bus, and UART TX do not have valid logic values and are floating or in tri-state. It is indicated by consecutive crc_err_o assertions during start-up. This can be resolved by placing initial values for LL, NL, and UART, as well as pull-up for the I2C bus.

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10.2. I2C Bus Hang

This issue sometimes occurs when the I2C transaction is abruptly ended or interrupted. In this scenario, the SCL or SDA of the LTPI I2C channel will remain indefinitely on logic low. This can be resolved through the following methods:

1. Inducing an external reset – this, however, does not guarantee that the issue will not recur.
2. Enabling the I2C timer for both SCM and HPM – this is discussed in Modifying the Reference Design section.
3. Sending an I2C bus reset through the offset 0x3C – Figure 10.2 describes the register format of offset 0x3C.

Offset	Register Name	Access	Default Value	Register Description		
				Bit	Field	Field Description
IP Control						
0x3C	I2C_BUS_RST	RO	32'h0	[31:24]	RSVD	Reserved bits.
		RW		[23:0]	i2c_bus_rst	I²C bus controller reset. When asserted, IP releases the local bus and resets the interface controller of the corresponding bus link number. Each bit index is mapped to each I²C bus link reset with bus link 0 occupying index 0. [0] – I²C bus 0 reset [1] – I²C bus 1 reset ... [23] – I²C bus 23 reset

Figure 10.2. I2C_BUS_RST Register

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References

- DC-SCM LTPI IP User Guide (FPGA-IPUG-02200)
- Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057)
- Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- MachXO3 sysCLOCK PLL Design and User Guide (FPGA-TN-02058)
- MachXO3D sysCLOCK PLL Usage Guide (FPGA-TN-02070)
- DC-SCM 2.0 Specification
- Open Compute Project web page
- LVDS Tunneling Protocol and Interface Reference Design web page
- MachXO3 web page
- MachXO3D web page
- MachXO5-NX web page
- Lattice Diamond Software web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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Revision History

Revision 1.5, September 2025

Section	Change Summary
All	• Added the OCP logo to the document cover page. • Updated all instances of *APB Slave Error* to *APB Completer Error*. • Made editorial fixes.
Abbreviations in This Document	Added *AC*, *AMBA*, *FPGA*, *GDDR*, *GUI*, *HDL*, *IPK*, *LUT*, *N/A*, *OCP*, *PFU*, *PLL*, *SCM*, and *USB*.
Introduction	• Added the *OCP Ready™* statement to the Introduction section. • Updated *Software Requirements* and *Hardware Requirements* in Table 1.1. Summary of the Reference Design.
Directory Structure and Files	• Updated Figure 2.1. Directory Structure. • Added *IPK Subfolder* to Table 2.1. File List.
Functional Description	• Removed the 25 MHz Generator module description in the Functional Description section. • Updated Figure 3.2. SCM Block Diagram, Figure 3.3. HPM Block Diagram, Figure 3.4. LTPI (SCM) Block Diagram, and Figure 3.5. LTPI (HPM) Block Diagram. • Updated Table 3.1. LTPI Clock Source Signals, Table 3.2. Reset Timer Signals, Table 3.4. PLL Streamer Logic Signals, and Table 3.4. PLL Streamer Logic Signals. • Removed the *25 MHz Generator*, *Initialization Logic*, *Clock Generator*, *APB Interconnect (SCM Only)*, and *APB Feedthrough (HPM Only)* sections. • Updated the descriptions in the Reset Timer, LTPI Clock Source, Clocking Scheme, and DC-SCM LTPI IP Control and Status Registers sections. • Removed *Table 3.15. DC-SCM LTPI IP Registers*.
Signal Description	Updated Table 4.1. SCM Top Module Signals and Table 4.2. HPM Top Module Signals.
Timing Constraints	Updated this section.

Modifying the Reference Design	• In the Changing the DC-SCM LTPI IP Settings section:
	  • Updated Figure 6.3. Check Generated Result Window – Figure 6.5. Frame Format Tab.
	  • Updated the General Tab and Frame Format Tab sections.
	  • Removed the *Capabilities Tab*, *LL GPIO Tab*, *NL GPIO Tab*, *I2C Tab*, *UART Tab*, and *OEM Tab* sections.
	  • Added the Channels Tab and Debug: IP Parameters sections.
	• Removed the *Removing the 25 MHz Generator*, *Changing the 25 MHz Generator Input*, and *Changing the 25 MHz Generator Input* sections.

Simulating the Reference Design	• Updated the following sections:
	  • Simulation Details and Results
	  • Link Training (including all figures)
	  • GPIO Test (including all figures)
	  • UART Test (including Figure 7.16. UART Test Console Messages)
	  • I2C Test (including Figure 7.18. I2C Test Console Messages)
	  • CSR Test (including Figure 7.20. CSR Test Console Messages)
	• Added the OEM Test section.

Hardware Implementation	• Removed *Table 8.1. Pin Assignments* and its description. • Updated the disclaimer in the Lattice FPGA Requirements section.
Common Issues and Troubleshooting	Removed the *Clock Mismatch* information in the Link Not Reaching Active State section.
Resource Utilization	Updated this section.
References	Added the *Open Compute Project* web page and removed *Lattice Propel 2024.2 Builder User Guide (FPGA-UG-02219)*, *Lattice Radiant Software 2024.2 User Guide*, and *Lattice Diamond 3.14 User Guide*.

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Revision 1.4, June 2025

Section	Change Summary
All	Minor editorial fixes.

Introduction	• Removed the following subsections:
	  • Limitations
	  • Conventions
	  • Attribute Names
	• Added new subsections:
	  • Quick Facts
	  • Naming Conventions
	• Removed support for Mach-NX.

Directory Structure and Files	• Added this section. • Added new directory structure overview and description.

Functional Description	• Removed the Pin Description section and replaced it with the *Functional Description* section.
	• Removed the following subsections:
	  • Overview
	  • Reference Design Specification
	  • Target Speed Setting
	  • Clock Recovery
	  • Additional Requirement for Mach-NX
	• Added the new subsections:
	  • Design Components
	  • Clocking Scheme
	  • Reset Scheme
	• Reworked subsection contents of LL GPIO Latency and renamed to GPIO Latency.

Signal Description	• Removed the Reference Design Macros section and replaced it with the *Signal Description* section. • Added top-level ports for SCM and HPM.
Timing Constraints	• Removed the *Diamond Design* and *Radiant Design* subsections. • Added Clock Definitions subsection.

Modifying the Reference Design	• Removed Generating the IP section and replaced it with *Modifying the Reference Design* section.
	• Added the following subsections:
	  • Lattice Propel
	  • Lattice Diamond
	  • Lattice Radiant

Simulating the Reference Design	• Removed HDL Simulation and Verification section and replaced it with *Simulating the Reference Design* section.
	• Added the following subsections:
	  • Setting Up the Simulation
	  • Simulation Details and Results
	• Added new simulation screenshots.

Hardware Implementation	Removed the Hardware Setup section and Hardware Validation section and replaced it with the *Hardware Implementation* section.
Resource Utilization	Updated the resource utilization numbers to match utilization for LTPI IP version 1.6.0.
Common Issues and Troubleshooting	Added I2C Bus Hang subsection.
Packaged Design	Removed this section.

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Revision 1.3, August 2024

Section	Change Summary
All	Added *User Guide* to the document title.
Disclaimers	Updated boilerplate.
Inclusive Language	Added boilerplate.
Abbreviations in This Document	• Replaced the word *acronyms* with *abbreviations*. • Added *Management Component Transport Protocol* (*MCTP*) to the list of abbreviations.

Introduction	• Updated the following items in the Features section:
	  • Added an introductory sentence.
	  • Updated the *LTPI version*.
	  • Removed the sentence: *for I2C interface, each can be configured as Controller, Target or Controller/Target (for multi-controller/main)*.
	  • Added the descriptions for *I^2C interface Single-node* and *Multi node* features.
	• Updated the versions of the *Lattice Diamond*, *Lattice Radiant*, and *Lattice Propel* software in the Limitation section.

Generating the IP	Added section 6.3. Sample Reference Design Setup.
References	Added the following references: • Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057) • Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065) • Implementing High-Speed Interfaces with Mach-NX Usage Guide (FPGA-TN-02234) • MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286) • Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Revision 1.2, June 2023

Section	Change Summary
Acronyms in This Document	Added CDC and removed SCM.
Introduction	• Updated LTPI version and supported data rates in the Features section. • Added MachXO5-NX to supported devices and updated software versions in the Limitations section.
Functional Description	• Updated the Overview section to add the DC-SCM. • General update to the Reference Design Specification (previously Reference Design Variations) and the Target Speed Setting sections. • Removed the Clock Recovery Diagram figure from the Clock Recovery section. Marked statement as Note. • Updated information on the latency of LL GPIO in the LL GPIO Latency section. • Deleted statement regarding a separate demo from the Additional Requirement for Mach-NX section.

Pin Description	• Removed the statement Note that some pins may not appear on every variation of the reference design from introductory paragraph.
	• In Table 3.1. Pin Descriptions:
	  • Moved int_o to the System group.
	  • Updated tgt_spd_o description.
	  • Updated values and description of rx_feat_cap_o.

Reference Design Macros	General update to this section (previously *Parameters and Synthesis Directives*)
Timing Constraints	• Added timing constraints guidelines for MachXO5-NX. • Added the Diamond Design, Lattice Radiant Design, Clocks, Resets, and False Paths subsections.
Generating the IP	Updated steps and figures in the main section and in the Sample SCM IP Configuration (Default Reference Design) subsection.
HDL Simulation and Verification	• Provided detailed information regarding Figure 7.1. Initialization after Reset. • Updated figures.

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Section	Change Summary
Hardware Setup	General update to this section.
Hardware Validation	Updated hardware validation information for MachXO3D and Mach-NX. Added information on MachXO5-NX.
Packaged Design	Updated the design directory structure and added note.
Resource Utilization	Updated section to show only the resource utilization of the Diamond and the Lattice Radiant demos.
References	Added references to product web pages.
Technical support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.1, November 2022

Section	Change Summary

Introduction	• In the Limitations section:
	  • added Mach-NX to the Supported Device Families;
	  • updated the Supported Lattice Propel version to 2.2.

Functional Description	• General update to the Target Speed Setting section.
	• Added the Using a Single PLL section.
	• Added the Additional Requirement for Mach-NX section.
	• In the section Clock Recovery:
	  • added a description for Figure 2.4. Clock Recovery Diagram;
	  • added information about additional clock recovery function of the IP.

Pin Descriptions	• Added information of the Initialization Interface.
	• In Table 3.1. Pin Descriptions:
	  • updated the Description for the sync_clk_i Port;
	  • updated the note of the Initialization Interface.

Timing Constraints	Added the current timing constraints applied to the design.

Generating the IP	• Added information about the usage of RTL files in step 8 of the IP generation process.
	• Updated Figure 6.9. Sample RTL File Path.
	• Updated step 9 of the IP generation process.
	• Added Figure 6.11. Sample Key File Path.
	• Added the Setting-up Diamond Software section.
	• Added information about the Enable Clock Compensation option in the section Sample SCM IP Configuration (Design 1) section.
	• Added the following tables:
	  • Table 6.1. General Tab Attributes
	  • Table 6.2. General Tab Attributes Description
	  • Table 6.5. Capabilities Tab Attributes
	  • Table 6.6. Capabilities Tab Attributes Description
	  • Table 6.7. LL GPIO Tab Attributes
	  • Table 6.8. LL GPIO Tab Attributes Description
	  • Table 6.9. NL GPIO Tab Attributes
	  • Table 6.10. NL GPIO Tab Attributes Description
	  • Table 6.11. I2C Tab Attributes
	  • Table 6.12. I2C Tab Attributes Description
	  • Table 6.13. UART Tab Attributes
	  • Table 6.14. UART Tab Attributes Description
	  • Table 6.15. OEM Tab Attributes
	  • Table 6.16. OEM Tab Attributes Description
	• Added Figure 6.20. NL GPIO Tab and Figure 6.23. OEM Tab.

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Section	Change Summary
HDL Simulation and Verification	Added the Running the Simulation section.
Hardware Setup	• In Table 8.1. Diamond Demo Pin Assignments, updated the Pin Assignment information of the following Ports of the LVDS Interface: lvds_tx_clk_o, lvds_tx_data_o, lvds_rx_clk_i, and lvds_rx_data_i. Added the LVDS Setup Considerations section.
Hardware Validation	Added information about the hardware validation for Mach-NX device.
References	Updated this section.

Revision 1.0, August 2022

Section	Change Summary
All	Production release
Introduction	Updated the features to match the new IP implementation.
Functional Description	• Updated section content to match the new IP implementation, including Figure 2.1. Block Diagram and Figure 2.2. State Machine. • Updated Table 2.1. Design to change Clock Recovery value for Design 1 (SCM), Design 2 (SCM), and Design 3 SCM to No.
Pin Descriptions	Updated pin list to match the new reference design top module in Table 3.1. Pin Descriptions.
Parameters and Synthesis Directives	Changed section name from *Parameters* to *Parameters and Synthesis Directives*. Added Table 4.1. Design Parameters and Table 4.2. Synthesis Directives.
Timing Constraints	Added this section.
Generating the IP	Added this section.
HDL Simulation and Verification	Updated section content to match the new IP implementation, including Figure 7.1. Initialization after Reset and Figure 7.2. Interface Activities.
Hardware Setup	Added this section.
Hardware Validation	Updated section content to include validation for MachXO3D.
Common Issues and Troubleshooting	Added this section.
Packaged Design	Updated section content to match the new reference design package, including Figure 11.1. Packaged Design Directory Structure.
Resource Utilization	Updated section content to match the new IP implementation, including adding Table 12.1. Resource Utilization for Design 1 and Table 12.2. Resource Utilization for Added Channels.

Revision 0.80, February 2022

Section	Change Summary
All	First preliminary release

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