CrossLink-NX-33 Image Sensor Module Design Guide

Application Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
HPIO	High-Performance IO
WRIO	Wide-Range IO

1. Introduction

The CrossLink-NX-33 is a member of the CrossLink-NX family targeted for Embedded Vision and Computer Vision applications. In order to support image sensors in these applications this device form factor is specifically design to fit in a narrow form factor of the image sensor module. This application note provides guidance to designing the image sensor modules.

2. Package Form Factor and IO Bank Design

The 84 ball WLCSP package of CrossLink-NX-33 is designed for narrow form factor with 3.1mm X 7.3mm (0.5mm pitch) dimensions. The corresponding IO banks are assigned in such a way that the wide-range IO banks (WRIO banks 0, 1 and 5) are at the top of the die/package orientation and the high-performance IO banks (HPIO banks 2, 3 and 4) are at the bottom of the die/package orientation.

2.1. Package Ball Locations

Figure 2.1 shows the physical ball map of 84 WLCSP package. The top side IO banks 0, 1 and 5 supports wide-range IO for control signals. The WRIO supports IO standards ranging from 1.2V to 3.3V VCCIO. The bottom side IO banks 2, 3 and 4 supports high-performance IO for high speed MIPI interface. HPIO banks supports IO standards ranging from 1.0V up to 1.8V VCCIO. In addition, HPIO banks supports data rates up to 1.2Gbps.

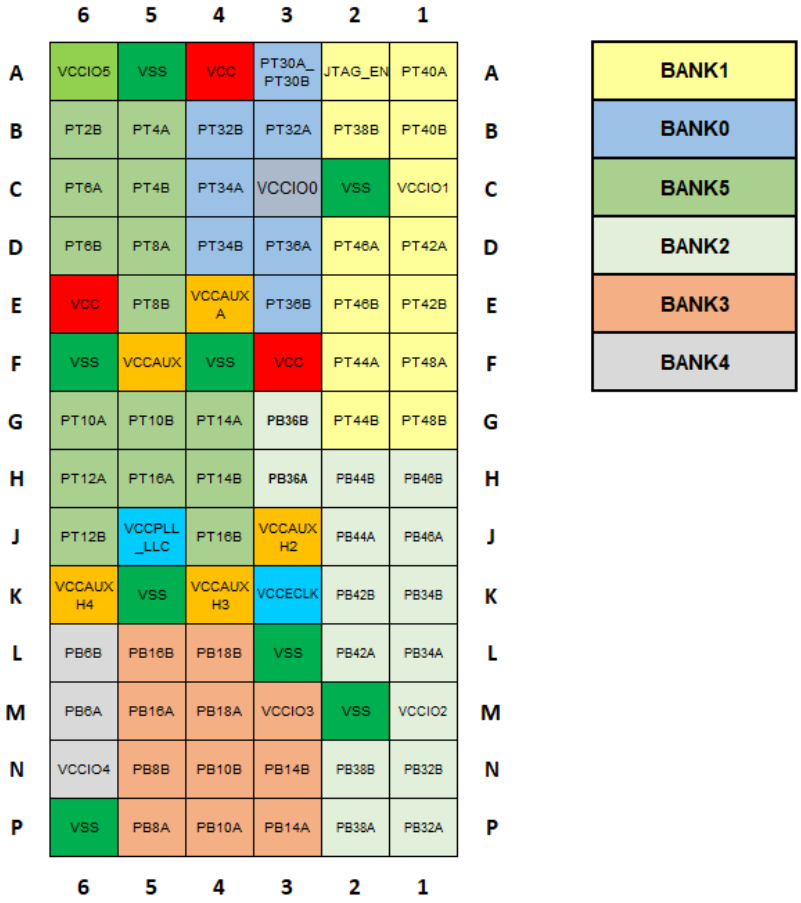

Figure 2.1. CrossLink-NX-33, 84 ball WLCSP ball map

2.2. Control Signal IO Pin Assignment

The WRIO banks 0, 1 and 5 are oriented at the top of the WLCSP. From the pin map table, these IO pins can be identified as PTxxx IO pad function. The table below shows the IO pad functions along with the dual purpose CFG and alternate functions. There are a total 32 usable IO pins across all the WRIO banks.

Table 2.1. 84 ball WLCSP top side pin table

FNC	TYPE	BANK	CFG/Alternate Function	WLCSP84
PT36A	FIO	0	MD2/SD6	D3
PT36B	FIO	0	MD3/SD7	E3
PT34A	FIO	0	MOSI/MD0/SD4	C4
PT34B	FIO	0	MISO/MD1/SD5	D4
PT32A	FIO	0	MCLK	B3
PT32B	FIO	0	MCSN	B4
VCCIO0	VCCIO	0	Unused	C3
PT30A_PT30B	PKGNET	0	Unused	A3
PT48A	FIO	1	DONE	F1
PT48B	FIO	1	Unused	G1
PT46A	FIO	1	TCK/SCLK/PCLKT1_3/S3_IN/PMU_EXT_CLK	D2
PT46B	FIO	1	PMU_WAKEUP/S3_OUT	E2
PT44A	FIO	1	SD3/SDA/USER_SDA/S2_IN	F2
PT44B	FIO	1	SD2/SCL/USER_SCL/S2_OUT	G2
PT42A	FIO	1	TDI/PCLKT1_1/OSC_HI/SSI/SD0/S1_IN	D1
PT42B	FIO	1	PCLKT1_2/TDO/OSC_BURST/SSO/SD1/S1_OUT	E1
PT40A	FIO	1	TMS/SCSN/PCLKT1_0/S0_IN	A1
PT40B	FIO	1	MCSNO/MSDO/S0_OUT	B1
JTAG_EN	I	1	Unused	A2
PT38B	FIO	1	INITN	B2
VCCIO1	VCCIO	1	Unused	C1
PT16A	FIO	5	SD14	H5
PT16B	FIO	5	SD15	J4
PT14A	FIO	5	SD12	G4
PT14B	FIO	5	SD13	H4
PT12A	FIO	5	SD10	H6
PT12B	FIO	5	SD11	J6
PT10A	FIO	5	SD8	G6
PT10B	FIO	5	SD9	G5
PT8A	FIO	5	Unused	D5
PT8B	FIO	5	Unused	E5
PT6A	FIO	5	Unused	C6
PT6B	FIO	5	Unused	D6
PT4A	FIO	5	Unused	B5
PT4B	FIO	5	Unused	C5
PT2B	FIO	5	Unused	B6
VCCIO5	VCCIO	5	Unused	A6

2.3. MIPI Sensor IO Pin Assignment

The HPIO banks 2, 3 and 4 are oriented at the bottom of the WLCSP. From the pin map table, these IO pins can be identified as PBxxx IO pad function. The table below shows the IO pad functions along with the dual purpose CFG and alternate functions. There are a total 26 usable IO pins across all the HPIO banks.

Table 2.2. 84 ball WLCSP bottom side pin table

FNC	TYPE	BANK	CFG/Alternate Function	WLCSP84
PB32A	FIO	2	VREF2_1	P1
PB32B	FIO	2	Unused	N1
PB34A	FIO	2	PCLKT2_0/S4_IN	L1
PB34B	FIO	2	PCLKC2_0/S4_OUT	K1
PB36A	FIO	2	Unused	H3
PB36B	FIO	2	Unused	G3
PB38A	FIO	2	PCLKT2_1/S5_IN	P2
PB38B	FIO	2	PCLKC2_1/S5_OUT	N2
PB42A	FIO	2	PCLKT2_2/S6_IN	L2
PB42B	FIO	2	PCLKC2_2/S6_OUT	K2
PB44A	FIO	2	Unused	J2
PB44B	FIO	2	Unused	H2
PB46A	FIO	2	PCLKT2_3/ATB_FORCE/S7_IN	J1
PB46B	FIO	2	PCLKC2_3/ATB_SENSE/VREF2_2/S7_OUT	H1
VCCIO2	VCCIO	2	Unused	M1
PB8A	FIO	3	VREF3_1	P5
PB8B	FIO	3	Unused	N5
PB10A	FIO	3	PCLKT3_0	P4
PB10B	FIO	3	PCLKC3_0	N4
PB14A	FIO	3	PCLKT3_1	P3
PB14B	FIO	3	PCLKC3_1	N3
PB16A	FIO	3	PCLKT3_2	M5
PB16B	FIO	3	PCLKC3_2	L5
PB18A	FIO	3	PCLKT3_3/S8_IN	M4
PB18B	FIO	3	PCLKC3_3/VREF3_2/S8_OUT	L4
VCCIO3	VCCIO	3	Unused	M3
PB6A	FIO	4	PCLKT4_1/LLC_GPLL0T_MFGOUT1	M6
PB6B	FIO	4	PCLKC4_1/LLC_GPLL0T_MFGOUT2/VREF4_2	L6
VCCIO4	VCCIO	4	Unused	N6

3. Image Sensor Module Physical Layout

With package and pinout information given in the previous section, a typical physical image sensor module design with PCB area estimate is shown in Figure 3.1. There are a few key physical considerations to fit the CrossLink-NX-33 on to a narrow bezel image sensor module.

- 84 WLSCP needs to be oriented in a similar narrow and long side orientation as the image sensor module.
- The top narrow part of the WLCSP package is facing the left side of the module where the control IO signals are routed.
- The bottom narrow part of the WLCSP package is facing the right side of the module that is physically closest to the RGB and IR image sensors in order to have the shortest trace routing from the NX-33 to the image sensors.
- Due to the space limitations of the narrow bezel, signal routing may require up to 6 PCB layers in addition to the power and GND layers.

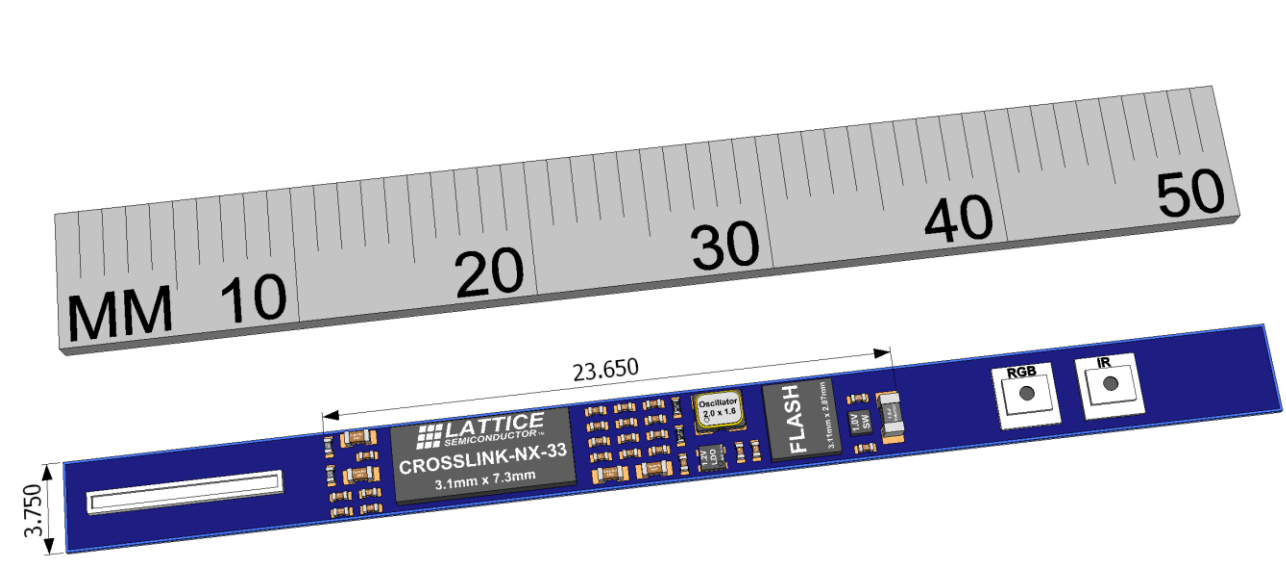

Figure 3.1. Mock-up image sensor module physical design

4. Summary

CrossLink-NX-33 is a new density point of the Lattice CrossLink-NX family. In addition to providing an intermediate density point between NX-17 and NX-40, NX-33 is designed with image sensor applications in mind. The form factor of the NX-33 84 WLCSP makes it an ideal device for state of the art image sensor module designs.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, March 2022.

Section	Change Summary
All	Initial release.

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