



# **AXI4 to APB Bridge Module**

IP Version: 1.4.0

## **User Guide**

FPGA-IPUG-02198-1.5

June 2025

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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## Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition                                 |
|---------|--------------------------------------------|
| AMBA    | Advanced Micro-controller Bus Architecture |
| AXI     | Advanced Extensible Interface Bus          |
| APB     | Advanced Peripheral Bus                    |
| FPGA    | Field Programmable Gate Array              |
| RTL     | Register Transfer Level                    |

# 1. Introduction

The Lattice Semiconductor AXI4 to APB Bridge Module provides an interface between the high-speed AXI4 and APB. The design is implemented in Verilog HDL. The IP can be configured based on [Table 1.1](#).

**Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation**

| Supported Devices | IP Configuration and Generation  | IP Implementation (Synthesis, Map, Place and Route) |
|-------------------|----------------------------------|-----------------------------------------------------|
| LatticeECP3™      | Lattice Propel™ Builder software | Lattice Diamond™ software                           |
| ECP5™             | Lattice Propel Builder software  | Lattice Diamond software                            |
| CrossLink™-NX     | Lattice Propel Builder software  | Lattice Radiant™ software                           |
| Certus™-NX        | Lattice Propel Builder software  | Lattice Radiant software                            |
| Certus-N2         | Lattice Propel Builder software  | Lattice Radiant software                            |
| MachXO5™-NX       | Lattice Propel Builder software  | Lattice Radiant software                            |
| CertusPro™-NX     | Lattice Propel Builder software  | Lattice Radiant software                            |
| Lattice Avant™    | Lattice Propel Builder software  | Lattice Radiant software                            |

## 1.1. Features

The key features of the AXI4 to APB Bridge Module include:

- Compliance with AMBA AXI4 and APB3 Protocol
- Support configurable data bus width: 8,16, and 32
- Support configurable AXI4 ID width: 1 to 11
- Support configurable AXI4 User width: 1 to 128
- Support of AXI4 INCR burst
- Support 32-bit Address width
- Number of supported APB completer is one
- Registered output

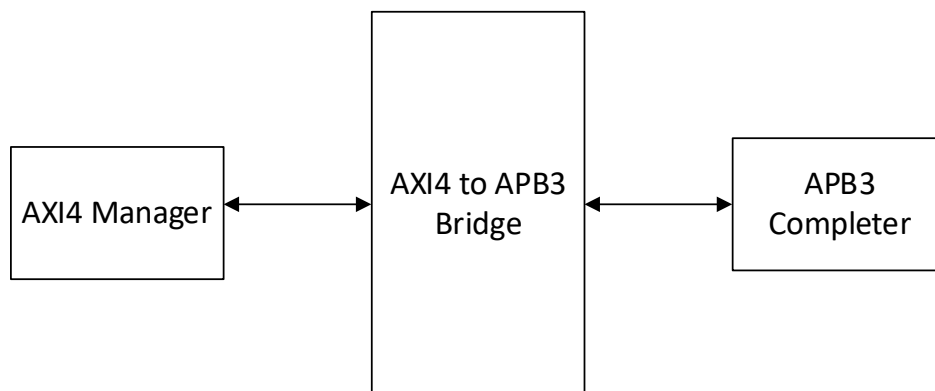
## 1.2. Assumptions

- AxQOS, AxREGION, AxCACHE, AxLOCK, and AxPROT are considered as don't care.
- AxUSER is passed back as such in the write and read response channels.
- AXI4 wrap and fixed burst not supported.
- AXI4 unaligned address is passed as such to the external APB completer during write and read. Based on the implementation of unaligned address in the external APB completer, the data read back from APB completer is passed as such to the AXI4 external manager.

## 2. Functional Descriptions

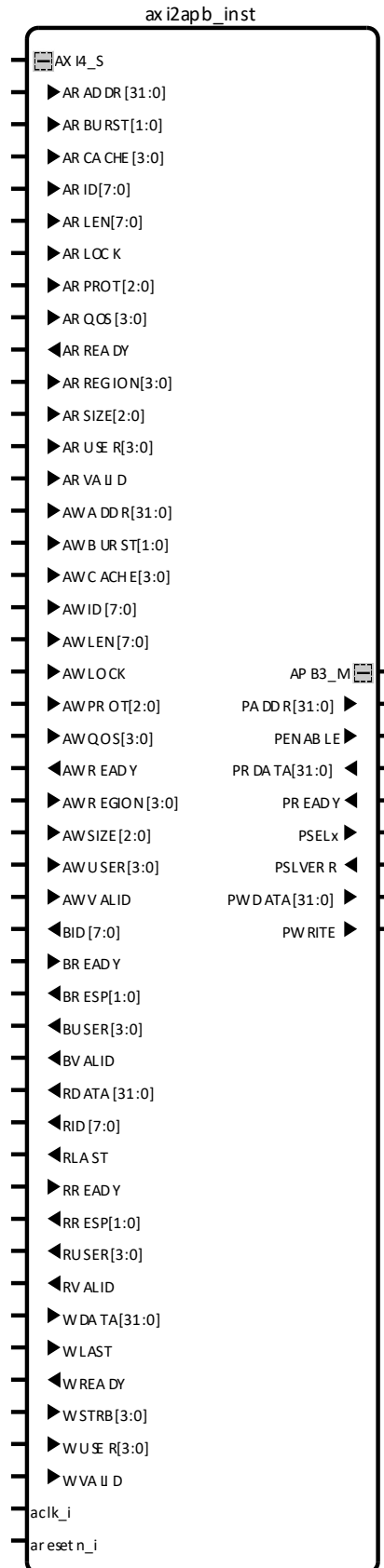
### 2.1. Overview

The Lattice Semiconductor AXI4 to APB Bridge core is used to connect AXI4 manager to APB completer. Read and write transfers on the AXI4 bus are converted into corresponding transfers on the APB.



**Figure 2.1. AXI4 to APB Bridge**

Figure 2.2 shows the interface diagram of the AXI4 to APB Bridge Module. The diagram shows all the available ports for the IP core.



**Figure 2.2. AXI4 to APB Bridge Module Interface Diagram**

**Table 2.1. AXI4 to APB Bridge Module Signal Description**

| Pin Name                          | Direction | Width (Bits)         | Description                                                                                                                                   |
|-----------------------------------|-----------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Clock and Reset</b>            |           |                      |                                                                                                                                               |
| aclk_i                            | In        | 1                    | AXI4 to APB bridge clock.                                                                                                                     |
| aresetn_i                         | In        | 1                    | Active low reset.                                                                                                                             |
| <b>AXI4 Subordinate Interface</b> |           |                      |                                                                                                                                               |
| axi_slv_awvalid_i                 | In        | 1                    | Write address valid. This signal indicates that the channel is signaling valid write address and control information.                         |
| axi_slv_awaddr_i                  | In        | 32                   | Write address. The write address gives the address of the first transfer in a write burst transaction.                                        |
| axi_slv_awsize_i                  | In        | 3                    | Burst size. This signal indicates the size of each transfer in the burst.                                                                     |
| axi_slv_awburst_i                 | In        | 2                    | Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated.              |
| axi_slv_awlen_i                   | In        | 8                    | Burst length. This indicates the number of beats per AXI4 burst.                                                                              |
| axi_slv_awid_i                    | In        | AXI_ID_WIDTH         | AXI4 write ID width.                                                                                                                          |
| axi_slv_awlock_i                  | In        | 1                    | Lock type.<br>AXI4: Optional                                                                                                                  |
| axi_slv_awcache_i                 | In        | 4                    | Memory type.<br>AXI4: Optional                                                                                                                |
| axi_slv_awprot_i                  | In        | 3                    | Protection type.<br>AXI4: Optional                                                                                                            |
| axi_slv_awqos_i                   | In        | 4                    | Quality of Service.<br>AXI4: Optional                                                                                                         |
| axi_slv_awregion_i                | In        | 4                    | Region<br>AXI4: Optional                                                                                                                      |
| axi_slv_awuser_i                  | In        | AXI_USER_WIDTH       | User signals.<br>AXI4: Optional                                                                                                               |
| axi_slv_awready_o                 | Out       | 1                    | Write address ready. This signal indicates that the subordinate is ready to accept an address and associated control signals.                 |
| axi_slv_wvalid_i                  | In        | 1                    | Write valid. This signal indicates the valid write data and strobes are available.                                                            |
| axi_slv_wdata_i                   | In        | AXI_APB_DATA_WIDTH   | Write data.                                                                                                                                   |
| axi_slv_wlast_i                   | In        | 1                    | Write last. This signal indicates the last transfer in a write burst.                                                                         |
| axi_slv_wstrb_i                   | In        | AXI_APB_DATA_WIDTH/8 | Write strobes. This signal indicates the byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus. |
| axi_slv_wuser_i                   | In        | AXI_USER_WIDTH       | AXI4 write user width.                                                                                                                        |
| axi_slv_wready_o                  | Out       | 1                    | Write data ready. This signal indicates that the subordinate is ready to accept write data.                                                   |
| axi_slv_bvalid_o                  | Out       | 1                    | Write response valid. This signal indicates that the channel is signaling a valid write response.                                             |
| axi_slv_bid_o                     | Out       | AXI_ID_WIDTH         | Write response ID.                                                                                                                            |
| axi_slv_buser_o                   | Out       | AXI_USER_WIDTH       | Write response User signal.                                                                                                                   |
| axi_slv_bresp_o                   | Out       | 2                    | Write response. This signal indicates the status of the write transaction.                                                                    |

| Pin Name                       | Direction | Width (Bits)       | Description                                                                                                                     |
|--------------------------------|-----------|--------------------|---------------------------------------------------------------------------------------------------------------------------------|
| axi_slv_bready_i               | In        | 1                  | Response ready. This signal indicates that the manager can accept a write response.                                             |
| axi_slv_arvalid_i              | In        | 1                  | Read address valid. This signal indicates that the channel is signaling valid read address and control information.             |
| axi_slv_araddr_i               | In        | 32                 | Read address. The read address gives the address of the first transfer in a read burst transaction.                             |
| axi_slv_arsize_i               | In        | 3                  | Burst size. This signal indicates the size of each transfer in the burst.                                                       |
| axi_slv_arburst_i              | In        | 2                  | Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated. |
| axi_slv_arlen_i                | In        | 8                  | AXI4 read burst length. This indicates the number of beats per AXI4 burst.                                                      |
| axi_slv_arid_i                 | In        | AXI_ID_WIDTH       | AXI4 read address ID width.                                                                                                     |
| axi_slv_arlock_i               | In        | 1                  | Lock type.<br>AXI4: Optional                                                                                                    |
| axi_slv_arcache_i              | In        | 4                  | Memory type.<br>AXI4: Optional                                                                                                  |
| axi_slv_arprot_i               | In        | 3                  | Protection type<br>AXI4: Optional                                                                                               |
| axi_slv_arqos_i                | In        | 4                  | Quality of Service.<br>AXI4: Optional                                                                                           |
| axi_slv_arregion_i             | In        | 4                  | Region<br>AXI4: Optional                                                                                                        |
| axi_slv_aruser_i               | In        | AXI_USER_WIDTH     | User signals.<br>AXI4: Optional                                                                                                 |
| axi_slv_arready_o              | Out       | 1                  | Read address ready. This signal indicates that the subordinate is ready to accept an address and associated control signals.    |
| axi_slv_rvalid_o               | Out       | 1                  | Read valid. This signal indicates that the channel is signaling the required read data.                                         |
| axi_slv_rdata_o                | Out       | AXI_APB_DATA_WIDTH | Read data.                                                                                                                      |
| axi_slv_rresp_o                | Out       | 2                  | Read response. This signal indicates the status of the read transfer.                                                           |
| axi_slv_ruser_o                | Out       | AXI_USER_WIDTH     | User signals.<br>AXI4: Optional                                                                                                 |
| axi_slv_rid_o                  | Out       | AXI_ID_WIDTH       | AXI4 read data ID width.                                                                                                        |
| axi_slv_rlast_o                | Out       | 1                  | Read last. This signal indicates the last transfer in a read burst.                                                             |
| axi_slv_rready_i               | In        | 1                  | Read ready. This signal indicates that the manager can accept the read data and response information.                           |
| <b>APB Requester Interface</b> |           |                    |                                                                                                                                 |
| apb_mas_sel_o                  | Out       | 1                  | APB Select. It indicates completer device is selected and that data transfer is required.                                       |
| apb_mas_en_o                   | Out       | 1                  | APB Enable.                                                                                                                     |
| apb_mas_addr_o                 | Out       | 32                 | Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.             |

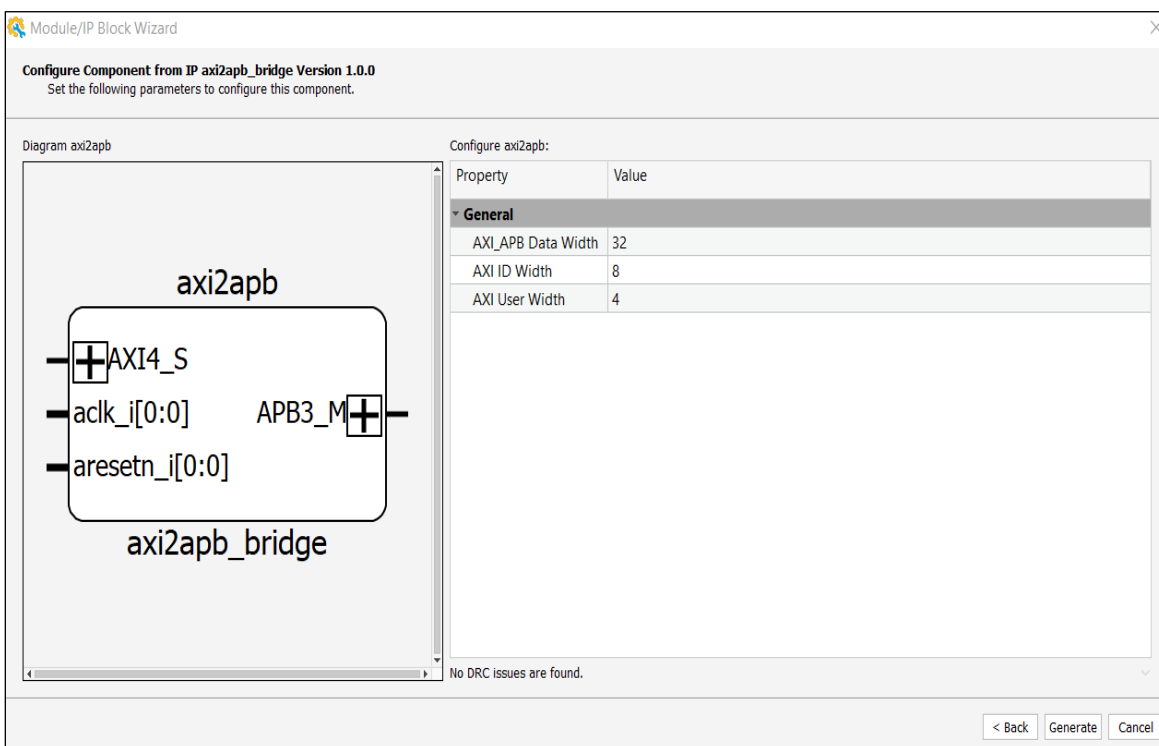
| Pin Name         | Direction | Width (Bits)       | Description                                                                                               |
|------------------|-----------|--------------------|-----------------------------------------------------------------------------------------------------------|
| apb_mas_write_o  | Out       | 1                  | APB transfer direction. This signal indicates an APB write access when High and APB read access when Low. |
| apb_mas_wdata_o  | Out       | AXI_APB_DATA_WIDTH | APB write data.<br>This bus is driven during write operation.                                             |
| apb_mas_ready_i  | In        | 1                  | APB Ready. Completer uses this signal to extend the APB transfer.                                         |
| apb_mas_rdata_i  | In        | AXI_APB_DATA_WIDTH | APB read data.<br>The selected completer drives this bus during read cycles when Write is LOW.            |
| apb_mas_slverr_i | In        | 1                  | APB completer error response.<br>This signal indicates transfer failure.                                  |

## 2.2. Attributes

Table 2.2 provides the list of user-configurable attributes for the AXI4 to APB Bridge Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.3.

**Table 2.2. Attribute Table**

| Attribute Name              | Attribute ID       | Selectable Values | Default | Dependency on Other Attributes |
|-----------------------------|--------------------|-------------------|---------|--------------------------------|
| <b>General Settings Tab</b> |                    |                   |         |                                |
| AXI_APB Data width          | AXI_APB_DATA_WIDTH | 8,16,32           | 32      | —                              |
| AXI User width              | AXI_USER_WIDTH     | 1-128             | 4       | —                              |
| AXI ID width                | AXI_ID_WIDTH       | 1-11              | 8       | —                              |



**Figure 2.3. AXI4 to APB Bridge Module Configuration User Interface**

**Table 2.3. Attribute Name**

| Attribute Name              | Description                                                                          |
|-----------------------------|--------------------------------------------------------------------------------------|
| <b>General Settings Tab</b> |                                                                                      |
| AXI_APB Data Width          | This describes the data bus width of both AXI4 and APB bus.                          |
| AXI User Width              | This decides the width of AXI4 user signals AWUSER, WUSER, BUSER, ARUSER, and RUSER. |
| AXI ID Width                | This decides the width of AXI4 AWID, ARID, BID, and RID signals.                     |

## Appendix A. Resource Utilization

The following tables show the resource utilization of the AXI4 to APB Bridge Module for different Lattice FPGA devices using Lattice Radiant Software 2022.1 with Synplify Pro (S-2021.09LR-SP2, Build 164R, Oct. 18, 2022) as the Synthesis Tool. The different Data Widths are used while the other attributes are the default configuration.

**Table A.1. Resource Utilization Using LAV-AT-E70-3LFG1156I**

| Configuration                                                   | Clock Fmax (MHz) | Registers | LUTs | EBRs |
|-----------------------------------------------------------------|------------------|-----------|------|------|
| AXI_APB Data Width = 32<br>AXI ID Width = 8, AXI User Width = 4 | 350.00           | 213       | 287  | 0    |
| AXI_APB Data Width = 16<br>AXI ID Width = 8, AXI User Width = 4 | 350.00           | 165       | 277  | 0    |
| AXI_APB Data Width = 8<br>AXI ID Width = 8, AXI User Width = 4  | 350.00           | 142       | 277  | 0    |

**Table A.2. Resource Utilization Using LAV-AT-E70-1LFG1156I**

| Configuration                                                   | Clock Fmax (MHz) | Registers | LUTs | EBRs |
|-----------------------------------------------------------------|------------------|-----------|------|------|
| AXI_APB Data Width = 32<br>AXI ID Width = 8, AXI User Width = 4 | 350.00           | 213       | 563  | 0    |
| AXI_APB Data Width = 16<br>AXI ID Width = 8, AXI User Width = 4 | 350.00           | 165       | 489  | 0    |
| AXI_APB Data Width = 8<br>AXI ID Width = 8, AXI User Width = 4  | 350.00           | 142       | 457  | 0    |

**Table A.3. Resource Utilization Using LFCPNX-100-9LFG672I**

| Configuration                                                   | Clock Fmax (MHz) | Registers | LUTs | EBRs |
|-----------------------------------------------------------------|------------------|-----------|------|------|
| AXI_APB Data Width = 32<br>AXI ID Width = 8, AXI User Width = 4 | 200.000          | 213       | 573  | 0    |
| AXI_APB Data Width = 16<br>AXI ID Width = 8, AXI User Width = 4 | 200.000          | 165       | 494  | 0    |
| AXI_APB Data Width = 8<br>AXI ID Width = 8, AXI User Width = 4  | 200.000          | 141       | 459  | 0    |

**Table A.4. Resource Utilization Using LFCPNX-100-7LFG672I**

| Configuration                                                   | Clock Fmax (MHz) | Registers | LUTs | EBRs |
|-----------------------------------------------------------------|------------------|-----------|------|------|
| AXI_APB Data Width = 32<br>AXI ID Width = 8, AXI User Width = 4 | 169.837          | 213       | 579  | 0    |
| AXI_APB Data Width = 16<br>AXI ID Width = 8, AXI User Width = 4 | 157.679          | 165       | 494  | 0    |
| AXI_APB Data Width = 8<br>AXI ID Width = 8, AXI User Width = 4  | 164.745          | 141       | 459  | 0    |

## References

- [AXI4 to APB Bridge Module Release Notes \(FPGA-RN-02047\)](#)
- [Lattice Propel 2022.1 Builder User Guide \(FPGA-UG-02177\)](#)
- [Lattice Radiant Timing Constraints Methodology \(FPGA-AN-02059\)](#)
- [AMBA AXI Protocol Specification](#) web page for IHI0022H\_c\_amba\_axi\_protocol\_spec
- [AMBA 3 APB Protocol Specification](#) web page
- [LatticeECP3](#) web page
- [ECP5](#) web page
- [CrossLink-NX](#) web page
- [CertusPro-NX](#) web page
- [Certus-NX](#) web page
- [Certus-N2](#) web page
- [MachXO5-NX](#) web page
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Diamond Software](#) web page
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## Revision History

### Revision 1.5, IP v1.4.0, June 2025

| Section      | Change Summary                                                                                                                                     |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Introduction | Renamed <i>Supported FPGA Family</i> to <i>Supported Devices</i> in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. |
| References   | Updated references.                                                                                                                                |

### Revision 1.4, IP v1.3.0, December 2024

| Section      | Change Summary                                                                                                                   |
|--------------|----------------------------------------------------------------------------------------------------------------------------------|
| Introduction | Added Certus-N2, LatticeECP3, and ECP5 devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. |
| References   | Updated references.                                                                                                              |

### Revision 1.3, June 2024

| Section                          | Change Summary                                                                                                                                                                                                                                                                                  |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| All                              | <ul style="list-style-type: none"> <li>This release is for version 1.2.0 of the AXI4 to APB Bridge Module.</li> <li>Renamed document from <i>AXI4 to APB Bridge Module – Lattice Propel Builder</i> to <i>AXI4 to APB Bridge Module</i>.</li> <li>Changed <i>AXI</i> to <i>AXI4</i>.</li> </ul> |
| Inclusive Language               | Added the inclusive language boilerplate.                                                                                                                                                                                                                                                       |
| Introduction                     | Added CrossLink-NX, Certus-NX, and MachXO5-NX devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.                                                                                                                                                         |
| Appendix A. Resource Utilization | Updated the device name for Avant devices from LAV-AT-500E to LAV-AT-E70.                                                                                                                                                                                                                       |
| References                       | Updated references.                                                                                                                                                                                                                                                                             |

### Revision 1.2, June 2023

| Section                      | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Introduction                 | <ul style="list-style-type: none"> <li>In Features, changed <i>Number of supported APB slave is one</i> to <i>Number of supported APB completer is one</i>.</li> <li>In Assumptions: <ul style="list-style-type: none"> <li>changed <i>APB slave</i> to <i>APB completer</i>;</li> <li>changed <i>AXI4 external master</i> to <i>AXI4 external manager</i>.</li> </ul> </li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Functional Descriptions      | <ul style="list-style-type: none"> <li>In Overview: <ul style="list-style-type: none"> <li>changed <i>AXI4 master</i> to <i>AXI4 manager</i>;</li> <li>changed <i>APB slave</i> to <i>APB completer</i>.</li> </ul> </li> <li>Table 2.1. AXI4 to APB Bridge Module Signal Description: <ul style="list-style-type: none"> <li>changed <i>AXI4 Slave Interface</i> to <i>AXI4 Subordinate Interface</i>;</li> <li>for <i>axi_slv_awready_o</i>, <i>axi_slv_wready_o</i> and <i>axi_slv_arready_o</i>, changed <i>slave</i> to <i>subordinate</i> in the Description column;</li> <li>for <i>axi_slv_bready_i</i> and <i>axi_slv_rready_i</i>, changed <i>master</i> to <i>manager</i> in the Description column;</li> <li>changed <i>APB Master Interface</i> to <i>APB Requester Interface</i>;</li> <li>for <i>apb_mas_sel_o</i>, <i>apb_mas_ready_i</i>, <i>apb_mas_rdata_i</i> and <i>apb_mas_slvrr_i</i>, changed <i>slave</i> to <i>completer</i> in the Description column.</li> </ul> </li> </ul> |
| Technical Support Assistance | Added the link to Lattice Answer Database.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

#### Revision 1.1, November 2022

| Section              | Change Summary                                                                                                      |
|----------------------|---------------------------------------------------------------------------------------------------------------------|
| Introduction         | Updated Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation adding LAV-AT device support. |
| Resource Utilization | Newly added Appendix for CertusPro-NX (LFCPNX) and Avant (LAV-AT) devices.                                          |

#### Revision 1.0, May 2022

| Section | Change Summary   |
|---------|------------------|
| All     | Initial release. |



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