AXI4 Interconnect Module

IP Version: 2.2.0

User Guide

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advanced eXtensible Interface
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CDC	Clock Domain Crossing
CPU	Central Processing Unit
DMA	Direct Memory Access
FIFO	First In First Out
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LPDDR	Low Power Double Data Rate
MC	Memory Controller
RTL	Register Transfer Level

1. Introduction

This document provides technical information about the AXI4 Interconnect Module and aims to provide information essential for IP/system development, verification, integration, testing, and validation.

In general, this document covers design specification from RTL to IP packaging and details the procedures for IP generation and integration.

The design is implemented in System Verilog HDL. Table 1.1 shows the software used for IP configuration, generation, and implementation.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported Devices	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
CrossLink™-NX	Lattice Propel™ Builder software	Lattice Radiant™ software
MachXO5™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus-N2	Lattice Propel Builder software	Lattice Radiant software
CertusPro™-NX	Lattice Propel Builder software	Lattice Radiant software
Lattice Avant™	Lattice Propel Builder software	Lattice Radiant software
LatticeECP3™	Lattice Propel Builder software	Lattice Diamond™ software
ECP5™	Lattice Propel Builder software	Lattice Diamond software

1.1. Features

The key features of the AXI Interconnect Module include:

- Compliance with AMBA AXI4 and AXI4-Lite Protocol
- Fully parameterized design
- Connection of multiple AXI4 Managers to multiple memory-mapped AXI4 Subordinates
- Support up to 32 AXI4 or AXI4-Lite Managers and 32 AXI4 or AXI4-Lite Subordinates
- Heterogeneous support - AXI4 and AXI4-Lite in single interconnect
- Configurable data bus width for each interface
- AXI4: 8, 16, 32, 64, 128, 256, 512, or 1024 width
- AXI4-Lite: 32 or 64 bits
- Address width up to 64-bits [13 to 64]
- Support AXI4 INCR and FIXED bursts.
- Automatic conversion between interfaces with different data widths
- Support multiple clock domains
- Automatic conversion for the transactions between interfaces with different clocks
- Clock domain crossing can be enabled/disabled for each interface
- Support fragmented address space of up to 16 fragments per external Subordinate
- Full connection between Managers and Subordinates
- External Subordinate side arbitration
- Selectable arbitration scheme:
  - Round Robin
  - Strict Priority (Fixed Priority)

1.2. Limitations

- No wrap burst support
- During AXI4 external Manager request:
  - AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK are ignored while passing to external AXI4-Lite Subordinate interface;
  - AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK and AxPROT are passed through as such while passing to external AXI4 Subordinate interface.

2. Functional Description

2.1. Overview

The Lattice™ Semiconductor AXI4 Interconnect is a flexible, versatile, and easy-to-use IP with high-performance and low latency interconnect fabric for AMBA 4 AXI/AXI-lite based systems. Any AXI4/AXI4-Lite compliant IP can be easily plug-and-play into the system for smooth integration. It supports different data width conversion and clock-domain-crossing. Furthermore, it supports multiple Managers with multiple memory-mapped Subordinates.

It supports three types of responses: AXI OKAY; DECERR, when undefined external Subordinate address region is accessed; and SLVERR, for pass through from the external Subordinate.

AXI Interconnect implements the features required for high-performance and low latency systems including:

- Multiple channels
- Single-clock edge operation
- Non-tristate implementation
- Burst transfers in AXI4 interface: INCR burst (1 to 256 beats/burst), Fixed burst (1 to 16 transfers) following the protocol
- Wide data bus configurations: 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide for AXI4 interface
- 32 or 64 for AXI4-Lite interface

Refer to the AMBA AXI Protocol Specification web page for IHI0022H_c_amba_axi_protocol_spec for more information about the protocol.

AXI Interconnect can be cascaded to implement multi-layer hierarchical interconnect to support multiple Managers and Subordinates. Each Manager is considered to be on its own layer and isolated from each other, but can share access to the Subordinates. Each Manager can access different Subordinates in parallel. When more than one Manager tries to access the same Subordinate, external arbitration is performed by the multi-layer interconnect.

Each port can be configured to support either AXI4 or AXI4-Lite.

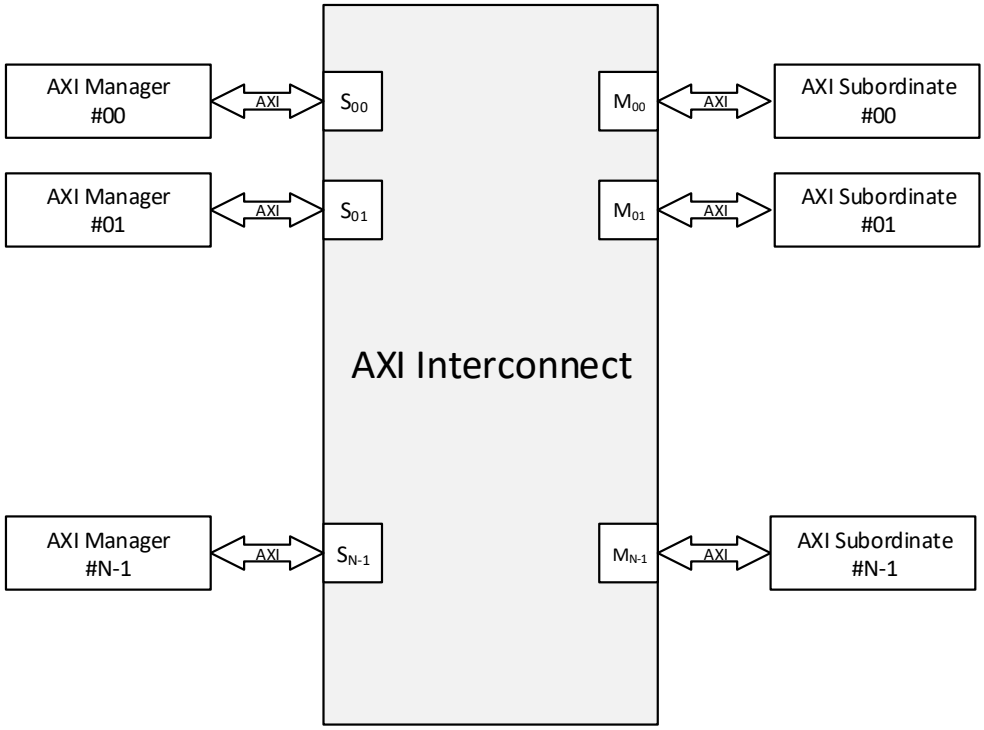

Figure 2.1. AXI4 Interconnect Module

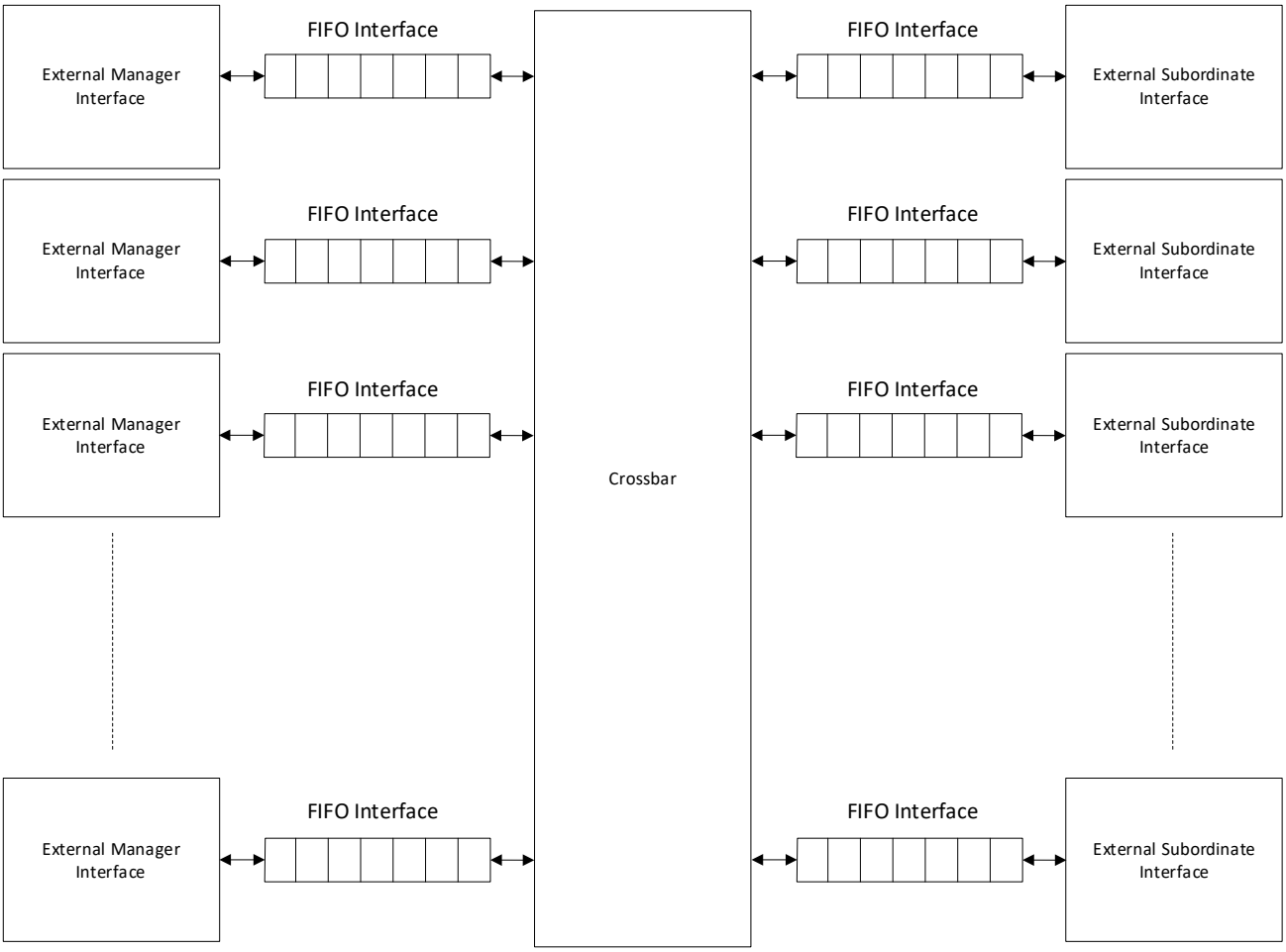

Figure 2.2. Internal Structure of the AXI4 Interconnect Module

2.1.1. External Manager Interface

This block interfaces with the external manager. When the AXI4 Interconnect is configured such that the external manager requires a data width up converter, the up converter block is instantiated. This module runs using the same clock or reset domain as the external manager the module is connected to. Clock or reset connected to this module is labelled as axi_S##_aclk/aresetn_i.

2.1.2. FIFO Interface

This block is part of a standard FIFO module. If the External Manager Interface or External Subordinate Interface has CDC disabled, this block is a Single Clock FIFO; if CDC is enabled, this block is a Dual Clock FIFO. Dual Clock FIFO is instantiated when CDC is enabled to handle clock domain crossing between the External Manager Interface or External Subordinate Interface and the Crossbar.

2.1.3. Crossbar

This block is where the arbitration modules are implemented. There is one arbiter per AXI4 channel, instantiated for each external manager and subordinate. The Crossbar runs off a separate clock or reset domain if CDC is enabled. Clock or reset connected to this module is labelled as axi_aclk/aresetn_i.

2.1.4. External Subordinate Interface

This block interfaces with the external subordinate. When the AXI Interconnect is configured such that the external subordinate requires a data width down converter, the down converter block is instantiated. This module runs using the

same clock or reset domain as the external subordinate. Clock or reset connected to this module is labelled as axi_M##_aclk/aresetn_i.

2.1.5. Width Conversion

2.1.5.1. Up Converter

When performing data width conversion from a narrower external manager data bus width to a wider external subordinate data bus width, the up converter merges the incoming beats to form the outgoing beats for a write transaction. For a read transaction, the incoming beats are split into smaller outgoing beats. The following example illustrates this concept.

Up conversion from a 32-bit data bus to 64-bit data bus.

- Number of beats = 4
- Size = 4 bytes

31 24	23 16	15 8	7 0	
0x03	0x02	0x01	0x00	1st transfer
0x07	0x06	0x05	0x04	2nd transfer
0x0B	0x0A	0x09	0x08	3rd transfer
0x0F	0x0E	0x0D	0x0C	4th transfer

Figure 2.3. Incoming Transaction (Write)/Outgoing Transaction (Read)

63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0	
0x07	0x06	0x05	0x04	0x03	0x02	0x01	0x00	1st transfer
0x0F	0x0E	0x0D	0x0C	0x0B	0x0A	0x09	0x08	2nd transfer

Figure 2.4. Outgoing Transaction (Write)/Incoming Transaction (Read)

2.1.5.2. Down Converter

When performing data width conversion from a wider external manager data bus width to a narrower external subordinate data bus width, the down converter splits the incoming beats into smaller outgoing beats for a write transaction. For a read transaction, the incoming beats are merged to form the outgoing beats.

Down conversion scenarios are as follows:

- Burst INCR: For AxLEN that exceeds 256 after down conversion, the transaction is split.
- Burst FIXED: Transactions are split into AxLEN+1 number of INCR transactions.
- AXI4-Lite to AXI4-Lite: Each incoming beat is converted into X number of transactions, where X denotes the downsize ratio.
- AXI4 to AXI4-Lite: A transaction of AxLEN is converted into X × Y number of transactions, where X is the downsize ratio and Y is AxLEN+1.

The following examples illustrate down conversion for burst INCR with split transactions and burst FIXED.

Burst INCR

Down conversion from a 64-bit data bus to 32-bit data bus.

- Number of beats = 130
- Size = 8 bytes

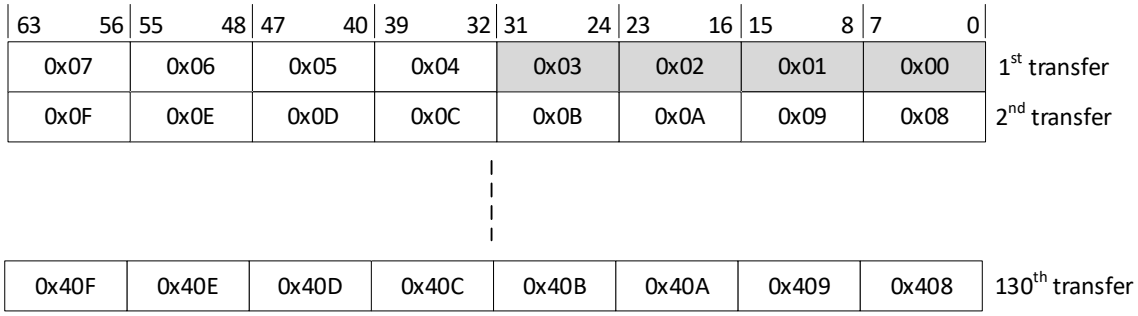

Figure 2.5. Incoming Beats (Write)/Outgoing Beats (Read)

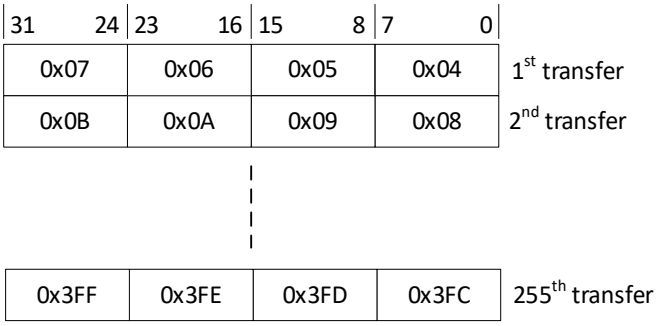

Figure 2.6. Outgoing Beats (Write)/Incoming Beats (Read) — First Transaction

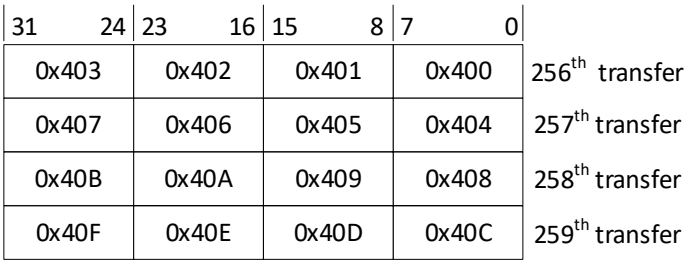

Figure 2.7.Outgoing Beats (Write)/Incoming Beats (Read) – Second Transaction

Burst FIXED

Down conversion from a 64-bit data bus to 32-bit data bus.

- Number of beats = 2
- Size = 8 bytes

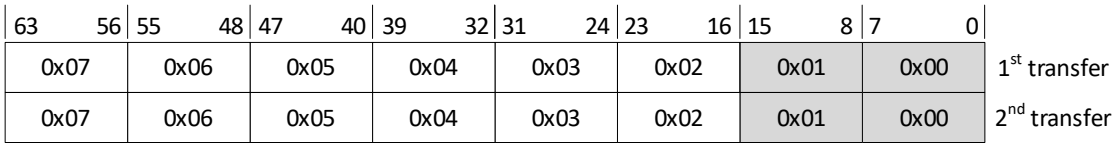

Figure 2.8. Incoming Beats (Write)/Outgoing Beats (Read)

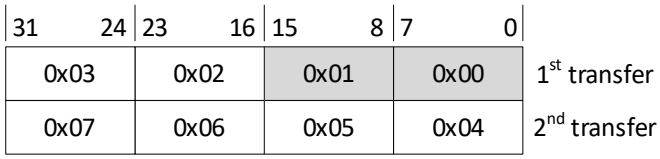

Figure 2.9. Outgoing Beats (Write)/ Incoming Beats (Read) – First Transaction

31 24	23 16	15 8	7 0	
0x03	0x02	0x01	0x00	1st transfer
0x07	0x06	0x05	0x04	2nd transfer

Figure 2.10. Outgoing Beats (Write)/ Incoming Beats (Read) – Second Transaction

2.1.6. Protocol Conversion

This module supports protocol conversion from AXI4 to AXI4-Lite and AXI4-Lite to AXI4.

2.2. Signal Description

Figure 2.11 shows the interface diagram for the AXI Interconnect Module. The diagram shows all of the available ports for the IP core, except clock domain crossing clock and reset ports.

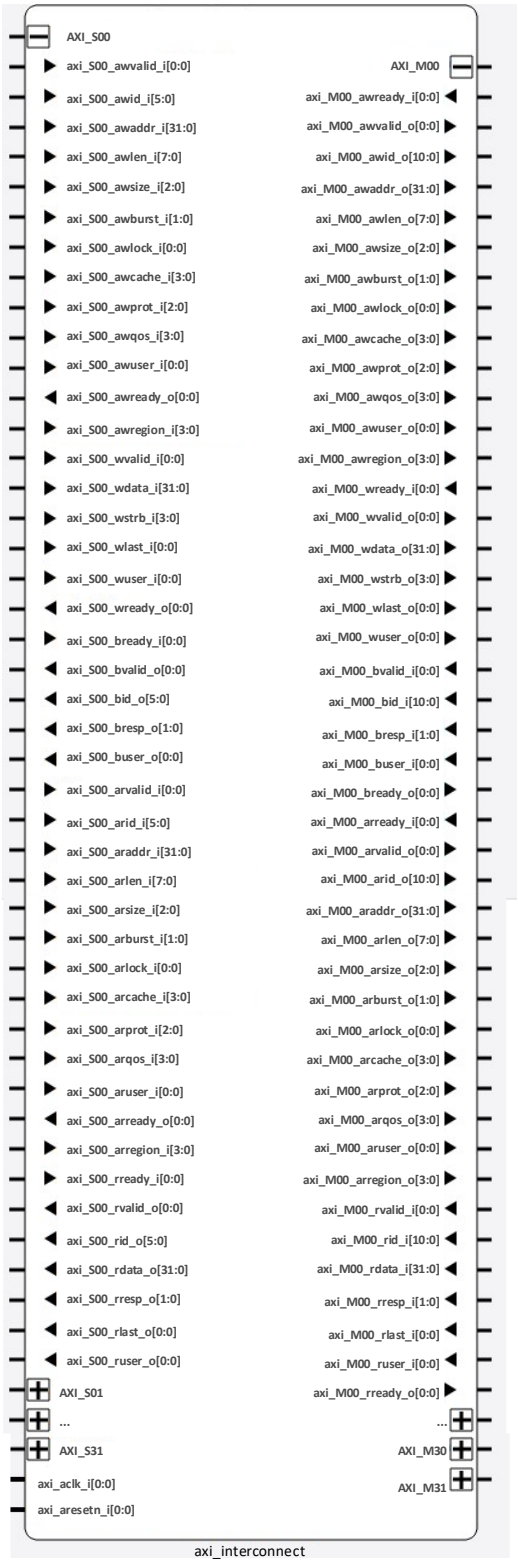

Figure 2.11. AXI4 Interconnect Module Interface Diagram

Table 2.1. AXI Interconnect Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
axi_aclk_i	In	1	AXI clock to AXI Interconnect
axi_aresetn_i	In	1	AXI active LOW reset
AXI Interconnect Subordinate 00 Clock and Reset (Available if CDC is Enabled for this Port S00)			
axi_S00_aclk_i(AL)	In	1	Input clock to AXI interconnected Subordinate 00 port. It is required only when CDC is enabled for external Manager 00 port.
axi_S00_aresetn_i(AL)	In	1	Input AXI active Low reset to AXI interconnected Subordinate 00 port. It is required only when CDC is enabled for external Manager 00 port.
AXI Interconnect Subordinate xx Clock and Reset (Available if CDC is Enabled for this Port Sxx)			
axi_Sxx_aclk_i(AL)	In	1	Input clock to AXI interconnected Subordinate xx port. It is required only when CDC is enabled for external Manager xx port.
axi_Sxx_aresetn_i(AL)	In	1	Input AXI active Low reset to AXI interconnected Subordinate xx port. It is required only when CDC is enabled for external Manager xx port.
AXI Interconnect Subordinate 00 Interface - Connected to External Manager 00			
axi_S00_awvalid_i(AL)	In	1	Write address valid
axi_S00_awid_i	In	EXT_MAS_AXI_ID_WIDTH	Write address ID AXI4: optional AXI4-Lite: N/A
axi_S00_awaddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Write address
axi_S00_awlen_i	In	8	Burst length, the exact number of transfers in a burst. AXI4: optional AXI4-Lite: N/A
axi_S00_awsize_i	In	3	Burst size, the size of each transfer in the burst. AXI4: optional AXI4-Lite: N/A
axi_S00_awburst_i	In	2	Burst type AXI4: optional AXI4-Lite: N/A
axi_S00_awlock_i	In	1	Lock type AXI4: optional AXI4-Lite: N/A
axi_S00_awcache_i	In	4	Memory type AXI4: optional AXI4-Lite: N/A
axi_S00_awprot_i(AL)	In	3	Protection type
axi_S00_awqos_i	In	4	Quality of service AXI4: optional AXI4-Lite: N/A
axi_S00_awregion_i	In	4	Region AXI4: required AXI4-Lite: N/A
axi_S00_awuser_i	In	AXI_USER_WIDTH	User signals AXI4: optional AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_S00_awready_o(AL)	Out	1	Write address ready
axi_S00_wvalid_i(AL)	In	1	Write valid
axi_S00_wdata_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH	Write data
axi_S00_wstrb_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH/8	Write strobes
axi_S00_wlast_i	In	1	AXI4 Last write beat/burst AXI4: optional AXI4-Lite: N/A
axi_S00_wuser_i	In	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_S00_wready_o(AL)	Out	1	Write ready
axi_S00_bvalid_o(AL)	Out	1	Write response valid
axi_S00_bid_o	Out	EXT_MAS_AXI_ID_WIDTH	AXI4: required AXI4-Lite: N/A
axi_S00_bresp_o(AL)	Out	2	Write response
axi_S00_buser_o	Out	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_S00_bready_i(AL)	In	1	Response ready
axi_S00_arvalid_i(AL)	In	1	Read address valid
axi_S00_arid_i	In	EXT_MAS_AXI_ID_WIDTH	Read address ID AXI4: optional AXI4-Lite: N/A
axi_S00_araddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Read address
axi_S00_arlen_i	In	8	Burst length AXI4: optional AXI4-Lite: N/A
axi_S00_arsize_i	In	3	Burst size AXI4: optional AXI4-Lite: N/A
axi_S00_arburst_i	In	2	Burst type AXI4: optional AXI4-Lite: N/A
axi_S00_arlock_i	In	1	Lock type AXI4: optional AXI4-Lite: N/A
axi_S00_arcache_i	In	4	Memory type AXI4: optional AXI4-Lite: N/A
axi_S00_arprot_i(AL)	In	3	Protection type
axi_S00_arqos_i	In	4	Quality of Service AXI4: optional AXI4-Lite: N/A
axi_S00_arregion_i	In	4	Region AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_S00_aruser_i	In	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_S00_arready_o(AL)	Out	1	Read address ready
Axi_S00_rvalid_o(AL)	Out	1	Read valid
Axi_S00_rid_o	Out	EXT_MAS_AXI_ID_WIDTH	Read ID AXI4: required AXI4-Lite: N/A
axi_S00_rdata_o(AL)	Out	EXT_MAS_MAX_AXI_DATA_WIDTH	Read data
Axi_S00_rresp_o(AL)	Out	2	Read response
Axi_S00_rlast_o	Out	1	Last read AXI4: required AXI4-Lite: N/A
axi_S00_ruser_o	Out	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_S00_rready_i(AL)	In	1	Read ready
AXI Interconnect xx Interface – Connected to External Manager xx			
axi_Sxx_awvalid_i(AL)	In	1	Write address valid
Axi_Sxx_awid_i	In	EXT_MAS_AXI_ID_WIDTH	Write address ID AXI4: optional AXI4-Lite: N/A
axi_Sxx_awaddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Write address
Axi_Sxx_awlen_i	In	8	Burst length, the exact number of transfers in a burst. AXI4: optional AXI4-Lite: N/A
axi_Sxx_awsize_i	In	3	Burst size, the size of each transfer in the burst. AXI4: optional AXI4-Lite: N/A
axi_Sxx_awburst_i	In	2	Burst type AXI4: optional AXI4-Lite: N/A
axi_Sxx_awlock_i	In	1	Lock type AXI4: optional AXI4-Lite: N/A
axi_Sxx_awcache_i	In	4	Memory type AXI4: optional AXI4-Lite: N/A
axi_Sxx_awprot_i(AL)	In	3	Protection type
axi_Sxx_awqos_i	In	4	Quality of service AXI4: optional AXI4-Lite: N/A
axi_Sxx_awregion_i	In	4	Region AXI4: required AXI4-Lite: N/A
axi_Sxx_awuser_i	In	AXI_USER_WIDTH	User signals AXI4: optional AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_Sxx_awready_o(AL)	Out	1	Write address ready
axi_Sxx_wvalid_i(AL)	In	1	Write valid
axi_Sxx_wdata_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH	Write data
axi_Sxx_wstrb_i(AL)	In	EXT_MAS_MAX_AXI_DATA_WIDTH/8	Write strobes
axi_Sxx_wlast_i	In	1	AXI4 Last write beat/burst AXI4: optional AXI4-Lite: N/A
axi_Sxx_wuser_i	In	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_Sxx_wready_o(AL)	Out	1	Write ready
axi_Sxx_bvalid_o(AL)	Out	1	Write response valid
axi_Sxx_bid_o	Out	EXT_MAS_AXI_ID_WIDTH	AXI4: required AXI4-Lite: N/A
axi_Sxx_bresp_o(AL)	Out	2	Write response
axi_Sxx_buser_o	Out	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_Sxx_bready_i(AL)	In	1	Response ready
axi_Sxx_arvalid_i(AL)	In	1	Read address valid
axi_Sxx_arid_i	In	EXT_MAS_AXI_ID_WIDTH	Read address ID AXI4: optional AXI4-Lite: N/A
axi_Sxx_araddr_i(AL)	In	EXT_MAS_MAX_AXI_ADDR_WIDTH	Read address
axi_Sxx_arlen_i	In	8	Burst length AXI4: optional AXI4-Lite: N/A
axi_Sxx_arsize_i	In	3	Burst size AXI4: optional AXI4-Lite: N/A
axi_Sxx_arburst_i	In	2	Burst type AXI4: optional AXI4-Lite: N/A
axi_Sxx_arlock_i	In	1	Lock type AXI4: optional AXI4-Lite: N/A
axi_Sxx_arcache_i	In	4	Memory type AXI4: optional AXI4-Lite: N/A
axi_Sxx_arprot_i(AL)	In	3	Protection type
axi_Sxx_arqos_i	In	4	Quality of service AXI4: optional AXI4-Lite: N/A
axi_Sxx_arregion_i	In	4	Region AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_Sxx_aruser_i	In	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_Sxx_arready_o(AL)	Out	1	Read address ready
axi_Sxx_rvalid_o(AL)	Out	1	Read valid
axi_Sxx_rid_o	Out	EXT_MAS_AXI_ID_WIDTH	Read ID AXI4: required AXI4-Lite: N/A
axi_Sxx_rdata_o(AL)	Out	EXT_MAS_MAX_AXI_DATA_WIDTH	Read data
axi_Sxx_rresp_o(AL)	Out	2	Read response
axi_Sxx_rlast_o	Out	1	Last read AXI4: required AXI4-Lite: N/A
axi_Sxx_ruser_o	Out	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_Sxx_rready_i(AL)	In	1	Read ready
AXI Interconnect Manager 00 Clock and Reset (Available if CDC is Enabled for this Port M00)			
axi_M00_aclk_i(AL)	In	1	Input clock to AXI interconnected Manager 00 port. It is required only when CDC is enabled for external Subordinate 00 port.
axi_M00_aresetn_i(AL)	In	1	Input AXI active Low reset to AXI interconnected Manager 00 port. It is required only when CDC is enabled for external Subordinate 00 port.
AXI Interconnect Manager yy Clock and Reset (Available if CDC is Enabled for this Port Myy)			
axi_Myy_aclk_i(AL)	In	1	Input clock to AXI interconnected Manager yy port. It is required only when CDC is enabled for external Subordinate yy port.
axi_Myy_aresetn_i(AL)	In	1	Input AXI active Low reset to AXI interconnected Manager yy port. It is required only when CDC is enabled for external Subordinate yy port.
AXI Interconnect Manager 00 Interface - Connected to External Subordinate 00			
axi_M00_awvalid_o(AL)	Out	1	Write address valid
axi_M00_awid_o	Out	EXT_SLV_AXI_ID_WIDTH	Write address ID AXI4: required AXI4-Lite: N/A
axi_M00_awaddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Write address
axi_M00_awlen_o	Out	8	Burst length, the exact number of transfers in a burst. AXI4: required AXI4-Lite: N/A
axi_M00_awsize_o	Out	3	Burst size, the size of each transfer in the burst. AXI4: required AXI4-Lite: N/A
axi_M00_awburst_o	Out	2	Burst type AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_M00_awlock_o	Out	1	Lock type AXI4: required AXI4-Lite: N/A
axi_M00_awcache_o	Out	4	Memory type AXI4: required AXI4-Lite: N/A
axi_M00_awprot_o(AL)	Out	3	Protection type
axi_M00_awqos_o	Out	4	Quality of service AXI4: required AXI4-Lite: N/A
axi_M00_awregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_M00_awuser_o	Out	AXI_USER_WIDTH	User signals AXI4: required AXI4-Lite: N/A
axi_M00_awready_i(AL)	In	1	Write address ready
axi_M00_wvalid_o(AL)	Out	1	Write valid
axi_M00_wdata_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH	Write data
axi_M00_wstrb_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH/8	Write strobes
axi_M00_wlast_o	Out	1	AXI4 Last write beat/burst AXI4: optional AXI4-Lite: N/A
axi_M00_wuser_o	Out	EXT_SLV_MAX_USER_WIDTH	User signal AXI4: required AXI4-Lite: N/A
axi_M00_wready_i(AL)	In	1	Write ready
Axi_M00_bvalid_i(AL)	In	1	Write response valid
Axi_M00_bid_i	In	EXT_SLV_AXI_ID_WIDTH	Write response ID AXI4: required AXI4-Lite: N/A
axi_M00_bresp_i(AL)	In	2	Write response
axi_M00_buser_i	In	AXI_USER_WIDTH	User signal AXI4: required AXI4-Lite: N/A
axi_M00_bready_o(AL)	Out	1	Response ready
axi_M00_arvalid_o(AL)	Out	1	Read address valid
axi_M00_arid_o	Out	EXT_SLV_AXI_ID_WIDTH	Read address ID AXI4: required AXI4-Lite: N/A
axi_M00_araddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Read address
axi_M00_arlen_o	Out	8	Burst length AXI4: required AXI4-Lite: N/A
axi_M00_arsize_o	Out	3	Burst size AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_M00_arburst_o	Out	2	Burst type AXI4: required AXI4-Lite: N/A
axi_M00_arlock_o	Out	1	Lock type AXI4: required AXI4-Lite: N/A
axi_M00_arcache_o	Out	4	Memory type AXI4: required AXI4-Lite: N/A
axi_M00_arprot_o(AL)	Out	3	Protection type
axi_M00_arqos_o	Out	4	Quality of service AXI4: required AXI4-Lite: N/A
axi_M00_arregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_M00_aruser_o	Out	AXI_USER_WIDTH	User signal AXI4: required AXI4-Lite: N/A
axi_M00_arready_i(AL)	In	1	Read address ready
axi_M00_rvalid_i(AL)	In	1	Read valid
axi_M00_rid_i	In	EXT_SLV_AXI_ID_WIDTH	Read ID AXI4: required AXI4-Lite: N/A
axi_M00_rdata_i(AL)	In	EXT_SLV_MAX_AXI_DATA_WIDTH	Read data
axi_M00_rresp_i(AL)	In	2	Read response
axi_M00_rlast_i	In	1	Last read AXI4: required AXI4-Lite: N/A
axi_M00_ruser_i	In	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_M00_rready_o(AL)	Out	1	Read ready
AXI Interconnect Manager yy Interface - Connected to External Subordinate yy			
axi_Myy_awvalid_o(AL)	Out	1	Write address valid
axi_Myy_awid_o	Out	EXT_SLV_AXI_ID_WIDTH	Write address ID AXI4: required AXI4-Lite: N/A
axi_Myy_awaddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Write address
axi_Myy_awlen_o	Out	8	Burst length, the exact number of transfers in a burst. AXI4: required AXI4-Lite: N/A
axi_Myy_awsize_o	Out	3	Burst size, the size of each transfer in the burst. AXI4: required AXI4-Lite: N/A
axi_Myy_awburst_o	Out	2	Burst type AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_Myy_awlock_o	Out	1	Lock type AXI4: required AXI4-Lite: N/A
axi_Myy_awcache_o	Out	4	Memory type AXI4: required AXI4-Lite: N/A
axi_Myy_awprot_o(AL)	Out	3	Protection type
axi_Myy_awqos_o	Out	4	Quality of service AXI4: required AXI4-Lite: N/A
axi_Myy_awregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_Myy_awuser_o	Out	AXI_USER_WIDTH	User signals AXI4: required AXI4-Lite: N/A
axi_Myy_awready_i(AL)	In	1	Write address ready
Axi_Myy_wvalid_o(AL)	Out	1	Write valid
Axi_Myy_wdata_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH	Write data
Axi_Myy_wstrb_o(AL)	Out	EXT_SLV_MAX_AXI_DATA_WIDTH/8	Write strobes
Axi_Myy_wlast_o	Out	1	AXI4 Last write beat/burst AXI4: optional AXI4-Lite: N/A
axi_Myy_wuser_o	Out	EXT_SLV_MAX_USER_WIDTH	User signal AXI4: required AXI4-Lite: N/A
axi_Myy_wready_i(AL)	In	1	Write ready
Axi_Myy_bvalid_i(AL)	In	1	Write response valid
Axi_Myy_bid_i	In	EXT_SLV_AXI_ID_WIDTH	Write response ID AXI4: required AXI4-Lite: N/A
axi_Myy_bresp_i(AL)	In	2	Write response
axi_Myy_buser_i	In	AXI_USER_WIDTH	User signal AXI4: required AXI4-Lite: N/A
axi_Myy_bready_o(AL)	Out	1	Response ready
axi_Myy_arvalid_o(AL)	Out	1	Read address valid
axi_Myy_arid_o	Out	EXT_SLV_AXI_ID_WIDTH	Read address ID AXI4: required AXI4-Lite: N/A
axi_Myy_araddr_o(AL)	Out	EXT_SLV_MAX_AXI_ADDR_WIDTH	Read address
axi_Myy_arlen_o	Out	8	Burst length AXI4: required AXI4-Lite: N/A
axi_Myy_arsize_o	Out	3	Burst size AXI4: required AXI4-Lite: N/A

Pin Name	Direction	Width (Bits)	Description
axi_Myy_arburst_o	Out	2	Burst type AXI4: required AXI4-Lite: N/A
axi_Myy_arlock_o	Out	1	Lock type AXI4: required AXI4-Lite: N/A
axi_Myy_arcache_o	Out	4	Memory type AXI4: required AXI4-Lite: N/A
axi_Myy_arprot_o(AL)	Out	3	Protection type
axi_Myy_arqos_o	Out	4	Quality of service AXI4: required AXI4-Lite: N/A
axi_Myy_arregion_o	Out	4	Region AXI4: required AXI4-Lite: N/A
axi_Myy_aruser_o	Out	AXI_USER_WIDTH	User signal AXI4: required AXI4-Lite: N/A
axi_Myy_arready_i(AL)	In	1	Read address ready
axi_Myy_rvalid_i(AL)	In	1	Read valid
axi_Myy_rid_i	In	EXT_SLV_AXI_ID_WIDTH	Read ID AXI4: required AXI4-Lite: N/A
axi_Myy_rdata_i(AL)	In	EXT_SLV_MAX_AXI_DATA_WIDTH	Read data
axi_Myy_rresp_i(AL)	In	2	Read response
axi_Myy_rlast_i	In	1	Last read AXI4: required AXI4-Lite: N/A
axi_Myy_ruser_i	In	AXI_USER_WIDTH	User signal AXI4: optional AXI4-Lite: N/A
axi_Myy_rready_o(AL)	Out	1	Read ready

Notes:

- xx refers to the number of external Managers. Possible values [0, 1, …, Total external Managers-1].
- yy refers to the number of external Subordinates. Possible values [0, 1, …, Total external Subordinates-1].
- AL- When the interface selected is AXI4-Lite, only these signals are part of the AXI4-Lite I/O interface.
- All AXI Manager/Subordinate interfaces are compliant with AXI4/AXI4-Lite protocol.
- All resets are asynchronously asserted but synchronously deasserted.

Refer to the AMBA AXI Protocol Specification web page for IHI0022H_c_amba_axi_protocol_spec for the timing diagrams and for more information about the protocol.

2.3. Attributes Summary

Table 2.2 provides the list of user-configurable attributes for the AXI Interconnect Module. The attribute values shown in Table 2.2 are specified using the IP Core Configuration user interface in the Lattice Propel Builder software.

Table 2.2. Attributes Table

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
General Settings Tab			
General			
Total External AXI4 Subordinates	1–32	2	Total AXI4 Managers and Total AXI4 Subordinates cannot both be one.
Total External AXI4 Managers	1–32	2	
AXI User width	1–128	4	AXI user width
Memory Type of Large FIFOs	LUT, EBR	0	Allows you to select the memory type for larger FIFOs.
External Manager Settings Tab			
General			
External Manager AXI ID width	1–6	1	External Manager AXI ID width
AXI Manager Max Address Width (bits)	13–64	32	External Manager maximum AXI address width Holds the maximum address bus width of the available external Manager.
AXI Manager Max Data Width (bits)	8, 16, 32, 64, 128, 256, 512,1024	32	External Manager maximum AXI data width Holds the maximum data bus width of the available external Manager.
AXI Manager Max no. of ID supports	1, 2, 4, 8, 16, 32, 64	1	External Manager maximum number of ID support Holds the maximum configured values for different External Manager.
External Manager Access Type Settings			
External Manager AXI access Type <N>	0–2	2	External Manager access type <N> = 0 to (Total External AXI4 Managers - 1) 0 – Write only port 1 – Read only port 2 – Write/Read port
External Manager Protocol Settings			
External Manager AXI protocol <N>	AXI4, AXI4-Lite	0	AXI protocol supported by the External Manager <N> = 0 to (Total External AXI4 Managers - 1) 0 – AXI4 1 – AXI4-Lite

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
External Manager CDC Enable Settings			
External Manager CDC enable <N>	0, 1	0	External Manager CDC enable <N> = 0 to (Total External AXI4 Managers - 1) 1 – Clock domain crossing enables for the connected external Manager <N> which is asynchronous to interconnect clock axi_aclk_i. 0 – CDC is not required for external Manager <N>
External Manager Address Settings			
External Manager Address width <N>	13–64	32	External Manager address width <N> = 0 to (Total External AXI4 Managers - 1)
External Manager Data Settings			
External Manager Data width <N>	8, 16, 32, 64, 128, 256, 512, 1024	32	External Manager data width <N> = 0 to (Total External AXI4 Managers - 1)
External Manager No. of IDs Support Settings			
External Manager No. of IDs <N>	1, 2, 4, 8, 16, 32, 64	1	External Manager No. of IDs <N> = 0 to (Total External AXI4 Managers - 1) Reordering Depth 1 – single thread 2 or more – multi-thread This value specifies the number of supported IDs and determines the supported ID values. Example: When this is configured to 4, supported IDs are 0, 1, 2 and 3.
External Manager IDs Order Enable Settings			
External Manager ID order enable <N>	0, 1	0	External Manager ID order enable <N> = 0 to (Total External AXI4 Managers - 1) To be set to 1, when the external Manager <N> issues the same ID to more than one external Subordinate.

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
External Manager Write Accept Settings			
External Manager Write accept <N>	2–16	8	Number of Outstanding Write transactions accepted by External Manager <N> connected to the AXI interconnect <N> = 0 to (Total External AXI4 Managers - 1) This configures the internal FIFO depth for the Write Address channel.
External Manager Read Accept Settings			
External Manager Read accept <N>	2–16	8	Number of Outstanding Read transactions accepted by External Manager<N> connected to the AXI interconnect <N> = 0 to (Total External AXI4 Managers - 1) This configures the internal FIFO depth for the Read Address channel.
External Manager Write Buffer Settings			
External Manager Write Response Buffer Depth <N>	2–16	8	The internal FIFO depth for the Write Response channel. <N>=0 to (Total External AXI4 Managers - 1)
External Manager Write Data Buffer Depth <N>	2–512	16	The internal FIFO depth for the Write Data channel. <N>=0 to (Total External AXI4 Managers - 1)
External Manager Read Buffer Settings			
External Manager Read Data Buffer Depth <N>	2–512	16	The internal FIFO depth for the Read Data channel. <N>=0 to (Total External AXI4 Managers - 1)
External Manager Priority Settings			
External Manager Priority <N>	Round Robin, Fixed Priority[4]	Round Robin	External Manager <N> priority scheme to choose responses from different external Subordinates (at write response channel and read response channel) <N> = 0 to (Total External AXI4 Managers - 1)
External Manager 0 Fixed Priority Settings			
Ext Subordinate 0 Ext Manager 0 Fixed Priority	0 to (Total External AXI4 Subordinates -1)	0	Ext Subordinate 0 Ext Manager 0 Fixed Priority
…			
Ext Subordinate <M> Ext Manager 0 Fixed Priority	0 to (Total External AXI4 Subordinates -1)	<M>	Ext Subordinate <M> Ext Manager 0 Fixed Priority <M> = 0 to (Total External AXI4 Subordinates -1)

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
External Manager <N> Fixed Priority Settings			
Ext Subordinate 0 Ext Manager N Fixed Priority	0 to (Total External AXI4 Subordinates -1)	0	Ext Subordinate 0 Ext Manager N Fixed Priority <N> = Total External AXI4 Managers -1
…			
Ext Subordinate <M> Ext Manager N Fixed Priority	0 to (Total External AXI4 Subordinates -1)	<M>	Ext Subordinate <M> Ext Manager N Fixed Priority <M> = 0 to (Total External AXI4 Subordinates -1) <N> = Total External AXI4 Managers -1
External Subordinate Settings Tab			
General			
External Subordinate AXI ID width	1–11	2	External Subordinate AXI ID width
AXI Subordinate Max Address Width (bits)	13–64	32	External Subordinate maximum AXI address width Holds the maximum address bus width of the available external Subordinate.
AXI Subordinate Max Data Width (bits)	8, 16, 32, 64, 128, 256, 512,1024	32	External Subordinate maximum AXI data width Holds the maximum data bus width of the available external Subordinate.
AXI Subordinate Max Fragment count	1–16	8	External Subordinate maximum fragment count Holds the maximum fragment count of the available external Subordinate.
External Subordinate Access Type Settings			
External Subordinate Access Type <M>	0–2	2	External Subordinate access type <M> = 0 to Total External AXI4 Subordinates -1 0 – Write only port 1 – Read only port 2 – Write/Read port
External Subordinate Protocol Type Settings			
External Subordinate Protocol type <M>	AXI4, AXI4-Lite	0	AXI protocol supported by the external Subordinate <M> = 0 to Total External AXI4 Subordinates -1

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
External Subordinate CDC Enable Settings			
External Subordinate CDC Enable <M>	0, 1	0	External Subordinate CDC enable <M> = 0 to Total External AXI4 Subordinates -1 1 – Clock domain crossing enables for the connected external Subordinate <M> which is asynchronous to interconnect “axi_aclk_i”. 0 – CDC is not required for external Subordinate<M>.
External Subordinate Address Settings			
External Subordinate Address width <M>	13–64	32	External Subordinate address width <M> = 0 to Total External AXI4 Subordinates -1
External Subordinate Data Settings			
External Subordinate Data width <M>	8, 16, 32, 64, 128, 256, 512, 1024	32	External Subordinate data width <M> = 0 to Total External AXI4 Subordinates -1
External Subordinate IDs Returned in Order Settings			
External Subordinate ID returned out-of-order <M>[1]	0, 1	1	External Subordinate ID returned out-of-order <M> = 0 to Total External AXI4 Subordinates -1 1 – Write Response and Read Data channels are returned out of order 0 – Write Response and Read Data channels are returned in order
External Subordinate Write Issue Settings			
External Subordinate Write Issue <M>	2–16	8	Number of Outstanding Write transactions issued from each external Subordinate <M> connected to the AXI interconnect <M> = 0 to Total External AXI4 Subordinates -1 This configures the internal FIFO depth for the Write Address channel
External Subordinate Read Issue Settings			
External Subordinate Read Issue <M>	2–16	8	Number of Outstanding Read transactions issued from each external Subordinate <M> connected to the AXI interconnect <M> = 0 to Total External AXI4 Subordinates -1 This configures the internal FIFO depth for the Read Address channel

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
External Subordinate Write Buffer Settings			
External Subordinate Write Response Buffer Depth <M>	2–16	8	The internal FIFO depth for the Write Response channel <M>=0 to (Total External AXI4 Subordinates -1)
External Subordinate Write Data Buffer Depth <M>	2–512	64	The internal FIFO depth for the Write Data channel <M>=0 to (Total External AXI4 Subordinates -1)
External Subordinate Read Buffer Settings			
External Subordinate Read Data Buffer Depth <M>	2–512	64	The internal FIFO depth for the Read Data channel <M>=0 to (Total External AXI4 Subordinates -1)
External Subordinate Fragment Settings			
External Subordinate <M> fragment count	1–16	8	External Subordinate fragment count <M> = 0 to Total External AXI4 Subordinates -1
External Subordinate Priority Settings			
External Subordinate Priority <M>	Round Robin, Fixed Priority[4]	Round Robin	External Subordinate <M> priority scheme to choose request from different external Managers (at write address and read address channel) <M> = 0 to Total External AXI4 Subordinates -1
External Subordinate 0 Fixed Priority Settings			
Ext Manager 0 Ext Subordinate 0 Fixed Priority	0 to (Total External AXI4 Managers -1)	0	Ext Manager 0 Ext Subordinate 0 Fixed Priority
…			
Ext Manager <N> Ext Subordinate 0 Fixed Priority	0 to (Total External AXI4 Managers -1)	<N>	Ext Manager <N> Ext Subordinate 0 Fixed Priority <N> = 0 to (Total External AXI4 Managers -1)
External Subordinate <M> Fixed Priority Settings			
Ext Manager 0 Ext Subordinate M Fixed Priority	0 to (Total External AXI4 Managers -1)	0	Ext Manager 0 Ext Subordinate <M> Fixed Priority <M> = Total External AXI4 Subordinates-1
…			
Ext Manager <N> Ext Subordinate M Fixed Priority	0 to (Total External AXI4 Managers -1)	<N>	Ext Manager <N> Ext Subordinate <M> Fixed Priority <M> = Total External AXI4 Subordinates-1 <N> = 0 to (Total External AXI4 Managers -1)

Attribute Name	Selectable Values	Default	Dependency on Other Attributes
Attributes Hidden in the Module/IP Block Wizard in the Lattice Propel Builder[3]			
External Subordinate 0 Base Address Settings			
Base address <F>	0 to ((2^ External Subordinate Address width 0) - 'h 1000)	—	Base address for external Subordinate 0 Fragment <F> <F> = 0 to (External Subordinate 0 fragment count-1)
…			
External Subordinate <M> Base Address Settings			
Base address <F>	0 to (2^ External Subordinate Address width <M>) - 'h 1000	—	Base address for external Subordinate M Fragment <F> <F> = 0 to (External Subordinate M fragment count-1) <M> = Total External AXI4 Subordinates-1
External Subordinate 0 End Address Settings			
End address <F>[2]	'h FFF - (2^ External Subordinate Address width 0)	—	End address for external Subordinate 0 Fragment <F> <F> = 0 to (External Subordinate 0 fragment count-1)
…			
External Subordinate <M> End Address Settings			
End address <F>[2]	‘h FFF - (2^ External Subordinate Address width 0)	—	End address for external Subordinate N Fragment <F> <F> = 0 to (External Subordinate M fragment count-1) <M> = Total External AXI4 Subordinates-1

Notes:

1. When the external subordinate connected to this block is guaranteed to return the write response or read data in order, regardless of IDs, this flag is unchecked to save internal logic during down-conversion on the AXI data bus.
2. Minimum size for each of the external Subordinate fragments must be a multiple of 4 KB.
   Examples:
   - Subordinate 0 fragment 0 base address = ‘h0000
   - Subordinate 0 fragment 0 end address = ‘h0FFF
   - Subordinate 0 fragment 1 base address = ‘h1000
   - Subordinate 0 fragment 1 end address = ‘h1FFF
3. These parameters are automatically configured by the Lattice Propel Builder.
4. Priority order 0, 1, 2, …, M (or N), with 0 being the highest priority.

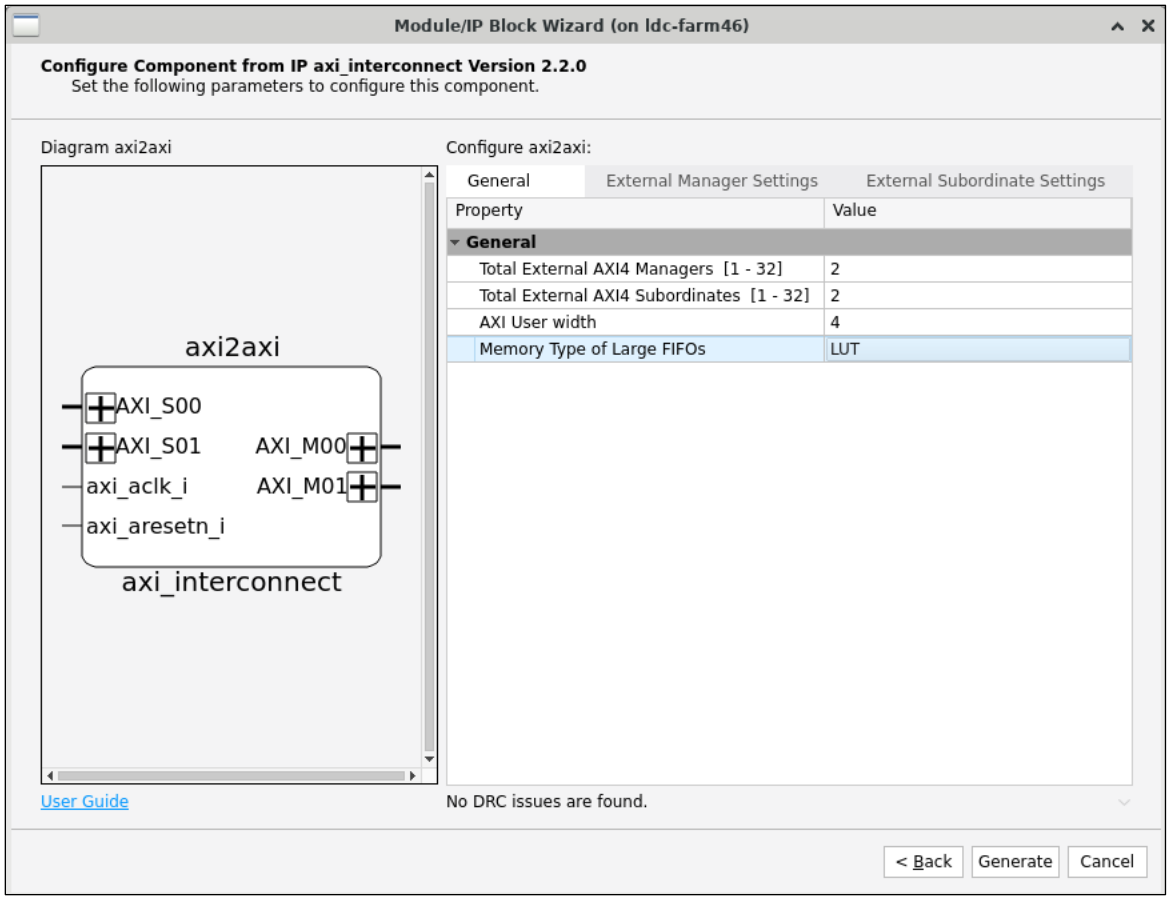

Figure 2.12. AXI4 Interconnect Module Configuration User Interface

Table 2.3. Attributes Description

Attribute Name	Description
General Settings Tab	
General	
Total External AXI4 Subordinates	Total external AXI4 Subordinates
Total External AXI4 Managers	Total external AXI4 Managers
AXI User Width	AXI user width This is the common bit width for all the AXI4 interfaces.
External Manager Settings Tab	
General	
External Manager AXI ID width	External Manager AXI ID width Holds the maximum ID bit width required by the external Manager port interfaces.
AXI Manager Max Address Width (bits)	External Manager maximum AXI address width Holds the maximum address bus width of the available external Manager.
AXI Manager Max Data Width (bits)	External Manager maximum AXI data width Holds the maximum data bus width of the available external Manager.
AXI Manager Max no. of ID supports	External Manager Maximum number of ID Support Holds maximum of the configured values for different external Manager.
External Manager Access Type Settings	
External Manager AXI access Type <N>	External Manager WO/RO/WR access type <N> = 0 to (Total External AXI4 Managers -1) 0 – Write only port 1 – Read only port 2 – Write/Read port
External Manager Protocol Settings	
External Manager AXI protocol <N>	AXI protocol supported by the external Manager N <N> = 0 to (Total External AXI4 Managers -1) The supported protocol types are AXI4 and AXI4-Lite.
External Manager CDC Enable Settings	
External Manager CDC enable <N>	External Manager port interface <N> clock domain crossing enable/disable This is enabled when external Manager port interface <N> is asynchronous to the AXI interconnect clock axi_aclk_i. <N> = 0 to (Total External AXI4 Managers -1).
External Manager Address Settings	
External Manager Address width<N>	External Manager address width <N> = 0 to (Total External AXI4 Managers -1). This is used for the configuration of each of the external Manager port address width.
External Manager Data Settings	
External Manager Data width <N>	External Manager data width <N> = 0 to (Total External AXI4 Managers -1) This is used for the configuration of each of the external Manager port data bus width.

Attribute Name	Description
External Manager No. of IDs Support Settings	
External Manager No. of IDs <N>	Number of different AXI4 IDs supported by external Manager <N> <N> = 0 to (Total External AXI4 Managers -1) Reordering Depth 1 – single thread 2 or more – multi-thread The supported IDs are in ascending order, starting from 0. For example: External Manager No. of IDs = 4 Supported IDs = 0, 1, 2, 3
External Manager IDs Order Enable Settings	
External Manager ID order enable <N>	ID order enable/disable for the external Manager <N> <N> = 0 to (Total External AXI4 Managers -1) When same ID is issued to more than one external Subordinate by an external Manager <N>, then AXI interconnect ensures that the write/read responses from different Subordinates are passed in the order of reception of requests received from the external Manager <N>.
External Manager Write Accept Settings	
External Manager Write accept<N>	Number of Outstanding Write transactions accepted by external Manager <N> connected to the AXI interconnect <N> = 0 to (Total External AXI4 Managers -1) This configures the internal FIFO depth for the Write Address channel
External Manager Read Accept Settings	
External Manager Read accept<N>	Number of Outstanding Read transactions accepted by external Manager<N> connected to the AXI interconnect <N> = 0 to (Total External AXI4 Managers -1) This configures the internal FIFO depth for the Read Address channel
External Manager Write Buffer Settings	
External Manager Write Response Buffer Depth<N>	Configures the internal FIFO depth for the Write Response channel. <N> = 0 to (Total External AXI4 Managers -1)
External Manager Write Data Buffer Depth<N>	Configures the internal FIFO depth for the Write Data channel. <N> = 0 to (Total External AXI4 Managers -1)
External Manager Read Buffer Settings	
External Manager Read Data Buffer Depth<N>	Configures the internal FIFO depth for the Read Data channel. <N> = 0 to (Total External AXI4 Managers -1)
External Manager Priority Settings	
External Manager Priority<N>	External Manager <N> priority scheme to choose responses from different external Subordinates (at write response channel and read response channel) <N> = 0 to (Total External AXI4 Managers -1). The available priority schemes are round robin and fixed priority.

Attribute Name	Description
External Manager 0 Fixed Priority Settings	
Ext Subordinate <M> Ext Manager 0 Fixed Priority	This is enabled when external Manager 0 is set to fixed priority. This configures the order of fixed priority to be followed between different external Subordinates for external Manager 0. Ext Subordinate <M> Ext Manager 0 Fixed Priority <M> = 0 to (Total External AXI4 Subordinates -1)
External Manager <N> Fixed Priority Settings	
Ext Subordinate <M> Ext Manager N Fixed Priority	This is enabled when external Manager N is set to fixed priority. This configures the order of fixed priority to be followed between different external Subordinates for external Manager N. Ext Subordinate <M> Ext Manager N Fixed Priority <M> = 0 to (Total External AXI4 Subordinates -1) <N> = Total External AXI4 Managers -1
External Subordinate Settings Tab	
General	
External Subordinate AXI ID width	External Subordinate AXI ID width Holds the maximum ID bit width required by the external Subordinate port interfaces. The External Subordinate AXI ID Width has to be equal or greater than External Manager AXI ID width + max(log2(Total External AXI4 Managers, 1)). Internally, the AXI4 Interconnect appends the index for each external manager to the External Manager ID on the LSBs. For example: Total External AXI4 Managers = 2 External Manager AXI ID width = 4 External Subordinate AXI ID width = 5 Bit 0 denotes either external manager 0 or 1 Bits 1 to 4 hold the 4-bit External Manager AXI ID
AXI Subordinate Max Address Width(bits)	External Subordinate maximum AXI address width Holds the maximum address bus width of the available external Subordinate.
AXI Subordinate Max Data Width(bits)	External Subordinate maximum AXI data width Holds the maximum data bus width of the available external Subordinate.
AXI Subordinate Max Fragment count	External Subordinate Max Fragment count Holds the maximum fragment count of the available external Subordinate.
External Subordinate Access Type Settings	
External Subordinate Access Type <M>	External Subordinate WO/RO/WR access type <M> = 0 to (Total External AXI4 Subordinates -1) 0 – Write only port 1 – Read only port 2 – Write/Read port
External Subordinate Protocol Type Settings	
External Subordinate Protocol type <M>	AXI protocol supported by the external Subordinate M <M> = 0 to (Total External AXI4 Subordinates -1) The supported protocol types are AXI4 and AXI4-Lite.

Attribute Name	Description
External Subordinate CDC Enable Settings	
External Subordinate CDC Enable <M>	External Subordinate port interface <M> clock domain crossing enable/disable This is enabled when external Subordinate port interface <M> is asynchronous to the AXI interconnect clock axi_aclk_i. <M> = 0 to (Total External AXI4 Subordinates -1).
External Subordinate Address Settings	
External Subordinate Address width <M>	External Subordinate address width <M> = 0 to (Total External AXI4 Subordinates -1). This is used for the configuration of each of the external Subordinate port address width.
External Subordinate Data Settings	
External Subordinate Data width <M>	External Subordinate data bus width <M> = 0 to (Total External AXI4 Subordinates -1). This is used for the configuration of each of the external Subordinate port data bus width.
External Subordinate IDs Returned in Order Settings	
External Subordinate ID returned out-of-order<M>	External Subordinate ID returned out-of-order <M> = 0 to Total External AXI4 Subordinates -1 1 – Write Response and Read Data channels are returned out of order 0 – Write Response and Read Data channels re returned in order
External Subordinate Write Issue Settings	
External Subordinate Write Issue <M>	Number of Outstanding Write transactions issued by each external Subordinate <M> connected to the AXI interconnect <M> = 0 to Total External AXI4 Subordinates -1 This configures the internal FIFO depth for the Write Address channel
External Subordinate Read Issue Settings	
External Subordinate Read Issue <M>	Number of Outstanding read transactions issued by each external Subordinate <M> connected to the AXI interconnect <M> = 0 to Total External AXI4 Subordinates -1 This configures the internal FIFO depth for the Read Address channel
External Subordinate Write Buffer Settings	
External Subordinate Write Response Buffer Depth <M>	Configures the internal FIFO depth for the Write Response channel. <M>=0 to (Total External AXI4 Subordinates -1)
External Subordinate Write Data Buffer Depth <M>	Configures the internal FIFO depth for the Write Data channel. <M>=0 to (Total External AXI4 Subordinates -1)
External Subordinate Read Buffer Settings	
External Subordinate Read Data Buffer Depth <M>	Configures the internal FIFO depth for the Write Response channel. <M>=0 to (Total External AXI4 Subordinates -1)

Attribute Name	Description
External Subordinate Fragment Settings	
External Subordinate <M> fragment count	Number of fragments per external Subordinate interface <M> = 0 to Total External AXI4 Subordinates -1 This fragment count should not exceed the AXI Subordinate maximum fragment count.
External Subordinate Priority Settings	
External Subordinate Priority <M>	External Subordinate <M> priority scheme to choose requests from different external Managers (at write and read address channel) <M> = 0 to (Total External AXI4 Subordinates -1) The available priority schemes are round robin and fixed priority.
External Subordinate 0 Fixed Priority Settings	
Ext Manager <N> Ext Subordinate 0 Fixed Priority	This is enabled when external Subordinate 0 is set to fixed priority. This configures the order of fixed priority to be followed between different external Managers for external Subordinate 0. Ext Manager <N> Ext Subordinate 0 Fixed Priority <N> = 0 to (Total External AXI4 Managers -1)
External Subordinate <M> Fixed Priority Settings	
Ext Manager <N> Ext Subordinate M Fixed Priority	This is enabled when external Subordinate M is set to fixed priority. This configures the order of fixed priority to be followed between different external Managers for external Subordinate M. Ext Manager <N> Ext Subordinate M Fixed Priority <N> = 0 to (Total External AXI4 Managers -1)
Attributes Hidden in the Module/IP Block Wizard in the Lattice Propel Builder[4]	
External Subordinate <M> Base Address Settings	
Base address <F>[1]	Base address for external Subordinate <M> Fragment <F> <F> = 0 to (External Subordinate M fragment count-1)
External Subordinate <M> End Address Settings	
End address <F>[2]	End address for external Subordinate <M> Fragment <F> <F> = 0 to (External Subordinate M fragment count-1)

Notes:

1. The base address has to be multiple of 4 KB (2^12), for example, 0, ‘h1000, ‘h2000, and so on.
2. The end address has to be multiple of 4 KB-1, for example, ‘hFFF, ‘h1FFF, and so on.
3. The address range per fragment starts from the Base address and ends at the End address. This address range should be non-overlapping between different fragments across the external Subordinates.
4. These parameters are automatically configured by the Lattice Propel Builder.

2.4. Use Models

The AXI Interconnect Module connects one or more AXI4/AXI4-Lite Manager devices to one or more AXI4/AXI4-Lite Subordinate devices.

Each connected AXI Manager device could either be:

- a device that originates AXI4/AXI4-Lite transactions, that is, endpoint Manager or
- a Manager interface of an upstream AXI Interconnect core being cascaded.

Similarly, each connected AXI4/AXI4-Lite Subordinate device could either be:

- the final target of AXI4/AXI4-Lite transactions, that is, endpoint Subordinate or
- a Subordinate interface of a downstream AXI Interconnect core being cascaded.

In general, AXI Interconnect Module can be configured for the following connectivity patterns:

- Single Manager Interconnect – refer to the Single Manager Interconnect diagram (Figure 2.13)
- Multi-Manager Interconnect – refer to the Multi-Manager Interconnect diagram (Figure 2.14)

An example of Single Manager Interconnect application is shown in Figure 2.13. The arrows in the figure are AXI4/AXI4-Lite interface connections, where M stands for an AXI Manager port, and S stands for an AXI Subordinate port. The AXI interface type can be configured as either AXI4 or AXI4-Lite.

In this example, the Instruction port of the CPU is directly connected to one port of Dual Port Memory while the Data port of the CPU is connected to the Subordinate port of Single Manager Interconnect. This connection allows parallel instruction fetch and data access execution. The Manager ports of Single Manager Interconnect are connected to one port of Dual Port Memory, AXI2AHB Bridge, AXI2APB Bridge, and LPDDR4 MC. This allows the CPU Data port to access the said Subordinates.

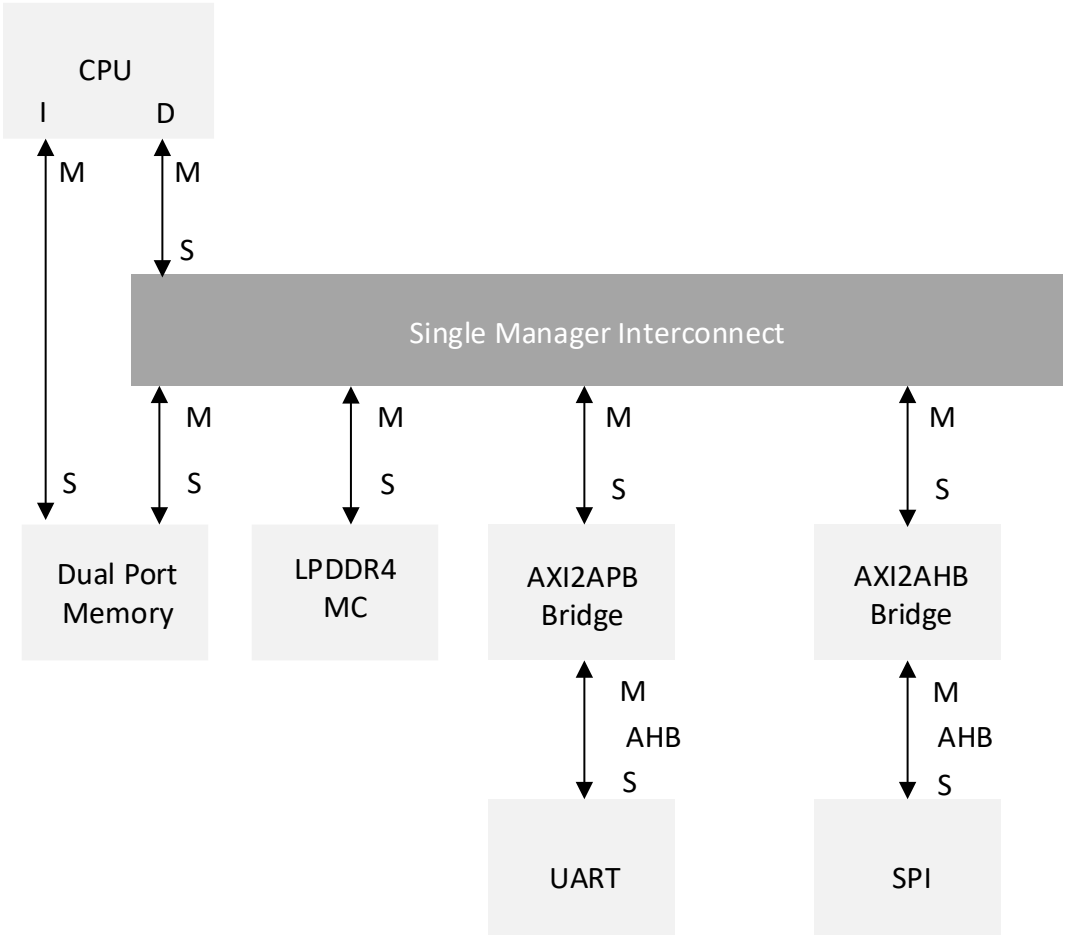

Figure 2.13. Example of Single Manager Interconnect Application

An example of Multi-Manager Interconnect application is shown in Figure 2.14.This is similar to Figure 2.13 with the addition of DMA IP. In this example, DMA is configured to have one AXI4 Manager port for reading and writing data to Memory and one AXI4-Lite Subordinate port for register access by the CPU.

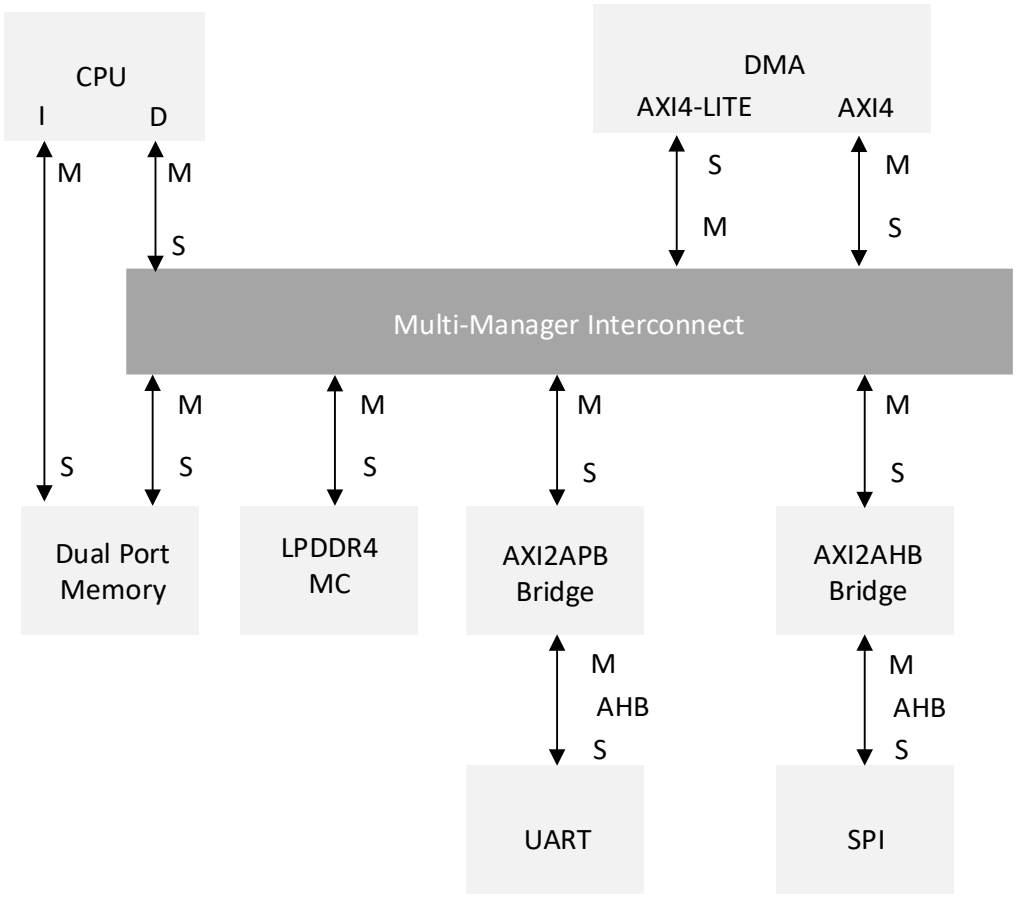

Figure 2.14. Example of Multi-Manager Interconnect Application

2.4.1. Default Subordinate

When a transfer is attempted to an address that does not map to an external Subordinate, the default Subordinate provides DECERR response.

Appendix A. Resource Utilization

The following tables show the resource utilization of the AXI Interconnect Module for different Lattice FPGA devices using the Lattice Radiant software 2025.1 with Synplify Pro as the synthesis tool. The data is collected on a build-by-build basis.

The tables are structured into three different sections: basic configuration, width conversion configuration, and mix-mode configurations.

These tables demonstrate how the resource usage and Fmax are affected by the width conversion block, CDC block, FIFO depth, and larger FIFO memory type.

Other configurations not mentioned are left as default.

Table A.1. Resource Utilization Using the LAV-AT-E70-3LFG1156I Device and LUT-based FIFO Mode

Basic Configuration	CDC	FIFO Depth	Clock Fmax (MHz)			Registers	LUTs	EBRs
			Subordinate Interface	Crossbar	Manager Interface			
External Managers: 1 External Subordinates: 2 Other default configurations	Enabled	Default	250	231.911	250	2470	4064	0
	Enabled	Minimum	250	250	250	2209	2817	0
	Disabled	Default	250			2592	4027	0
	Disabled	Minimum	250			2252	2834	0
External Managers: 2 External Subordinates: 1 Other default configurations	Enabled	Default	250	250	250	2487	3847	0
	Enabled	Minimum	250	250	250	2263	3074	0
	Disabled	Default	250			2633	3817	0
	Disabled	Minimum	250			2317	3140	0
External Managers: 2 External Subordinates: 2 Other default configurations	Enabled	Default	250	250	250	3394	5666	0
	Enabled	Minimum	250	250	250	3062	4335	0
	Disabled	Default	250			3569	5542	0
	Disabled	Minimum	250			3135	4641	0
Width Conversion Configuration	**Mode**		**Clock Fmax (MHz)**			**Registers**	**LUTs**	**EBRs**
			Subordinate Interface	**Crossbar**	**Manager Interface**			
External Managers: 4 External Subordinates: 1 External Managers Data Width: 32 External Subordinate Data Width: 256 CDC Enabled Other default configurations	Up Converter		163.747	188.147	250	13806	20152	0
External Managers: 1 External Subordinates: 4 External Managers Data Width: 256 External Subordinate Data Width: 32 CDC Enabled Other default configurations	Down Converter		250	200.924	166.279	17203	30894	0

Table A.2. Resource Utilization Using the LAV-AT-E70-3LFG1156I Device and EBR-based FIFO Mode

Basic Configuration	CDC	FIFO Depth	Clock Fmax (MHz)			Registers	LUTs	EBRs
			Subordinate Interface	Crossbar	Manager Interface			
External Managers: 1 External Subordinates: 2 Other default configurations	Enabled	Default	250	250	250	2486	2182	12
	Enabled	Minimum	250	213.447	250	2223	1826	12
	Disabled	Default	250			250	2098	12
	Disabled	Minimum	250			250	1881	12
External Managers: 2 External Subordinates: 1 Other default configurations	Enabled	Default	250	246.427	250	2525	2491	12
	Enabled	Minimum	250	246.124	250	2304	2253	12
	Disabled	Default	250			250	2395	12
	Disabled	Minimum	250			250	2258	12
External Managers: 2 External Subordinates: 2 Other default configurations	Enabled	Default	250	245.881	250	3436	3494	16
	Enabled	Minimum	250	250	250	3110	3116	16
	Disabled	Default	250			250	3392	16
	Disabled	Minimum	250			3155	3257	16
Width Conversion Configuration	**Mode**		**Clock Fmax (MHz)**			**Registers**	**LUTs**	**EBRs**
			Subordinate Interface	**Crossbar**	**Manager Interface**			
External Managers: 4 External Subordinates: 1 External Managers Data Width: 32 External Subordinate Data Width: 256 CDC Enabled Other default configurations	Up Converter		168.265	182.582	250	13892	12055	55
External Managers: 1 External Subordinates: 4 External Managers Data Width: 256 External Subordinate Data Width: 32 CDC Enabled Other default configurations	Down Converter		186.22	210.04	250	17262	13795	55

Table A.3. Resource Utilization Using the LFCPNX-100-9LFG672I Device and LUT-based FIFO Mode

Basic Configuration	CDC	FIFO Depth	Clock Fmax (MHz)			Registers	LUTs	EBRs
			Subordinate Interface	Crossbar	Manager Interface			
External Managers: 1 External Subordinates: 2 Other default configurations	Enabled	Default	200	194.818	200	2453	4417	0
	Enabled	Minimum	200	182.282	200	2192	2767	0
	Disabled	Default	200			2571	4330	0
	Disabled	Minimum	200			2232	2814	0
External Managers: 2 External Subordinates: 1 Other default configurations	Enabled	Default	200	179.565	200	2477	4088	0
	Enabled	Minimum	200	182.183	200	2243	3062	0
	Disabled	Default	183.318			2621	3926	0
	Disabled	Minimum	200			2301	3063	0
External Managers: 2 External Subordinates: 2 Other default configurations	Enabled	Default	200	188.715	200	3381	6106	0
	Enabled	Minimum	200	187.301	200	3051	4279	0
	Disabled	Default	185.563			3559	5909	0
	Disabled	Minimum	188.501			3119	4286	0
Width Conversion Configuration	**Mode**		**Clock Fmax (MHz)**			**Registers**	**LUTs**	**EBRs**
			Subordinate Interface	**Crossbar**	**Manager Interface**			
External Managers: 4 External Subordinates: 1 External Managers Data Width: 32 External Subordinate Data Width: 256 CDC Enabled Other default configurations	Up Converter		135.08	152.045	184.06	13788	21319	0
External Managers: 1 External Subordinates: 4 External Managers Data Width: 256 External Subordinate Data Width: 32 CDC Enabled Other default configurations	Down Converter		194.175	140.193	127.356	17178	35917	0

Table A.4. Resource Utilization Using the LFCPNX-100-9LFG672I Device and EBR-based FIFO Mode

Basic Configuration	CDC	FIFO Depth	Clock Fmax (MHz)			Registers	LUTs	EBRs
			Subordinate Interface	Crossbar	Manager Interface			
External Managers: 1 External Subordinates: 2 Other default configurations	Enabled	Default	200	166.722	200	2480	2191	24
	Enabled	Minimum	200	192.012	200	2220	1858	24
	Disabled	Default	175.009			2596	2105	24
	Disabled	Minimum	192.938			2256	1888	24
External Managers: 2 External Subordinates: 1 Other default configurations	Enabled	Default	200	170.474	200	2519	2491	24
	Enabled	Minimum	200	180.05	200	2285	2185	24
	Disabled	Default	173.329			2663	2403	24
	Disabled	Minimum	167.224			2343	2194	24
External Managers: 2 External Subordinates: 2 Other default configurations	Enabled	Default	200	165.728	200	3421	3451	32
	Enabled	Minimum	200	165.837	200	3091	3069	32
	Disabled	Default	156.887			3599	3410	32
	Disabled	Minimum	180.538			3159	3070	32
Width Conversion Configuration	**Mode**		**Clock Fmax (MHz)**			**Registers**	**LUTs**	**EBRs**
			Subordinate Interface	**Crossbar**	**Manager Interface**			
External Managers: 4 External Subordinates: 1 External Managers Data Width: 32 External Subordinate Data Width: 256 CDC Enabled Other default configurations	Up Converter		140.135	139.218	200	13867	12046	105
External Managers: 1 External Subordinates: 4 External Managers Data Width: 256 External Subordinate Data Width: 32 CDC Enabled Other default configurations	Down Converter		200	145.243	124.969	17234	13888	105

Table A.5. Resource Utilization Using the LAV-AT-E70-3LFG1156I Device – Mix Mode Resource Comparison

This table illustrates how to reduce resource usage, if the external subordinate always returns write responses or read data in order. The External Subordinate ID returned out-of-order flag is marked as *0*, and the IP core instantiates a reordering depth of 1.

Mix Mode Configuration	Response Out of Order (Has Reorder Buffers)	Memory Type of Large FIFOs	Registers	LUTs	EBRs
External Managers: 4 External Subordinates: 5	Yes	LUT	52320	98399	0
		EBR	54211	54443	179
External Managers Data Width: 16, 32, 64, 512 External Subordinates Data Width: 8, 32, 64, 128, 256 Numbers of supported IDs: 4 External Subordinate ID returned out-of-order: unchecked CDC Enabled Other default configurations	No	LUT	53510	93069	0
		EBR	55222	49072	179

Appendix B. Known Issues

Data Width Conversion

If data width conversion is required on the AXI4 interconnect, use the following recommended conversion for AXI4 interconnect to function properly:

- 32-bit to 128-bit (upsize)
- 32-bit to 256-bit (upsize)
- 64-bit to 32-bit (downsize), with CDC disabled

During downsizing, wuser data location at the subordinate may be incorrect.

Write Response Buffer Depth with AXI4-Lite

For AXI4 interconnect to function properly, if *AXI4-Lite* is selected for the *External Manager AXI Protocol* or the *External Subordinate AXI Protocol* setting, it is recommended to retain the default values of the following settings:

- In the **External Manager Settings** tab:
  - Write Response Buffer Depth
  - *Read Data Buffer Depth*
- In the **External Subordinate Settings** tab:
  - *Write Response Buffer Depth*
  - *Read Data Buffer Depth*

References

- AXI4 Interconnect Module Release Notes (FPGA-RN-02045)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- AMBA AXI Protocol Specification web page for IHI0022H_c_amba_axi_protocol_spec
- LatticeECP3 web page
- ECP5 web page
- CrossLink-NX web page
- CertusPro-NX web page
- Certus-NX web page
- Certus-N2 web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.8, IP v2.2.0, June 2025

Section	Change Summary
Introduction	Renamed *Supported FPGA Family* to *Supported Devices* in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.

Functional Description	• Updated Table 2.2. Attributes Table as follows:
	  • Removed the Full Address Decoding up to 4kB attribute.
	  • Added the *Memory Type of Large FIFOs* attribute.
	• Updated Figure 2.12. AXI4 Interconnect Module Configuration User Interface.

Resource Utilization	Updated LUT-based FIFO mode resource utilization and added EBR-based FIFO mode resource utilization for the Lattice Radiant software 2025.1.
Known Issues	Added description on data location during downsizing in the Data Width Conversion section.
References	Updated references.

Revision 1.7, IP v2.1.0, December 2024

Section	Change Summary
Introduction	Added Certus-N2, LatticeECP3, and ECP5 devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Resource Utilization	Updated the LUTs for the *External Managers: 2, External Subordinates: 2* configuration when CDC is disabled and FIFO path is set to default in Table A.1. Resource Utilization Using the LAV-AT-E70-3LFG1156I Device.
Known Issues	Added this section.
References	Updated references.

Revision 1.6, September 2024

Section	Change Summary
Functional Description	Removed the *Enable Simulation* attribute in the following tables: • Table 2.2. Attributes Table • Table 2.3. Attributes Description

Revision 1.5, June 2024

Section	Change Summary
All	• This revision is for version 2.0.0 of the AXI4 Interconnect Module. • Removed Appendix B. *Known Issues*. • Performed minor formatting and typo edits.
Acronyms in This Document	Added definition for FIFO.
Introduction	Added CrossLink-NX, Certus-NX, and MachXO5-NX devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.

Functional Description	• Added Figure 2.2. Internal Structure of the AXI4 Interconnect Module.
	• Added the following sections:
	  • External Manager Interface
	  • FIFO Interface
	  • Crossbar
	  • External Subordinate Interface
	  • Width Conversion
	  • Protocol Conversion
	• Added a note on reset assertion and deassertion in Table 2.1. AXI Interconnect Module Signal Description.

Section	Change Summary

	• Updated Table 2.2. Attributes Table.
	  • Added attributes: Enable Simulation, External Manager Write Response Buffer Depth<N>, External Manager Write Data Buffer Depth<N>, External Manager Read Data Buffer Depth<N>, External Subordinate ID returned out-of-order<M>, External Subordinate Write Response Buffer Depth <M>, External Subordinate Write Data Buffer Depth <M>, External Subordinate Read Data Buffer Depth <M>.
	  • Updated the default values for attributes: External Manager AXI ID width, AXI Manager Max no. of ID supports, External Manager No. of IDs <N>, External Manager Write accept<N>, External Manager Read accept<N>, External Manager Priority<N>, External Subordinate AXI ID width, External Subordinate Write Issue <M>, External Subordinate Read Issue <M>, External Subordinate Priority <M>.
	  • Mentioned that Base Address and End Address attributes are hidden in the Module/IP Block Wizard in the Lattice Propel Builder.
	• Updated Table 2.3. Attributes Description.
	  • Added attributes: External Manager Write Response Buffer Depth<N>, External Manager Write Data Buffer Depth<N>, External Manager Read Data Buffer Depth<N>, External Subordinate ID returned out-of-order<M>, External Subordinate ID returned out-of-order<M>, External Subordinate Write Response Buffer Depth<M>, External Subordinate Write Data Buffer Depth<M>, External Subordinate Read Data Buffer Depth<M>.
	  • Updated description for attributes: Enable Simulation, External Manager No. of IDs <N>, External Manager Write accept<N>, External Manager Read accept<N>, External Subordinate AXI ID width, External Subordinate Write Issue <M>, External Subordinate Read Issue <M>.
	  • Mentioned that Base Address and End Address attributes are hidden in the Module/IP Block Wizard in the Lattice Propel Builder.

Appendix A. Resource Utilization	Updated resource utilization per the Lattice Radiant software version 2024.1.
References	Updated references.
Technical Support Assistance	Updated the link to the Lattice Answer Database.

Revision 1.4, December 2023

Section	Change Summary
Functional Description	• Removed the following ports from Table 2.1. AXI Interconnect Module Signal Description: *axi_S00_aclken_i*, *axi_Sxx_aclken_i*, *axi_M00_aclken_i*, and *axi_Myy_aclken_i*. • Updated Figure 2.3. AXI Interconnect Module Configuration User Interface.
References	Added links to Lattice Avant-G and Avant-X devices web pages.

Revision 1.3, November 2023

Section	Change Summary
All	This revision is for version 1.2.1 of AXI Interconnect Module.
Disclaimers	Updated this section.
Inclusive Language	Newly added this section.
Introduction	In the Features section, changed *support fragmented address space of up to eight fragments per external Subordinate* to *support fragmented address space of up to 16 fragments per external Subordinate*.
Functional Description	Table 2.2. Attributes Table: • changed the Selectable Values of AXI Subordinate Max Fragment count from *1-8* to *1-16*; • changed the Selectable Values of External Subordinate <M> fragment count from *1-8* to *1-16*.
Known Issues	Updated the known issues of the IP.

Revision 1.2, June 2023

Section	Change Summary
Attributes Summary	Table 2.2. Attributes Table: • changed the Default value of AXI User Width from *1* to *4*; • changed the Default value of AXI Manager Max no. of ID supports from *64* to *16*; • changed the Default value of External Manager No. of IDs <N> from *64* to *16*; • changed the Default value of External Manager Write accept<N> from *16* to *8*; • changed the Default value of External Manager Read accept<N> from *16* to *8*; • changed the Default value of External Subordinate Write Issue <M> from *16* to *8*; • changed the Default value of External Subordinate Read Issue <M> from *16* to *8*.
Appendix A. Resource Utilization	Changed *Other default configurations or common configurations* to *Other default configurations* in the Configuration column, showing common configurations are no longer used.
Appendix B.	Newly added this section.

Revision 1.1, November 2022

Section	Change Summary
All	Updated to use Manager and Subordinate keywords.
Introduction	Updated Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. Added Lattice Avant under Supported FPGA Family.
Appendix A. Resource Utilization	Added Resource Utilization for CertusPro-NX and Lattice Avant devices.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.0, May 2022

Section	Change Summary
All	Initial release

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