



PCIe Throughput Demo for Lattice Nexus-based FPGAs

User Guide

FPGA-UG-02147-1.3

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DMA	Direct Memory Access
BAR	Base Address Register
FDSOI	Fully Depleted Silicon on Insulator
FPGA	Field-Programmable Gate Array
GUI	Graphic User Interface
LED	Light-emitting diode
MIPI	Mobile Industry Processor Interface
PCIe	PCI Express
PHY	Physical Layer
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

1. Introduction

This guide describes how to setup and run the PCIe DMA Throughput demo using devices built on the Lattice Nexus™-platform devices, specifically, CrossLink™-NX family, Certus™-NX family, and CertusPro-NX™.

For CrossLink-NX family, the demo is targeted to the CrossLink-NX PCIe Bridge Board, which features the CrossLink-NX FPGA in the 400-ball caBGA package (LIFCL-40-8BG400C). For Certus-NX family, the demo is targeted towards the Certus-NX Versa Evaluation Board, which features the Certus-NX FPGA in the 256-ball caBGA package (LFD2NX-40-8BG256C). For CertusPro-NX, the demo is targeted to the CertusPro-NX Versa Evaluation Board, which features the CertusPro-NX FPGA in the LFG672 package. The above-mentioned FPGAs are built on the Nexus FPGA platform using low power 28 nm FDSOI technology.

This guide familiarizes you with the process of setting up your PCI Express development environment. It is assumed that you do not have any associated tools installed on your system.

The demo discussed in this document includes the PCI Express DMA Throughput Demo.

1.1. Learning Objectives

After completing the steps in this guide, you should be able to perform the following:

- Set up and install all applicable development tools and PCI Express demos;
- Establish communication between the FPGA and the system through the PCI Express link;
- Run the PCI Express DMA Throughput Demo, which allows you to initiate DMA read and write transactions, transferring data from the host to the FPGA and vice versa;
- Modify and rebuild the PCI Express DMA Throughput Demo;
- Become familiar with the software development tools and major design flow steps employed in this kit;
- Use other existing documentation in conjunction with this guide.

This document assumes that you have already installed the Lattice Radiant™ design software. This document covers some of the basic of function of Lattice Radiant software. If you would like to learn more about Lattice Radiant software, refer to the Lattice Radiant software Help system.

2. Hardware and Software Requirements

2.1. Hardware Requirements

To install the kit design and run the demo software, a computer with a PCI Express ×16, ×8, ×4, or ×1 slot is required. The computer must also have a USB port and be able to run the Lattice Radiant Software. All other hardware and drivers are included in the kit.

- Mini-USB to USB-A cable for programming the bitstream
- 12 V Power Adapter
- Evaluation Board
 - CrossLink-NX PCIe Bridge Board for CrossLink-NX family
 - Certus-NX Versa Evaluation Board for Certus-NX family
 - CertusPro-NX Versa Board for CertusPro-NX family

2.2. Software Requirements

The following software is required to obtain the expected results for the procedures described in this guide:

- Lattice Radiant Software 2.2 or later (available at the Lattice website Design Software and IP page).
- PCIe DMA Throughput Demo for Windows 10 or Linux
- Windows 10 or Ubuntu 18.04.6
- Bit file for the SPI Flash
- LIFCL_40_PClEBMD_throughput.bit for CrossLink-NX family
- LFD2NX_PClE_BMD.bit for Certus-NX family
- LFCPNX100_PClE_BMD.bit for CertusPro-NX family

3. Set Up the Demo

3.1. Hardware Setup

This section covers the steps in programming the demo to the SPI memory of the FPGA Board.

Make sure the board is plugged into a PCIe slot or connected to the 12 V input supply.

For CrossLink-NX device, if the board is plugged into the PCIe slot, external power is provided by the system, and SW2 should be in the *up* position to receive power from the PCIe slot. If external 12 V power is provided, then SW2 should be in the *down* position to receive power from the external 12 V connection. Connect the board to the PC running the Lattice Radiant software with the Mini USB Type A Cable as shown in Figure 3.1.

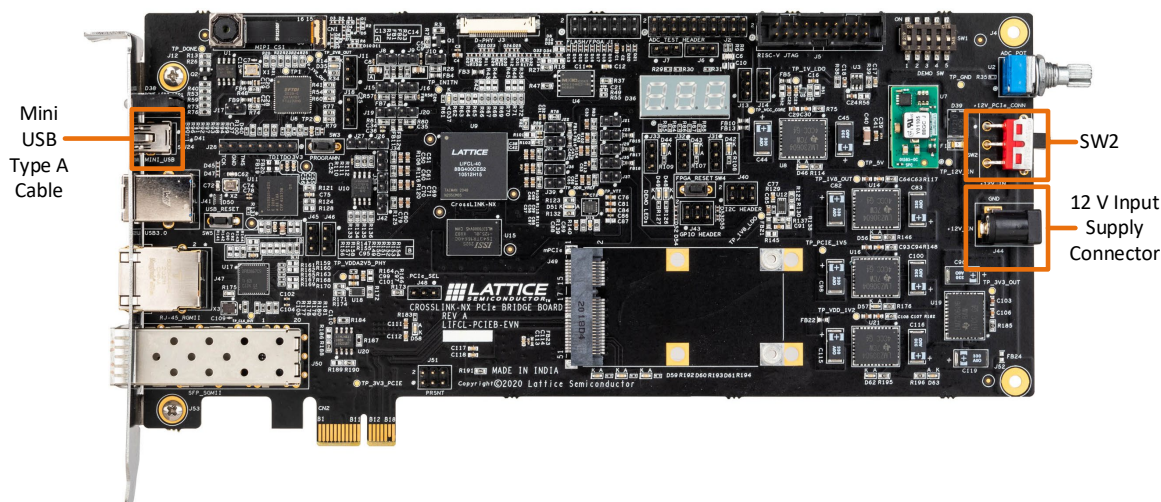


Figure 3.1. CrossLink-NX PCIe Bridge Board Connection

For Certus-NX device, there is no toggle switch to select the power source, and the board can be powered through the PCIe slot or from an external 12 V input supply. If the board is powered from the PCIe slot, the external 12 V input supply connector does not need to be connected. Connect the board to the PC running the Lattice Radiant software with the Mini USB Type A Cable as shown in Figure 3.2.

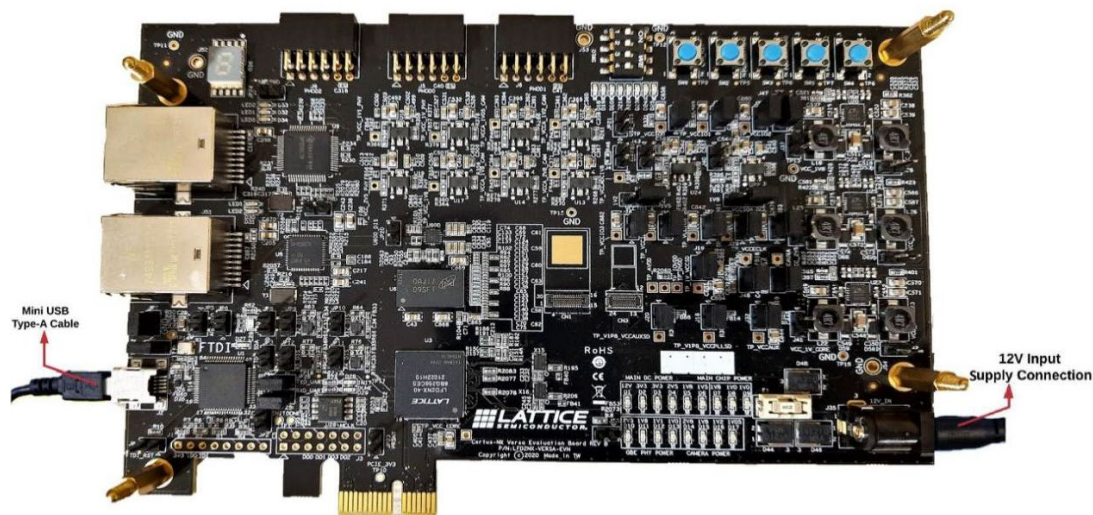


Figure 3.2 Certus-NX PCIe Versa Evaluation Board Connection

For CertusPro-NX, there are no jumpers to configure beyond the default. Refer to the [CertusPro-NX Versa Board User Guide \(FPGA-EB-02053\)](#) for a detailed list of jumpers on the board. When the board is plugged into the PCIe slot, external power is provided by the system, and SW6 should be in the up position to receive power from the PCIe slot. Connect the board to the PC running the Lattice Radiant software with the Mini USB Type A Cable as shown in [Figure 3.3](#).

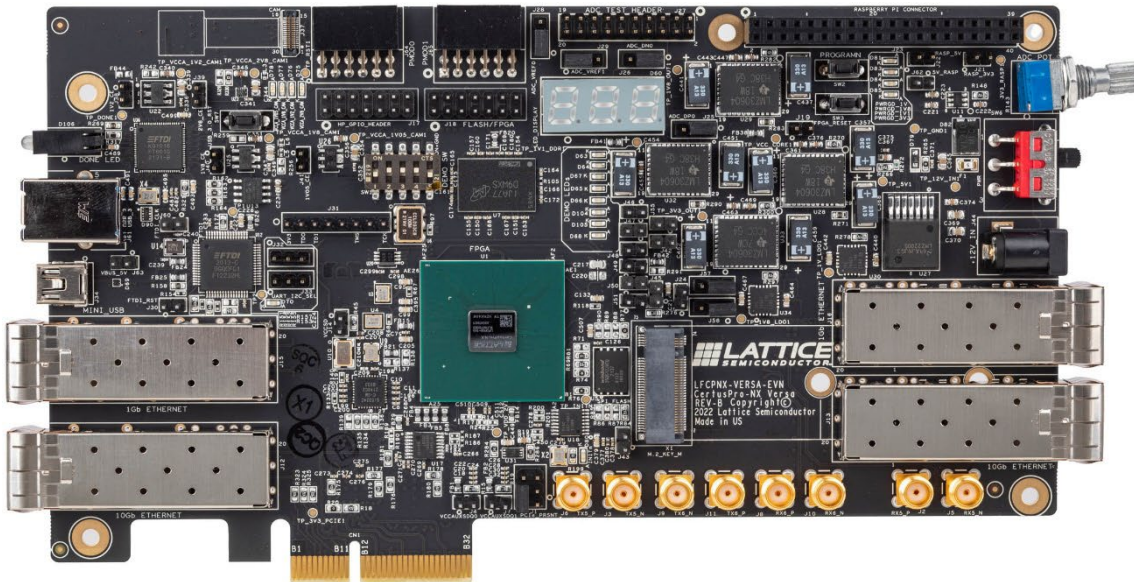


Figure 3.3. CertusPro-NX Versa Board Connection

3.1.1. Programming the FPGA

To program the FPGA device:

1. Create a new project using the Lattice Radiant Programmer software. In the **Getting Started** dialog box, indicate **Project Name** and **Location** as shown in [Figure 3.4](#).
2. Select Create a new project from a scan. Values are indicated in the Cable, Port, and TCK Divider Setting (0-30x) fields.
3. Click **OK**.

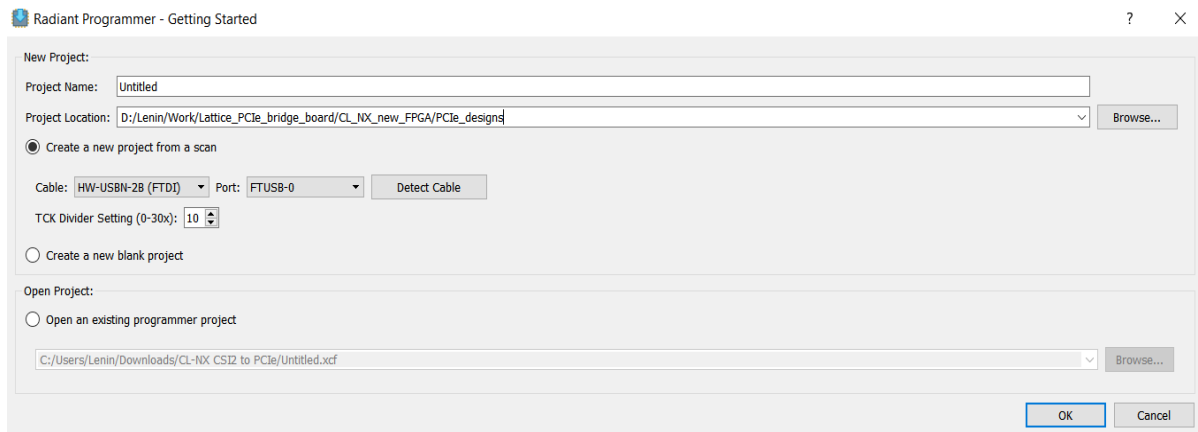


Figure 3.4. Creating a New Project from a Scan

4. The main interface opens as shown in [Figure 3.5](#).

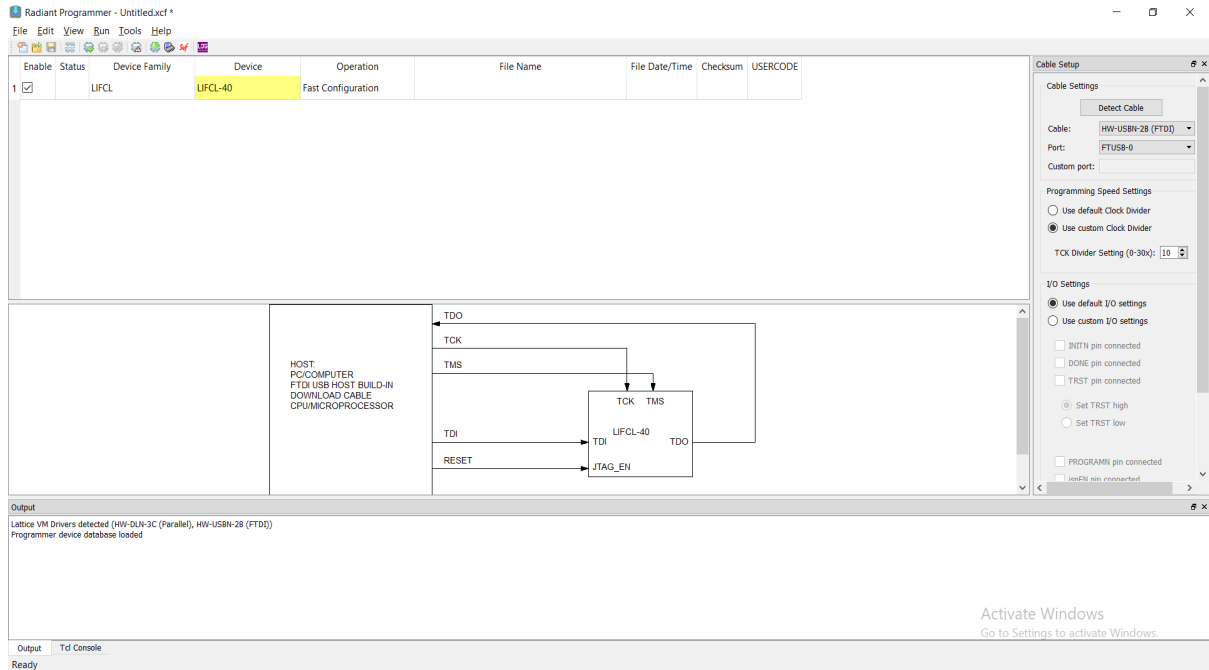


Figure 3.5. Radiant Programmer Window

5. Make sure the Programmer settings match the settings shown in [Figure 3.6](#) for CrossLink-NX device or [Figure 3.7](#) for Certus-NX device or [Figure 3.8](#) for CertusPro-NX device. If the settings do not match, select these settings manually from the drop-down menus.

Enable	Status	Device Family	Device	Operation	File Name	File Date/Time	Checksum	USERCODE
1	☒	LIFCL	LIFCL-40	Fast Configuration				

Figure 3.6. CrossLink-NX FPGA Device Settings

Enable	Status	Device Family	Device	Operation	File Name	File Date/Time	Checksum	USERCODE
1	☒	LFD2NX	LFD2NX-40	Fast Configuration				

Figure 3.7. Certus-NX FPGA Device Settings

Enable	Status	Device Family	Device	Operation	File Name	File Date/Time	Checksum	USERCODE
1	☒	LFCPNX	LFCPNX-100	Fast ...				

Figure 3.8. CertusPro-NX FPGA Device Settings

To select programming settings:

- Browse and select the Programming file.
 - For CrossLink-NX family, select LIFCL_40_PClEBMD_throghput.bit from CL-NX_BridgeBoard_PClE_BMD\Demonstration\Bitstream
 - For Certus-NX family, select LFD2NX_PClE_BMD.bit from CertusNX_PClE_BMD\Demonstration\Bitstream
 - For CertusPro-NX family, select LFCPNX100_PClE_BMD.bit from Demonstration\Bitstream
- Click **OK**.
- Double-click under **Operation** to open the **Device Properties** dialog box.
 - For CrossLink-NX family, select the settings as shown in [Figure 3.9](#) below.

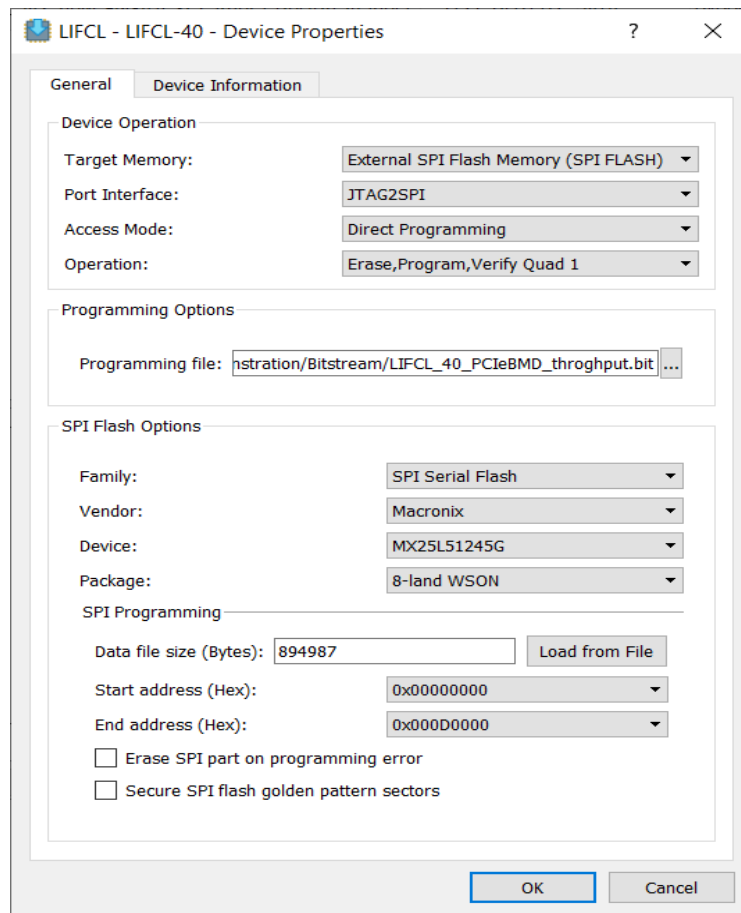


Figure 3.9. Device Properties Window for CrossLink-NX SPI Flash Programming

- For Certus-NX family, select the settings as shown in [Figure 3.10](#) below.

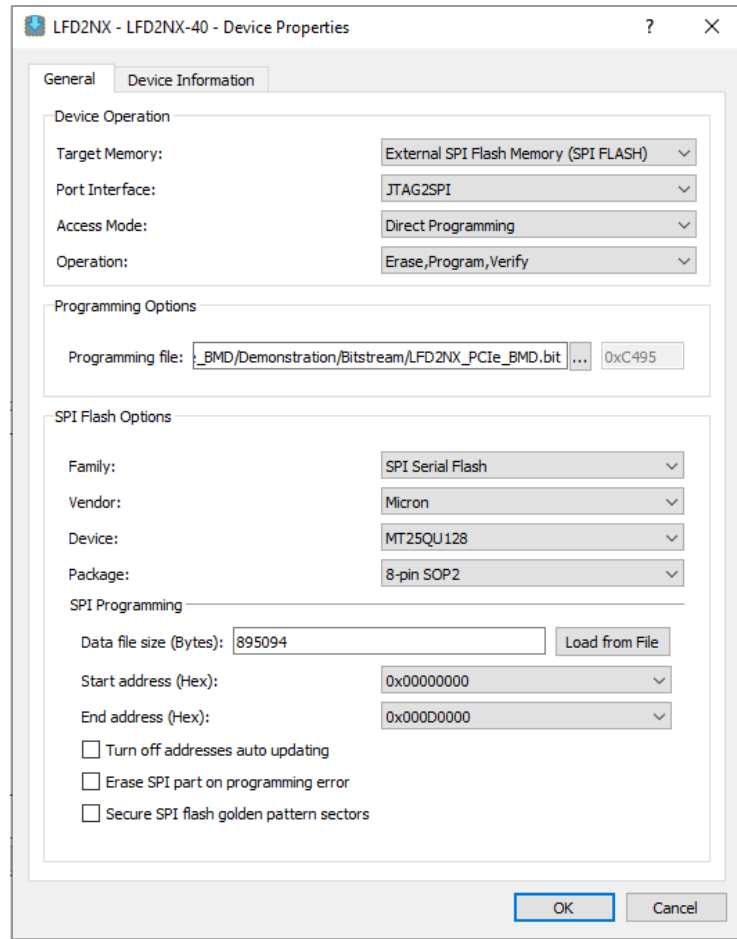


Figure 3.10. Device Properties Window for Certus-NX SPI Flash Programming

- For CertusPro-NX family, select the settings as shown in [Figure 3.11](#) below.

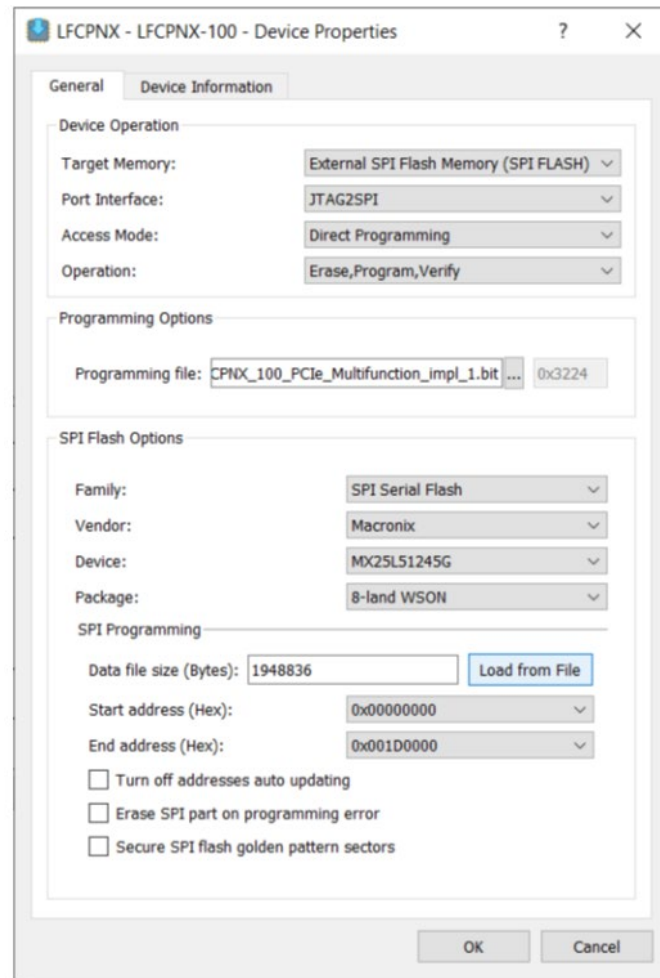


Figure 3.11. Device Properties Window for CertusPro-NX SPI Flash Programming (with Macronix Flash)

4. Click the **Programming** icon from the menu bar as shown in [Figure 3.12](#) to start programming.

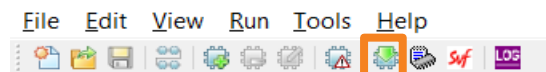


Figure 3.12. Programmer Menu Bar

When the FPGA programming is successful, the output console shows an Operation Successful message ([Figure 3.13](#)).

INFO - Execution time: 00 min : 28 sec

INFO - Elapsed time: 00 min : 32 sec

INFO - Operation: successful.

Output Tcl Console

Figure 3.13. Programmer Output Window

If the programming operation was not successful, refer to the [Troubleshooting](#) section of this document.

After programming, power cycle the board and check the status LEDs on the board. For CrossLink-NX family, refer to [Figure 3.14](#) and [Table 3.1](#). For Certus NX family, refer to [Figure 3.15](#). For CertusPro-NX family, refer to [Figure 3.16](#).

3.1.2. Status LED

For CrossLink-NX family, three status LEDs are shown (Figure 3.14).

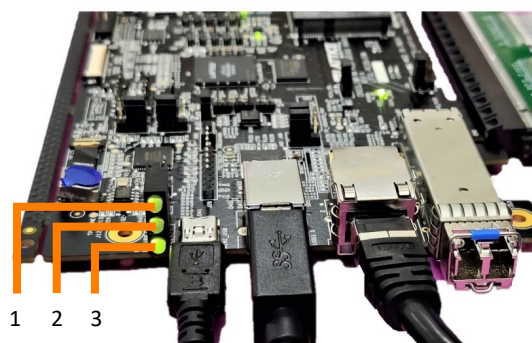


Figure 3.14. CrossLink-NX Status LED

The description of each status LED is provided in Table 3.1.

Table 3.1. CrossLink-NX Status LED Description

Sl. No	Name	Description
1	125 MHz Clock present	Green Blinking when clock presents.
2	PCIe Link Up	Green: Lights up if PCIe link up is successful.
		Red: Lights up if PCIe link up is not successful.
3	DONE	Green: Lights if configuration is successful.

For Certus-NX family, the programming done LED lights up green if configuration is successful. The LED is located at D29 on the board, as circled in orange in Figure 3.15.

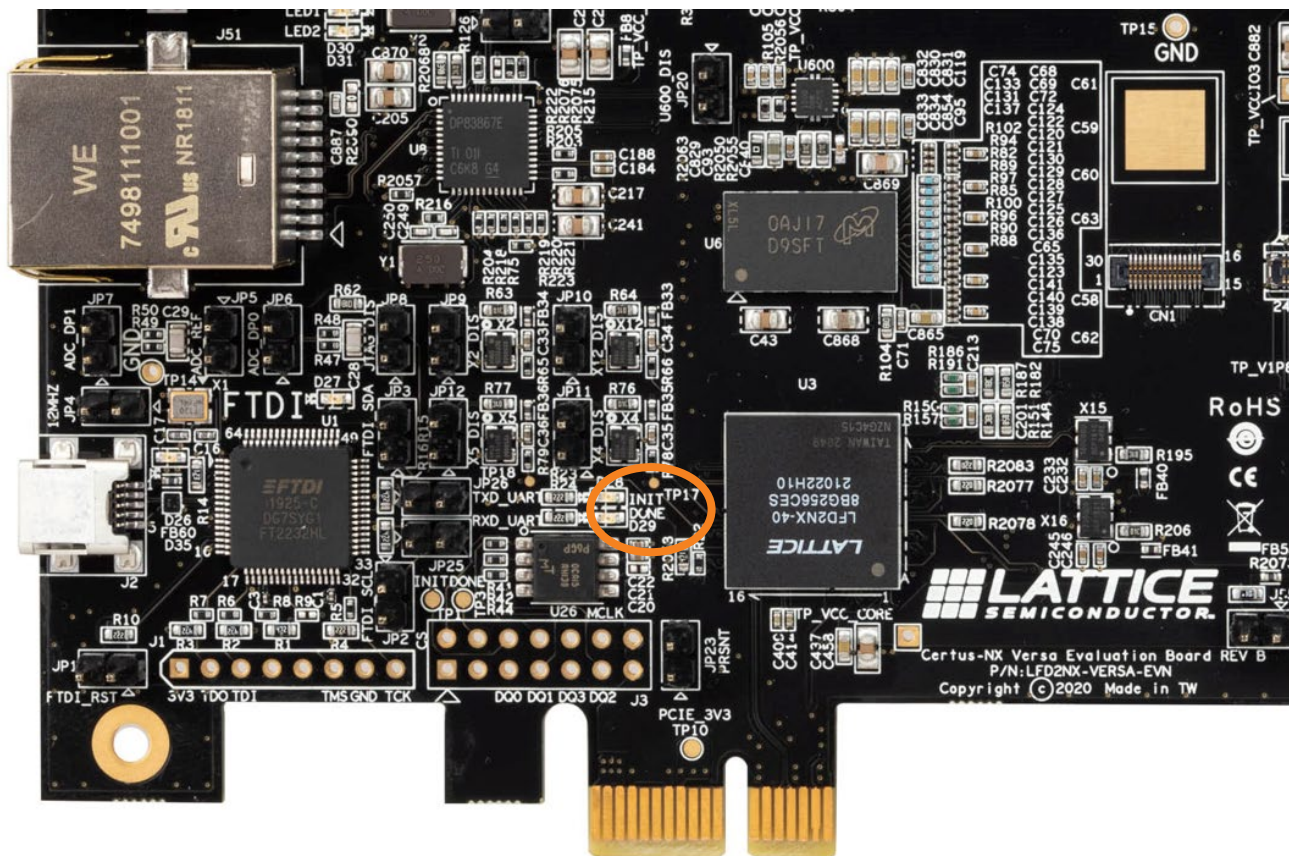


Figure 3.15 Certus-NX Programming Done LED

For CertusPro-NX, the programming done LED lights up in green if configuration is successful. The LED is located as shown in Figure 3.16.



Figure 3.16. CertusPro-NX Programming Done LED

3.2. Software Setup

This section provides the procedure for installing software onto the host machine.

3.2.1. Software Setup and Installation for Windows

Before installing the driver, driver signature enforcement should be disabled.

3.2.1.1. Disabling Driver Signature Enforcement Permanently

To permanently disable driver signature enforcement:

1. Start the Command Prompt as administrator.
2. Enter the following lines and press Enter.

```
bcdedit.exe -set loadoptions DISABLE_INTEGRITY_CHECKS
```

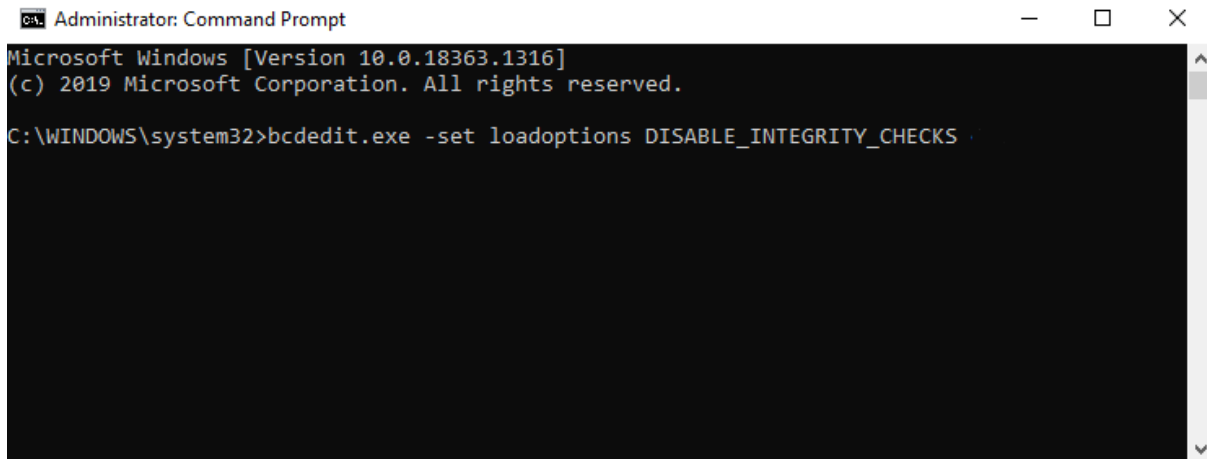


Figure 3.17. Running Disable Integrity Checks Command

```
bcdedit.exe -set TESTSIGNING ON
```

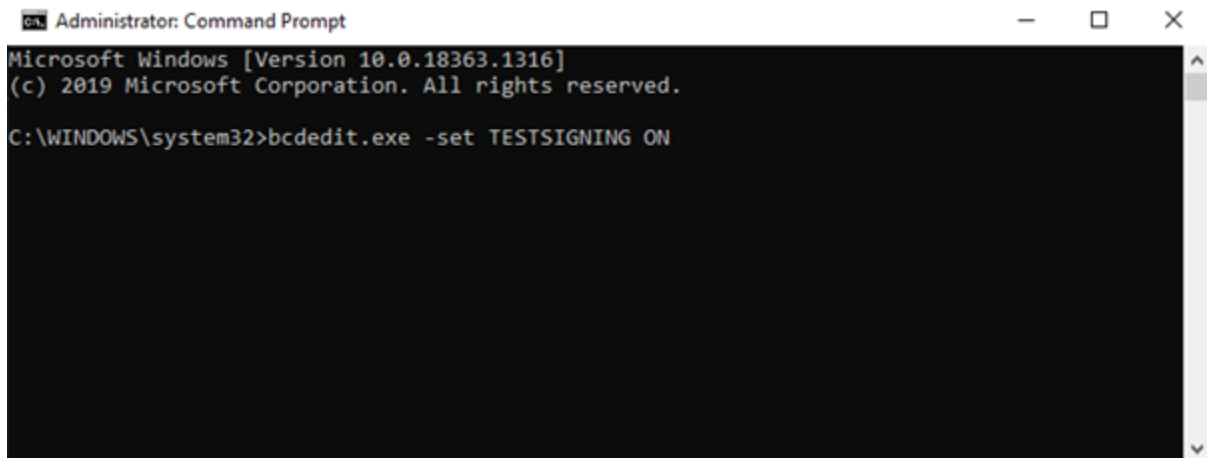


Figure 3.18. Running Test Sign On Command

3. Close the Command Prompt and restart your PC.

3.2.1.2. Disabling Driver Signature Enforcement Temporarily

To disable the driver signature enforcement temporarily on Windows 10:

Note: if Driver Signature Enforcement is already disabled, skip this section and proceed to the [Driver Installation](#) section.

1. Press the Windows key and click the power button.
2. Press and hold the Shift key and click **Restart**.
3. When the **Choose an option** screen appears as shown in [Figure 3.19](#), release the Shift key.
4. Click **Troubleshoot**.

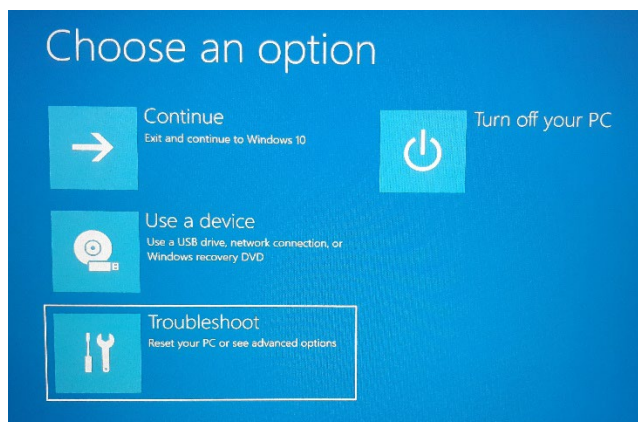


Figure 3.19. Troubleshoot Option

5. Select **Advanced options** and press Enter.

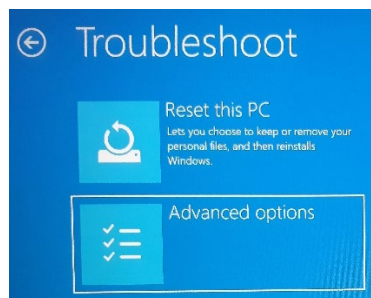


Figure 3.20. Advanced Options

6. Select **Startup Settings** and press Enter.



Figure 3.21. Select Startup Settings

7. Press Enter to restart.

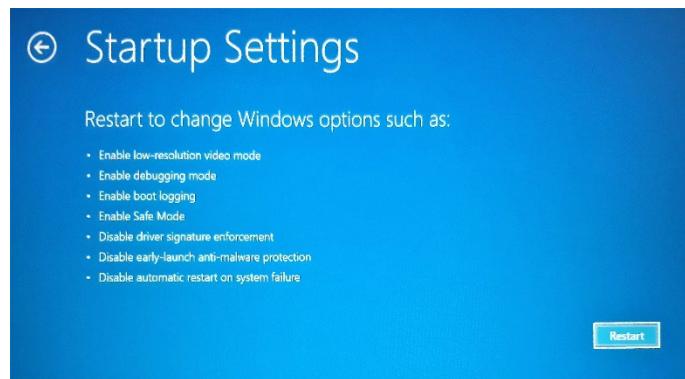


Figure 3.22. Restarting Windows

8. After restarting, select Option 7 to disable driver signature verification.

3.2.1.3. Driver Installation

There are two procedures to install the device driver:

- Install through user interface installer
- Install manually

Installing the DMA Throughput Demo Device Driver through the User Interface Installer

The DMA Throughput Demo device driver is installed during the installation of the user interface as described in the following section.

The Installer provides a standard packaging format for applications and a standard method for customizing the applications. The installer helps to install the CrossLink-NX PCIe Bridge Board DMA Throughput Demo application in your system.

The Framework supported version is Windows 10, WDF 1.25 or earlier.

To install the DMA Throughput Demo device driver through user interface:

1. In the *Demonstration\Windows10\Application* folder, double click *setup.exe*.
2. The Welcome page appears (Figure 3.23). Click **Next**.

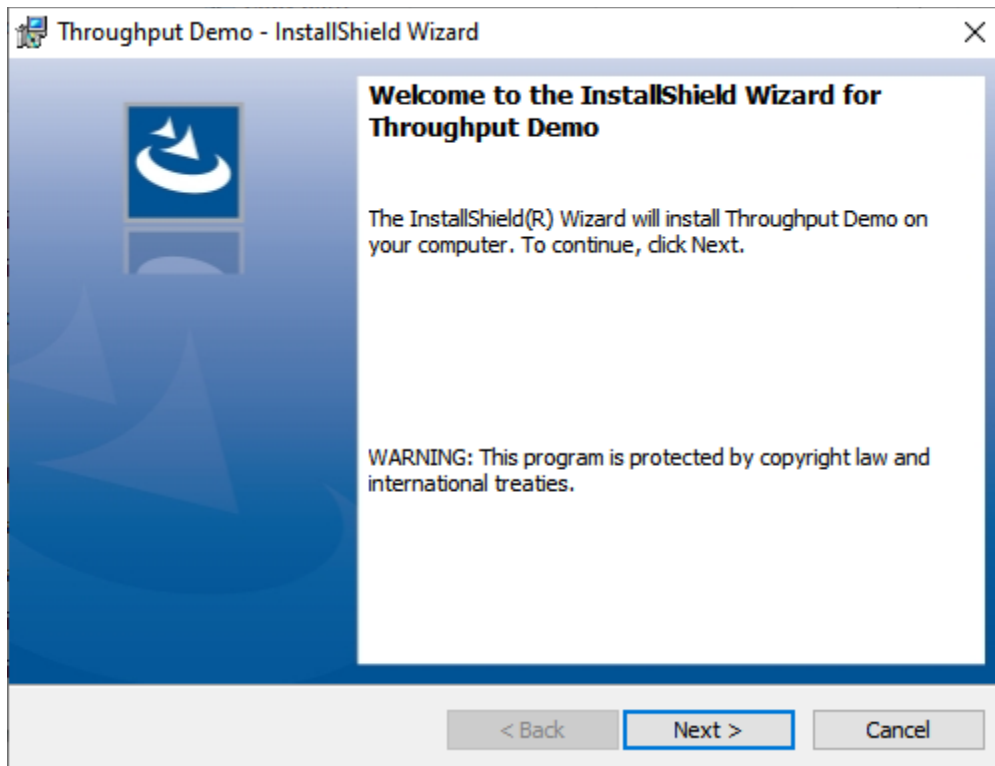


Figure 3.23. Welcome Page

3. Provide the location where you want to install the application (Figure 3.24). Click **Next**.

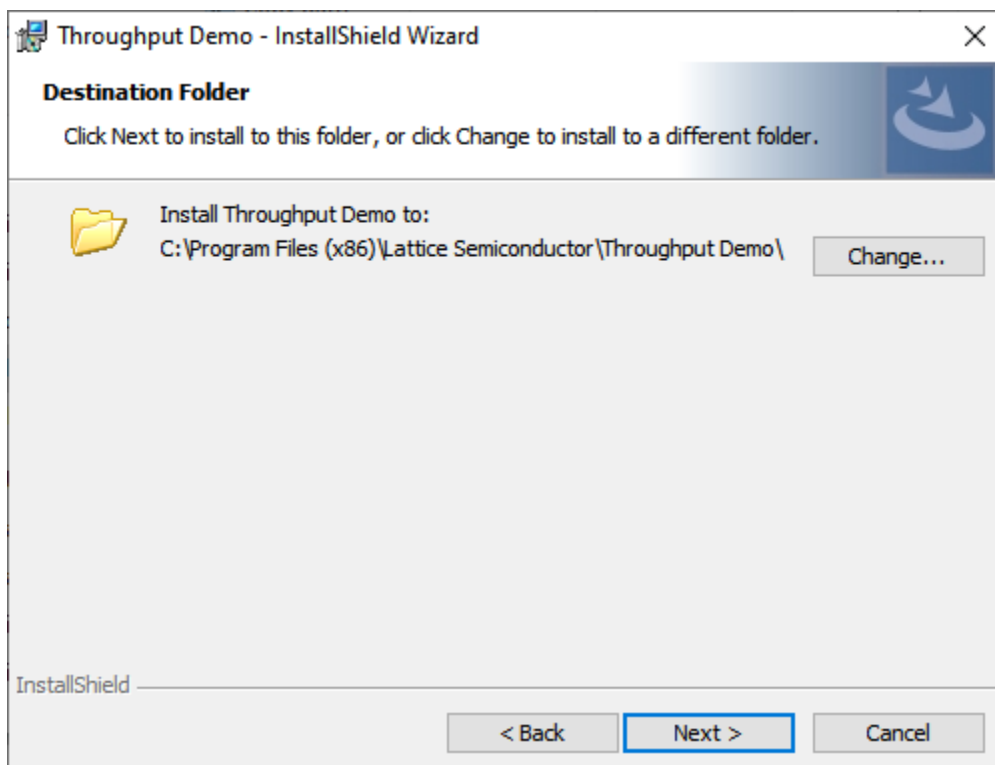


Figure 3.24. Destination Folder Page

4. The installation summary page is shown (Figure 3.25). Click **Install**.

Note: Administrative access is required to run this command.

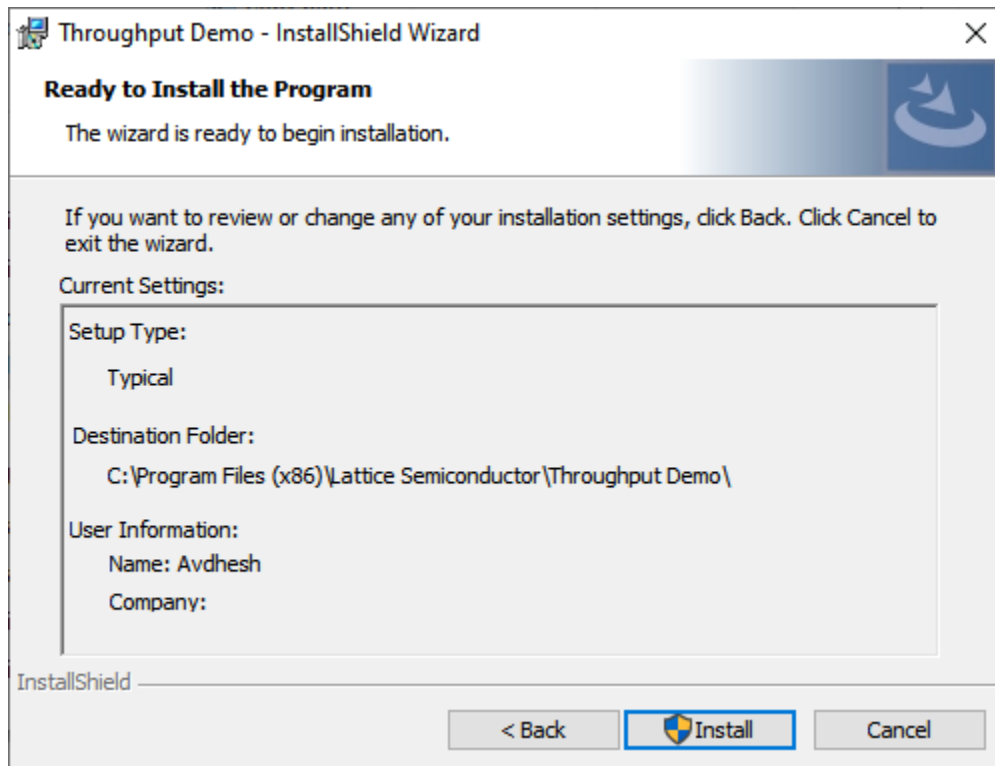


Figure 3.25. Summary Page

5. Installation of the DMA Throughput Demo application starts. When installation of the software is completed (Figure 3.26), the drivers are installed.

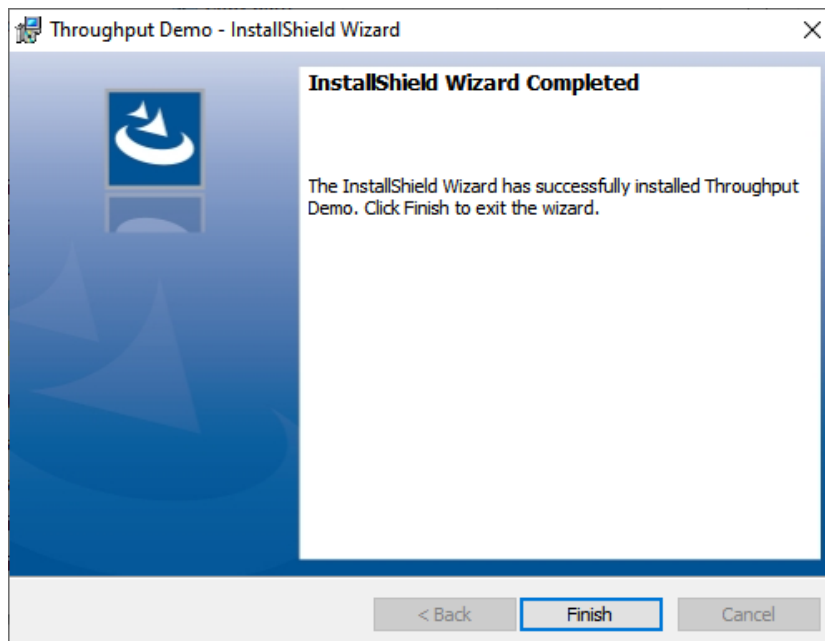


Figure 3.26. Application Installed

6. A message box appears (Figure 3.27). Click **Yes**.

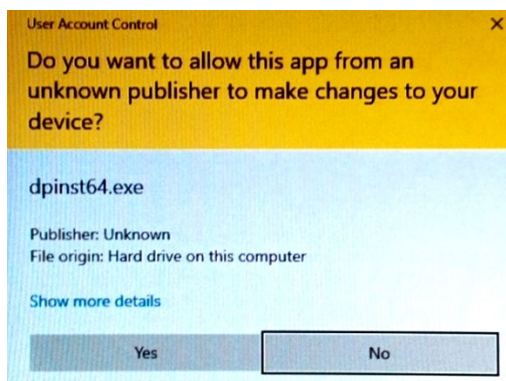


Figure 3.27. Device Configuration Prompt

7. The device driver installation wizard opens (Figure 3.28). Click **Next**.

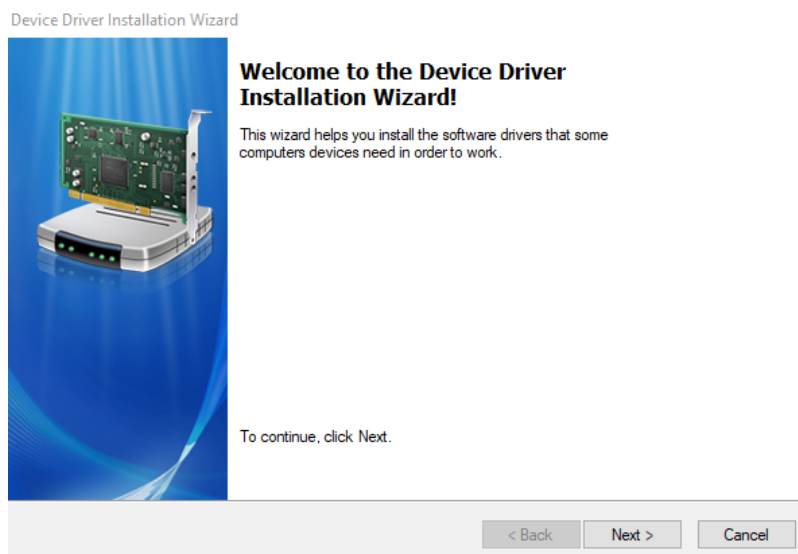


Figure 3.28. Device Driver Installation Wizard

8. If you receive a Windows Security prompt, select **Install this driver software anyway** as shown in Figure 3.29.

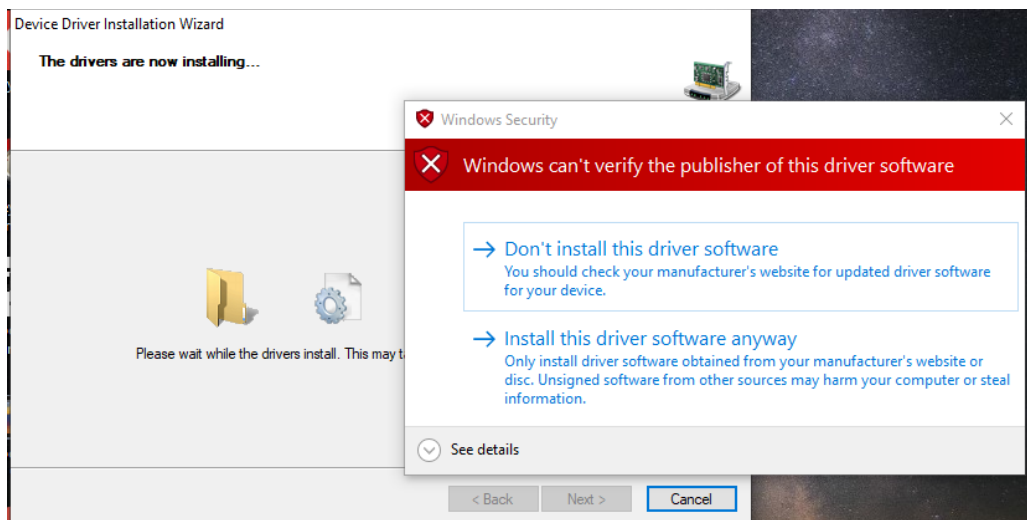


Figure 3.29. Windows Security in Driver Installation

9. If the driver is installed successfully, a message is displayed as shown in [Figure 3.30](#).

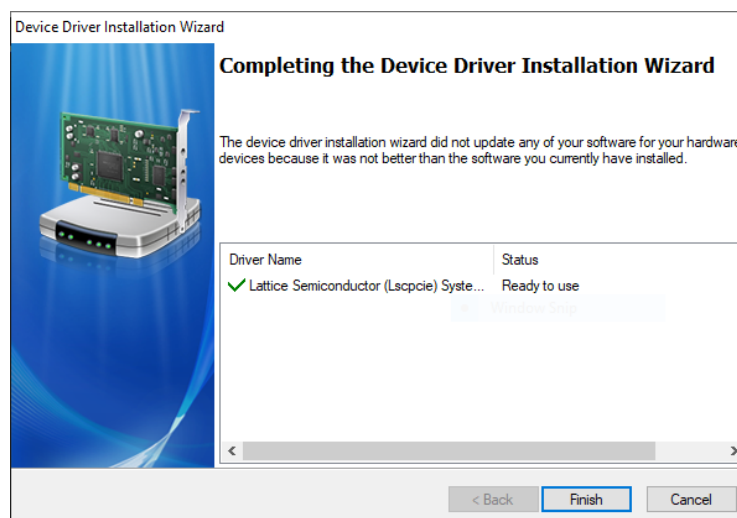


Figure 3.30. Device Driver Installation Completed

Installing DMA Throughput Demo Device Driver Manually

The drivers for the DMA Throughput Demo can also be installed manually. The drivers can be found in the *Demonstration > Windows10 > Driver* folder.

To install the device driver manually:

1. Open **Device Manager**, which shows the connected PCIe devices, as shown in [Figure 3.31](#).

Note: If the Device Manager does not show the connected PCIe device, see the [Troubleshooting](#) section.



Figure 3.31. Device Manager

2. Right-click the device and select **Properties** as shown in Figure 3.32.

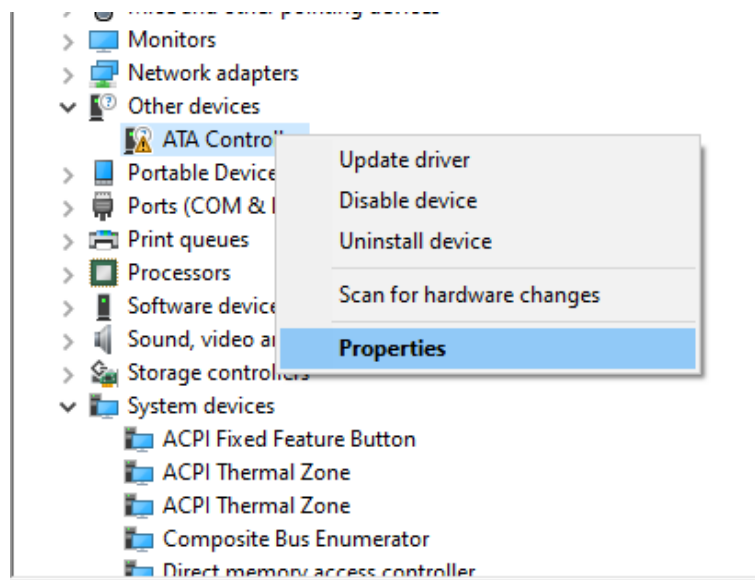


Figure 3.32. Showing Device Properties

3. The information in **Hardware IDs** is needed to install the correct driver for the corresponding device.
 - For CrossLink-NX family, the Hardware IDs of the Base System Device for the DMA Throughput Demo is `PCI\VEN_1204&DEV_9C1E&SUBSYS_E00419AA` as shown in [Figure 3.33](#).

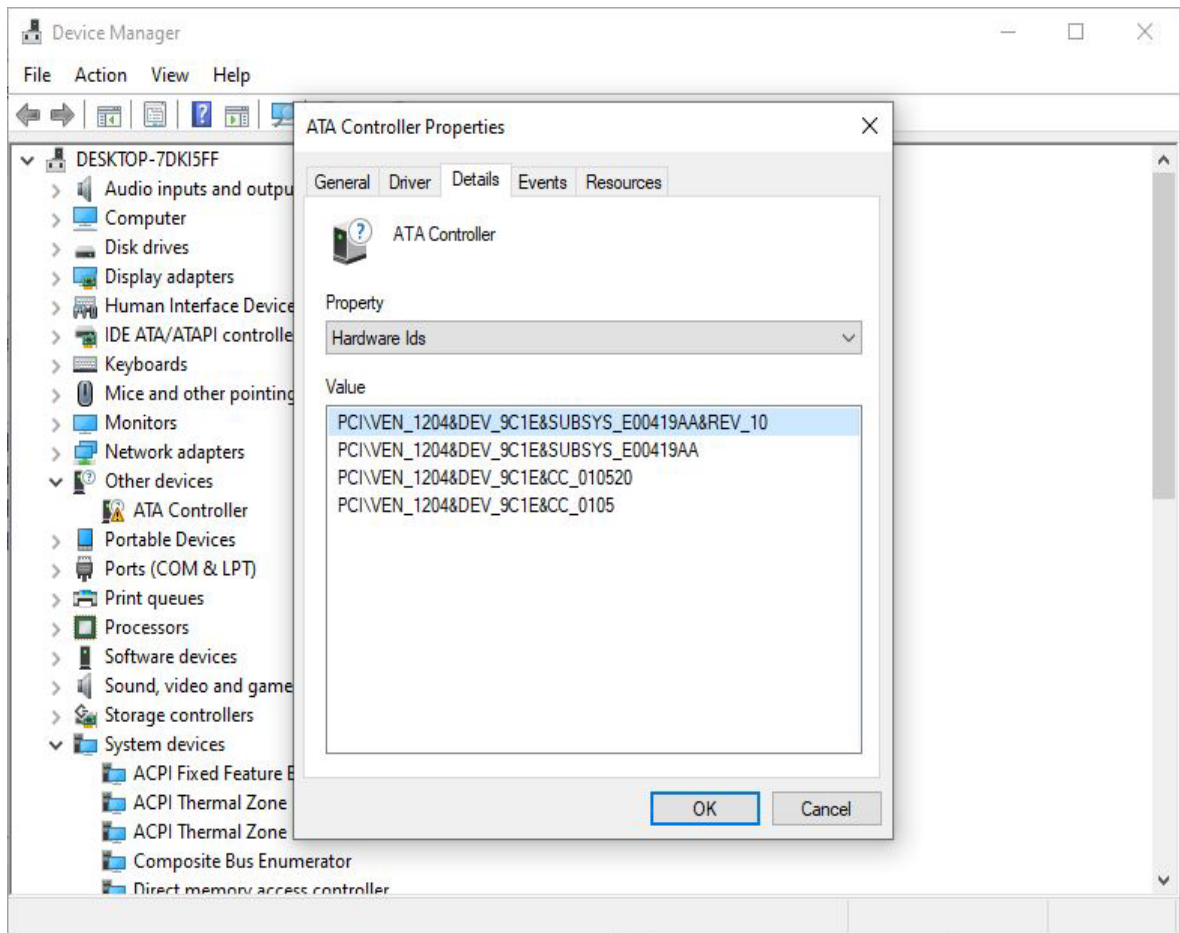


Figure 3.33. Hardware IDs of CrossLink-NX DMA Throughput Demo Device

- For Certus-NX family, the Hardware IDs of the Base System Device for the DMA Throughput Demo is `PCI\VEN_1204&DEV_9C2E&SUBSYS_E00419AA` as shown in [Figure 3.34](#).

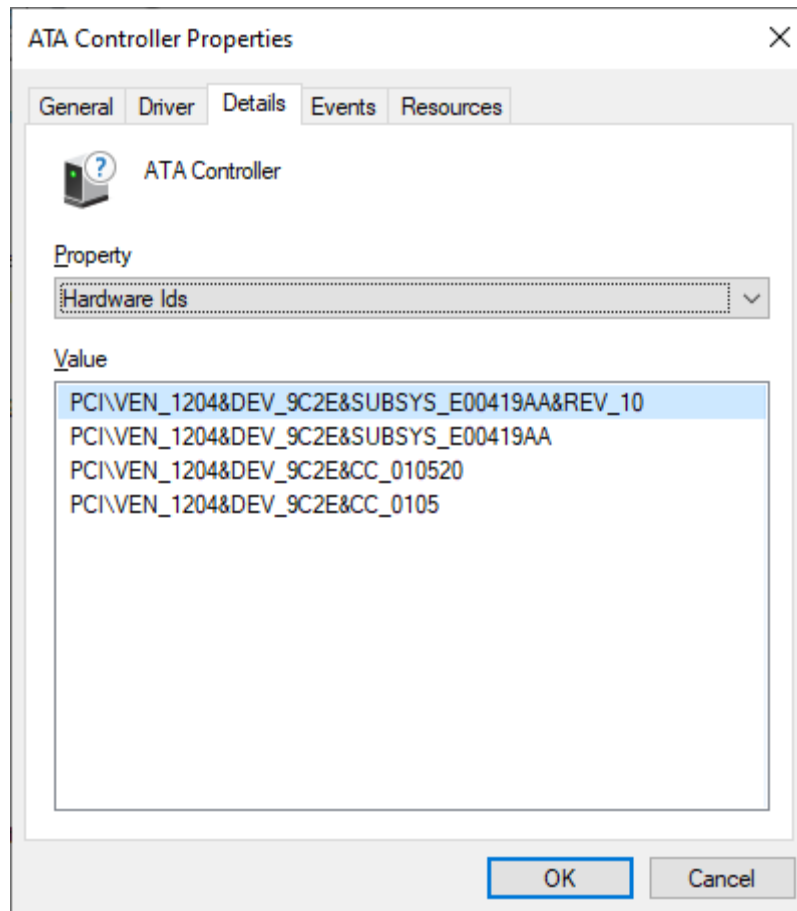


Figure 3.34. Hardware IDs of Certus-NX DMA Throughput Demo Device

- For CertusPro-NX family, the Hardware IDs of the Base System Device for the DMA Throughput Demo is PCI\VEN_1204&DEV_9C3E&SUBSYS_E00419AA as shown in [Figure 3.35](#).

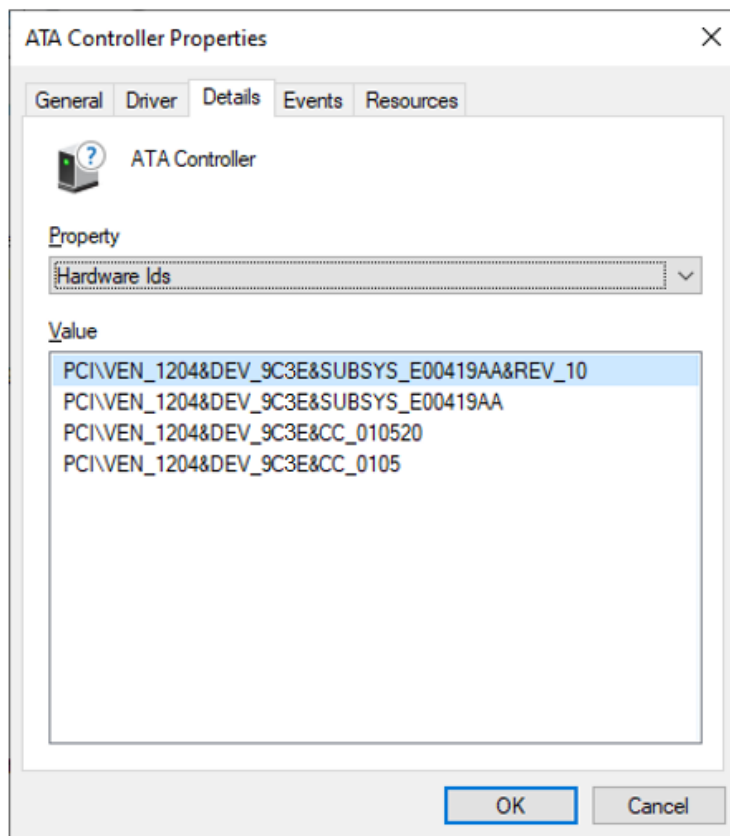


Figure 3.35. Hardware IDs of CertusPro-NX DMA Throughput Demo Device

4. Right click on the device and select **Update driver**.

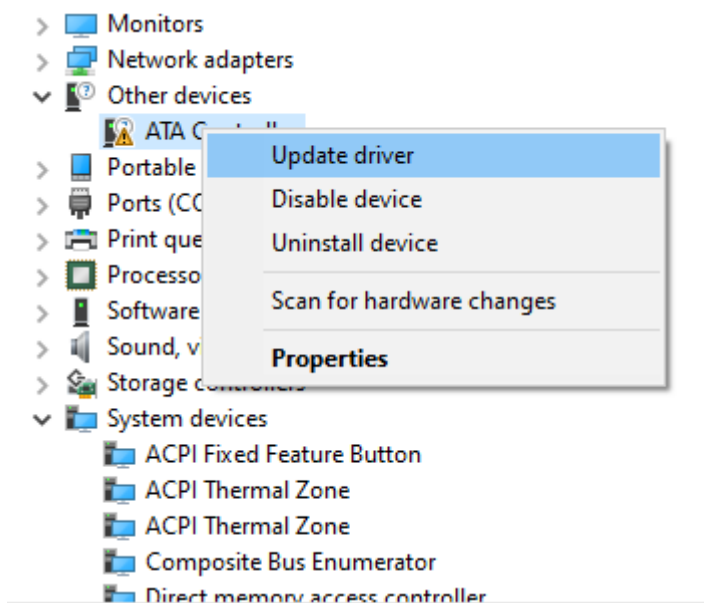


Figure 3.36. Update Driver Menu in Device Manager

5. Select the **Browse my computer for driver software** option as shown in Figure 3.37.

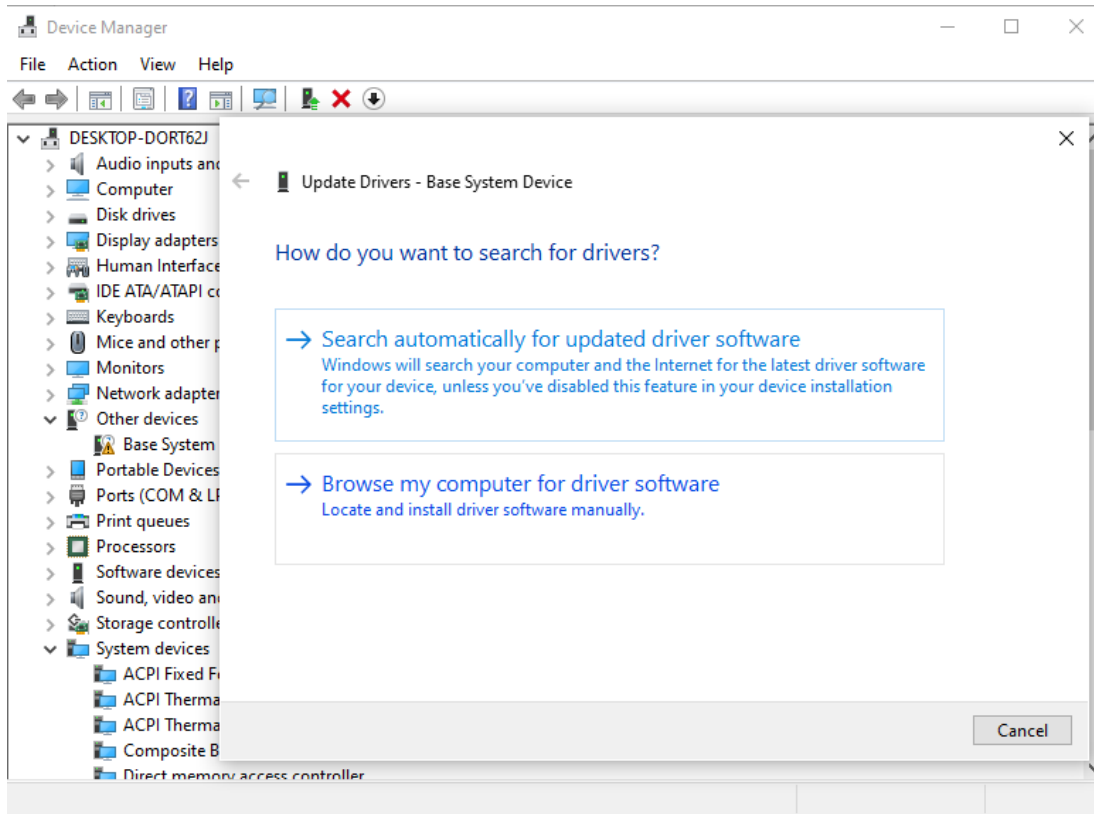


Figure 3.37. Update Driver Options

6. Browse for the DMA Throughput Demo device driver as shown in [Figure 3.38](#).

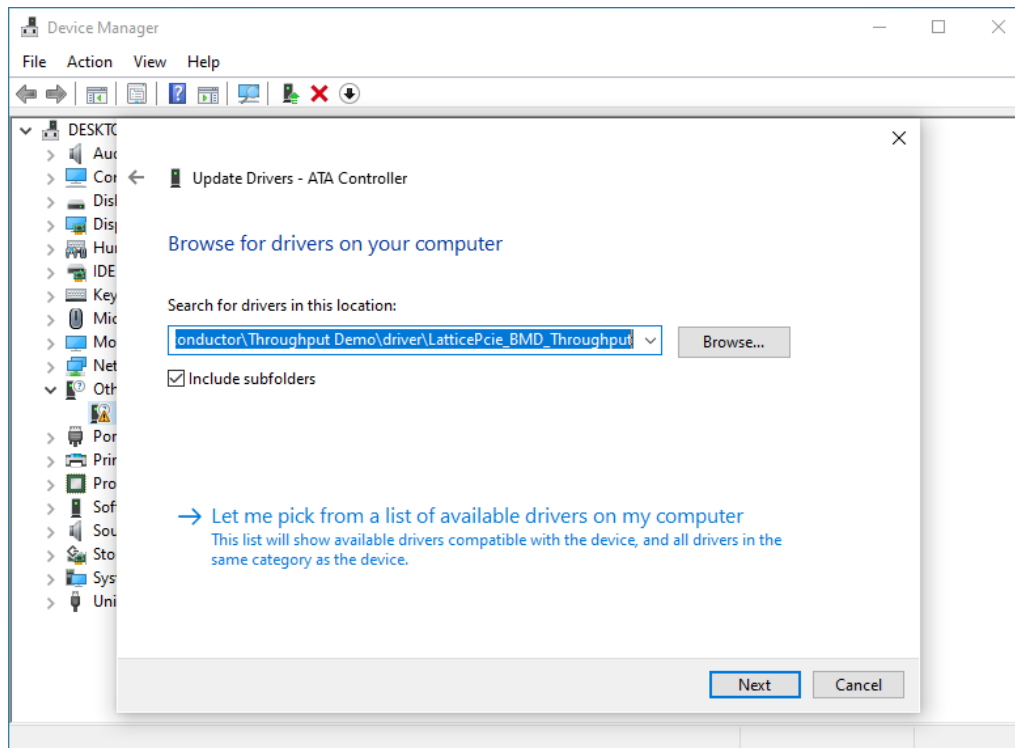


Figure 3.38. Browse the Driver for Device

7. If you receive a Windows Security prompt, select **Install this driver software anyway** as shown in [Figure 3.39](#).

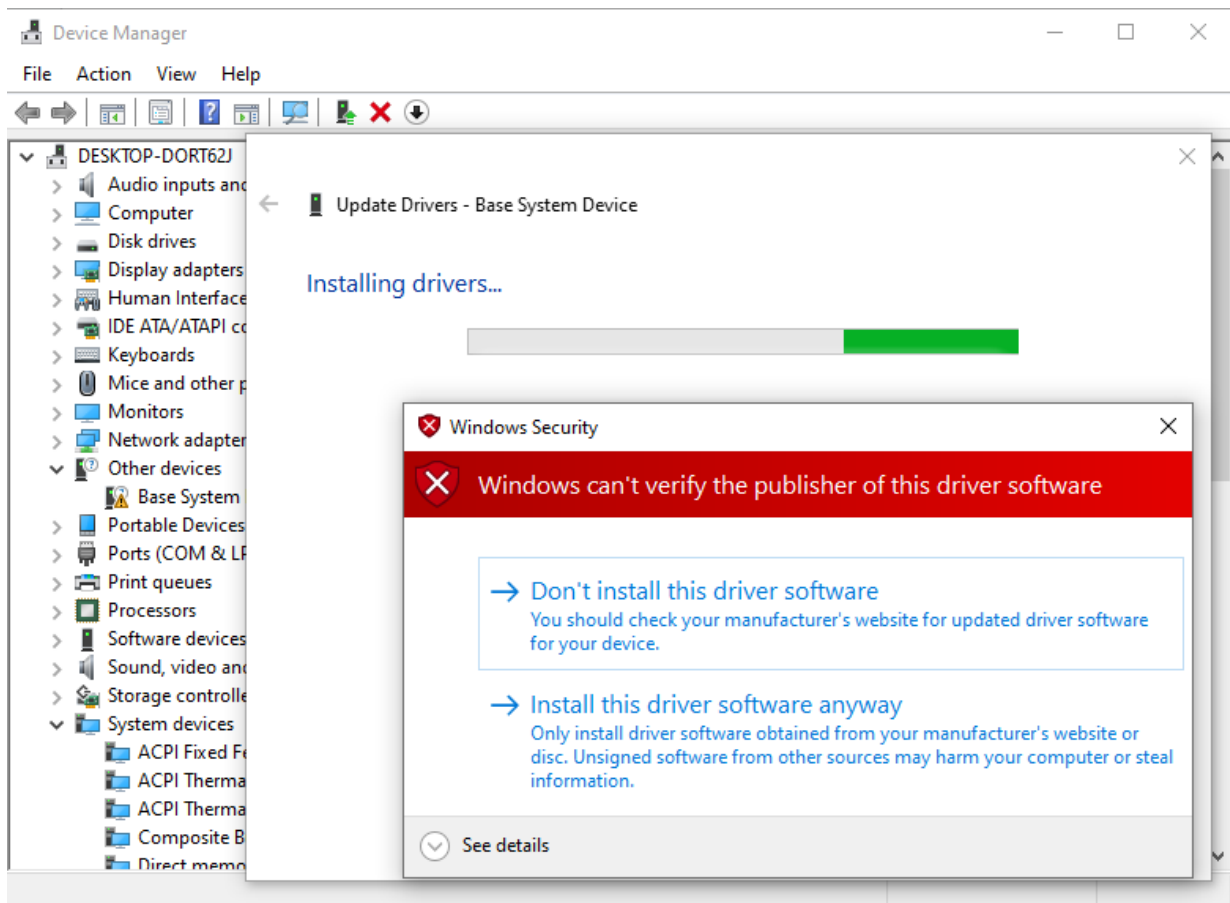


Figure 3.39. Windows Security in Device Manager

8. If the driver is installed successfully, a message is displayed as shown in [Figure 3.40](#) for CrossLink-NX family and [Figure 3.41](#) for Certus-NX family and [Figure 3.42](#) for CertusPro-NX family.

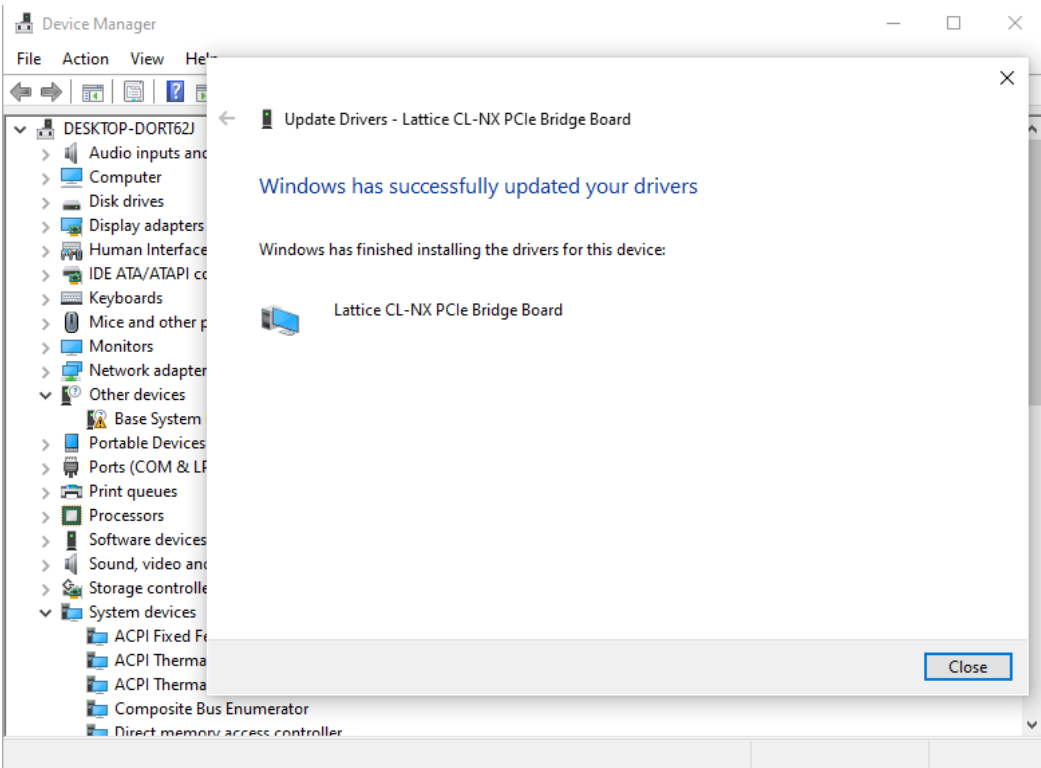


Figure 3.40. CrossLink-NX Driver Installation Status Message

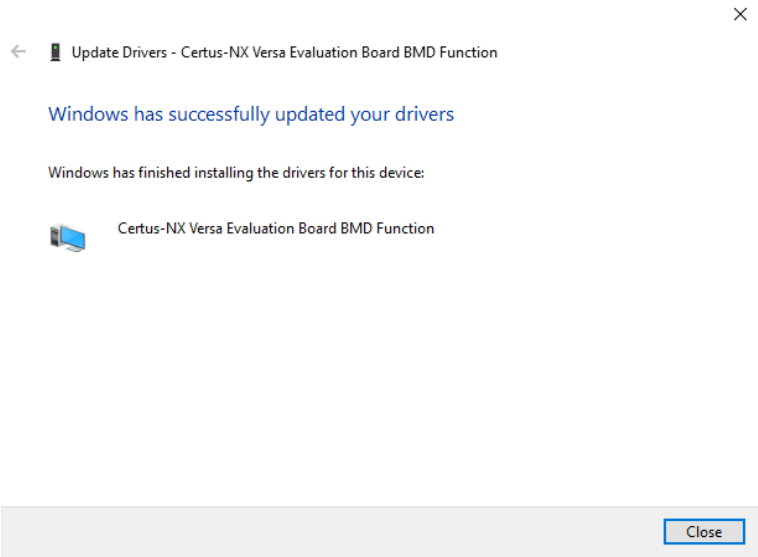


Figure 3.41. Certus-NX Driver Installation Status Message

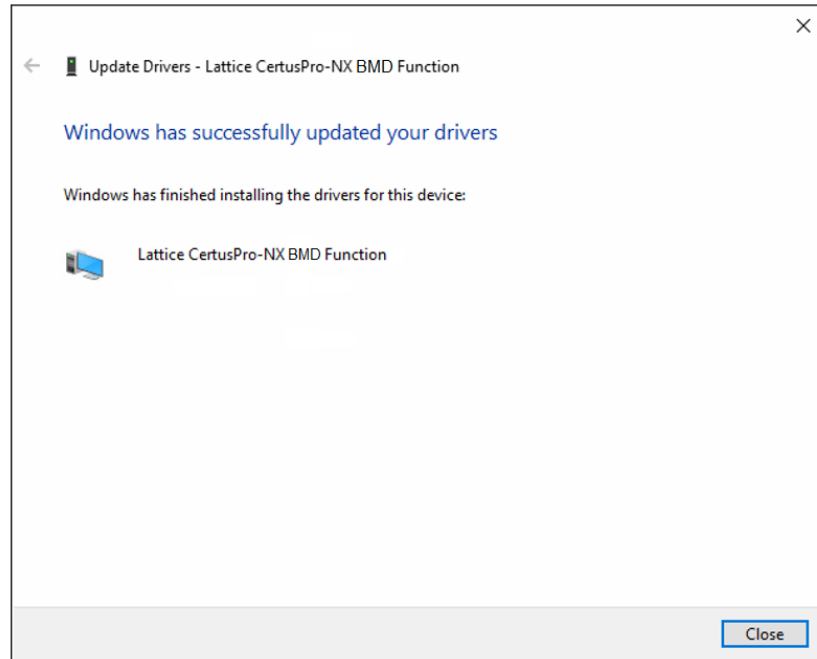


Figure 3.42. CertusPro-NX Driver Installation Status Message

- After the driver is installed, the device driver name is displayed in Device Manager, as shown in [Figure 3.43](#) for CrossLink-NX family, [Figure 3.44](#) for Certus-NX family, and [Figure 3.45](#) for CertusPro-NX family.

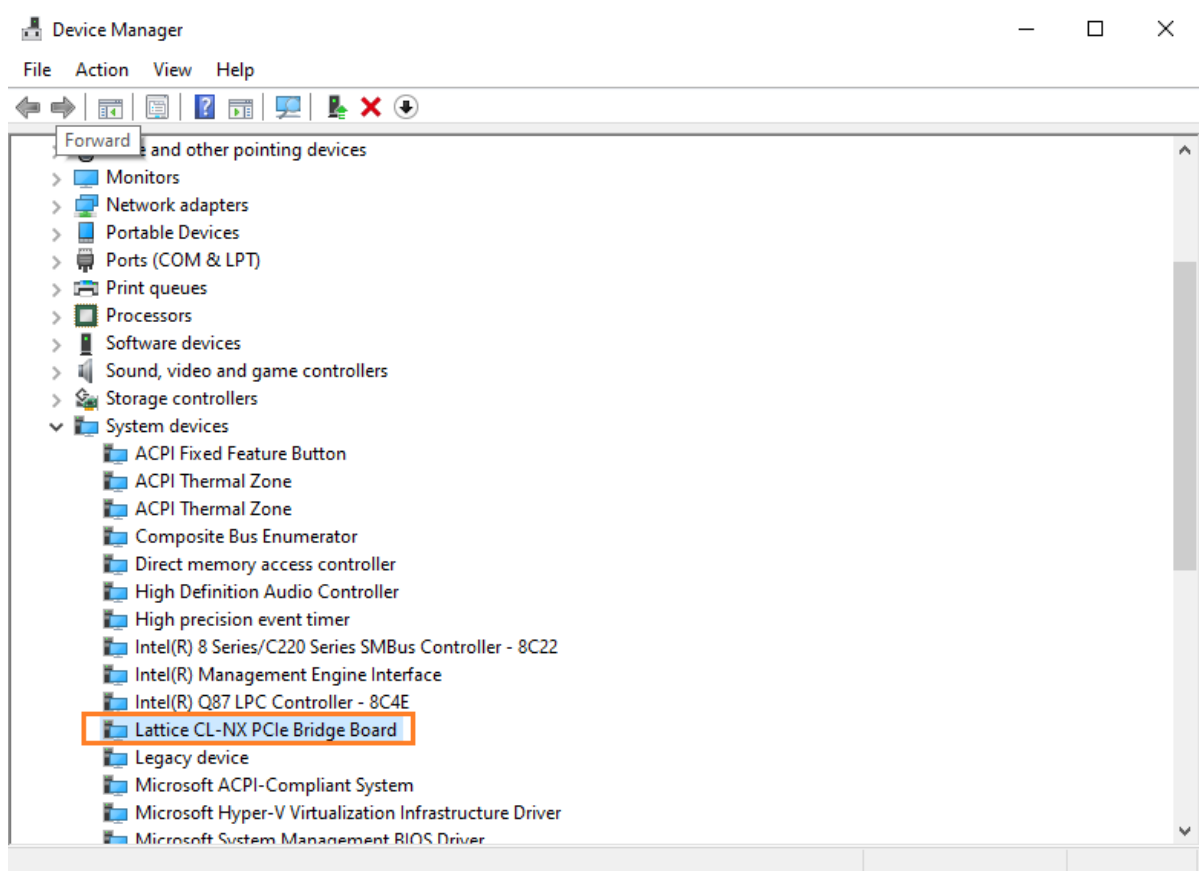


Figure 3.43. CrossLink-NX DMA Throughput Demo Device Name Displayed in Device Manager

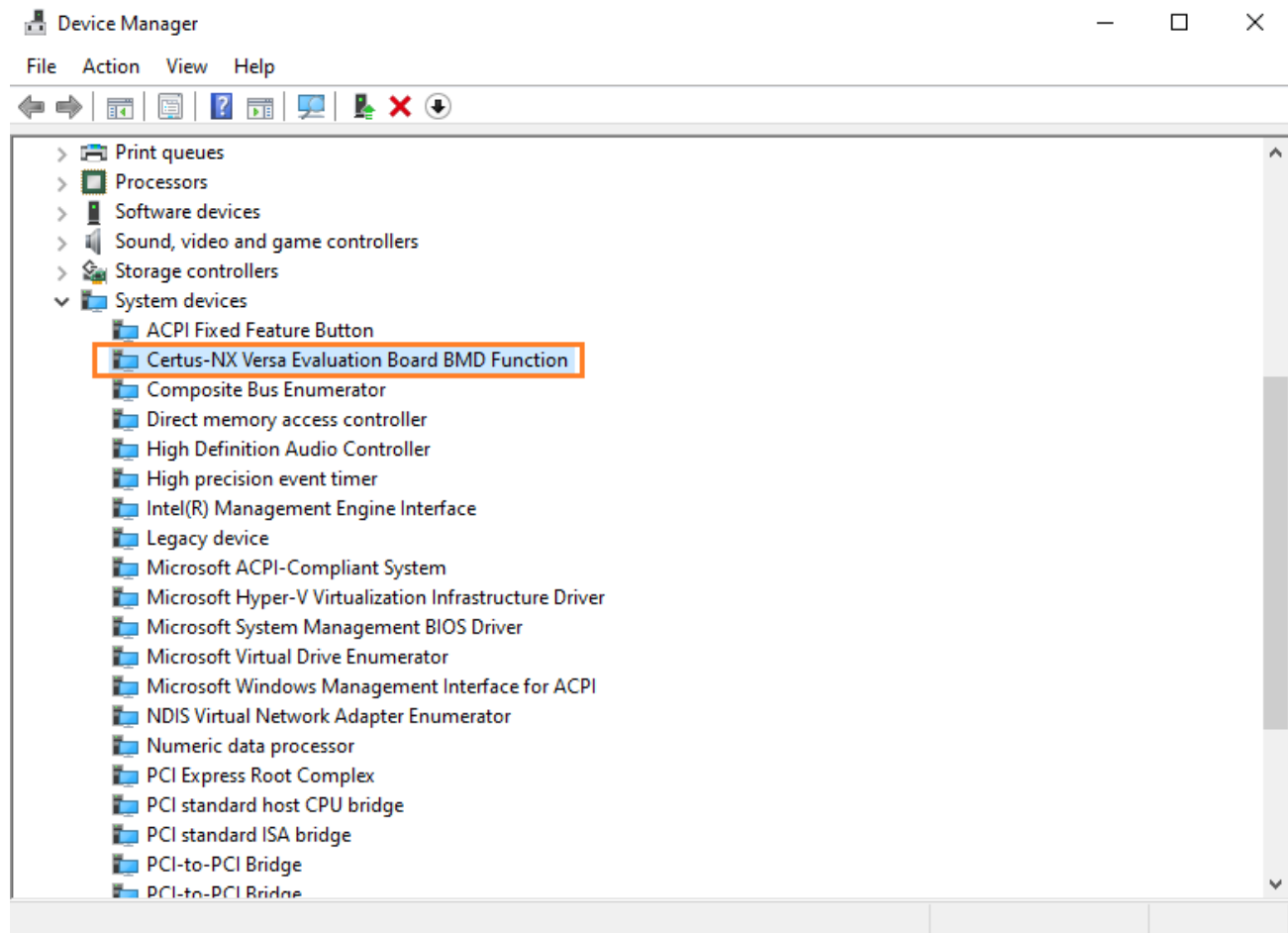


Figure 3.44. Certus-NX DMA Throughput Demo Device Name Displayed in Device Manager

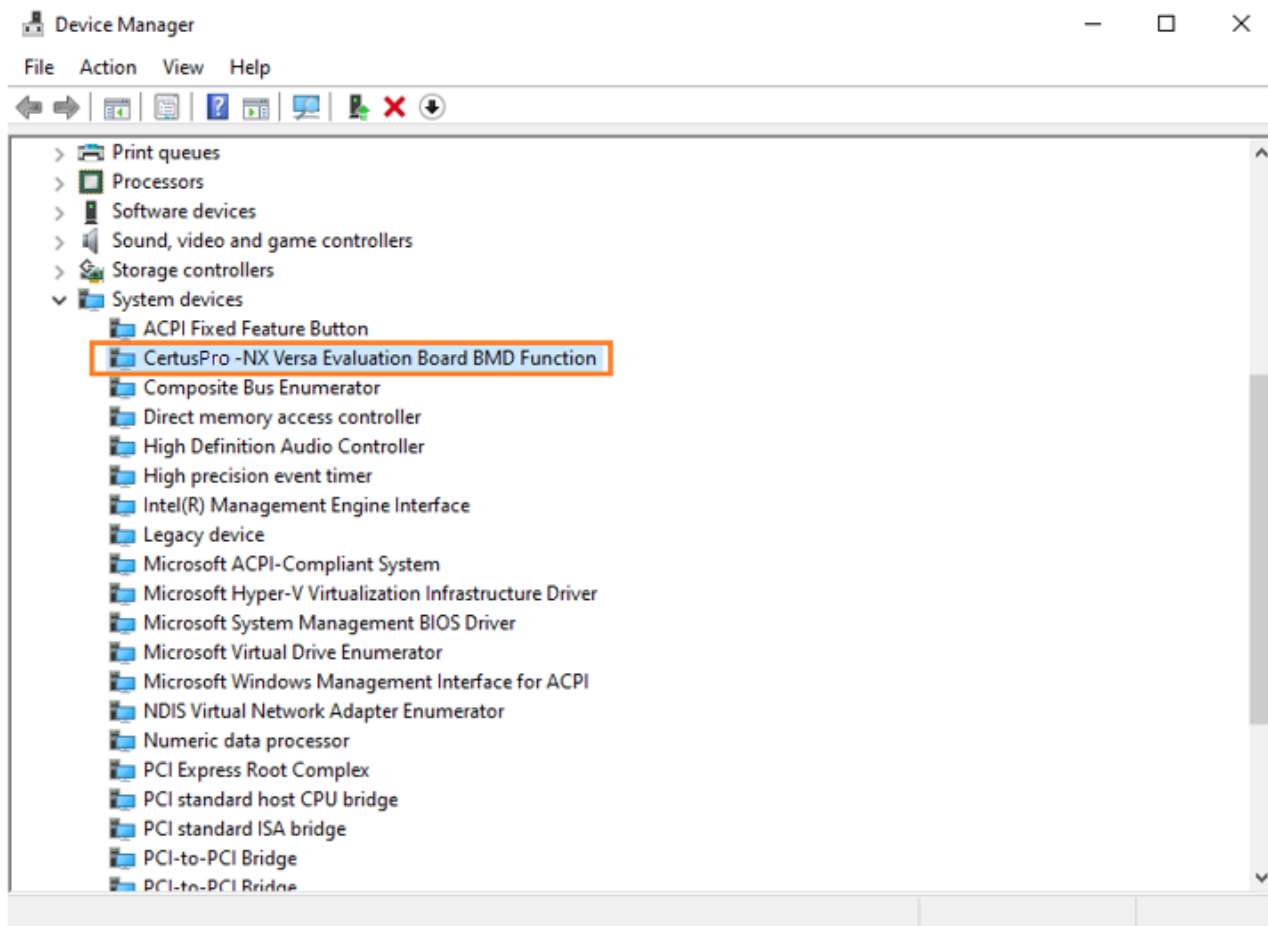


Figure 3.45. CertusPro-NX DMA Throughput Demo Device Name Displayed in Device Manager

3.2.2. Software Setup for Linux

3.2.2.1. Supported Operating System

- Distribution: Ubuntu
- Description: Ubuntu 18.04.6 LTS
- Release: 18.04.6
- OS Type: 64 bit.
- Codename: bionic

3.2.2.2. Required Packages

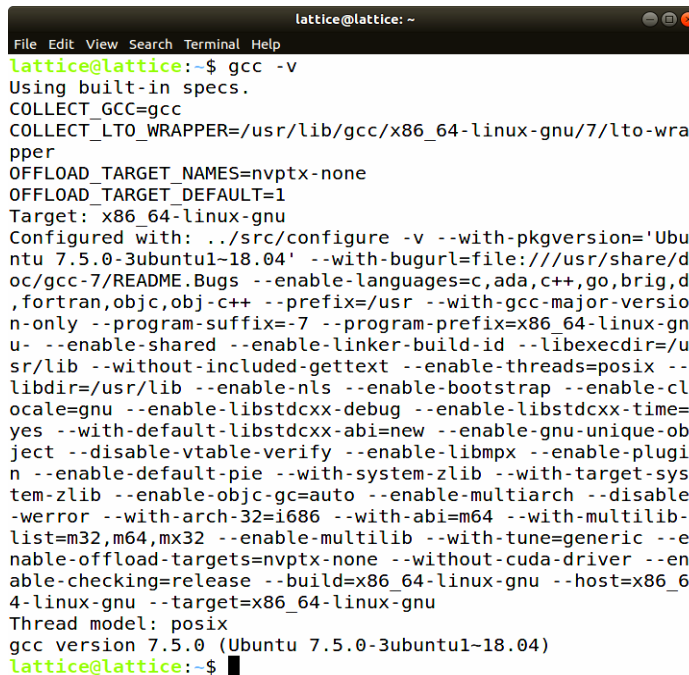
To check whether the required packages are installed or not, run the following commands on a terminal as shown below.

```
make
```



```
lattice@lattice: ~  
File Edit View Search Terminal Help  
lattice@lattice:~$ make -v  
GNU Make 4.1  
Built for x86_64-pc-linux-gnu  
Copyright (C) 1988-2014 Free Software Foundation, Inc.  
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>  
This is free software: you are free to change and redistribute it.  
There is NO WARRANTY, to the extent permitted by law.  
lattice@lattice:~$
```

```
gcc
```



```
lattice@lattice: ~  
File Edit View Search Terminal Help  
lattice@lattice:~$ gcc -v  
Using built-in specs.  
COLLECT_GCC=gcc  
COLLECT_LTO_WRAPPER=/usr/lib/gcc/x86_64-linux-gnu/7/lto-wrapper  
OFFLOAD_TARGET_NAMES=nvptx-none  
OFFLOAD_TARGET_DEFAULT=1  
Target: x86_64-linux-gnu  
Configured with: ../src/configure -v --with-pkgversion='Ubuntu 7.5.0-3ubuntu1~18.04' --with-bugurl=file:///usr/share/doc/gcc-7/README.Bugs --enable-languages=c,ada,c++,go,brig,d,fortran,objc,obj-c++ --prefix=/usr --with-gcc-major-version-only --program-suffix=-7 --program-prefix=x86_64-linux-gnu- --enable-shared --enable-linker-build-id --libexecdir=/usr/lib --without-included-gettext --enable-threads=posix --libdir=/usr/lib --enable-nls --enable-bootstrap --enable-clocale=gnu --enable-libstdcxx-debug --enable-libstdcxx-time=yes --with-default-libstdcxx-abi=new --enable-gnu-unique-object --disable-vtable-verify --enable-libmpx --enable-plugin --enable-default-pie --with-system-zlib --with-target-system-zlib --enable-objc-gc=auto --enable-multiarch --disable-werror --with-arch=32=i686 --with-abi=m64 --with-multilib-list=m32,m64,mx32 --enable-multilib --with-tune=generic --enable-offload-targets=nvptx-none --without-cuda-driver --enable-checking=release --build=x86_64-linux-gnu --host=x86_64-linux-gnu --target=x86_64-linux-gnu  
Thread model: posix  
gcc version 7.5.0 (Ubuntu 7.5.0-3ubuntu1~18.04)  
lattice@lattice:~$
```

```
g++
```

```
lattice@lattice: ~
File Edit View Search Terminal Help
lattice@lattice:~$ g++ -v
Using built-in specs.
COLLECT_GCC=g++
COLLECT_LTO_WRAPPER=/usr/lib/gcc/x86_64-linux-gnu/7/lto-wrapper
OFFLOAD_TARGET_NAMES=nvptx-none
OFFLOAD_TARGET_DEFAULT=1
Target: x86_64-linux-gnu
Configured with: ../src/configure -v --with-pkgversion='Ubuntu 7
.5.0-3ubuntu1~18.04' --with-bugurl=file:///usr/share/doc/gcc-7/R
EADME.Bugs --enable-languages=c,ada,c++,go,brig,d,fortran,objc,o
bj-c++ --prefix=/usr --with-gcc-major-version-only --program-suf
fix=-7 --program-prefix=x86_64-linux-gnu- --enable-shared --enab
le-linker-build-id --libexecdir=/usr/lib --without-included-gett
ext --enable-threads=posix --libdir=/usr/lib --enable-nls --enab
le-bootstrap --enable-clocale=gnu --enable-libstdcxx-debug --ena
ble-libstdcxx-time=yes --with-default-libstdcxx-abi=new --enable
-gnu-unique-object --disable-vtable-verify --enable-libmpx --ena
ble-plugin --enable-default-pie --with-system-zlib --with-target
-system-zlib --enable-objc-gc=auto --enable-multiarch --disab
le-werror --with-arch=32=i686 --with-abi=m64 --with-multilib-list=m
32,m64,mx32 --enable-multilib --with-tune=generic --enable-offlo
ad-targets=nvptx-none --without-cuda-driver --enable-checking=re
lease --build=x86_64-linux-gnu --host=x86_64-linux-gnu --target=
x86_64-linux-gnu
Thread model: posix
gcc version 7.5.0 (Ubuntu 7.5.0-3ubuntu1~18.04)
lattice@lattice:~$
```

3.2.2.3. Packages Installation Steps

Run the following commands on a terminal to install the required packages:

```
sudo apt update
sudo apt install build-essential
sudo apt install flex
```

3.2.2.4. Automatic Setup and Installation

To setup the demo in automatic mode:

1. Go to the *Demonstration/Linux* directory.
2. Change the permission of the *install.sh* file by running *chmod* command.

```
sudo chmod 777 install.sh
```
3. Run the command below, which builds the driver and API library, install the driver, and launch the QT use interface application.

```
sudo ./install.sh
```
4. To uninstall the driver, go to the *Demonstration/Linux* directory and run the command below.

```
sudo ./uninstall.sh
```

3.2.2.5. Manual Setup and Installation

Before installing the driver, the driver must be built.

To build the driver:

1. Go to the *Demonstration* directory.
2. Run the following command on terminal.

```
sudo chmod 777 -R Linux
```

3. Go to the *Linux* directory.
4. Go to in *Source_Code* directory.
5. Run the following commands.

```
sudo make clean  
sudo make
```

This builds the driver and API library.

6. Make sure that the driver is not installed.
7. To remove an existing driver, run the following command in a terminal window:

```
sudo rmmod lthruput_main.ko
```

To install the driver:

1. Go to *drv_src/drvr/* directory.
2. Run the command below.

```
sudo lthruput_main.ko
```

3. To launch the user interface application, go to the *app_src/gui/deploy/* directory and run the command below.

```
sudo ./PCIeThruputDemo.sh
```

4. Demo Design Overview

4.1. Theory of Operation

The demo runs on a standard x64 PC and accesses the FPGA Board installed in a PCIe slot. [Figure 4.1](#) shows the relationship of the hardware and software components of the demo. The purpose of this demo is to show the performance of the Lattice PCI Express SERDES hardware and PCI Express Endpoint IP core when operating in a PC PCI Express expansion slot. The data rates for writes to the PC system memory and reads from the PC system memory are measured and displayed in a graphical user interface. The demo performs Direct Memory Access (DMA) operations with the FPGA acting as the bus master. Data is transferred directly to and from the PC memory. You can select the type of transfer to perform, for example, write, read, as well as how many bytes of data to transfer. You also have the option of selecting the size of the TLP in which to perform the transfer.

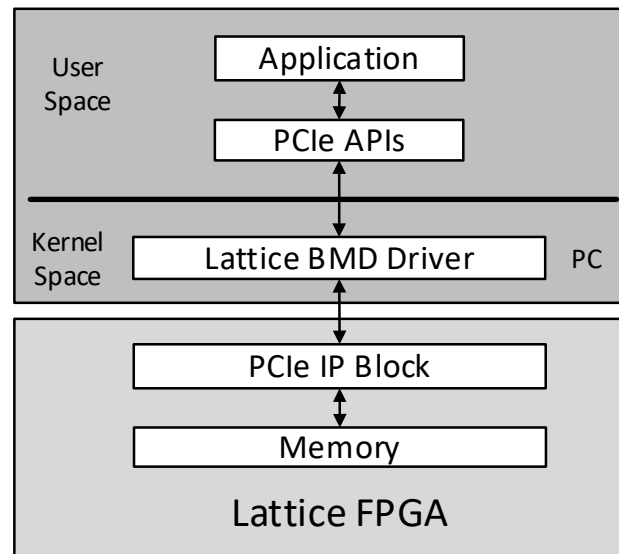


Figure 4.1. Relationship of the Hardware and Software Components

4.2. Design Overview

A user interface application is provided for demonstrating the PCIe DMA Throughput demo. Application software is developed using a layered architecture consisting of the following layers:

- GUI application
- Driver API
- Device Drivers
- Device Hardware (FPGA Design)

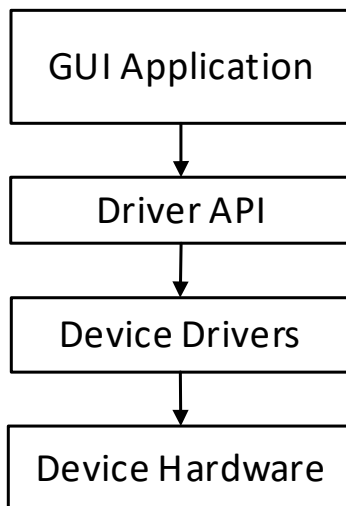


Figure 4.2. PCIe Throughput Demo SW Design

4.2.1. GUI Application

Demo applications are the demos that you actually run. The demos are "main ()" programs that instantiate classes in the API library to access and control the hardware. The throughput demo includes a GUI written in Qt, and demonstrates how to open a driver and send control plane read/writes to registers in the IP.

The GUI application uses the driver API to communicate with the device hardware. The Driver API is a C++ dynamic library which provides an interface to access the hardware.

4.2.2. Driver API

On Windows, the MemRwApis.dll library is a DLL that bridges the user space demo applications to the kernel space driver code and provides routines to control the IP modules.

On Linux, the library is named libmem_rw.so.

4.2.3. Device Drivers

The Hardware Drivers provide access to the Lattice PCIe board. On Windows, the LatticePcie_BMD_Throughput.sys driver supports the PCIe throughput demo.

On Linux, the lthruput_main.ko driver supports the demo.

4.2.4. Device Hardware (FPGA Design)

Figure 4.3 shows the top-level architecture of the FPGA design. DMA support is an option provided by the Lattice PCIe soft IP to enable more efficient data transfer when endpoint is acting as initiator or master. This feature is only available when the AHB-Lite data interface is selected.

In order to support DMA operations, the FPGA design has two queues implemented in local memory, a descriptor queue and a status queue. To initiate a DMA transfer, the host writes a descriptor into the descriptor queue, which contains the source address, destination address, length, and direction of data transfer. When the operation is

completed or aborted, the status of the transfer (including done status, error status, length of transfer, and data address offset) is written into the status queue. The DMA descriptor and status queues can be read via a register space implemented in the design.

FPGA memory is instantiated inside the FIFO Wrapper block, along with a pattern checker to verify DMA read data, and a pattern generator to generate data for DMA write operations.

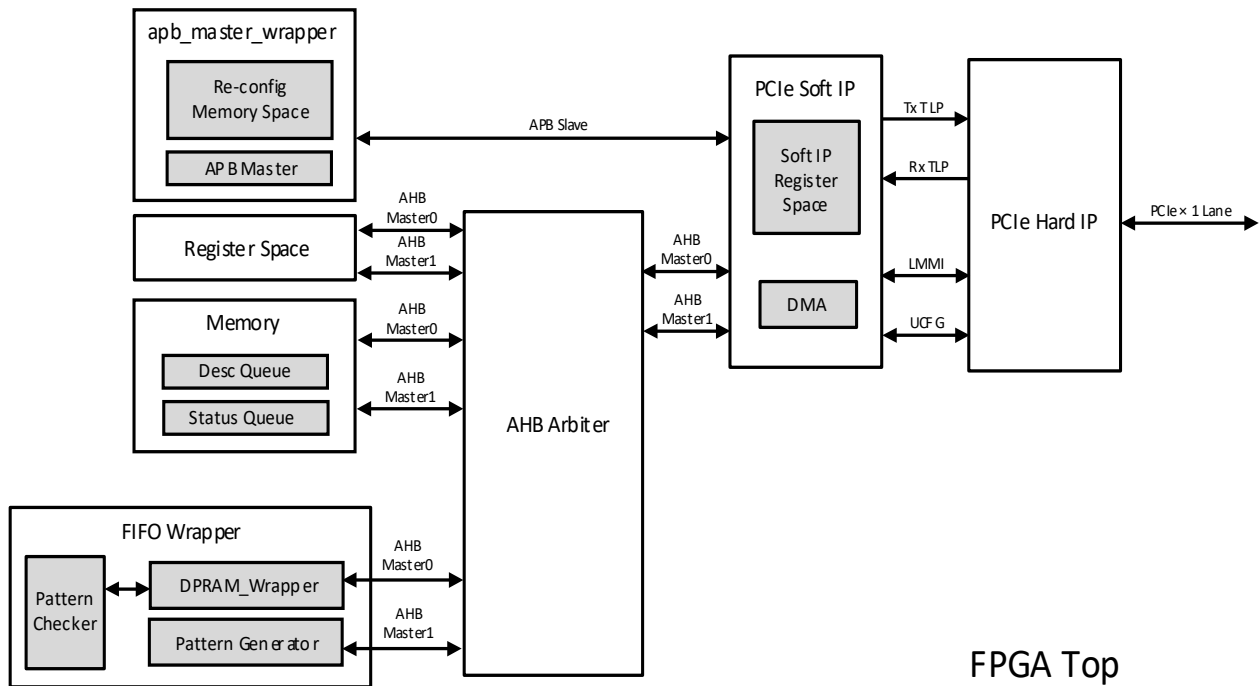


Figure 4.3. Top-level Architecture of FPGA Design

5. Application Overview

The PCIe DMA throughput demo is intended to show the DMA performance between the Lattice FPGA and a host system. With this application, you can read/write a pattern or counter data between the host system and FPGA memory. There are three pages in the application, GUI Device info, Test Run, and View memory pages.

5.1. Running the PCI Express DMA Throughput Demo Application

This section describes how to run the demo software after installation. On Linux platform, the demo can be launched by running the `./PCIeThruputDemo.sh` script, which is located in the `Demonstration/Linux/Source_Code/app_src/gui/deploy` directory. On Windows platform, the application can be launched using the `PCIeThroughputDemo.exe` which is located in the `/ProgramData/Microsoft/Windows/Start Menu/Programs/Lattice Semiconductor/Crosslink-NX Throughput` directory or `/ProgramData/Microsoft/Windows/Start Menu/Programs/Lattice Semiconductor/Certus-NX Throughput` directory or `/ProgramData/Microsoft/Windows/Start Menu/Programs/Lattice Semiconductor/CertusPro-NX Throughput` directory. The Graphical User Interface (GUI) opens the PCI Express Test Application software for Crosslink-NX and Certus-NX devices with the **Device Info** tab selected as shown in [Figure 5.1](#).

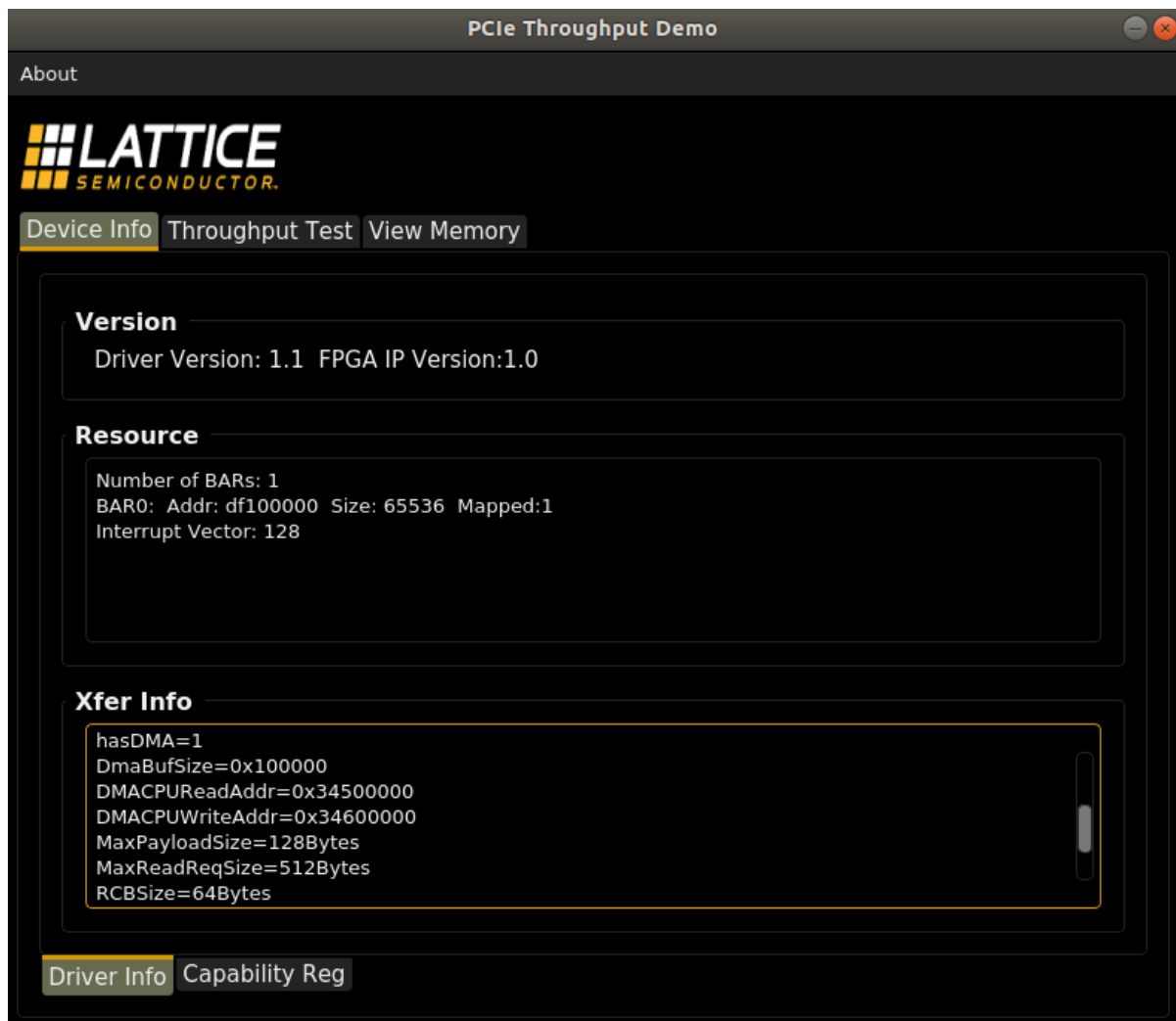


Figure 5.1. PCIe Throughput Demo Device Info Tab for Crosslink-NX and Certus-NX Devices

The Graphical User Interface (GUI) opens the PCI Express Throughput Demo application software for CertusPro-NX device with the Device Info tab selected is shown in [Figure 5.2](#).

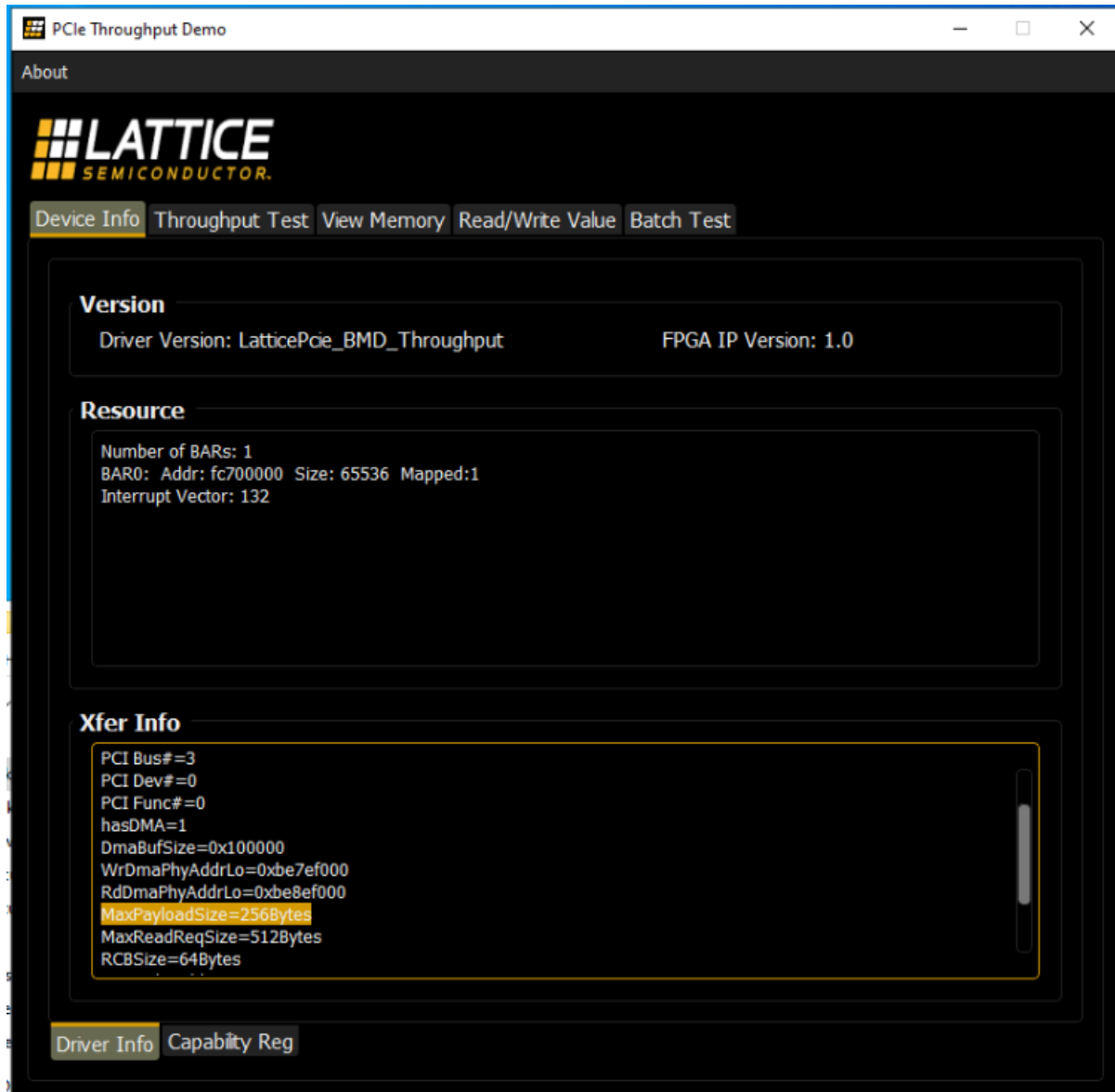


Figure 5.2. PCIe Throughput Demo Device Info Tab for CertusPro-NX Devices

5.2. PCIe Throughput Demo Walkthrough

5.2.1. Device Info

The Device Info page is first displayed when the GUI starts. It shows information about the system and FPGA, outlined in the following sections.

5.2.1.1. Version

This section shows the Driver and FPGA IP version information (Figure 5.3).

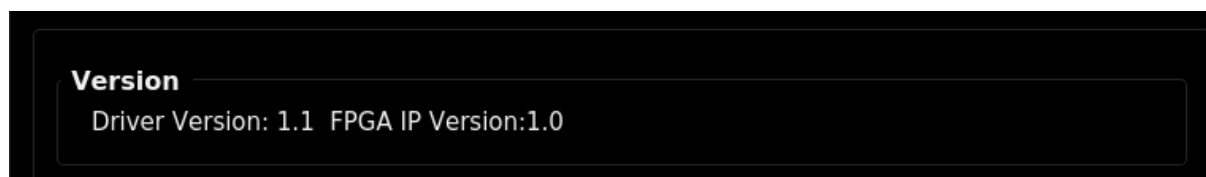


Figure 5.3. Version Information

5.2.1.2. Resource

Resource section shows PCIe device resource information, such as the number of BARs, BAR address, and size (Figure 5.4).

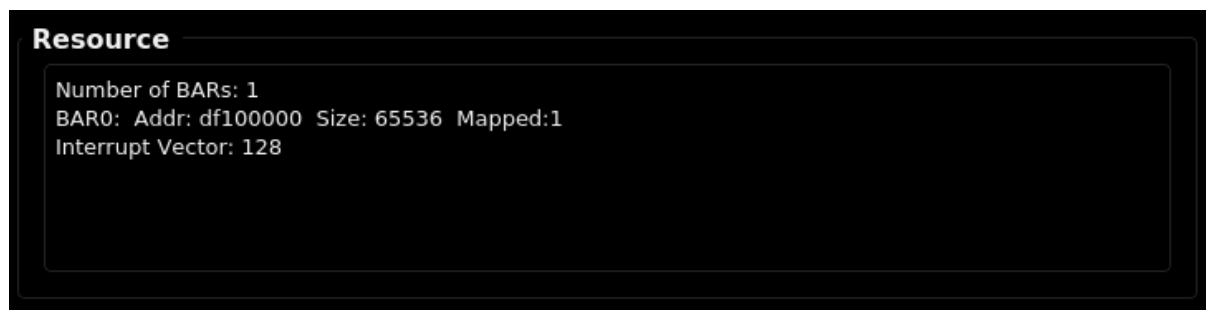


Figure 5.4. Resource Information

5.2.1.3. Xfer Info

The Xfer Info box provides the buffer sizes for the root complex for Posted and Non-Posted TLPs, along with addresses and capabilities (Figure 5.5).

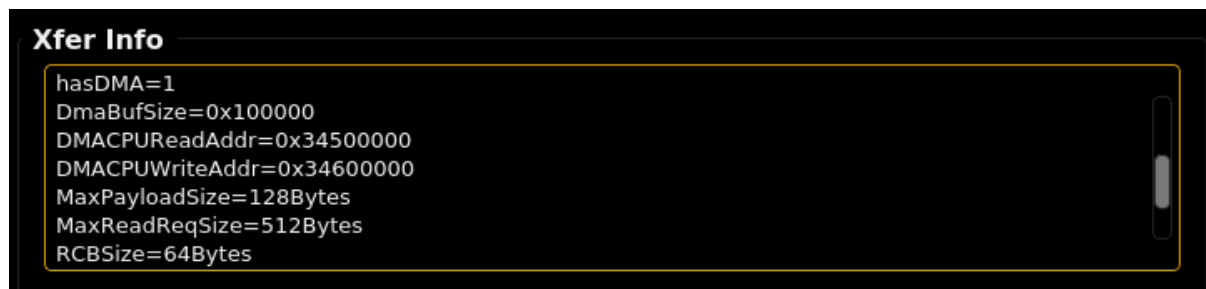


Figure 5.5. Xfer Info

5.2.1.4. Capability Reg

This page provides a readout of the endpoint PCIe configuration space, including all device capabilities (Figure 5.6 for Crosslink-NX and Certus-NX devices) and Figure 5.7 for CertusPro-NX device. Note that some of the information may vary between different FPGA devices (such as the Device ID).

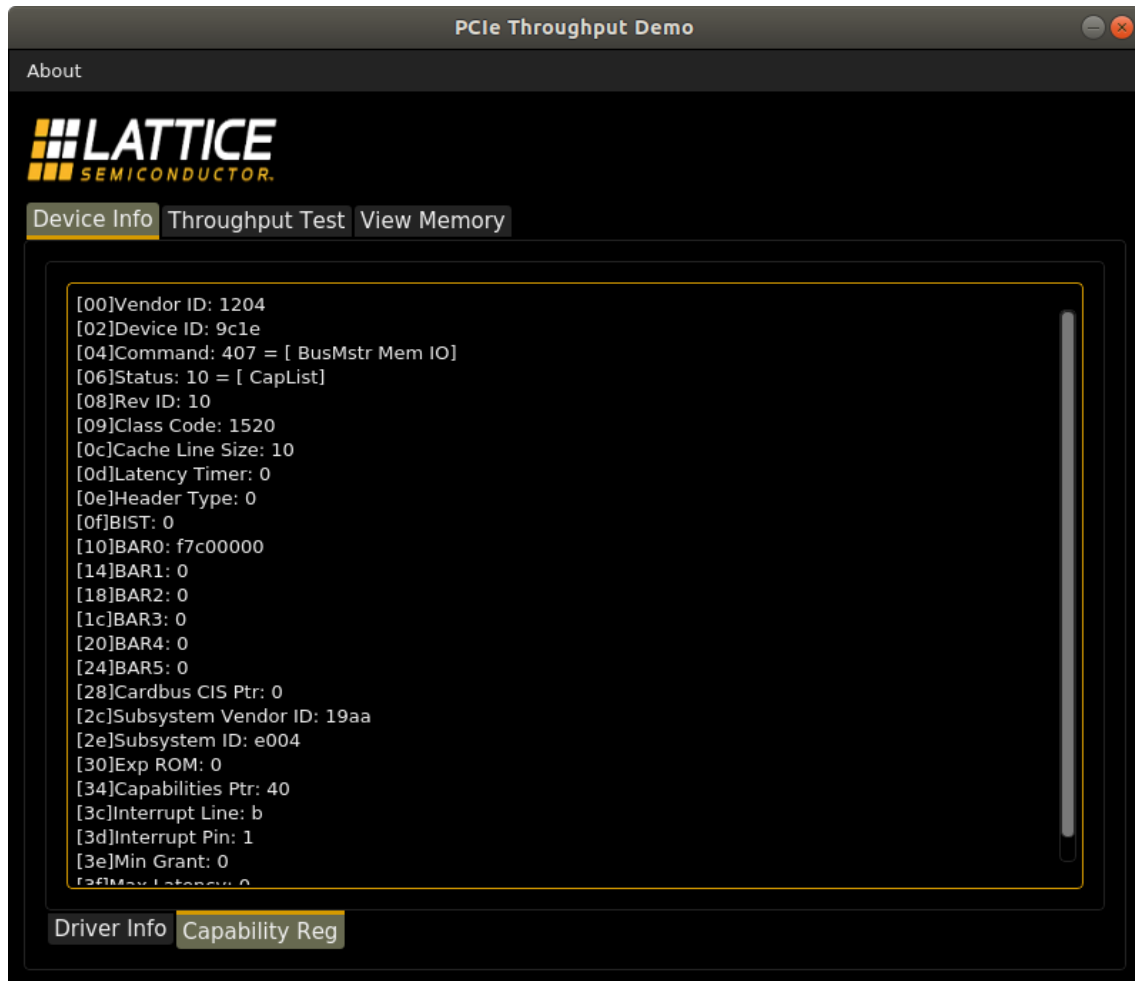


Figure 5.6. Capability Reg

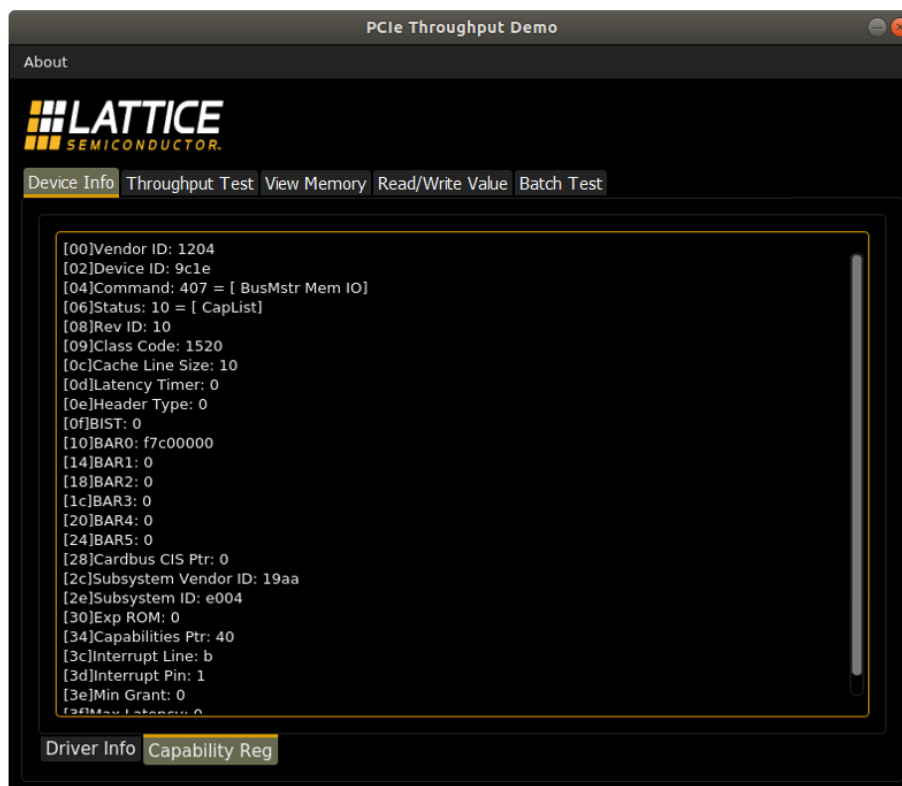


Figure 5.7. Capability Reg for CertusPro-NX Devices

5.2.2. Throughput Test

This page provides the primary test interface through which you can initiate DMA transfers. Due to a design limitation, simultaneous read and write operations are not possible. Throughput Test Page image for write and read operation is shown in Figure 5.8 and Figure 5.9 for Crosslink-NX and CertusPro-NX devices. The throughput Test Page image for write and read operation is shown in Figure 5.10 and Figure 5.11 for CertusPro-NX device whereby an additional option to specify the Endpoint DMA descriptor size in bytes is included. The controls are the same for Write and Read operations, but the resulting operations are different.

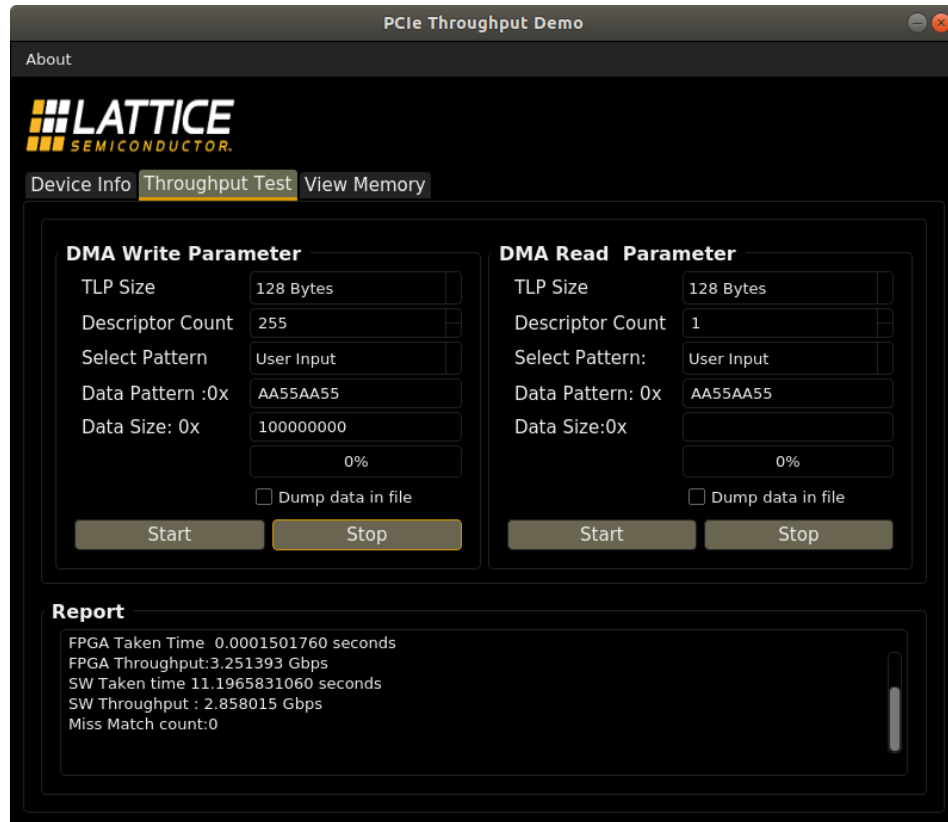


Figure 5.8. DMA Write Operation for Crosslink-NX and Certus-NX devices

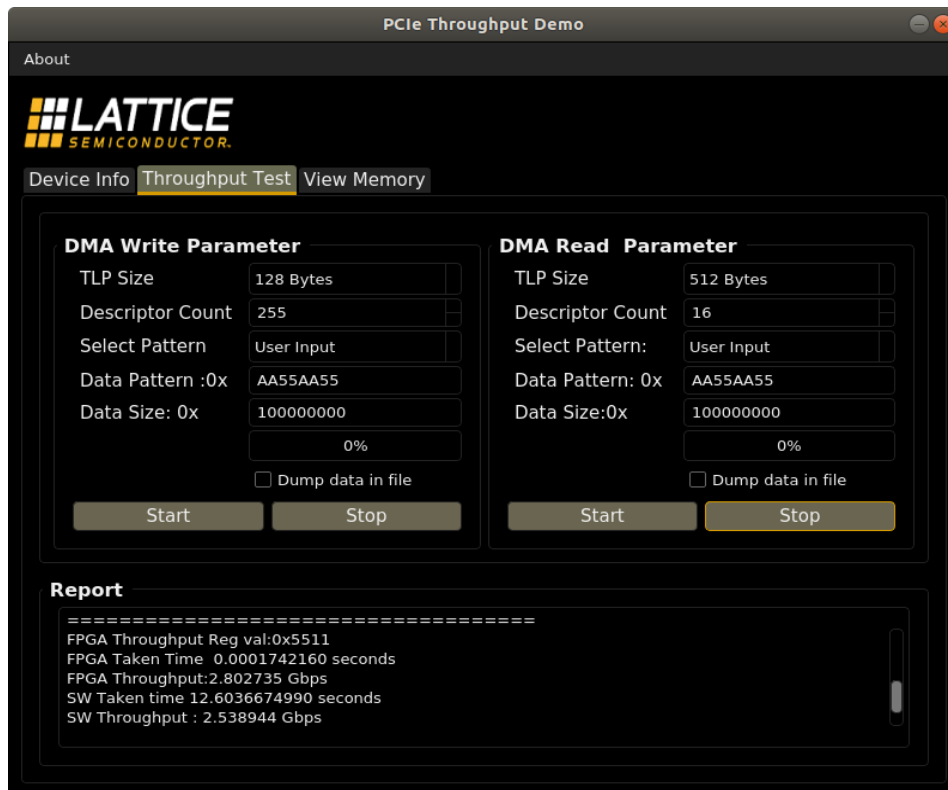


Figure 5.9. DMA Read Operation for Crosslink-NX and Certus-NX devices

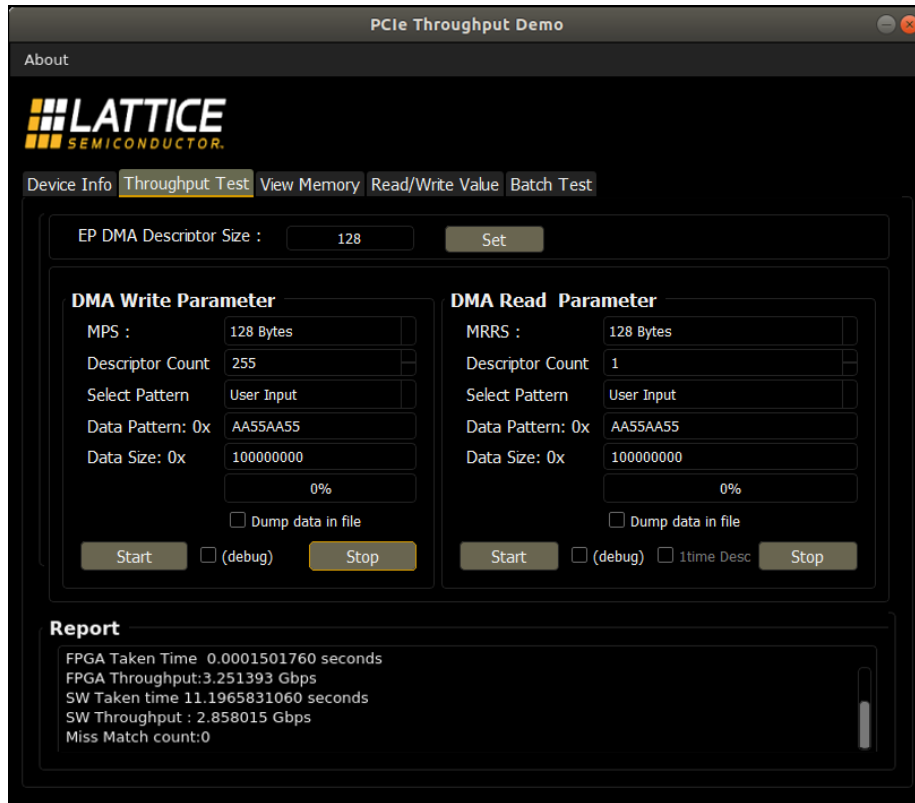


Figure 5.10. DMA Write Operation for CertusPro-NX device

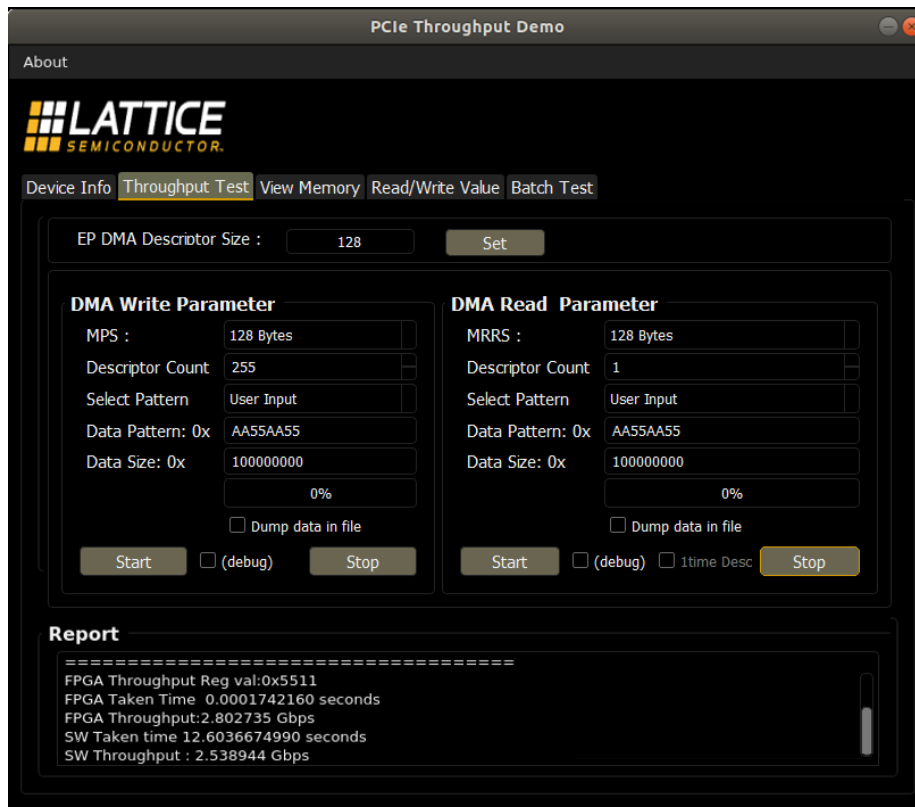
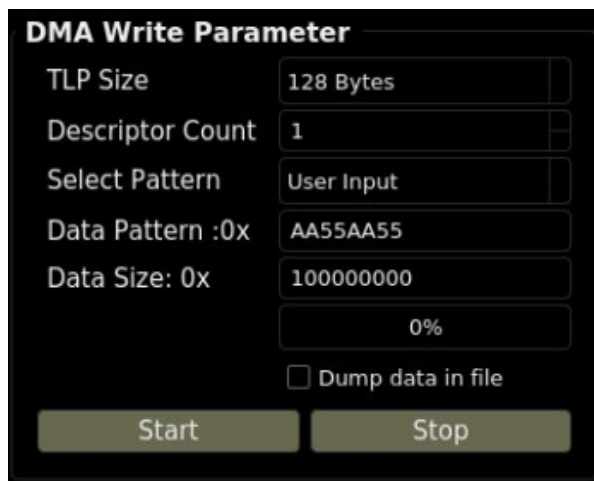


Figure 5.11. DMA Read Operation for CertusPro-NX device

5.2.3. DMA Write and Read Parameter

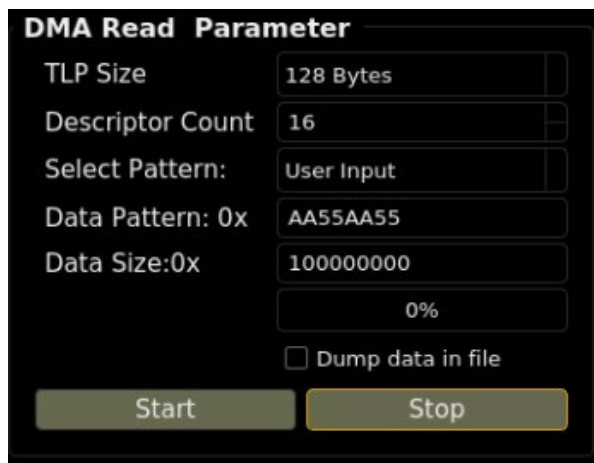
For DMA Writes, the data moves from the FPGA to PC memory, so a data checker is implemented in the software application running on the host (Figure 5.12). For DMA reads, the data moves from the PC to FPGA memory, so a data checker is implemented in the FPGA (Figure 5.13).



The DMA Write Parameter dialog box contains the following fields and controls:

- TLP Size:** 128 Bytes
- Descriptor Count:** 1
- Select Pattern:** User Input
- Data Pattern :0x:** AA55AA55
- Data Size: 0x:** 100000000
- Progress:** 0%
- Checkbox:** ☐ Dump data in file
- Buttons:** Start, Stop

Figure 5.12. DMA Write Parameter



The DMA Read Parameter dialog box contains the following fields and controls:

- TLP Size:** 128 Bytes
- Descriptor Count:** 16
- Select Pattern:** User Input
- Data Pattern: 0x:** AA55AA55
- Data Size:0x:** 100000000
- Progress:** 0%
- Checkbox:** ☐ Dump data in file
- Buttons:** Start, Stop

Figure 5.13. DMA Read Parameter

5.2.3.1. TLP Size

This control is used to configure the PCIe TLP size. All supported TLP sizes are shown in the drop-down list. If available, you can configure TLP size and apply the value to the link.

5.2.3.2. Descriptor Count

The descriptor count control is used to calculate the burst size for DMA operations. A single descriptor can transfer up to 4096 bytes. If you enter a descriptor count of 1, the burst size is (4096×1) . This means the application requests 4096 bytes in single iteration. For DMA writes, the maximum number of descriptors is 255 for a total of 4096×255 bytes of data. For DMA reads, the maximum number of descriptors is 16 for a total of 4096×16 bytes of data.

5.2.3.3. EP DMA Descriptor Size (only for CertusPro-NX devices)

The descriptor size control is also used to calculate the burst size for DMA operations together with descriptor count. set the amount of bytes a single descriptor can transfer. If you enter a descriptor count of 1 with descriptor size of 4096 bytes, the burst size is (4096×1) . CertusPro-NX allows the descriptor size of 128, 256, 512 and 4096 bytes to be selected.

5.2.3.4. Select Pattern

You can select the data pattern for the DMA operation using this control. Two types of input are supported: *User Input* and *Counter Data*. For *User Input*, the pattern entered in the Data Pattern control box is used for all data in the operation. The data pattern selected is repeated for each 32-bits in the transfer. For *Counter Data*, the data in the DMA operation consists of sequential data starting at 0x00000000 and incrementing by one for each 32-bit word.

5.2.3.5. Data Pattern

You can specify the Data Pattern when the *Select Pattern* control is set to *User Input*. The Data Pattern is specified as a hexadecimal number, and the valid input range is from 0 to 0xFFFFFFFF.

5.2.3.6. Data Size

This control is used to specify the total amount of data to be transferred. The DMA operations are repeated (to/from the same addresses in memory) until the total amount of data is transferred. The data size is specified in bytes, and the valid input range is from 0x1000 to 0x100000000. For DMA reads, the data checker on the FPGA verifies each 32 bits of data as it is received. For DMA writes, the data is verified by the software after the entire operation is completed.

5.2.3.7. Dump Data in File

This control is used to select whether or not the data from the DMA operation should be saved to a file. Note that if a large DMA operation is chosen, the file size can be very large (around four GB) and may increase runtime significantly. The files are dumped in binary format into the `./Demonstration/Linux/Source_Code/app_src/gui/deploy` folder as DMARead.hex or DMAWrite.hex.

5.2.3.8. Report

The Report section is read only (Figure 5.14) and it displays the result of the DMA operation. It shows the FPGA throughput for single iteration and Software throughput for complete size transfer. The FPGA throughput is the calculated data transfer rate across the PCIe link. The SW throughput includes time for data verification and buffer set-up time. For the best transfer throughput, it is recommended to use a large data size of at least one GB.

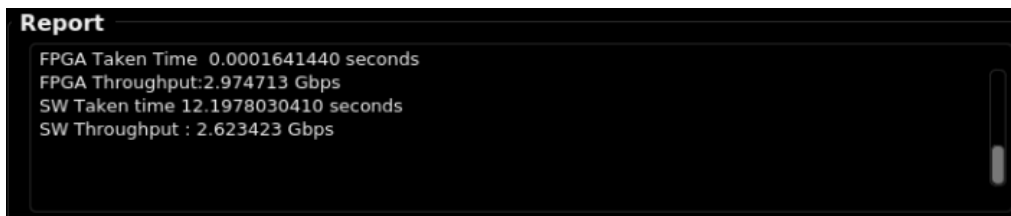


Figure 5.14. Report

5.2.4. View Memory

The View Memory tab (Figure 5.15) shows the FPGA memory (HWRxBuffer) and the system memory (HWTxBuffer) allocated by the driver. For CertusPro-NX additional the View Memory Tab also incorporates the and Endpoint Descriptor memory (EPDescriptor) allocated. The total size of this buffer is 0x100000. The memory can be read by clicking the Refresh button.

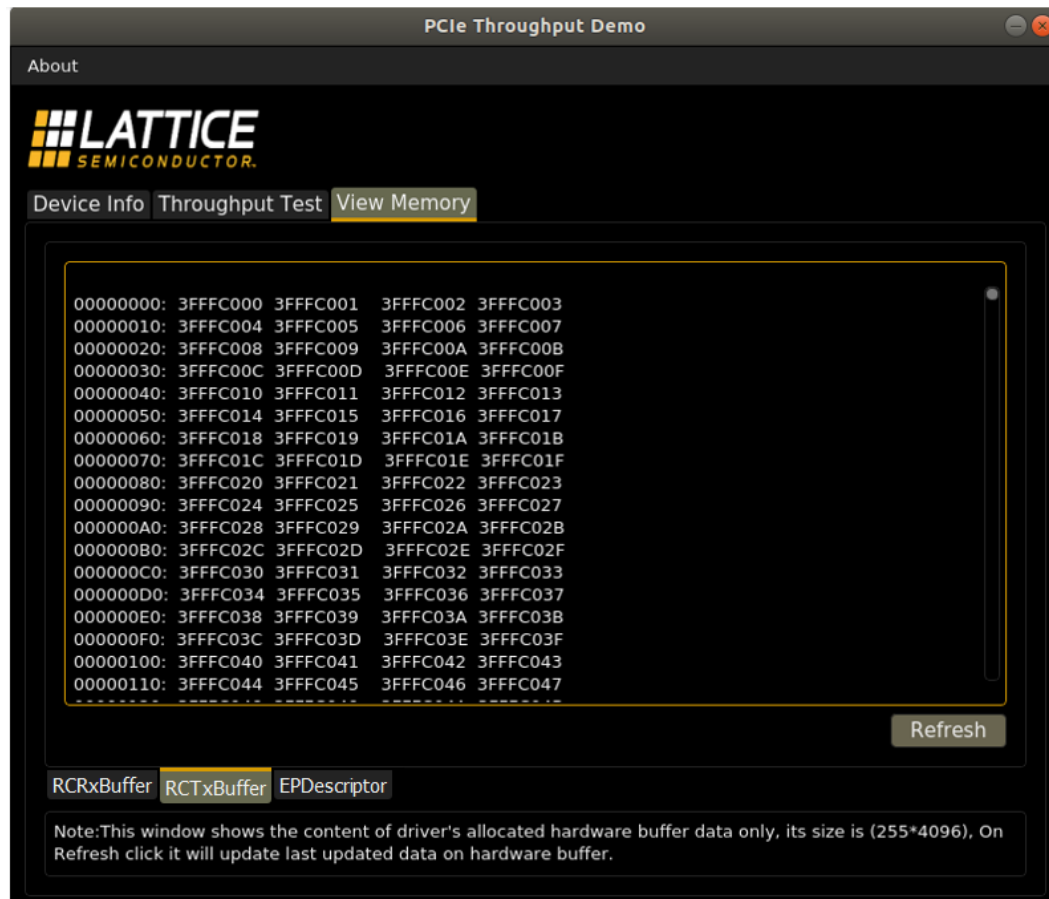


Figure 5.15. View Memory

6. Import and Build the FPGA Demonstration

The package includes the PCIe IP, .bit file, and synthesis projects using Lattice Radiant Software for the demo.

6.1. Hardware Directory Structure

The Hardware folder inside the package contains the following subfolders.

`./CL_NX_BridgeBoard_BMD_throughput/` or `./CertusNX_PCl_e_BMD/` or `./LFCPNX100_PCl_e_BMD/`

- IP – Contains the pre-generated IPs used in the designs for the different FPGA devices. These IPs can be configured by clicking the .ipx file after opening the project in the Radiant software.
- Implementation – Contains the Lattice Radiant project (.rdf) file, constraints file (.pdc), and implemented design and bit files.
- Source – Contains RTL files required for the design.

6.2. Build Lattice Radiant Project

To generate the bit stream file:

1. Open the Lattice Radiant software.
2. Click **Open project** and browse to the .rdf file
 - For CrossLink-NX family, the file is LIFCL-40_PCl_eBMD.rdf file, which is located in the `./CL-NX_BridgeBoard_PCl_e_BMD/Hardware/CL_NX_BridgeBoard_PCl_e_BMD_throughput/Implementation/LIFCL-40_PCl_eBMD` folder.
 - For Certus-NX family, the file is LFD2NX_PCl_e_BMD.rdf, which is located in the `./CertusNX_PCl_e_BMD/Hardware/LFD2NX_PCl_e_BMD/Implementation/LFD2NX_PCl_e_BMD` folder.
 - For CertusPro-NX family, the file is LFCPNX100_PCl_e_BMD.rdf, which is located in the `./Hardware/LFCPNX100_PCl_e_BMD` folder.
3. Once your project loads, click **Task Detail View**. This shows a list of actions that Lattice Radiant can perform to build the .bit file.
4. Select the files and reports that you want to generate.
Note: The options needed to regenerate the .bit file selected by default.
5. After selecting your preferred reports, click **Run All**.

This creates a .bit file with your current project name in the `impl_1` subfolder.

7. Troubleshooting

7.1. SPI Flash Update

- If you get a verification error while dumping the .bit file, try changing the TCK frequency to a value greater than 4. The TCK Divider Setting option is in the Cable Setup dialog box of the Lattice Radiant Programmer Window, as shown in Figure 7.1. Restart programming by clicking the Program button.

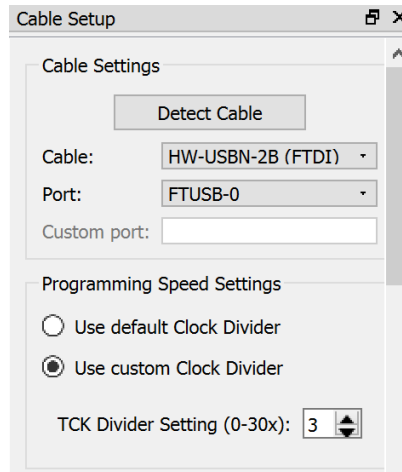


Figure 7.1. TCK Frequency Setting

- If the verification error problem still occurs, press and hold the PROGRAMN push button on the board before clicking the Program button.
- If the device is not detected on port FTUSB-0, click Detect cable and select the port FTUSB-1.

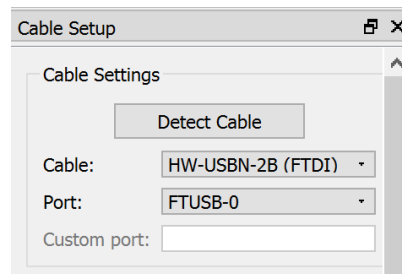


Figure 7.2. Port Selection

7.2. Driver Installation and User Interface Launch for Windows

7.2.1. Problem with Driver Installation

- If the hardware IDs are not found in the Device Manager, ensure that the board is properly installed in a PCIe slot.
- Ensure that the board has a valid PCIe bitstream file loaded in the SPI Flash. Shut down the system and try another slot. If the board is present, check the Properties and the Resource tab to verify if memory is assigned to it.

Also, verify if the Vendor ID and Device ID are valid, as seen by Windows Plug-n-Play. If the values are invalid, perhaps the bitstream file is corrupt and needs to be reloaded into SPI flash. If the PCIe board is shown in the list of Device Manager, install the driver manually.

- If the driver is not being installed even though the device is present in the Device Manager, make sure that the driver signature enforcement is disabled permanently. If not, follow the steps described in the [Disabling Driver Signature Enforcement Permanently](#) section.

7.2.2. Problem with Launching User Interface

Ensure that the driver is installed properly. Otherwise, the Device Info section of the user interface displays the message shown in [Figure 7.3](#).

The *Driver Open [FAILED]* message is displayed if the driver is not installed properly. The Device information is present if the drivers are installed properly.

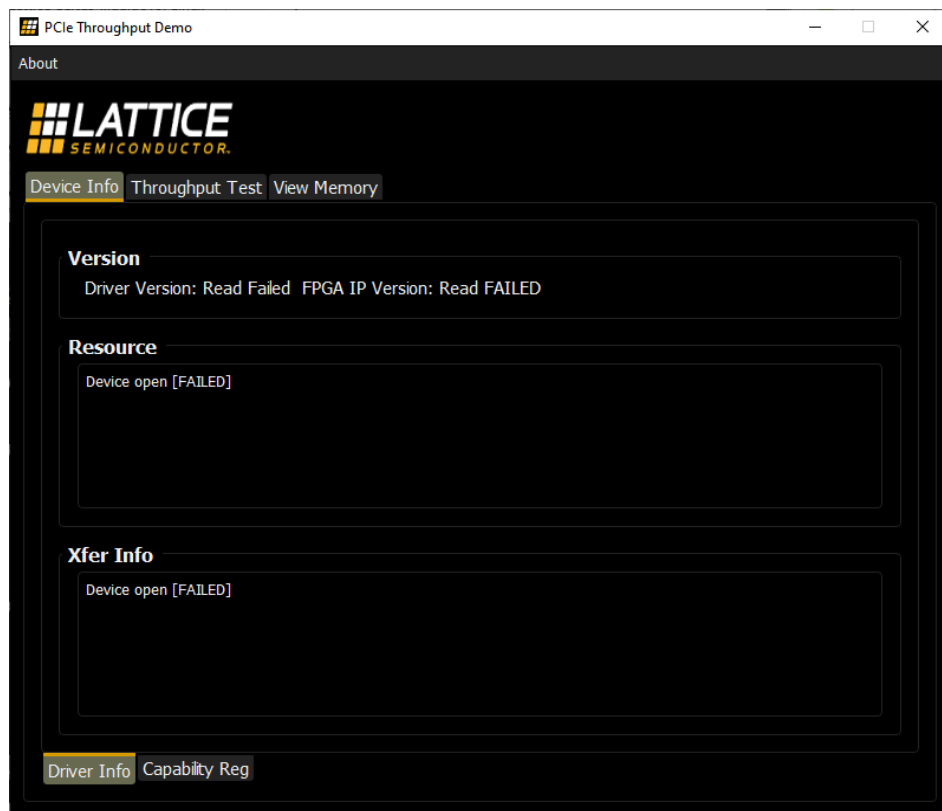


Figure 7.3. User Interface with No Device Driver

If the device is not inserted in the system or the device driver is not installed, any read or write operation is not executed. A sample error message is shown in [Figure 7.4](#).

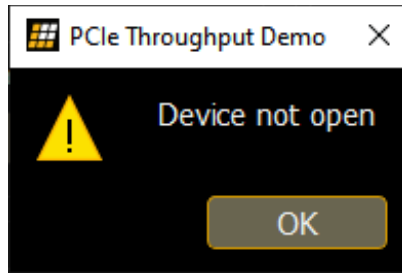


Figure 7.4. Error Message

If any such error message occurs, ensure that the device is properly inserted in the system. After that, verify that drivers are installed. When all the issues are resolved, restart the user application.

It is also possible that there could be a driver conflict due to another PCIe demo being installed. In this case, manual deletion of the driver may be needed. It is recommended to uninstall the device from the system and delete the 'LatticePcie_BMD_Throughput.sys' and 'LatticePcie_BMD_Colourbar.sys' drivers from the *Windows\System32\drivers* directory, and then reinstall the Colorbar demo manually from the start.

When using file saving operations in the Memory portion of the demo, ensure that you have write permissions for the location where the file is being saved.

If the throughput demo shortcut icon is accidentally deleted, the application can be launched by double-clicking on *PCleThruputDemo.exe* file present in [INSTALLATION FOLDER]/Lattice Semiconductor/CL-NX Bridge Board Throughput Demo (or Certus-NX Throughput Demo)/bin folder.

7.3. Driver Installation User Interface Launch for Linux

This section describes trouble shooting steps for Linux.

7.3.1. Problem with Driver Loading

After launching the user interface, if the driver is not loaded properly, a *Driver open[Failed]* message is displayed in the Info section.

- Make sure that the board is properly connected to the PC.
- Run the command below in a terminal window to show the list of PCIe devices connected to PC.

```
sudo lspci -vnm
```

Ensure that the Lattice device is present by checking the device and vendor IDs, as shown in [Figure 7.5](#) for CrossLink-NX family, [Figure 7.6](#) for Certus-NX family, and [Figure 7.7](#) for CertusPro-NX family.

```
Device: 01:00.0
Class: 1180
Vendor: 1204
Device: 9c1e
SVendor: 19aa
SDevice: e004
Rev: 04
```

Figure 7.5. lspci -vnm for CrossLink-NX Output Image


```
Device: 01:00.0
Class: 1180
Vendor: 1204
Device: 9c2e
SVendor:      19aa
SDevice:      e004
Rev: 04
```

Figure 7.6. lspci -vnm for Certus-NX Output Image

```
Device: 01:00.0
Class: 1180
Vendor: 1204
Device: 9c3e
SVendor:      19aa
SDevice:      e004
Rev: 04
```

Figure 7.7. lspci -vnm for CertusPro-NX Output Image

- If the device is present, then perform the manual setup and installation steps one by one.
- If the driver does not build properly, check to find the software or kernel dependencies.

7.3.2. Problem with User Interface Launching

- Go to the *Demonstration/Linux* directory. Check all contents of this directory. Default contents are shown in Figure 7.8. Check the permissions of these files.

```
total 16
-rw-r--r-- 1 root root 249 Feb 18 04:28 install.sh
-rw-r--r-- 1 root root 247 Feb 18 04:28 Readme.txt
drwxr-xr-x 6 root root 4096 Feb 18 04:28 Source_Code
-rw-r--r-- 1 root root 20 Feb 18 04:28 uninstall.sh
```

Figure 7.8. Contents List of Demonstration/Linux Directory

- The script files should have *execute* permission – to set permissions on the file, run the command below in the terminal and try to run the application again.

```
sudo chmod 777 filename
```
- If the user interface still does not launch, change directory into the *Source_Code* directory and verify that all files are present in this directory, according to Figure 7.9.

```
total 44
drwxr-xr-x 6 root root 4096 Feb 18 04:28 app_src
-rw-r--r-- 1 root root  27 Feb 18 04:28 compile.sh
drwxr-xr-x 3 root root 4096 Feb 18 04:28 drv_src
drwxr-xr-x 2 root root 4096 Feb 18 04:28 include
-rw-r--r-- 1 root root  63 Feb 18 04:28 install_drv.sh
-rw-r--r-- 1 root root  44 Feb 18 04:28 launch_gui.sh
drwxr-xr-x 2 root root 4096 Feb 18 04:28 lib
-rw-r--r-- 1 root root 388 Feb 18 04:28 Makefile
-rw-r--r-- 1 root root 165 Feb 18 04:28 Readme.txt
-rw-r--r-- 1 root root  73 Feb 18 04:28 run_console_app.sh
-rw-r--r-- 1 root root  76 Feb 18 04:28 run_thruput_demo.sh
```

Figure 7.9. Contents List of Software/Linux Directory

- If all files are present in this directory, change directory to *app_src/gui/deploy* and try to run the command below directly.

```
sudo ./PCIEThruputDemo.sh
```

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.3, May 2023

Section	Change Summary
All	Included CertusPro-NX information throughout the document.
Introduction	Included CertusPro-NX information in Introduction section.
Hardware and Software Requirements	- Added bullet information <i>CertusPro-NX Versa Board for CertusPro-NX family</i> in Hardware Requirements section. - Added bullet information <i>LFCPNX100_PCl_e_BMD.bit for CertusPro-NX family</i> in Software Requirements section.
Set Up the Demo	- Added paragraph <i>For CertusPro-NX, there are no jumpers to configure beyond the default. Refer to the CertusPro-NX Versa Board User Guide (FPGA-EB-02053) for a detailed list of jumpers on the board. When the board is plugged into the PCIe slot, external power is provided by the system, and SW6 should be in the up position to receive power from the PCIe slot. Connect the board to the PC running the Lattice Radiant software with the Mini USB Type A Cable as shown in Figure 3.3 in Hardware Setup section.</i> - Added bullet <i>For CertusPro-NX family, select LFCPNX100_PCl_e_BMD.bit from Demonstration\Bitstream</i> in Programming the FPGA section. - Added bullet <i>For CertusPro-NX family, the Hardware IDs of the Base System Device for the DMA Throughput Demo is PCI\VEN_1204&DEV_9C3E&SUBSYS_E00419AA as shown in Figure 3.35 in Driver Installation section.</i> - Added Figure 3.3. CertusPro-NX Versa Board Connection, Figure 3.8. CertusPro-NX FPGA Device Settings, Figure 3.11. Device Properties Window for CertusPro-NX SPI Flash Programming (with Macronix Flash), Figure 3.16. CertusPro-NX Programming Done LED, Figure 3.35. Hardware IDs of CertusPro-NX DMA Throughput Demo Device, Figure 3.42. CertusPro-NX Driver Installation Status Message, and Figure 3.45. CertusPro-NX DMA Throughput Demo Device Name Displayed in Device Manager.
Application Overview	- Replaced <i>On Windows platform, click the Bridge Board Throughput Demo icon to On Windows platform, the application can be launched using the PCIeThroughputDemo.exe which is located in the /ProgramData/Microsoft/Windows/Start Menu/Programs/Lattice Semiconductor/Crosslink-NX Throughput directory or /ProgramData/Microsoft/Windows/Start Menu/Programs/Lattice Semiconductor/Certus-NX Throughput directory or /ProgramData/Microsoft/Windows/Start Menu/Programs/Lattice Semiconductor/CertusPro-NX Throughput directory</i> in Running the PCI Express DMA Throughput Demo Application section. - Updated the title of Figure 5.1. PCIe Throughput Demo Device Info Tab for Crosslink-NX and Certus-NX Devices to PCIe Throughput Demo Device Info Tab for Crosslink-NX and Certus-NX Devices. - Added bullet <i>The Graphical User Interface (GUI) opens the PCI Express Throughput Demo application software for CertusPro-NX device with the Device Info tab selected is shown in Figure 5.2 in Running the PCI Express DMA Throughput Demo Application section.</i> - Added Figure 5.2. PCIe Throughput Demo Device Info Tab for CertusPro-NX Devices, Figure 5.7. Capability Reg for CertusPro-NX Devices, Figure 5.10. DMA Write Operation for CertusPro-NX device, and Figure 5.11. DMA Read Operation for CertusPro-NX device. - Updated from <i>This page provides the primary test interface through which you can initiate DMA transfers. Due to a design limitation, simultaneous read and write operations are not possible. Throughput Test Page image for write and read operation is shown in Figure 5.6 and Figure 5.7. The controls are the same for Write and Read operations, but the resulting operations are different to This page provides the primary test interface through which you can initiate DMA transfers. Due to a design limitation, simultaneous read and write operations are not possible. Throughput Test Page image</i>

	for write and read operation is shown in Figure 5.8 and Figure 5.9 for Crosslink-NX and CertusPro-NX devices. The throughput Test Page image for write and read operation is shown in Figure 5.10 and Figure 5.11 for CertusPro-NX device whereby an additional option to specify the Endpoint DMA descriptor size in bytes is included. The controls are the same for Write and Read operations, but the resulting operations are different in Throughput Test section. • Updated Figure 5.8. DMA Write Operation for Crosslink-NX and Certus-NX devices and Figure 5.9. DMA Read Operation for Crosslink-NX and Certus-NX devices to add Crosslink-NX and Certus-NX devices in the title. • Added EP DMA Descriptor Size (only for CertusPro-NX devices) section. • Replaced from <i>The View Memory tab (Figure 5.11) shows the FPGA memory (HWRxBuffer) and the system memory (HWTxBuffer) allocated by the driver to The View Memory tab (Figure 5.11) shows the FPGA memory (HWRxBuffer) and the system memory (HWTxBuffer) allocated by the driver. For CertusPro-NX additional the View Memory Tab also incorporates the and Endpoint Descriptor memory (EPDescriptor) allocated in View Memory section.</i>
Import and Build the FPGA Demonstration	• Added ./LFCPNX100_PClE_BMD/ in Hardware Directory Structure section. • Added bullet For CertusPro-NX family, the file is LFCPNX100_PClE_BMD.rdf, which is located in the ./ Hardware/LFCPNX100_PClE_BMD folder in Build Lattice Radiant Project section.
Troubleshooting	Added Figure 7.7. lspci -vnm for CertusPro-NX Output Image in Problem with Driver Loading section.
Technical Support AssistanceHardware and Software Requirements	Added Lattice FAQ website link in Technical Support Assistance section.

Revision 1.2, April 2022

Section	Change Summary
All	Changed the document title to <i>PCIe Throughput Demo for Lattice Nexus-based FPGAs User Guide</i> .

Revision 1.1, March 2022

Section	Change Summary
All	Changed the document title to <i>Nexus Platform PCIe DMA Throughput Demo User Guide</i> .
Introduction	General update reflecting the support from CrossLink-NX family only to the Nexus platform.
Hardware and Software Requirements	• Changed to <i>Evaluation Board</i> including one board each for different device families in the Hardware Requirements section. • Changed <i>Bit file for the SPI Flash</i> including one bit file each for different device families in the Software Requirements section.
Set Up the Demo	• General update to reflect the support from CrossLink-NX family only to the Nexus platform. • Newly added Figure 3.2 Certus-NX PCIe Versa Evaluation Board Connection and Figure 3.12 Certus-NX Programming Done LED.
Demo Design Overview	Updated Figure 4.1. Relationship of the Hardware and Software Components reflecting the change to the Nexus platform.
Import and Build the FPGA Demonstration	General update reflecting the support change from CrossLink-NX family only to the Nexus Platform.
Troubleshooting	

Revision 1.0, January 2022

Section	Change Summary
All	Initial release.



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