# Lattice mVision AR0234 Sensor Board

# User Guide

FPGA-UG-02124-1.1

February 2022

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| EVDK | Embedded Vision Development Kit |
| FPGA | Field-Programmable Gate Array |
| ISP | Image Signal Processing |
| JTAG | Joint Test Action Group |
| MIPI | Mobile Industry Processor Interface |
| SCLK | Serial Clock Signal |

# 1. Introduction

The Lattice mVision™ AR0234CS sensor board uses a 1/2.6−inch 2.3 Mp Color 0deg Global Shutter CMOS digital image sensor with an active−pixel array of 1920 (H) × 1200 (V) from On Semiconductor. The sensor board can be interfaced to the EVDK (Embedded Vision Development Kit). The EVDK combines the bridging capability of our CrossLink™ FPGA, the low-power, small form factor ECP5™ and the high-resolution benefits of our HDMI ASSP, onto this modular platform enabling flexible connectivity and energy efficient image processing for robotics, drones, ADAS, smart surveillance and AR/VR systems. The included software provides a comprehensive setup interface and flexibility to evaluate the Lattice mVision ISP solution from Lattice and full sensor features and capabilities.

The sensor board comes with a lens suitable for evaluation with M12 lens holder to use standard M12 compatible lenses. You can use your own lens as long as it is compatible with the mechanical and optical requirements.

An IR-CUT driver circuit using TI's DRV8838 integrated motor driver solution for cameras allows the use of IR-CUT filter.

## 1.1. Features

The key features of the Lattice mVision AR0234CS sensor board are:

- ON Semiconductor CMOS ½.6", Color, 0deg, Image Sensor AR02345CS with following specifications:
  - Active pixels: 1920H × 1200V
  - Pixel size: 3.0 um × 3.0 um
  - Color sensor
  - Interface: MIPI output
  - Global Shutter
  - Part#: AR0234CS3C00SUKA0-CP-E
- IR_CUR driver circuit for use of IR_CUT filters
- Included PT-0620 lens with following specifications:
  - Focal Length: 6.0 mm
  - Iris: F2.0
  - Mount: M12x0.5
  - Image Sensor Size: 1/3"
  - Angle of View: 51°
  - Housing: Metal
  - Optics: Glass
- M12 lens holder
- External connection for Flash and Shutter control
- External connection for all power supplies
- External connection for EVDK kit (including power, data, and control signals)
- Tripod Connection

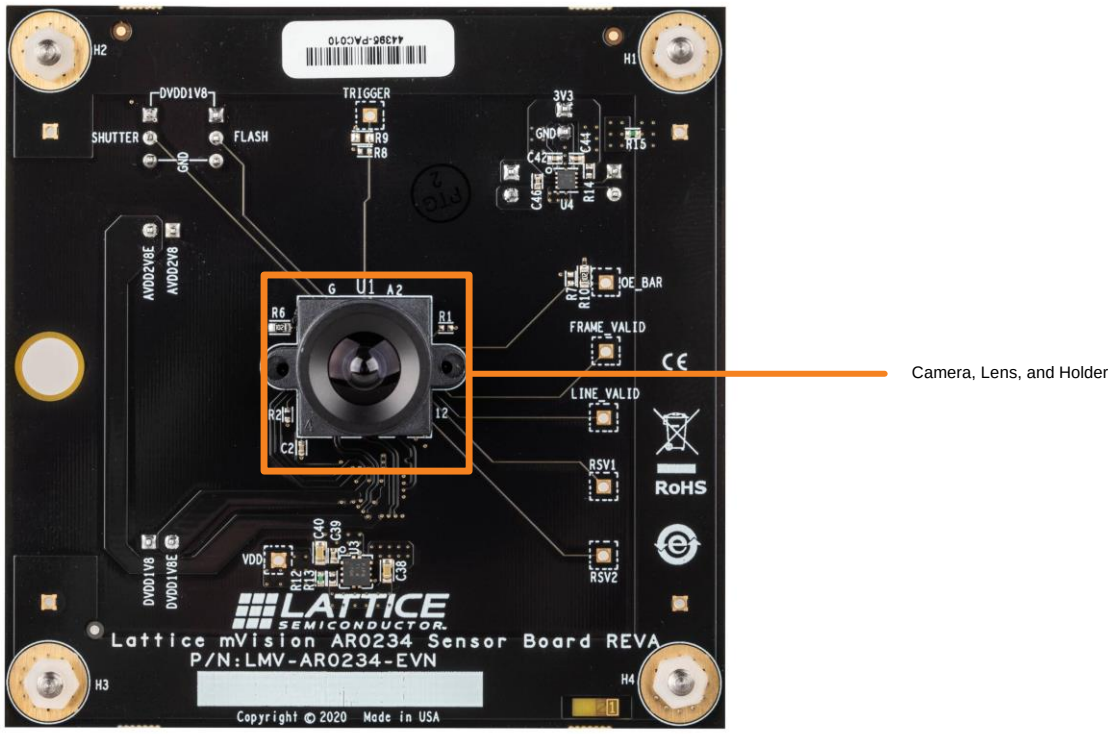



**Figure 1.1. Top View of Lattice mVision AR0234CS Sensor Board**

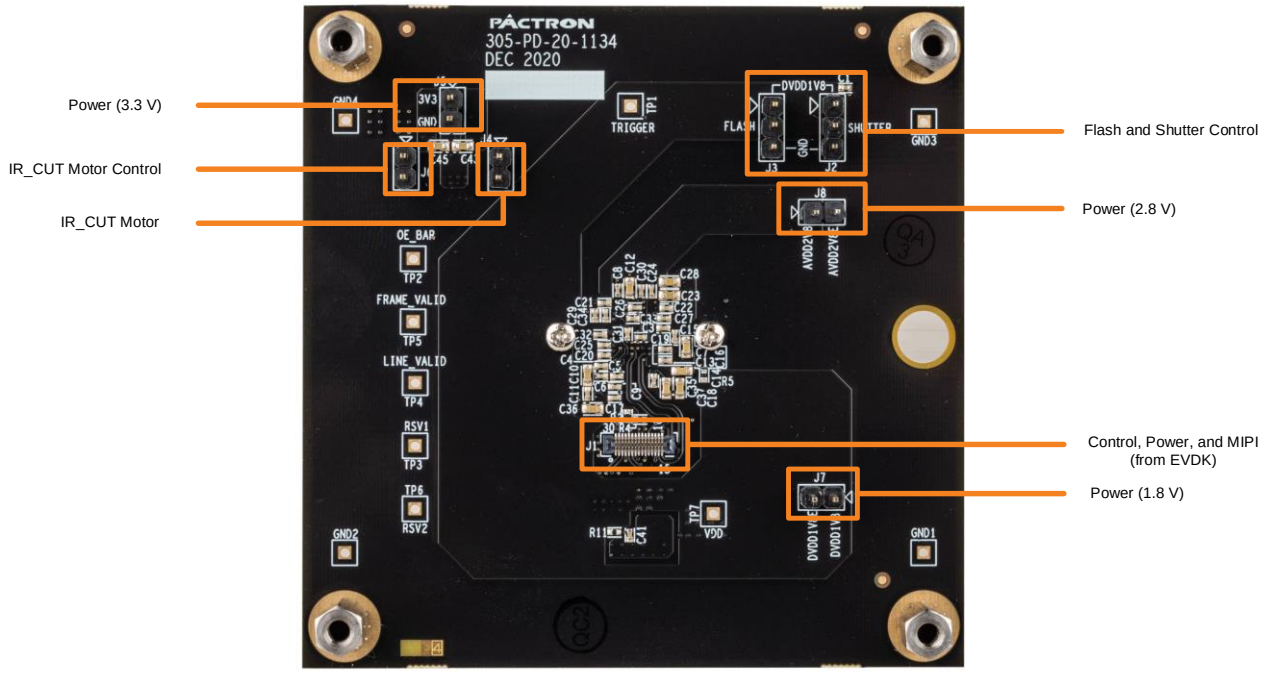



**Figure 1.2. Bottom View of Lattice mVision AR0234CS Sensor Board**

# 2. Required Components

Before starting the evaluation, the following items must be available and ready to use on the test bench.

- Embedded Vision Development Kit (EVDK) with camera modules removed

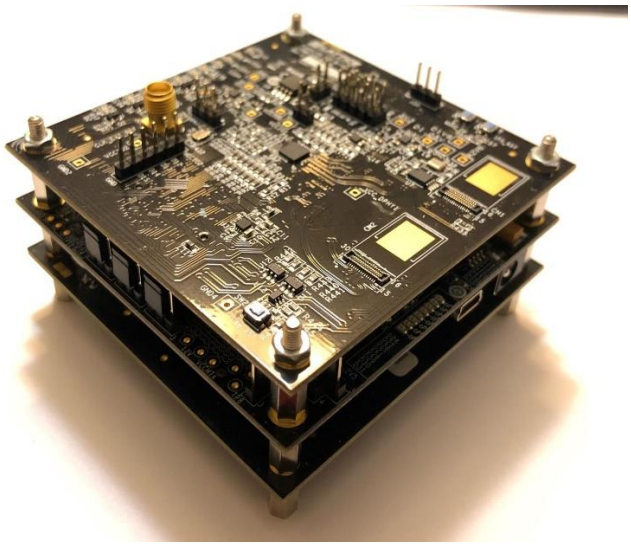


**Figure 2.1. Embedded Vision Development Kit**

- mVision AR0234 Sensor Board with lens holder and lens assembled


**Figure 2.2. Lattice mVision AR0234 Sensor Board**

- HDMI Monitor
- HDMI Cable
- Flexible Cable
- Two jumpers placed on J7 and J8 headers of AR0234 Sensor Board

Once all required items are available, connect the EVDK and AR0234 sensor board together using the Flex cable as shown in Figure 2.3.

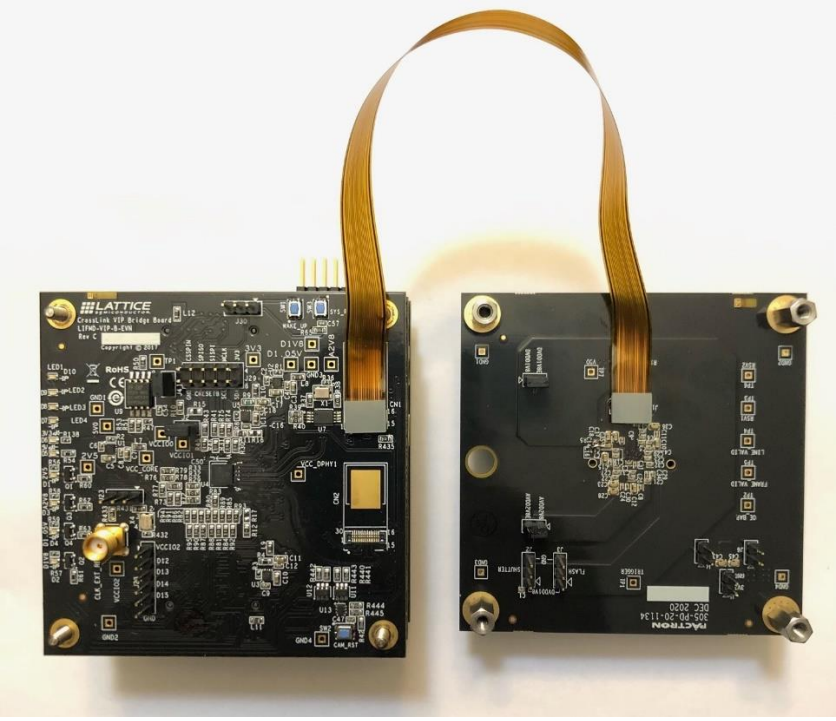


**Figure 2.3. EVDK and AR0234 Sensor Boards Connected with Flex Cable**

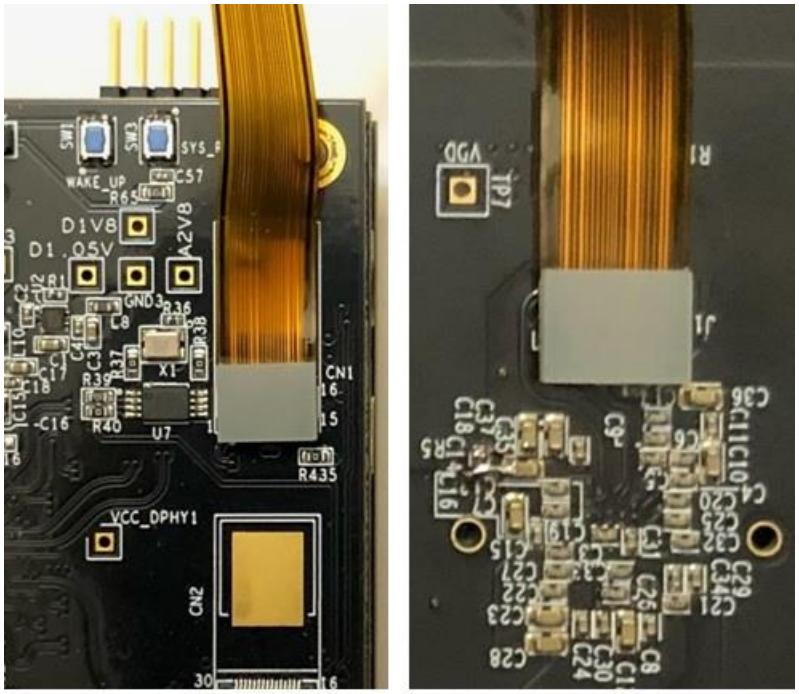



**Figure 2.4. Flex Cable Connection Detail**

# 3. Headers and Jumpers

Table 3.1 lists the headers and jumpers as shown in Figure 1.2.

**Table 3.1. AR0234 Sensor Board**

| S. No. | Jumper Name | Description |
|---|---|---|
| 1 | J7 | Short |
| 2 | J8 | Short |

**Table 3.2. CrossLink VIP Input Bridge Board**

| S. No. | Jumper Name | Description |
|---|---|---|
| 1 | J4 | Short |
| 2 | J30 | Open |
| 3 | J2 | Short |
| 4 | — | All other headers should be kept open |

**Table 3.3. ECP5 VIP Processor Board**

| S. No. | Jumper Name | Description |
|---|---|---|
| 1 | J55 | Connect 2 and 3 |
| 2 | J51 | Connect 1 and 2 |
| 3 | J5 | Connect 1 and 2 |
| 4 | J9 | Connect 1 and 2 |
| 6 | J6 | Connect 1 and 2 |
| 7 | J3 | Connect 1 and 2, also 5 and 6 |
| 8 | J50 | Connect 1 and 2, also 3 and 5 |
| 9 | J7 | Connect 2 and 3 |
| 10 | J52 | Connect 1 and 2 for SPI, 2 and 3 for JTAG |
| 11 | J53 | Connect 1 and 2 |
| 12 | — | All other headers should be kept open |

# 4. Programming the Board

## 4.1. Programming the Device

The board is programmed through the Lattice Radiant™ programmer software, which can be started as a standalone tool or from a Lattice Radiant Project.

To program the Lattice mVision AR0234 Sensor Board using the Lattice EVDK:

1. Connect the LF-EVDK1-EVN board to the DC power adapter (12 V).
2. Connect the board to PC through the USB mini port.
3. Start the Lattice Diamond® Programmer version 3.10 or higher.
4. In the Getting Started dialog box, select the configurations shown in Figure 4.1. Click **OK**.

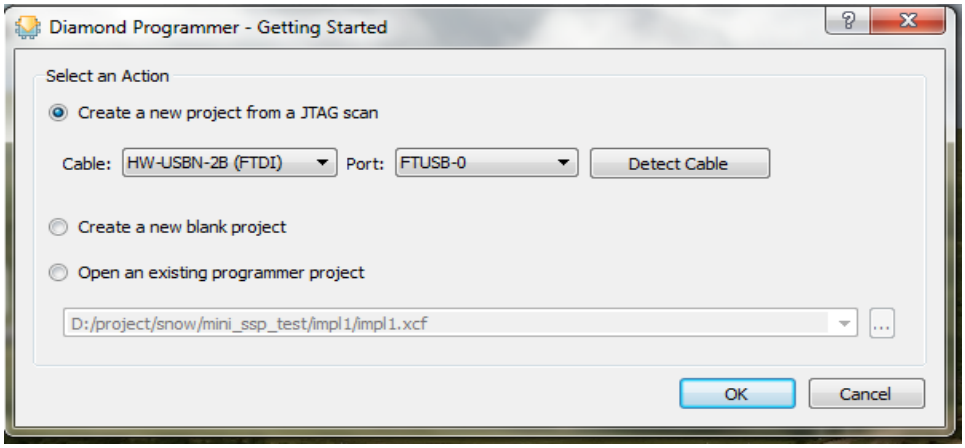



**Figure 4.1. Programming Cable Setup**

5. Select **LIFMD** for Device Family, **LIF-MD6000** for Device, **Fast Program** for Operation, and **mVision_CSI2_2_parallel_impl1.bit** for File Name as shown in Figure 4.5.

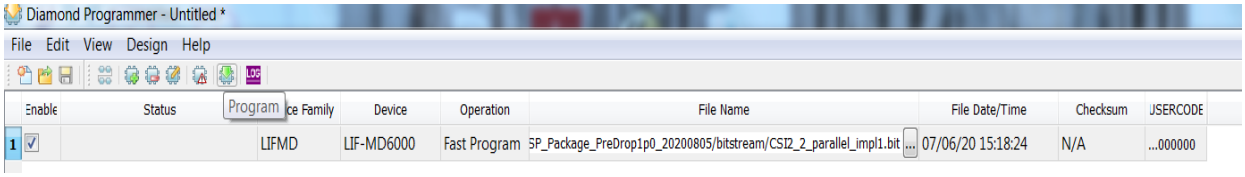



**Figure 4.2. CrossLink Programming Setup**

6. Click the **Program** button to program and check the status.

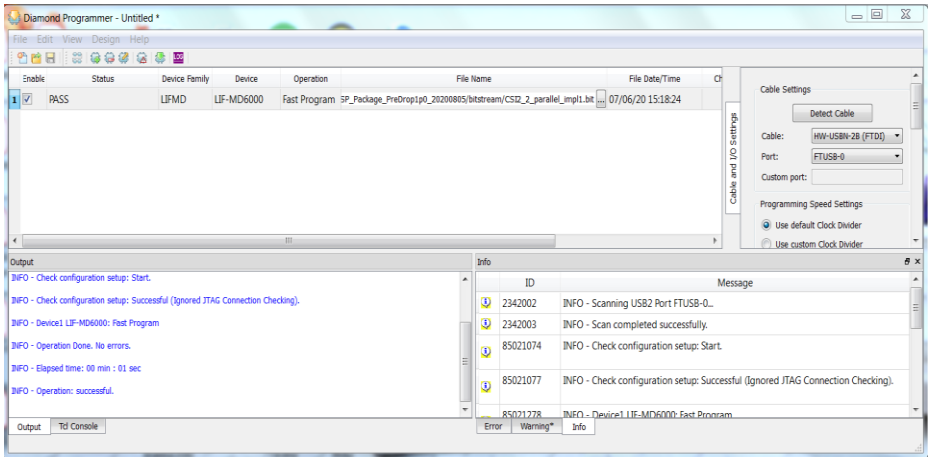



**Figure 4.3. CrossLink Programming Status**

7. Select **ECP5UM** for Device Family, **LFE5UM-85F** for Device, **Fast Program** for Operation, and **mVision_ISP_1080p_impl1.bit** for File Name as shown in Figure 4.4.

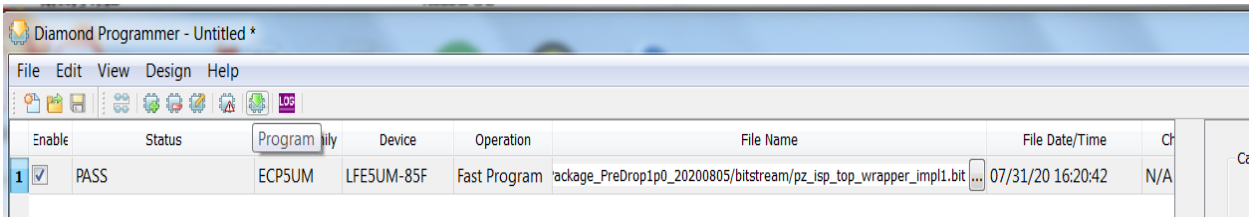



**Figure 4.4. ECP5 Programming Setup**

8. Click the **Program** button to program and check the status.

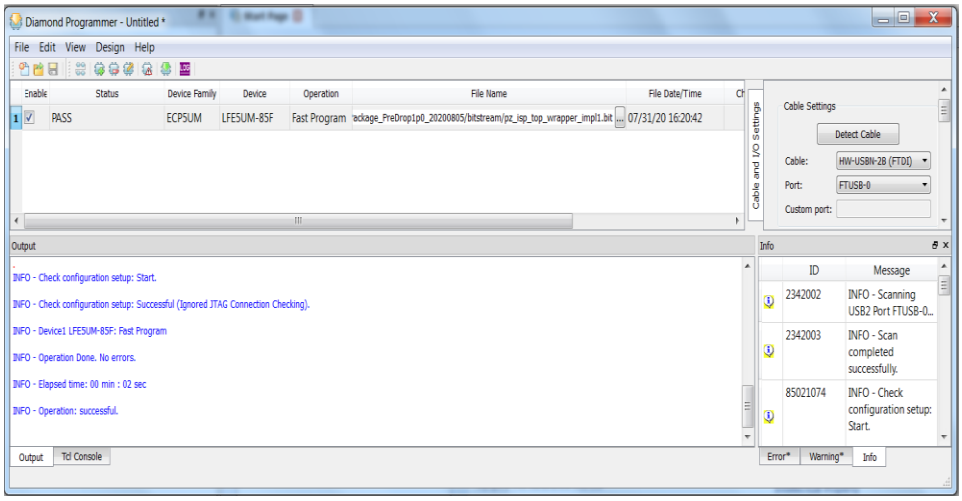



**Figure 4.5. ECP5 Programming Status**

9. Connect the HDMI monitor to the board using the HDMI cable.
10. Toggle the **SW3 (SYS_RST)** button on the Crosslink VIP Bridge Board. The sensor-captured video is displayed on the HDMI monitor.

# 5. Interfaces

## 5.1. J1 Interface

The J1 interface includes power, control, and MIPI signals connection to EVDK.

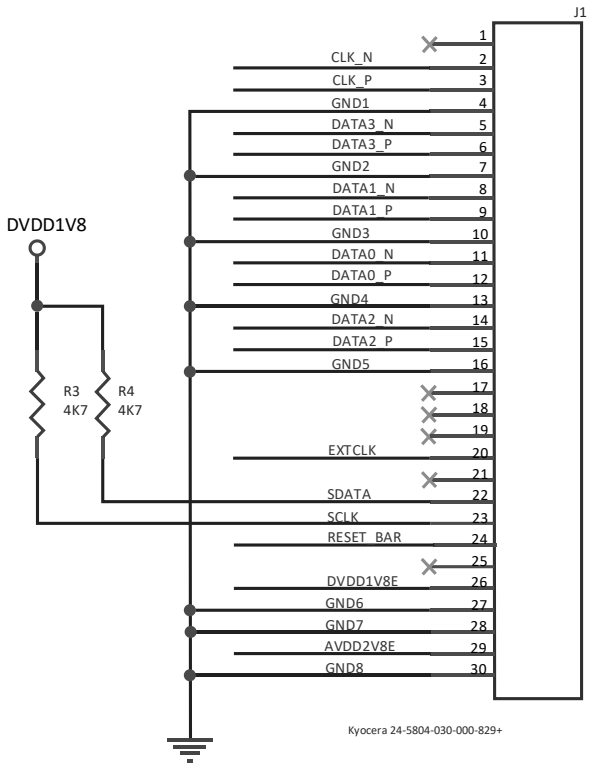



**Figure 5.1. J1 Interface**

## 5.2. External Power Supply Connections

The J5, J7, and J8 headers allow external power supply connection to the sensor board. Using a jumper to short pin 1 and 2 of the J7 header supplies 1.8 V from J1 connector. Using a jumper to short pin 1 and 2 of the J8 header supplies 2.8 V from J1 connector.

To use external supplies, use pin 1 of these headers. Note that 3.3 V supply for IR_CUT circuit is not provided through J1.

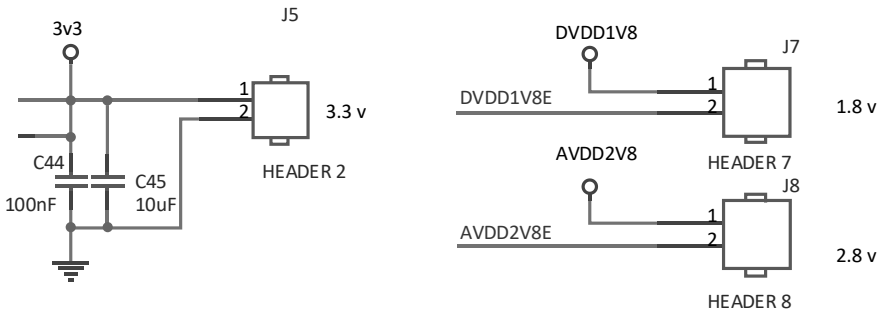



**Figure 5.2. External Power Supply Connections**

## 5.3. Flash and Shutter Control Connections

J2 and J3 allow external control for Shutter and Flash.

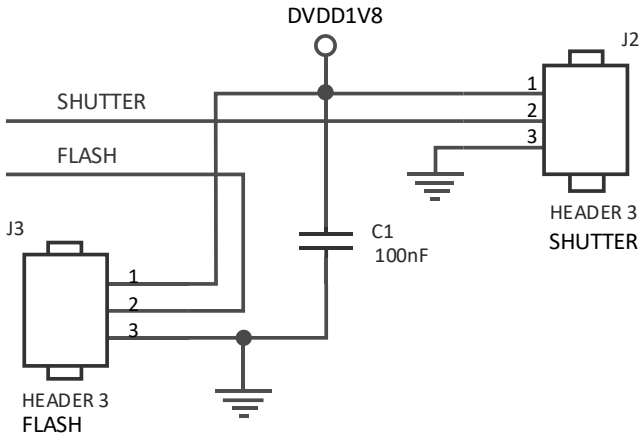



**Figure 5.3. Flash and Shutter Control Connections**

## 5.4. IR_CUT Driver Circuit

Figure 5.4 shows the IR_CUT driver circuit. A 3.3 V supply power must be applied using the J5 header. J6 allows external control of the driver. J4 must be connected to appropriate IR_CUT motor.

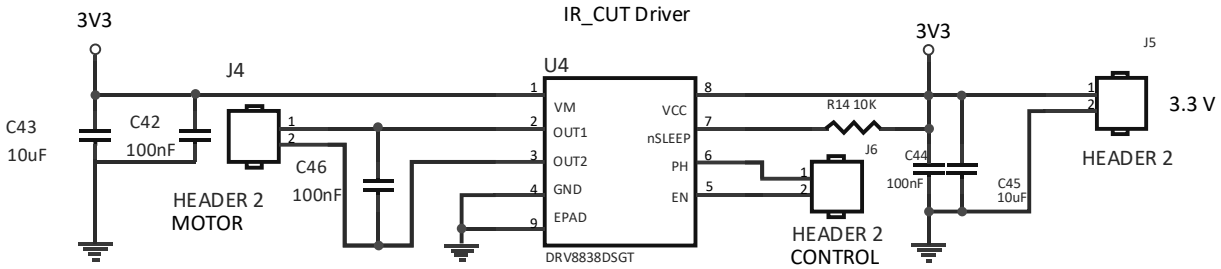



**Figure 5.4. IR_CUT Driver Circuit**

# 6. Electrical Characteristics

## 6.1. Absolute Maximum Ratings

**Table 6.1. Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{SUPPLY}$ | Power Supply Voltage | –0.3 | 4.5 | V |
| $I_{SUPPLY}$ | Total Power Supply Current | — | 200 | mA |
| $I_{GND}$ | Total Ground Current | — | 200 | mA |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{DD}$_IO + 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{DD}$_IO + 0.3 | V |
| $T_{STG}$ | Storage Temperature[2] | –40 | +125 | °C |

**Notes**:
1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur, and reliability may be affected.
2. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 6.2. DC Electrical Characteristics

**Table 6.2. DC Electrical Characteristics**

| Symbol | Definition | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DO}$ | Core Digital Voltage | | 1.14 | 1.2 | 1.26 | V |
| $V_{DD}$_IO | I/O Digital Voltage | | 1.7/2.5 | 1.8/2.8 | 1.9/3.1 | V |
| $V_{DD}$_IO_PHY | I/O Power Supply | | 1.7/2.5 | 1.8/2.8 | 1.9/3.1 | V |
| $V_{AA}$ | Analog Voltage | | 2.5 | 2.8 | 3.1 | V |
| $V_{AA}$_PIX | Pixel Supply Voltage | | 2.5 | 2.8 | 3.1 | V |
| $V_{DD}$_PHY | MIPI Supply Voltage | | 1.14 | 1.2 | 1.26 | V |
| $V_{DD}$_DATA | MIPI Supply Voltage | | 1.14 | 1.2 | 1.26 | V |
| $V_{AA}$_PHY | MIPI Supply Voltage | | 2.5 | 2.8 | 3.1 | V |
| $V_{IH}$ | Input HIGH Voltage | | $V_{DD}$_IO × 0.7 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | | — | — | $V_{DD}$_IO × 0.3 | V |
| $I_{IN}$ | Input Leakage Current | No pull-up resistor; $V_{IN}$ = $V_{DD}$_IO or $D_{GND}$ | 20 | — | — | µA |
| $V_{OH}$ | Output HIGH Voltage | | $V_{DD}$_IO - 0.3 | — | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$_IO = 2.8 V | — | — | 0.4 | V |
| $I_{OH}$ | Output HIGH Current | At specified $V_{OH}$ | –22 | — | — | mA |
| $I_{OL}$ | Output LOW Current | At specified $V_{OL}$ | — | — | 22 | mA |

**Note**: Stresses greater than those listed in Table 6.2 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## 6.3. Operating Current Consumption for MIPI Output

**Table 6.3. Operating Current Consumption for MIPI Output**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$_PHY + $I_{DD}$_DATA + $I_{DD}$ | Digital Operating Current | MIPI, Streaming, Full Resolution 120 fps | TBD | 147 | TBD | mA |
| $I_{DD}$IO_PHY + $I_{DD}$_IO | I/O Digital Operating Current | MIPI, Streaming, Full Resolution 120 fps | TBD | 8 | — | mA |
| $I_{AA}$_PHY + $T_{AA}$ | Analog Operating Current | MIPI, Streaming, Full Resolution 120 fps | TBD | 55 | TBD | mA |
| $I_{AA}$_PIX | Pixel Supply Current | MIPI, Streaming, Full Resolution 120 fps | TBD | 6 | TBD | mA |

**Notes:**
1. ($V_{AA}$ = $V_{AA}$_PIX = $V_{DD}$_IO = 2.8 V; $V_{DD}$ = $V_{DD}$_PHY = 1.2 V; $V_{DDIO}$_PHY = 1.8 V; PLL Enabled and PIXCLK = 90 MHz; $T_A$ = 25 °C; $C_{LOAD}$ = 10 pF)
2. Values in Table 6.3 are subject to change.
3. The following supply rails can be connected together:
   a. $V_{DD}$, $V_{DD}$_PHY, and $V_{DD}$_DATA
   b. $V_{DD}$_IO and $V_{DD}$IO_PHY
   c. $V_{AA}$, $V_{AA}$_PHY, and $V_{AA}$_PIX

## 6.4. Standby Current Consumption

**Table 6.4. Standby Current Consumption**

| Definition | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Apply XSHUTDOWN (Clock Off) | Analog, 2.8 V | TBD | 10 | TBD | µA |
| | Digital, 1.8 V | TBD | 40 | TBD | µA |
| Apply XSHUTDOWN (Clock On) | Analog, 2.8 V | TBD | 25 | TBD | µA |
| | Digital, 1.8 V | TBD | 55 | TBD | µA |
| Soft Standby (Clock Off, Driven Low) | Analog, 2.8 V | TBD | 15 | TBD | µA |
| | Digital, 1.8 V | TBD | 270 | TBD | µA |
| Soft Standby (Clock On, EXTCLK = 27 MHz) | Analog, 2.8 V | TBD | 70 | TBD | µA |
| | Digital, 1.8 V | TBD | 2600 | TBD | µA |

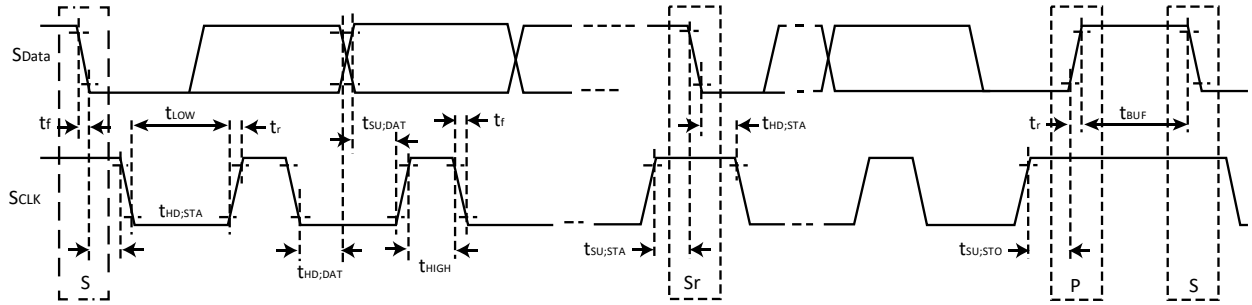
**Notes:**
1. (Analog = $V_{AA}$ + $V_{AA}$_PIX + $V_{AA}$_PHY; Digital = $V_{DD}$ + $V_{DD}$_IO + $V_{DD}$_PHY + $V_{DDIO}$_PHY + $V_{DD}$_DATA; $T_A$ = 25 °C)
2. Values in Table 6.4 are subject to change.

## 6.5. Two-Wire Serial Bus Timing Parameters

Unless otherwise stated, the following specifications apply to the following conditions:

- $V_{DD}$ = $V_{DD}$_PHY = $V_{DD}$_DATA = 1.2 V +/-0.06;
- $V_{DD}$_IO = $V_{AA}$ = $V_{AA}$_PIX = 2.8 V +/-0.3 V; $V_{DDIO}$_PHY = 1.8 V +/-0.1 V
- $T_A$ = −40 °C to + 105 °C;
- Output Load = 10 pF;
- PIXCLK Frequency = 90 MHz;
- MIPI off

The electrical characteristics of the two−wire serial register interface ($S_{CLK}$, $S_{DATA}$) are shown in Figure 6.1 and Table 6.5.




NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

**Figure 6.1. Two-Wire Serial Bus Timing Parameters Diagram**

## 6.6. Two-Wire Serial Bus Characteristics

**Table 6.5. Two-Wire Serial Bus Characteristics**

| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $S_{CLK}$ Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Hold Time (Repeated) START Condition (after this period, the First Clock Pulse is generated) | $t_{HD;STA}$ | 4.0 | — | 0.6 | — | µs |
| LOW Period of the $S_{CLK}$ Clock | $t_{LOW}$ | 4.7 | — | 1.3 | — | µs |
| HIGH Period of the $S_{CLK}$ Clock | $t_{HIGH}$ | 4.0 | — | 0.6 | — | µs |
| Set-Up Time for a Repeated START Condition | $t_{SU;STA}$ | 4.7 | — | 0.6 | — | µs |
| Data Hold Time | $t_{HD;DAT}$ | 0[5] | 3.45[6] | 0[7] | 0.9[6] | µs |
| Data Set-Up Time | $t_{SU;DAT}$ | 250 | — | 100[7] | | µs |
| Rise Time of both $S_{DATA}$ and $S_{CLK}$ Signals | $t_r$ | — | 1000 | 20 + 0.1 Cb[8] | | µs |
| Fall Time of both $S_{DATA}$ and $S_{CLK}$ Signals | $t_f$ | — | 300 | 20 + 0.1 Cb[8] | | µs |
| Set-Up Time for STOP Condition | $t_{SU;STO}$ | 4.0 | — | 0.6 | — | µs |
| Bus Free Time between a STOP and START Condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Capacitive Load for each Bus Line | $C_b$ | — | 400 | — | 400 | pF |
| Serial Interface Input Pin Capacitance | CIN_SI | — | 3.3 | — | 3.3 | pF |
| $S_{DATA}$ Max Load Capacitance | CLOAD_SD | — | 30 | — | 30 | pF |
| $S_{DATA}$ Pull-Up Resistor | RSD | 1.5 | 4.7 | 1.5 | 4.7 | kΩ |

**Notes:**

1. ($f_{EXTCLK}$ = 27 MHz; $V_{DD}$ = 1.2 V; $V_{DD}$_IO = 2.8 V; $V_{AA}$ = 2.8 V; $V_{AA}$_PIX = 2.8 V; $V_{DD}$_PHY = 1.2 V; $V_{DDIO}$_PHY = 1.8 V; $T_A$ = 25 °C)
2. This table is based on $I^2C$ standard (v2.1 January 2000) Philips Semiconductor.
3. Two-wire control is $I^2C$-compatible.
4. All values referred to $V_{IHmin}$ = 0.9 V $V_{DD}$_IO and $V_{ILmax}$ = 0.1 $V_{DD}$_IO levels. Sensor EXCLK = 27 MHz.
5. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK. The two-wire standard specifies a minimum rise and fall time for Fast Mode operation. This specification is not a timing requirement that is enforced on ON Semiconductor sensor's as a receiver, because our receivers are designed to work in mixed systems with std-mode where no such minimum rise and fall times are required/specified. However, it is the host's responsibility when using fast edge rates, especially when two-wire slew-rate driver control is not available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current-clamping circuits. This is typically not an issue in most applications., but should be checked if below minimum fall times and rise times are required. A device must internally provide a hold time of at least 300 ns for the $S_{DATA}$ signal to bridge the undefined region of the falling edge of $S_{CLK}$.

6. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW}$) of the $S_{CLK}$ signal.
7. A Fast mode $I^2C$ bus device can be used in a standard mode I2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the $S_{CLK}$ signal. If such a device does stretch the LOW period of the $S_{CLK}$ signal, it must output the next data bit to the $S_{DATA}$ line $t_f$ max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode $I^2C$ bus specification) before the $S_{CLK}$ line is released.
8. Cb = total capacitance of one bus line in pF.

# 7. Power-On Reset and Standby Timing

## 7.1. Power-Up Sequence

The recommended power-up sequence for the AR0234 is shown in Figure 7.1. The available power supplies (VAA/VAA_PIX/VAA_PHY, VDDIO, VDDIO_PHY, VDD/VDD_PHY, and VDD_DATA) must have the separation specified below.

- Turn on VAA/VAA_PIX/VAA_PHY power supply.
- After 100 µs, turn on VDDIO power supply.
- After 100 µs, turn on VDDIO_PHY (1.8 V) power supply.
- After 100 µs, turn on VDD/VDD_PHY power supply.
- After 100 µs, turn on VDD_DATA power supply.
- After the last power supply is stable, enable EXTCLK.
- Assert RESET_N for at least 1 ms. The parallel interface is tristated during this time.
- Wait for ~150000 EXTCLKs for internal initialization into soft standby where M3ROM and full OTPM upload is complete.
- Set streaming mode (mode_select/stream (R0x301A[2]) = 1) and the internal PLL is enabled (not locked yet).
- Wait for 1 ms for PLL lock to complete, and then part goes into streaming mode.

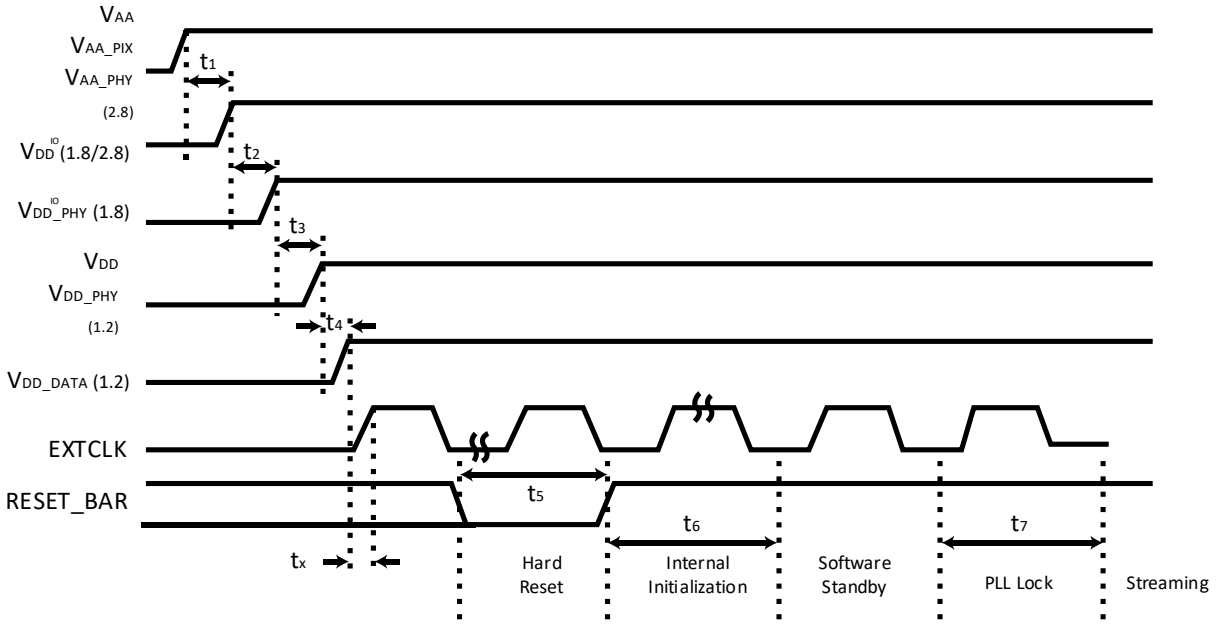



**Figure 7.1. Power-up Sequence**

**Table 7.1. Power-up Sequence**

| SN | Definition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $V_{AA}$/$V_{AA}$_PIX/$V_{AA}$_PHY to $V_{DD}$IO | $t_1$ | 0 | 100 | — | µs |
| 2 | $V_{DD}$IO to $V_{DD}$IO_PHY | $t_2$ | 0 | 100 | — | µs |
| 3 | $V_{DD}$IO_PHY to $V_{DD}$/$V_{DD}$_PHY | $t_3$ | 0 | 100 | — | µs |
| 4 | $V_{DD}$/$V_{DD}$_PHY to $V_{DD}$_DATA | $t_4$ | 0 | 100 | — | µs |
| 5 | Xtal Settle Time (Component Dependent) | $t_x$ | — | 30 ms | — | ms |
| 6 | Hard Reset | $t_5$ | 1 | — | — | ms |
| 7 | Internal Initialization | $t_6$ | 16000 | — | — | EXTCLK |
| 8 | PLL Lock Time | $t_7$ | 1 | — | — | ms |

**Notes:**
1. $V_{DD}$ and $V_{DD}$_DATA can be tied together ($t_4$ becomes *0* in this case).
2. $V_{AA}$/$V_{AA}$PIX/$V_{AA}$_PHY can be tied together.

## 7.2. Power-Down Sequence

The recommended power-down sequence for the AR0234 is shown in Figure 9. The available power supplies (VAA/VAA_PIX/VAA_PHY, VDDIO, VDDIO_PHY, VDD/VDD_PHY, and VDD_DATA) must have the separation specified below.

Disable streaming if output is active by setting standby R0x301a[2] = 0.

The soft standby state is reached after the current row or frame, depending on configuration, has ended.

- Turn off VDD_DATA.
- Turn off VDD/VDD_PHY.
- Turn off VDDIO_PHY.
- Turn off VDDIO.
- Turn off VAA/VAA_PIX/VAA_PHY

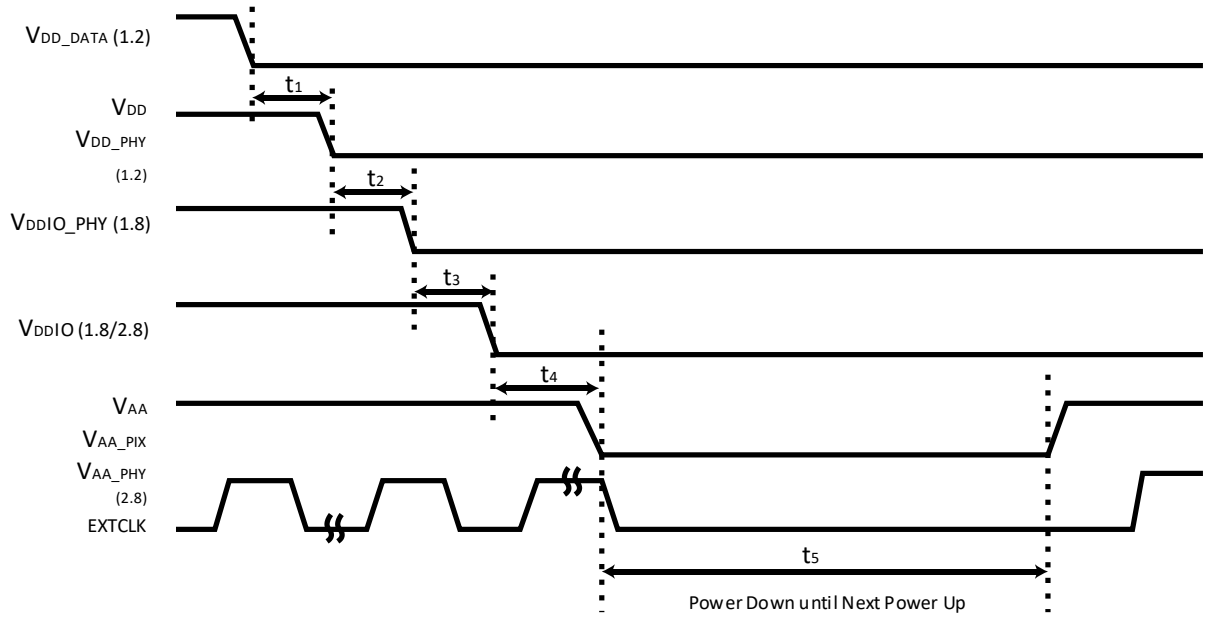



**Figure 7.2. Power-down Sequence**

**Table 7.2. Power-down Sequence**

| SN | Definition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $V_{DD}$_DATA to $V_{DD}$/$V_{DD}$_PHY | $t_1$ | 0 | — | — | — |
| 2 | $V_{DD}$/$V_{DD}$_PHY to $V_{DD}$IO_PHY | $t_2$ | 0 | — | — | — |
| 3 | $V_{DD}$IO_PHY to $V_{DD}$IO | $t_3$ | 0 | — | — | — |
| 4 | $V_{DD}$IO to $V_{AA}$/$V_{AA}$_PIX/$V_{AA}$_PHY | $t_4$ | 0 | — | — | — |
| 5 | PwrDn until next PwrUp Time | $t_5$ | 100 | — | — | ms |

**Notes:**
1. $V_{DD}$ and $V_{DD}$_DATA can be tied together.
2. $V_{AA}$/$V_{AA}$PIX/$V_{AA}$_PHY can be tied together.

# References

For more information, refer to Lattice mVision ISP Reference Design Quick Start Guide (FPGA-AN-02034).

# Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

# Revision History

**Revision 1.1, February 2022**

| Section | Change Summary |
|---|---|
| All | Minor adjustments in formatting across the document. |
| Introduction | Updated Figure 1.1 and Figure 1.2. |
| Required Components | Added this section. |
| Headers and Jumpers | Added this section. |
| Programming the Board | Added this section. |

**Revision 1.0, March 2021**

| Section | Change Summary |
|---|---|
| All | Initial release |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