LPTM21L Evaluation Board

User Guide

FPGA-EB-02026-2.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ASC	Analog Sense and Control (such as the L-ASC10 device)
CC	Central Controller
DIP	Dual in-line Package
FPGA	Field Programmable Gate Array
FTDI	Future Technology Devices International
HE	Hardware Expander
I^2C	Inter-Integrated Circuit
LED	Light Emitting Diode
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances Directive
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

1. Introduction

The LPTM21L Evaluation Board is designed to function as either a Platform Manager 2 central controller (CC) or a Platform Manager 2 hardware expander (HE). This is to demonstrate that the LPTM21L device itself can be used as either a CC or HE. The LPTM21L Evaluation Board has support circuits and jumpers to configure the board for a variety of Platform Manager 2 designs. A single board can be used as a central controller. Two boards can be used with one as the central controller and the second as a hardware expander. Scalability is one of the key features of the LPTM21L and up to four boards can be connected to monitor 40 rails; one board is the central controller and the other three are hardware expanders.

2. Features

The LPTM21L (100-ball csBGA) Evaluation Board has the following features:

- Three D25 male connectors to control additional hardware expanders (ASC Breakout or LPTM21L Evaluation boards)
- One D25 female connector to function as a hardware expander
- FTDI USB support of JTAG and I^2C
- SPI memory to support dual-boot or fault logging
- Ten Red LEDs to indicate the GPIO status
- 25 amber LEDs to indicate the DIO status
- Two slider potentiometers to simulate power supply outputs
- Eight-position DIP switch to set the ASC section I^2C address
- Two tactile push button switches
- Four-position DIP switch to set the FPGA section I^2C address
- Thru-hole and SMD prototyping area

These features and more are identified in Figure 2.1 and Figure 2.2.

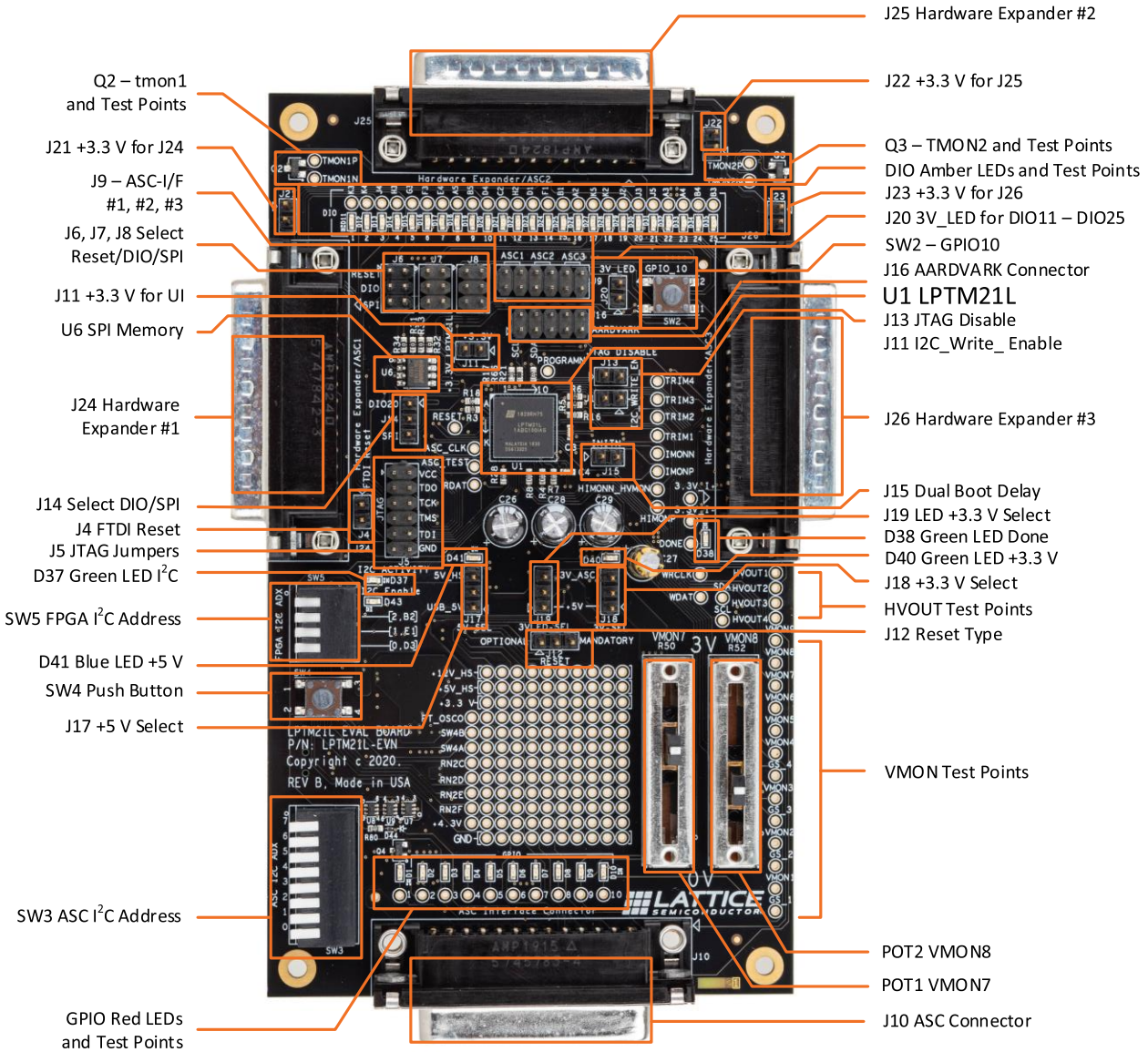

Figure 2.1. LPTM21L Evaluation Board Features on Top

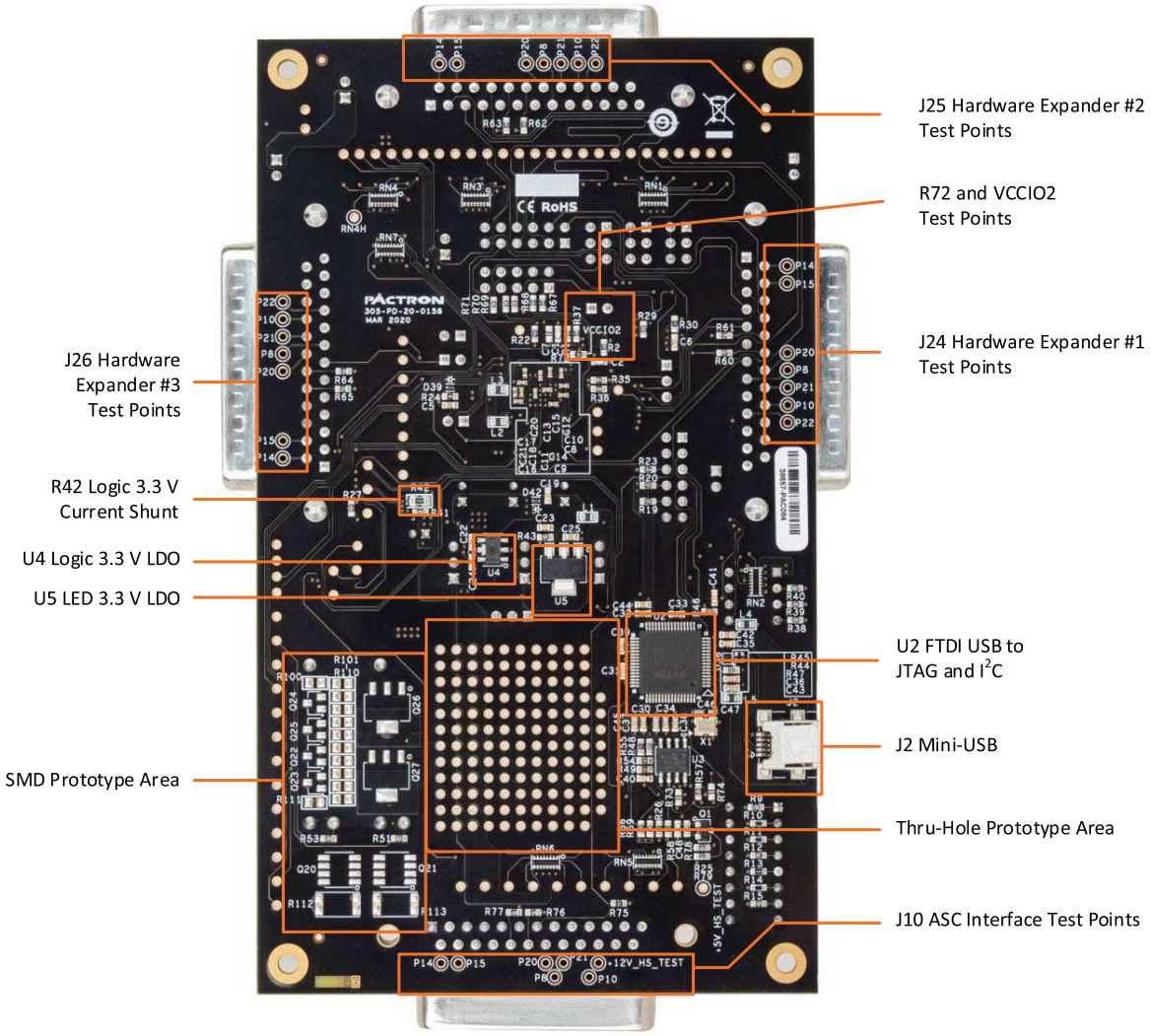

Figure 2.2. LPTM21L Evaluation Board Features on Bottom

3. Factory Default Board Settings

The board has many jumpers and options to support both the central controller and hardware expander functions of the LPTM21L. This section is provided so the user can restore the board to the factory default settings and reprogram the LPTM21L with the default demo. Table 3.1 and Table 3.2 list the factory default settings for the jumpers and DIP switches.

After restoring the jumpers and switches, connect the board to a USB cable that is also connected to the computer with Diamond Programmer installed. If the USB port is powered then the blue LED (D41) should be on to indicate that +5 V is being provided. Also, the green LED (D40) should be on to indicate that +3.3 V is also active.

Table 3.1. Factory Default Jumper Settings

Jumper	Installed on Pins	Connection/Description
J5	3 to 4	TDO to LPTM21L
J5	5 to 6	TCK to LPTM21L
J5	7 to 8	TMS to LPTM21L
J5	9 to 10	TDI to LPTM21L
J6	3 to 4	DIO17 to LPTM21L
J7	3 to 4	DIO18 to LPTM21L
J8	3 to 4	DIO19 to LPTM21L
J11	1 to 2	+3.3 V to LPTM21L
J12	2 to 3	Mandatory Reset
J14	1 to 2	DIO20 to LPTM21L
J17	1 to 2	USB +5 V to 3.3 V LDO (U4)
J18	1 to 2	+5 V is +3.3 V main source
J19	1 to 2	+5 V is +3.3 V_LED main source
J20	1 to 2	+3.3V_LED to DIO11 to DIO25 LEDs
J21	1 to 2	+3.3 V to Hardware Expander 1
J22	1 to 2	+3.3 V to Hardware Expander 2
J23	1 to 2	+3.3 V to Hardware Expander 3

Table 3.2. Factory Default Dip Switch Settings

Dip Switch	Setting	Description
SW3	Only the *0* switch down	ASC_I2C_ADX = 0x60
SW5	All Up	FPGA_I2C_ADX = 0x20

To reprogram the LPTM21L with the quick start demo:

1. Create a new blank project in Diamond Programmer as shown in Figure 3.1.

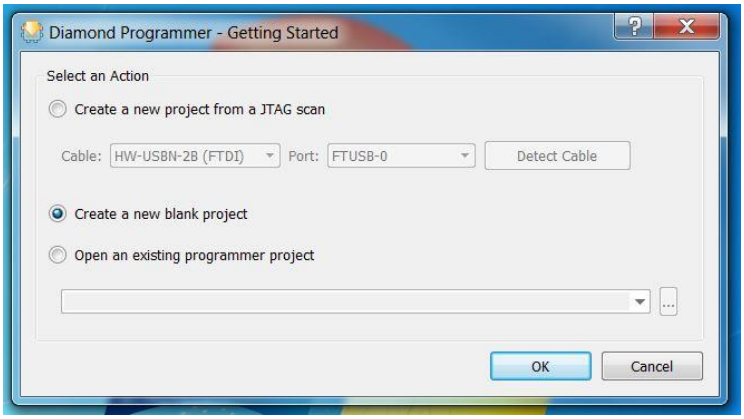

Figure 3.1. Diamond Programmer New Blank Project

2. Select **Platform Manager 2** from the drop-down list under **Device Family**.
3. Select **LPTM21L** from the drop-down list under **Device**.
4. Double-click FLASH Erase,Program,Verify under Operation.
5. The **Device Properties** dialog box opens as shown in Figure 3.2. Browse to the folder where the **LPTM21L_Test_Quick_Start_RevB.jed** file is located and click **OK**.

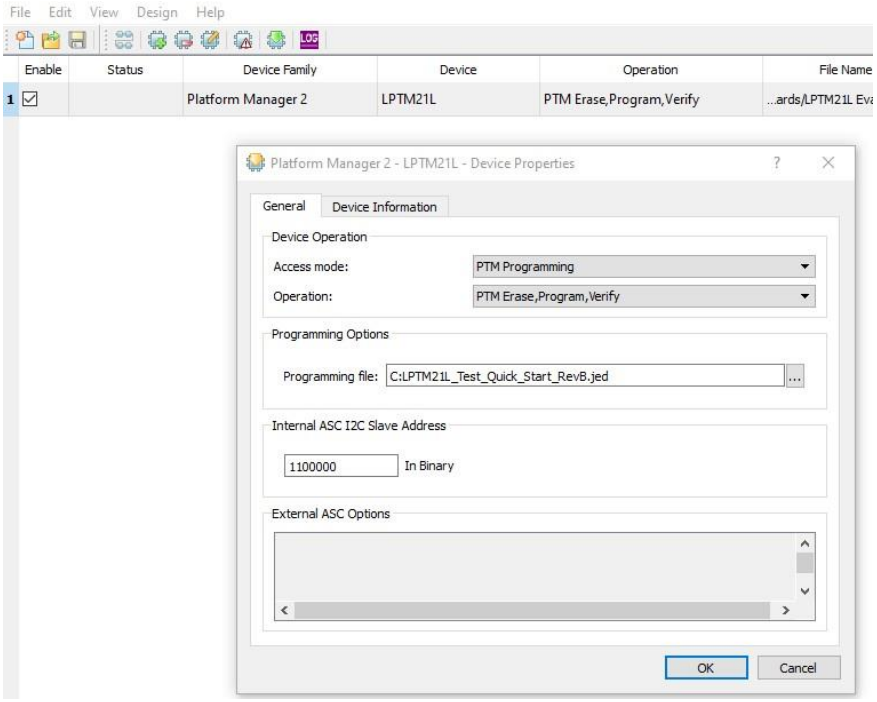

Figure 3.2. Diamond Programmer Device Properties

6. In the menu bar, click **Design > Program** or click on the **Program** tool icon shown in Figure 3.3 to re-program the LPTM21L with the factory default quick start design.

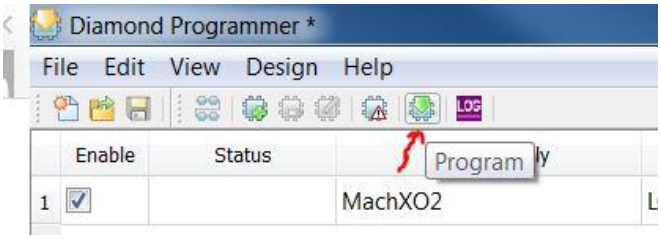

Figure 3.3. Diamond Programmer - Program Tool

When programming is complete the **Status** displays **PASS** if no errors were detected.

Once the quick start design is loaded into the LPTM21L the amber LEDs turn on and off - scanning back and forth. Only the DIO5 thru DIO20 LEDs scan back and forth. Seven of red LEDs are also on (GPIO1 – GPIO6, and GPIO10) and three red LEDs are off (GPIO7 – GPIO9); indicating the ASC section is in the safe state (ASC-I/F is not active). The scanning back and forth of the amber LEDs (DIO5 thru DIO20) stops under the following conditions:

- The LPTM21L is erased and reprogrammed with a user design
- The LPTM21L is a hardware expander and the ASC-I/F from the central controller is active

DIO1 thru DIO4 LEDs display four of the bits of the FPGA I^2C address as set by the FPGA_I2C_ADX DIP switch (SW5). Table 3.3 lists the SW5 settings, corresponding LEDs, and resulting FPGA I^2C address. With SW5 in the factory default setting (all up), the only LED turned on is DIO4, which corresponds to an I^2C address of 0x20.

Table 3.3. Quick Start FPGA Address Settings and Corresponding LED Bits

SW5			LED (1= On, 0 = Off)				FPGA I^2C Address
A2	A1	A0	DIO1	DIO2	DIO3	DIO4	
Up	Up	Up	0	0	0	1	0x20
Up	Up	Dn	1	0	0	1	0x24
Up	Dn	UP	0	1	0	1	0x28
Up	Dn	Dn	1	1	0	1	0x2C
Dn	Up	Up	0	0	1	1	0x30
Dn	Up	Dn	1	0	1	1	0x34
Dn	Dn	Up	0	1	1	1	0x38
Dn	Dn	Dn	1	1	1	1	0x3C

In order to set and keep the FPGA I^2C address stored in the feature row the following steps must be followed:

1. With power removed from the board set the desired address using SW5.
2. Apply power to the board and verify the address with DIO1 – DIO4 LEDs.
3. In Diamond Programmer use the **FLASH CFG Erase,Program,Verify** operation as shown in Figure 3.4 to configure the FPGA section with a user pattern but, not erase and reprogram the feature row. Additionally, the **FLASH CFG and UFM Erase, Program Verify** operation can be used and retain the I^2C address.

With a new pattern in the FPGA the DIO1 – DIO4 LEDs no longer display the FPGA I^2C address. However, as long as a bulk erase or feature row erase is not performed, the FPGA I^2C address remains intact.

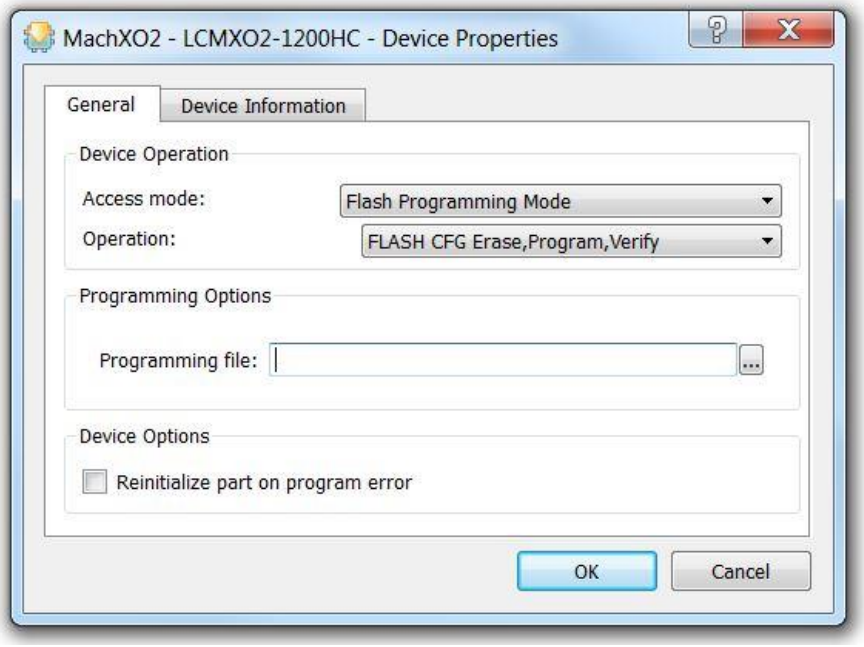

Figure 3.4. Diamond Programmer CFG Erase, Program, Verify Operation

4. Applying Power to the Board

Because the board has been designed to operate as either the central controller (CC) or as a hardware expander (HE), the applied power can be easily configured with jumpers to support any of the following scenarios:

- Central controller: USB_5V from USB cable (factory default)
- Central controller: +5V_HS from hardware expander interface
- Central controller: +3.3V from hardware expander interface
- Hardware expander: +3.3V_ASC from ASC interface

Table 4.1 lists the specific jumper settings to support the power source being used. Note that if 3.3V is being supplied to the central controller from one of the hardware expanders, then the corresponding 2-pin jumper must also be in place (J21 – J23).

Table 4.1. Jumper Settings to Support the Various Power Sources

Mode	J17	J18	J19	Power Net	Power Connection
CC	1 to 2	1 to 2	1 to 2	USB_5V	J2
CC	2 to 3	1 to 2	1 to 2	+5V_HS	J24, J25, or J26
CC	2 to 3	1 to 2	1 to 2	+3.3V +3.3V +3.3V	J24 and J21 J25 and J22 J26 and J23
HE	n/c	2 to 3	2 to 3	+3.3V_ASC	J10

The green LED (D40) will be on when +3.3 V is active and the blue LED (D41) will be on when +5 V is being provided.

5. Electrical, Mechanical, and Environmental Specifications

Electrical Specifications

- 5 V input +/- 10 % : less than 1 Amp (from USB, or any of the D25 connectors)
- 3.3 V input +/- 10% : less than 1 Amp (from any of the D25 connectors)

Mechanical Specifications

Dimensions: 6.5 in. [L] x 4 in. [W] x 1 in. [H]

Environmental Specifications

- Operation temperature: 0 deg. C to 55 deg. C
- Storage temperature: -40 deg. C to 100 deg. C
- Humidity: < 95% without condensation

6. Jumpers

The LPTM21L evaluation board can function as either a central controller (CC) or hardware expander (HE) so several jumpers are provided to support a wide range of platforms and applications. In each of the following tables a **Silkscreen** column is included if the board has corresponding silkscreen text next to the jumper to aid in setting up the board.

6.1. Power Jumpers

While Table 4.1 in the Applying Power to the Board section provided a summary of settings to power up the board, this section provides explicit details of all the power jumpers on the board. Power can be supplied by either the central controller or the hardware expander regardless of the function of the LPTM21L.

Table 6.1 details the jumper J17 settings that select the +5 V source, if it is used.

Table 6.1. J17 Jumper Settings for +5 V Power Select

J17	Silkscreen	+5V Power Select	Mode
Removed		+5V is not used to power the board	CC / HE
Pin 1 to Pin 2	USB_5V	+5V is provided by the USB connector (J2)	CC
Pin 2 to Pin 3	5V_HS	+5V is provided from a hardware expander (J24, J25, J26)	CC

Table 6.2 details the jumper J18 settings that select the +3.3 V power for the LPTM21L and SPI memory.

Table 6.2. J18 Jumper Settings for +3.3 V Power Select

J18	Silkscreen	+3.3V Power Select	Mode
Removed		+3.3 V is provided from a Hardware Expander (J24, J25, J26)	CC
Pin 1 to Pin 2	+5V	+3.3 V is provided from LDO (U4 powered from +5V)	CC
Pin 2 to Pin 3	3V_ASC	+3.3 V is provided from the ASC Connector (J10)	HE

Table 6.3 details the jumper J11 settings to power the LPTM21L. J11 is provided to monitor the current consumed by the LPTM21L (U1). To measure the current remove the jumper and attach a current meter. Also, off board power can be used to power only the LPTM21L by connecting power to pin 2 while the rest of the board is powered from the sources described in this section.

Table 6.3. J11 Jumper Settings for LPTM21L Power

J11	Silkscreen	+3.3V Power Select	Mode
Removed	—	U1 is powered from off board by pin 2 of J11	CC/HE
Pin 1 to Pin 2	—	U1 is powered from the 3.3 V on board	CC/HE

Table 6.4 details the jumper J19 settings to power the LEDs on the board. A separate +3.3 V supply rail is provided for the LEDs to support fault logging. The separate rail prevents the LED load from draining the hold-up capacitors (C27, C28, and C29) when power is removed. The SPI memory and LPTM21L are powered by the hold-up capacitors to store the fault record as power is failing. VMON5 can be used for early detection that +5 V has been removed and start the shutdown and fault logging processes.

Table 6.4. J19 Jumper Settings for LED Power

J19	Silkscreen	+3.3V_LED Power Select	Mode
Removed	—	+3.3V_LED is not provided and all I/O LEDs are off	CC / HE
Pin 1 to Pin 2	+5V	+3.3V_LED is provided from LDO (U5 powered from +5V)	CC
Pin 2 to Pin 3	3V_ASC	+3.3V_LED is provided from the ASC Connector (J10)	HE

Table 6.5 details the jumper J20 settings to power LEDs connected to DIO11 thru DIO25. Since DIO11 thru DIO25 have dual functions, it may be desirable to disable the LEDs associated with these I/O. Jumper J20 can be removed and the amber LEDs will remain off while the DIO11 thru DIO25 outputs are used for non-sequencing functions. J20 should be installed to power the amber LEDs when DIO11 thru DIO25 are being used as Platform Management I/O; the LEDs will turn on when a low is output.

Table 6.5. J20 Jumper Settings for DIO11 – DIO25 LED Power

J20	+3.3V_LED Power for DIO11 – DIO25	Mode
Removed	+3.3V_LED is not provided to the LEDs for DIO11 – DIO25	CC / HE
Installed	+3.3V_LED is provided to the LEDs for DIO11 – DIO25	CC / HE

Table 6.6 details the jumper settings for J21, J22, and J23. These jumpers are used in conjunction with their respective Hardware Expander connectors.

Table 6.6. J19 Jumper Settings for LED Power

Jumper	+3.3V To/From Hardware Expander	Mode
J21	Install to connect +3.3V to hardware expander #1 (J24)	CC
J22	Install to connect +3.3V to hardware expander #2 (J25)	CC
J23	Install to connect +3.3V to hardware expander #3 (J26)	CC

6.2. USB/JTAG/I²C Jumpers

This section describes the jumpers that support USB, JTAG, and I²C communications.

Table 6.7 details the jumper J5 settings to support JTAG. These jumpers should be installed for JTAG programming but can be removed if JTAG programming is not used.

Table 6.7. J5 Jumper Settings for JTAG Support

J5	Silkscreen	JTAG	Mode
Pin 1, 2	VCC	+3.3 V	CC / HE
Pin 3 to Pin 4	TDO	Installed – TDO connected to FTDI	CC
		Removed – DIO22 available w/JTAG disabled	CC / HE
Pin 5 to Pin 6	TCK	Installed – TCK connected to FTDI	CC
		Removed – DIO23 available w/JTAG disabled	CC / HE
Pin 7 to Pin 8	TMS	Installed – TMS connected to FTDI	CC
		Removed – DIO24 available w/JGAG disabled	CC / HE
Pin 9 to Pin 10	TDI	Installed – TDI connected to FTDI	CC
		Removed – DIO25 available w/JTAG disabled	CC / HE
Pin 11, 12	GND	Ground	CC / HE

Table 6.8 details the jumper J13 settings to support JTAG disable. The JTAGENB pin is not active by default and is typically available as a FPGA section I/O. The JTAGENB pin is activated when the JTAG_PORT is disabled in the Spreadsheet (Global Preferences tab) view in Diamond software as shown in Figure 6.1.

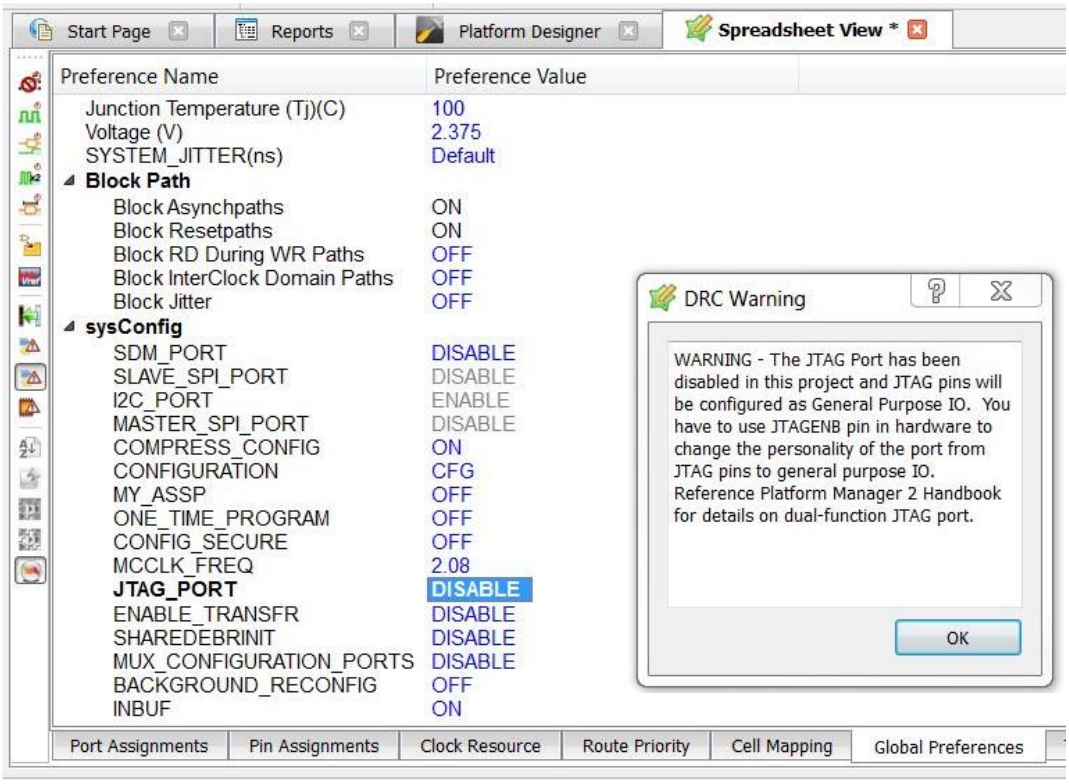

Figure 6.1. JTAG Port Disabled in Diamond Spreadsheet View

When the JTAG port is disabled, the JTAGENB pin must be pulled low to disable the JTAG function while DIO22 thru DIO25 are being used as LPTM21L I/O. The jumper can be removed to enable the JTAG interface on DIO22 thru DIO25.

Table 6.8. J13 Jumper Settings for JTAGENB Support

J13	JTAG Disable	Mode
Removed	JTAG interface is enabled	CC
Pin 1 to Pin 2	JTAG interface is disabled*	CC

***Note:** JTAG interface is only disabled with the jumper if the device has been configured as described in the text above.

Table 6.9 details the jumper J4 settings to support resetting the FTDI chip (U2).

Table 6.9. J4 Jumper Settings for FTDI Reset

J4	FTDI Reset	Mode
Removed	FTDI U2 is not reset	CC / HE
Pin 1 to Pin 2	FTDI U2 is reset and it's I/O are disabled	CC / HE

Table 6.10 details the jumper J1 settings to support the I²C write protect feature. The Platform Designer tool in Diamond can be used to enable the LPTM21L I²C write protect feature, as shown in Figure 6.2. The software provides three modes of I²C write control:

- always enabled,
- always disabled (except programming mode)
- controlled by GPIO1

When I²C writes are enabled by GPIO1, J1 can be used to connect with DIO10. When J1 is installed DIO10 can be driven by logic to enable or disable I²C writes. When DIO10 is logic 1 I²C writes are enabled and when it is logic 0 writes are disabled.

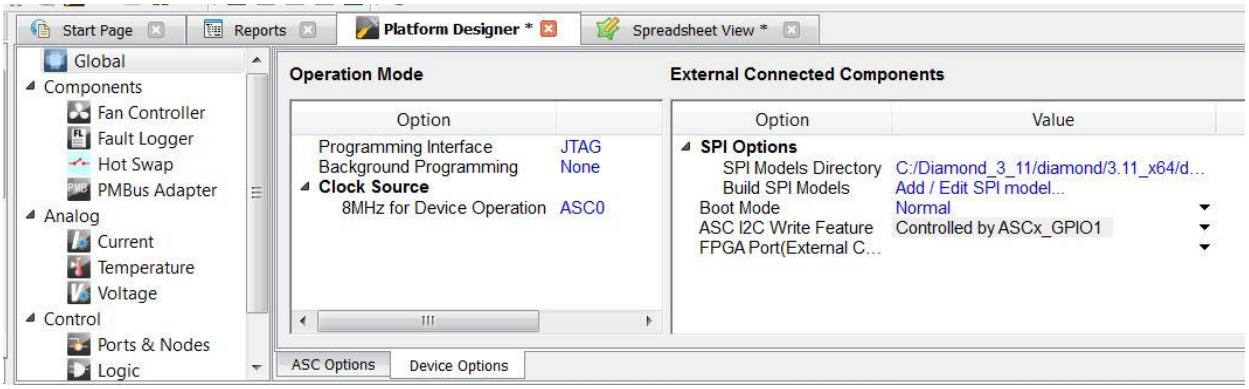

Figure 6.2. I²C Write Protect Enabled in Diamond Platform Designer Global View

Table 6.10. J1 Jumper Settings for I²C Write Enable

J1	I²C Write Enable	Mode
Removed	I²C Write Enable / Protect is not used	CC / HE
Pin 1 to Pin 2	I²C Write is Enabled by DIO10	CC / HE

6.3. Reset / DIO / SPI Jumpers

This section describes jumpers that are used to select the function of several LPTM21L pins. The function supported by the pins depends on the mode of the LPTM21L (CC or HE) and the specific application. In general the jumpers allow the selection between the following: optional reset, digital I/O, and SPI support.

Table 6.11 details the jumper J6 settings for LPTM21L (U1) pin K5. This pin can be used for the three following different functions: 1) as an optional reset input RST_1 from Hardware Expander, 2) general purpose digital I/O DIO17, and 3) SPI memory interface support SISPI.

Table 6.11. J6 Jumper Settings for RST_1 / DIO17 / SISPI Support

J6	Reset/DIO/ SPI	Mode
Pin 1 to Pin 2	Hardware Expander RST_1 Optional Reset	CC
Pin 3 to Pin 4	DIO17	CC / HE
Pin 5 to Pin 6	SISPI (SPI Memory Support)	CC

Table 6.12 details the jumper J7 settings for LPTM21L (U1) pin K2. This pin can be used for the three following different functions: 1) as an optional reset input RST_2 from Hardware Expander, 2) general purpose digital I/O DIO18, and 3) SPI memory interface support SPISO.

Table 6.12. Jumper Settings for RST_2/DIO18/SPISO Support

J7	Reset/DIO/ SPI	Mode
Pin 1 to Pin 2	Hardware Expander 2 Optional Reset	CC
Pin 3 to Pin 4	DIO18	CC / HE
Pin 5 to Pin 6	SPISO (SPI Memory Support)	CC

Table 6.13 details the jumper J8 settings for LPTM21L (U1) pin J2. This pin can be used for the three following different functions: 1) as an optional reset input RST_3 from Hardware Expander, 2) general purpose digital I/O DIO19, and 3) SPI memory interface support CSSPIN.

Table 6.13. J8 Jumper Settings for RST_3/DIO19/CSSPIN Support

J8	Reset/DIO/SPI	Mode
Pin 1 to Pin 2	Hardware Expander 3 Optional Reset	CC
Pin 3 to Pin 4	DIO19	CC / HE
Pin 5 to Pin 6	CSSPIN (SPI Memory Support)	CC

Table 6.14 details the jumper J14 settings for LPTM21L (U1) pin J3. This pin can be used for the two following functions: 1) general purpose digital I/O DIO20, and 2) SPI memory interface support MCLK.

Table 6.14. J14 Jumper Settings for DIO20/MCLK Support

J14	DIO20/MCLK	Mode
Pin 1 to Pin 2	DIO20	CC / HE
Pin 2 to Pin 3	MCLK (SPI Memory Support)	CC

6.4. DIO / ASC-I/F Jumpers

This section details the jumper settings to support external hardware expanders or digital I/O.

Table 6.15 details the jumper J9 settings that select between the 3-wire interface ASC-I/F to external hardware expanders or digital I/O. When the WDAT and WRCLK jumpers are in place they connect the LPTM21L to the corresponding hardware expander connector. Note, the RDAT signals are pre-wired between the connector and the LPTM21L.

Table 6.15. J9 Jumper Settings for DIO/ASC-I/F Support

J9	Silkscreen	DIO / ASC-I/F	Mode
Pin 1 to Pin 2	ASC1	Installed – Hardware Expander 1 ASC-I/F WRCLK	CC
		Removed – DIO11	CC / HE
Pin 3 to Pin 4		Installed – Hardware Expander 1 ASC-I/F WDAT	CC
		Removed – DIO12	CC / HE
Pin 5 to Pin 6	ASC2	Installed – Hardware Expander 2 ASC-I/F WRCLK	CC
		Removed – DIO13	CC / HE
Pin 7 to Pin 8		Installed – Hardware Expander 2 ASC-I/F WDAT	CC
		Removed – DIO14	CC / HE
Pin 9 to Pin 10	ASC3	Installed – Hardware Expander 3 ASC-I/F WRCLK	CC
		Removed – DIO15	CC / HE
Pin 11 to Pin 12		Installed – Hardware Expander 3 ASC-I/F WDAT	CC
		Removed – DIO16	CC / HE

Table 6.16 details the jumper J12 settings to support optional or mandatory reset. If no other hardware expanders are part of the platform, then as a central controller J12 is not required.

If the board is an optional hardware expander, then J12 should be installed between pins 1 and 2 to route the RST_x signal to the central controller board via the ASC connector (J10). Note that the corresponding Reset jumper on the controller board must be in place, see Table 6.11 thru Table 6.13.

J12 should be installed between pins 2 and 3 if the board is a central controller and other hardware expanders are a mandatory part of the design; the jumper is used to connect all the RESETb pins together so the sequence will start after all the ASC sections are out of reset.

Table 6.16. J12 Jumper Settings for Reset Support

J12	Optional Reset / Mandatory Reset	Mode
Removed	No Mandatory Hardware Expanders are connected	CC
Pin 1 to Pin 2	Optional Reset	HE
Pin 2 to Pin 3	Mandatory Hardware Expander(s)	CC / HE

6.5. Other Jumpers

This section covers two jumpers that are provided for testing and demos. First is the Aardvark connector, next is the Dual Boot delay jumper.

Table 6.17 details the connector J16 pins to support interface with the Aardvark cable with I2C and SPI support.

Table 6.17. J16 Aardvark Connector Pins

J16 Pin	AARDVARK	Mode
1	I²C SCL	CC / HE
2	Ground	CC / HE
3	I²C SDA	CC / HE
4	N / C	n/a
5	SPI Memory Data Out	CC
6	N / C	n/a
7	SPI Memory Clock	CC
8	SPI Memory Data In	CC
9	SPI Memory Chip Select (active low)	CC
10	Ground	CC / HE

Table 6.18 details the jumper J15 settings to delay configuration from SPI memory when using Dual Boot. The large RC delay allows the 3.3 V supply to stabilize before the platform manager 2 starts to read it's configuration from the SPI memory (U6).

Table 6.18. J15 Jumper Settings for Dual Boot Delay

J15	Dual Boot Delay	Mode
Removed	Dual Boot RC-Delay is not connected to U1 INITN (pin C5)	CC
Pin 1 to Pin 2	Dual Boot RC-Delay is connected to U1 INITN (pin C5)	CC

7. Switches

This section describes the switches of the board.

7.1. ASC Section I²C Address DIP Switch

The board provides an 8-position DIP switch (SW3) to set the lowest three bits of the I²C address of the ASC section of the LPTM21L. The switch, combined with a set of on-board resistors (R9 – R15), connects to the I2C_ADDR pin (K6) of the LPTM21L (shown in Figure 7.1, taken from Sheet 3 of the schematic). Each switch corresponds to a different resistor setting and address selection. See the Platform Manager 2 Data Sheet (FPGA-DS-02036) for more details. The LPTM21L device only checks the resistor setting at power-on-reset, updating the switches while the board is powered will have no effect. Only one switch should be closed at a time. When the board is used as a central controller, then the *0* switch should be in the down position which grounds the I2C_ADDR pin and sets the lower three bits of the I²C address to zeros.

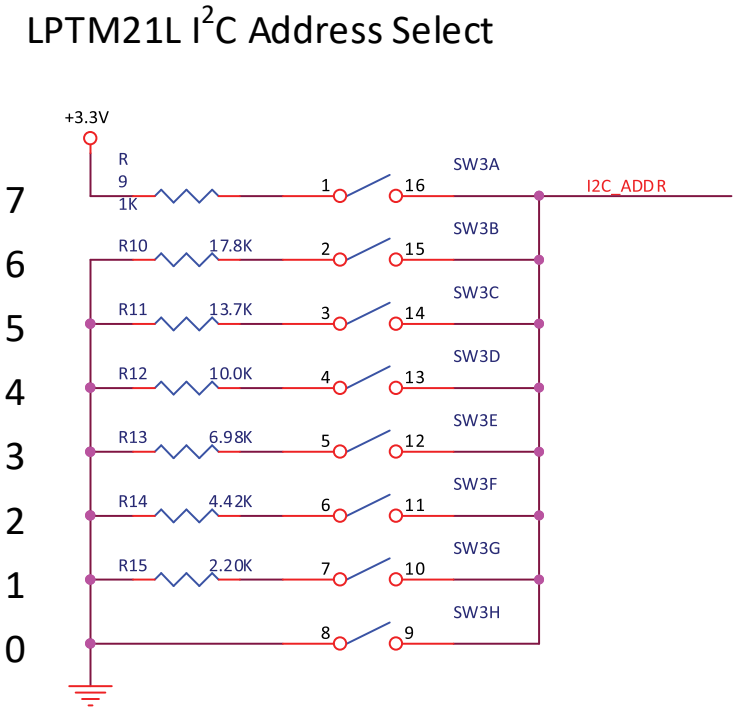

Figure 7.1. ASC Section I²C Address Selection DIP Switch

7.2. FPGA Section I²C Address DIP Switch

The board provides a 4-position DIP switch (SW5) that can be used to set the I²C address of the FPGA section of the LPTM21L (shown in Figure 7.2, taken from sheet 4 of the schematic). The primary reason for this feature is to "move" the unused I²C interface in the hardware expanders to prevent address conflict on the bus. Three switches of SW5 connect 1k pull-up resistors to the I2C_ADDRx pins of U1. The encoding and use of SW5 was already covered in Table 3.3 in the Factory Default Board Settings section.

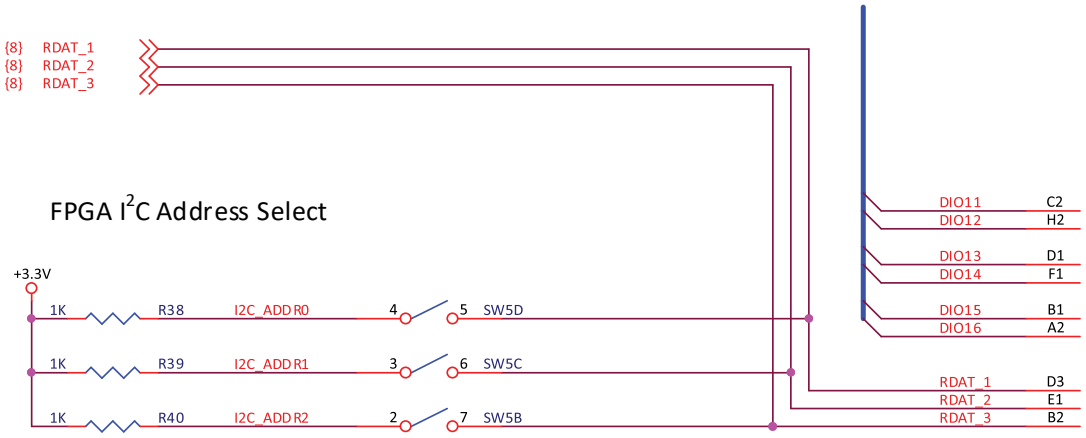

Figure 7.2. FPGA Section I²C Address Selection DIP Switch

7.3. Push Button Switches

Two push button switches are provided on the board as shown in Figure 7.3. Push button SW2 (on sheet 6 of the schematic, located in the upper right of the board) is connected to GPIO10 of the ASC section of LPTM21L. GPIO10 must be configured as an input in Platform Designer in order to use the push-button. When the button is pressed, GPIO10 is set to 0. When the button is released, GPIO10 is pulled to 1 by a 2.2k resistor (section D or RN7). The input signal can be used in the logic design of the central controller. GPIO10 is shared with the red LED (D10), so pressing the push-button (SW2) will cause the LED to illuminate.

Push button SW4 (on sheet 9 of the schematic, located in the middle left of the board) is connected to test points SW4A and SW4B to allow users to "blue-wire" the switch into a custom design which can build on the board.

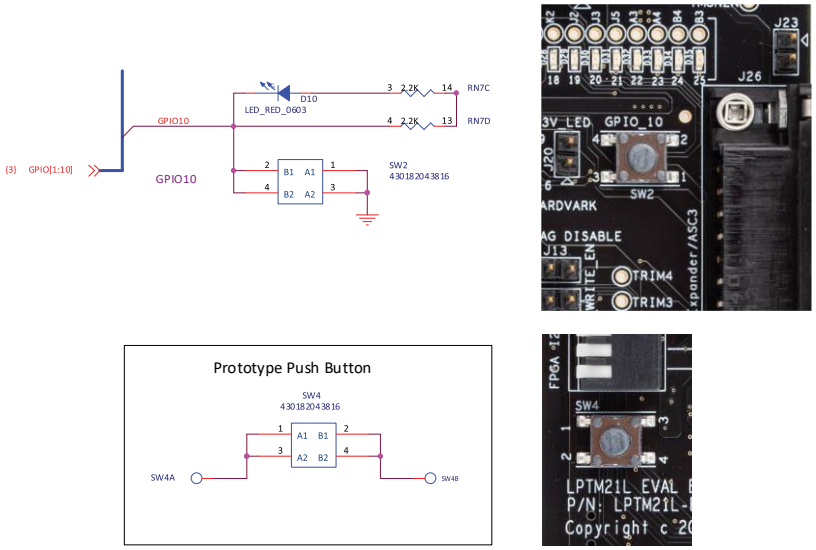

Figure 7.3. Push Button Switches SW2 and SW4

8. LEDs

This section describes the LEDs on the board. There are four main groups of LEDs:

- Power Indicator LEDs
- GPIO LEDs
- DIO LEDs
- Status LEDs

8.1. Power Indicator LEDs

The board has a blue LED (D41) to indicate that +5 V power is connected and a green LED (D40) to indicate that +3.3 V power is available. The LEDs are shown in Figure 8.1 (from sheet 5 of the schematic) and located near the middle of the board.

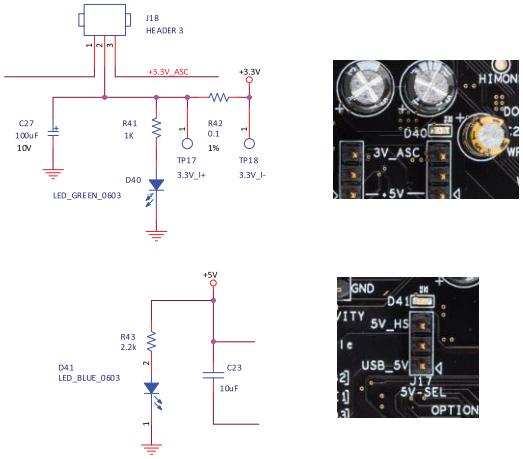

Figure 8.1. Power Indicator LEDs

8.2. Red GPIO LEDs

The board has 10 red LEDs tied to the open-drain outputs (GPIO) of the ASC section of the LPTM21L. The LEDs are pulled up to the +3.3V_LED supply bus and are lit when GPIO1 – GPIO10 are driven to a logic low. The GPIO LEDs are located near the bottom of the board (near J10) as shown in Figure 8.2 (from sheet 6 of the schematic). A test point for each GPIO is provided with each LED for easy testing and prototype development.

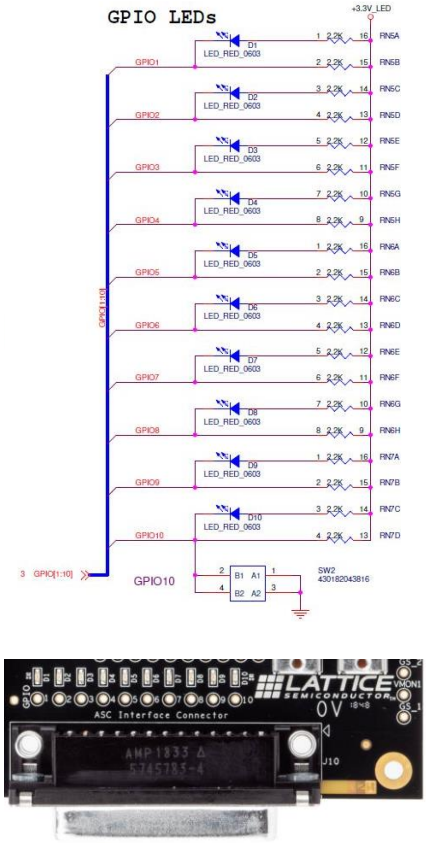

Figure 8.2. GPIO Red LEDs

8.3. Amber DIO LEDs

The board has 25 amber LEDs tied to I/O of the FPGA section of the LPTM21L. The LEDs for DIO1 – DIO7 are pulled up to VCCIO2, which is connected to +3.3V_LED (via zero Ω R72 on sheet 5 of the schematic). R72 can be removed and a wire attached by careful soldering to support other Bank 2 supply voltages. The remainder of DIO LEDs are pulled up to the +3.3V_LED supply bus. All LEDs are lit when DIO1 – DIO25 are driven to a logic low. The DIO LEDs are located near the top of the board (near J25) as shown in Figure 8.3 (from sheet 6 of the schematic). A test point for each DIO is provided with each LED for easy testing and prototype development.

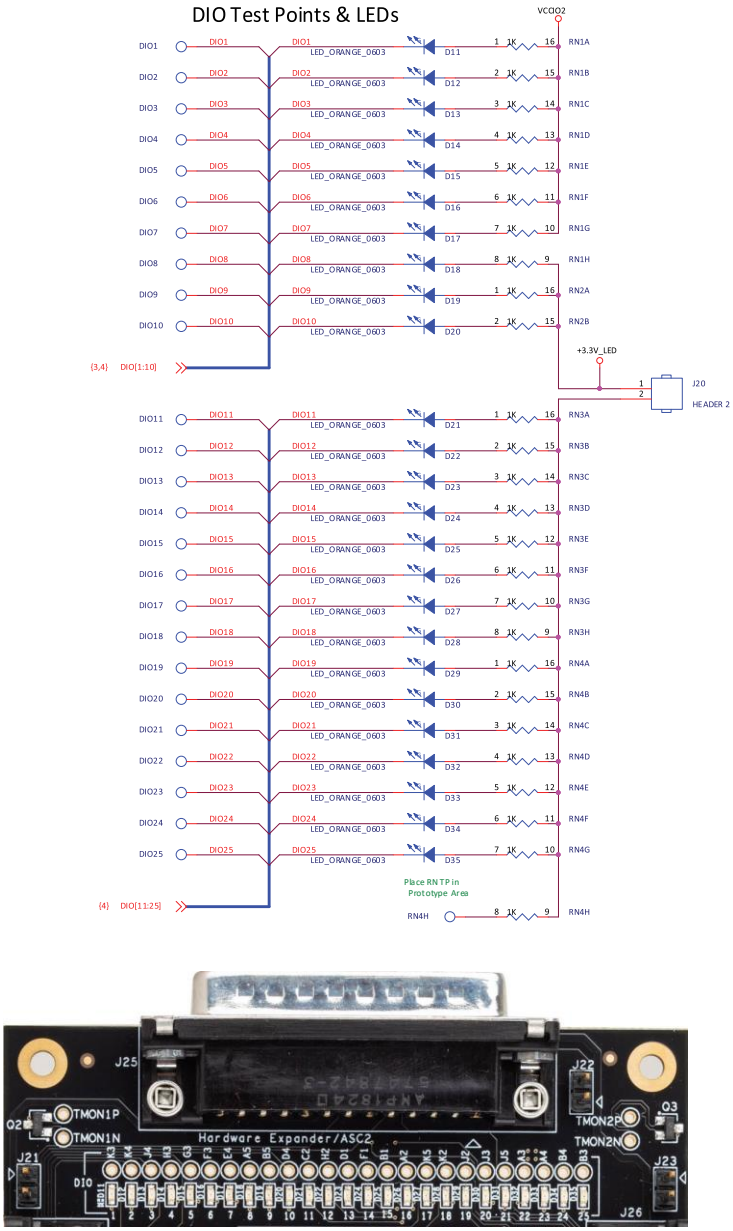

Figure 8.3. DIO1 thru DIO25 Amber LEDs

8.4. Status LEDs

Three status LEDs are included on theLPTM21L board as shown in Figure 8.4 (sheets 4 and 5 of the schematic). The green LED (D37) indicates I^2C activity using a pulse stretching circuit so even short bursts can be seen on the LED. The red LED D43 indicates when the FTDI (U2) device is connected to the I^2C bus (see U7, U8, and U9 on sheet 4 of the schematic). A green LED (D38) indicates when the LPTM21L DONE pin is low. The DONE pin (C6) is low when the FPGA section of the LPTM21L is booting from external SPI memory (U6).

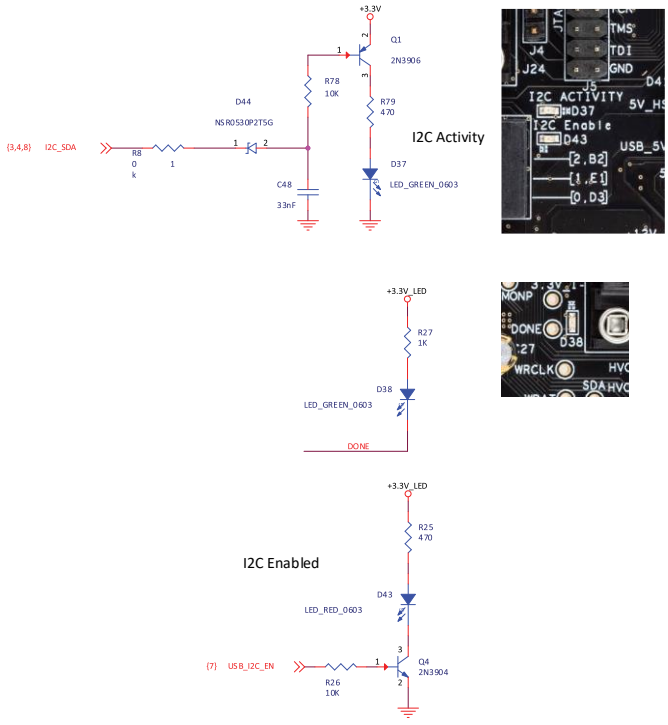

Figure 8.4. Status LEDs

9. Temperature Monitoring

The board has PNP transistors mounted in the upper two corners (near J25). The PNP transistors are connected in the beta-compensated PNP temperature monitor configuration, as shown in Figure 9.1 (from sheets 3 and 6 of the schematic). The beta-compensated PNP is the preferred configuration for temperature monitors and must be enabled in Platform Designer software in order to use. When the temperature monitors are enabled in the software, the temperature of each sensor can be read out using I^2C. The sensors can also be used to simulate over or under-temperature conditions.

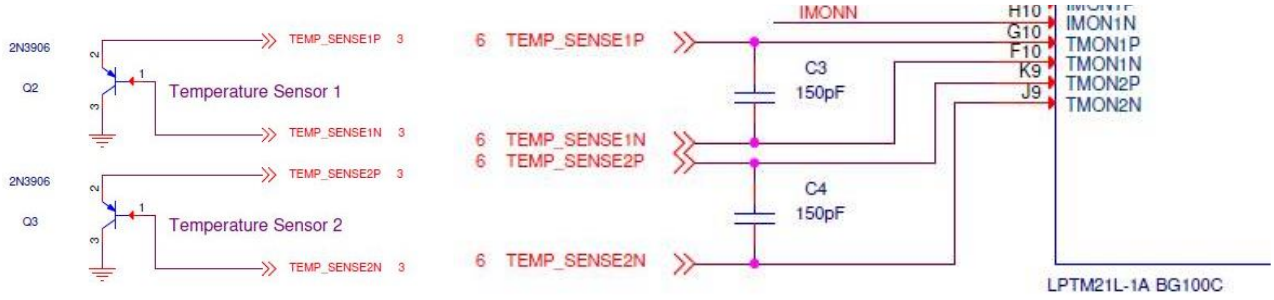

Figure 9.1. Temperature Monitor Circuits

10. Voltage Monitoring

The LPTM21L has 10 voltage monitor (VMON) inputs as part of the ASC section of the device (including the HIMONN_HVMON pin). Most of the VMONs on the board have low value series resistors connected between the VMON pin and the on-board components. These series resistors are populated so that the on-board voltage monitor test points can be driven by an off-board source or a circuit built in the prototype area, without damaging the on-board components. However, it is a good practice to use series resistors, located near the load, with the VMON inputs; this allows small signal traces to be used on the PCB from the VMON pin to monitor the voltage right at the load. All voltages can be read out from the A/D converter using I^2C.

The two potentiometers (R50 and R52) are connected to VMON7 and VMON8 these can be used for any of the following: simulate a power supply output, trip a comparator, and/or generate a fault (see Figure 10.1). The slide potentiometers provide a voltage in the range of 0 V to 3.3 V depending on their position. R51 and R53 are 1 kΩ series resistors which allow connecting different sources directly to the VMON7 and VMON8 test points. The voltage on either potentiometer can be read out from the A/D converter using the I^2C port.

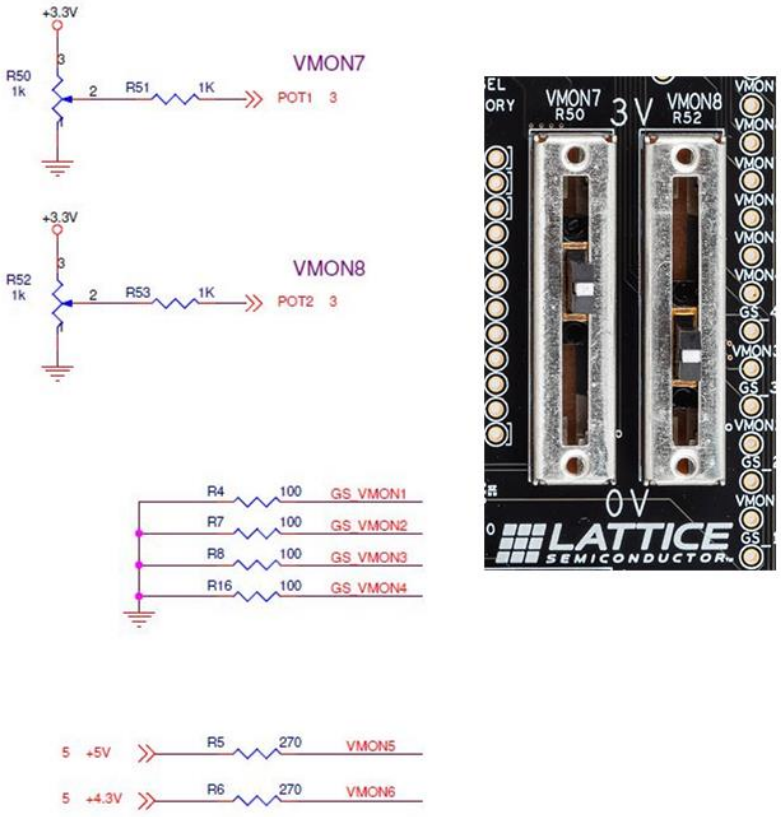

Figure 10.1. VMON Inputs - Slider POTs and on Board Supplies

11. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LPTM21L Evaluation Board	LPTM21L-EVN	

Appendix A. Schematics

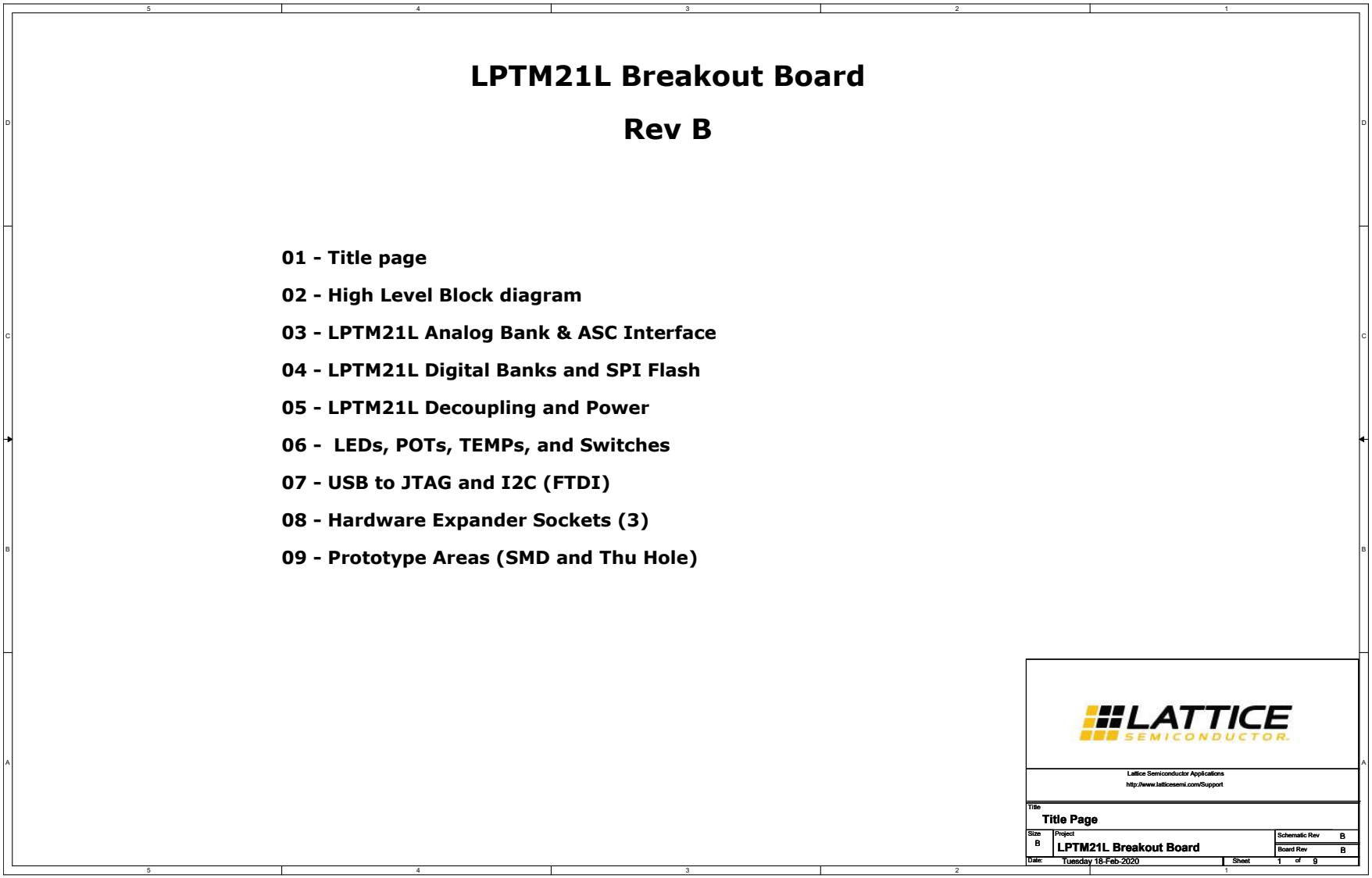

Figure A.1. Title Page

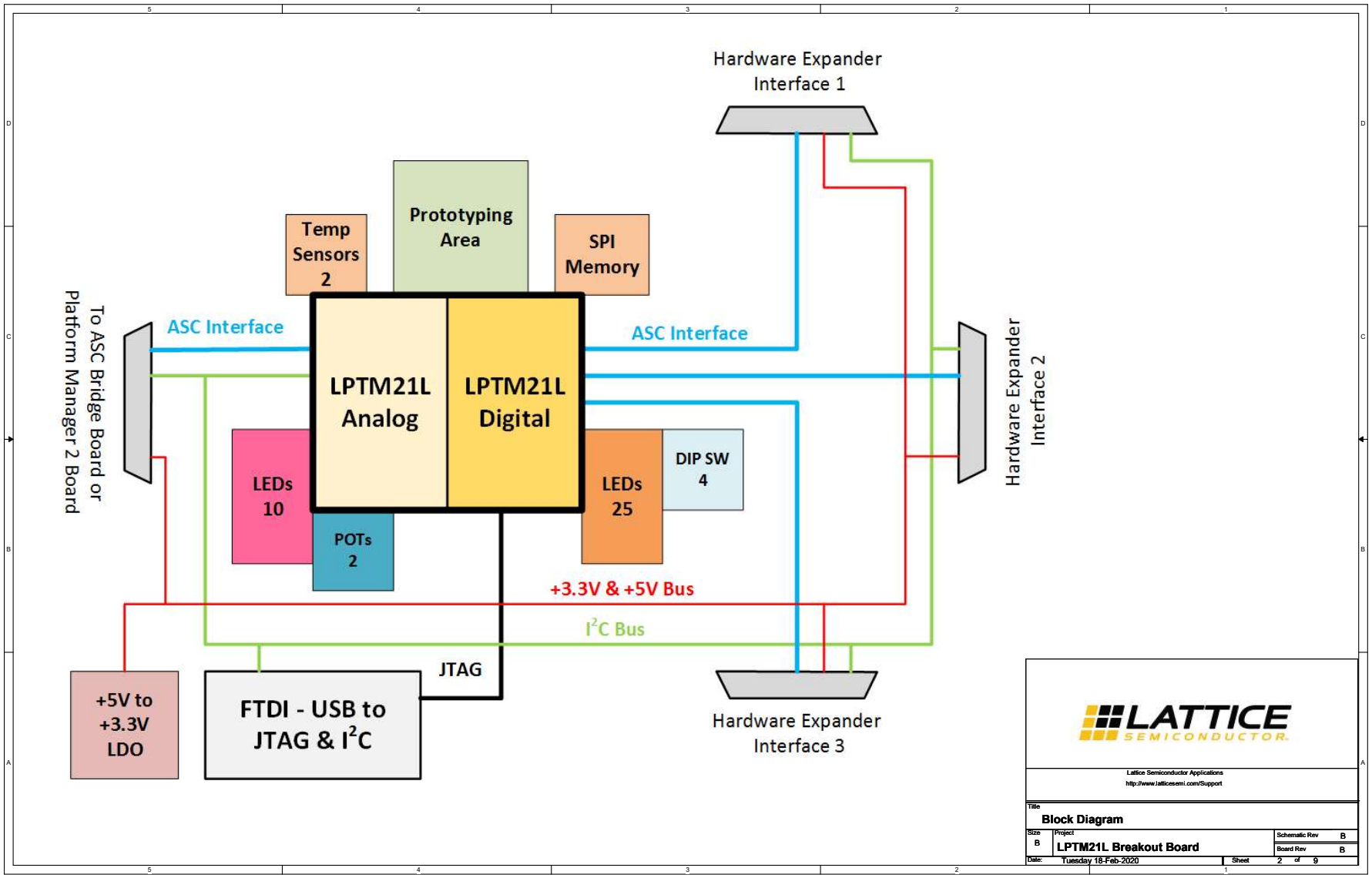

Figure A.2. Block Diagram

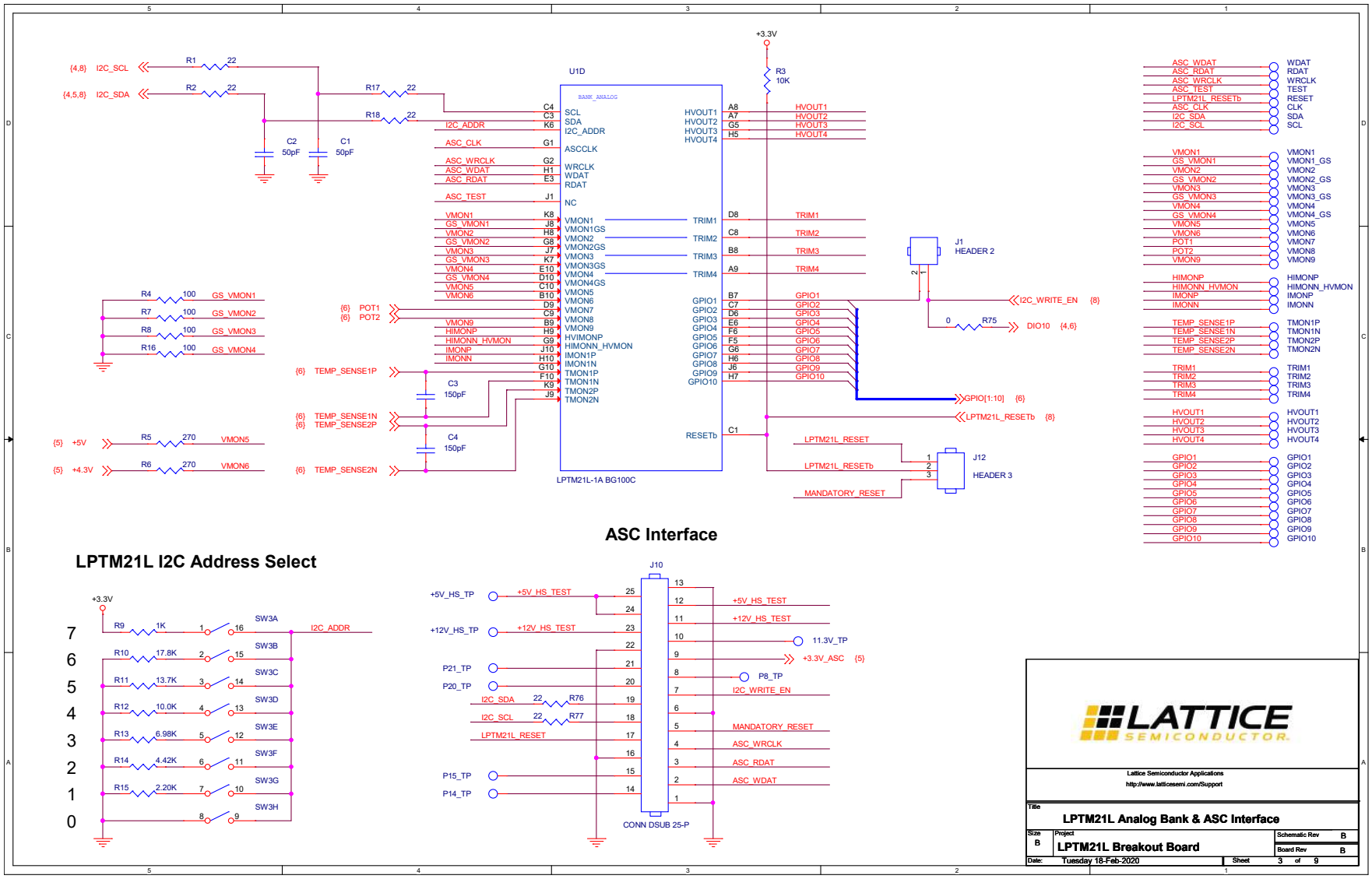

Figure A.3. LPTM21L Analog Bank and ASC Interface

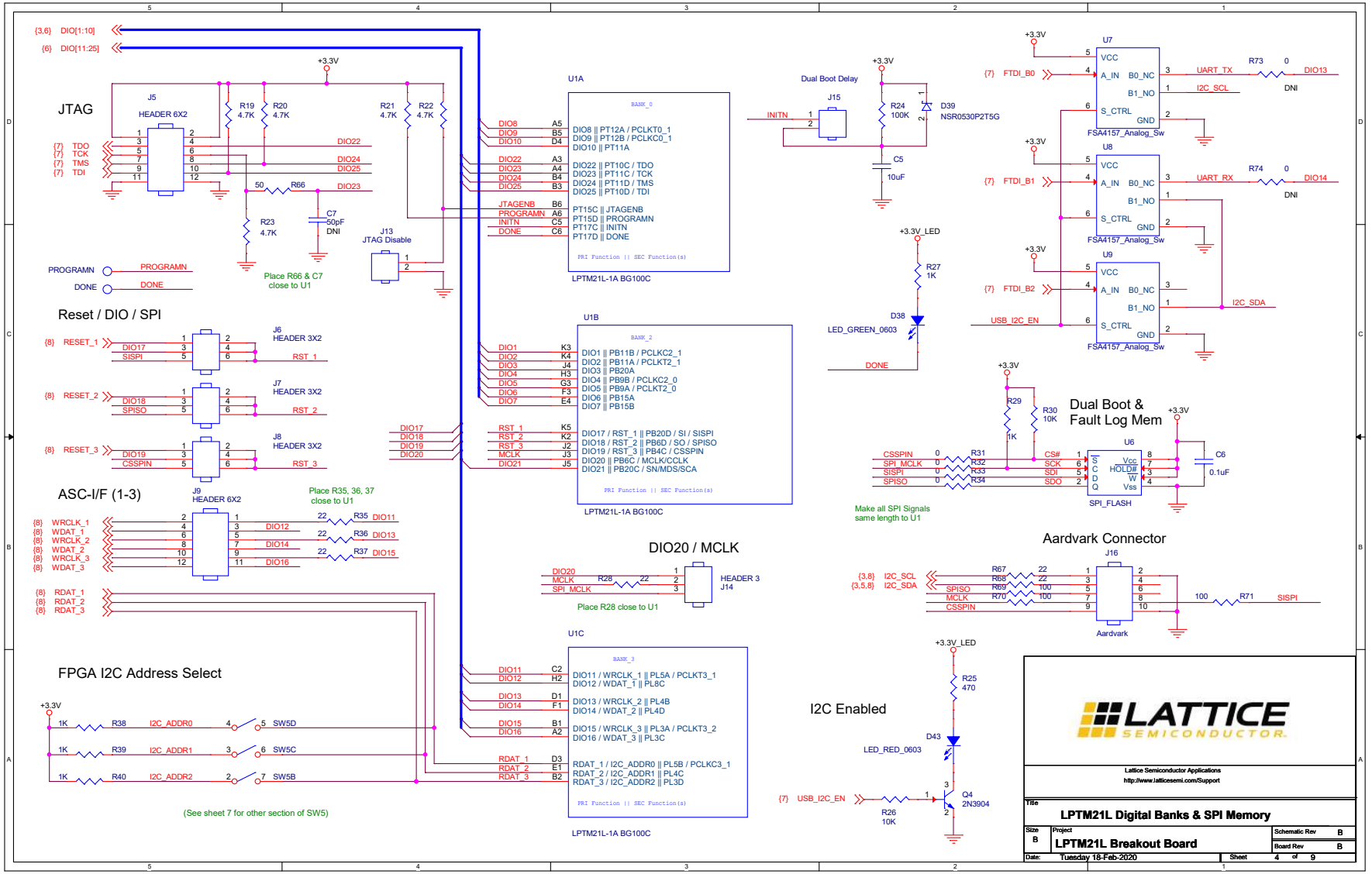

Figure A.4. LPTM21L Digital Banks and SPI Memory

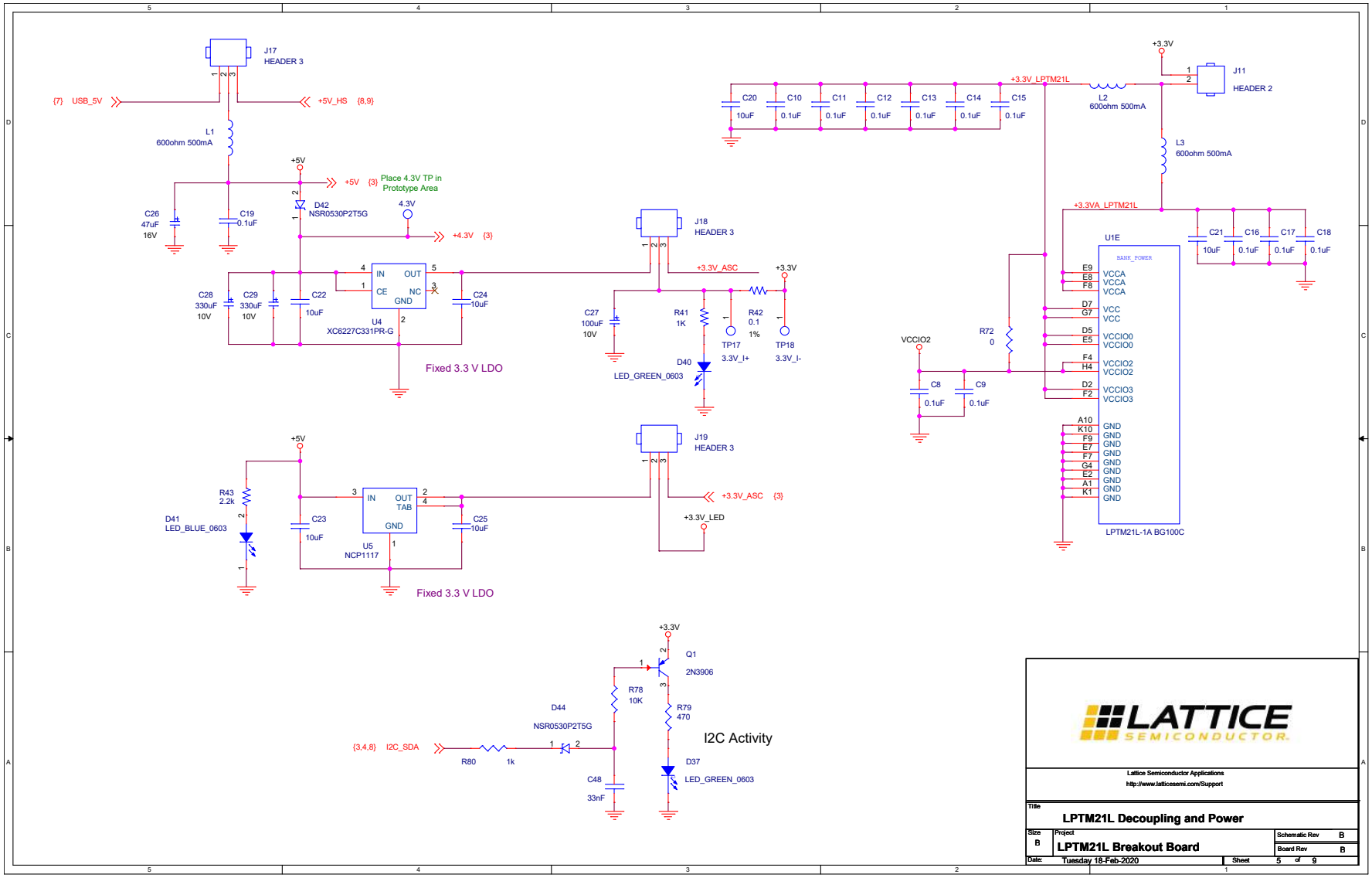

Figure A.5. LPTM21L Decoupling and Power

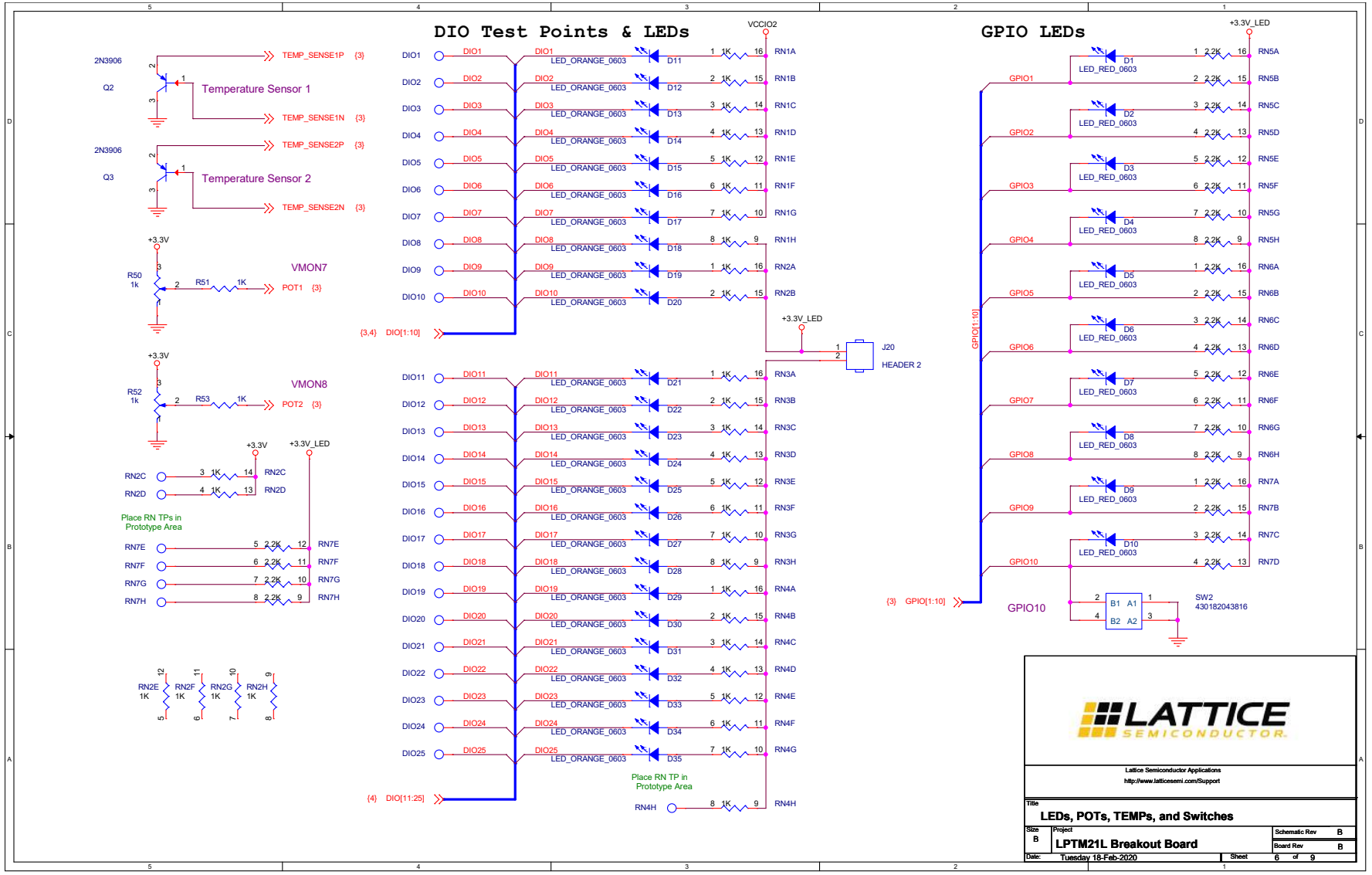

Figure A.6. LEDs, POTs, TEMPs, and Switches

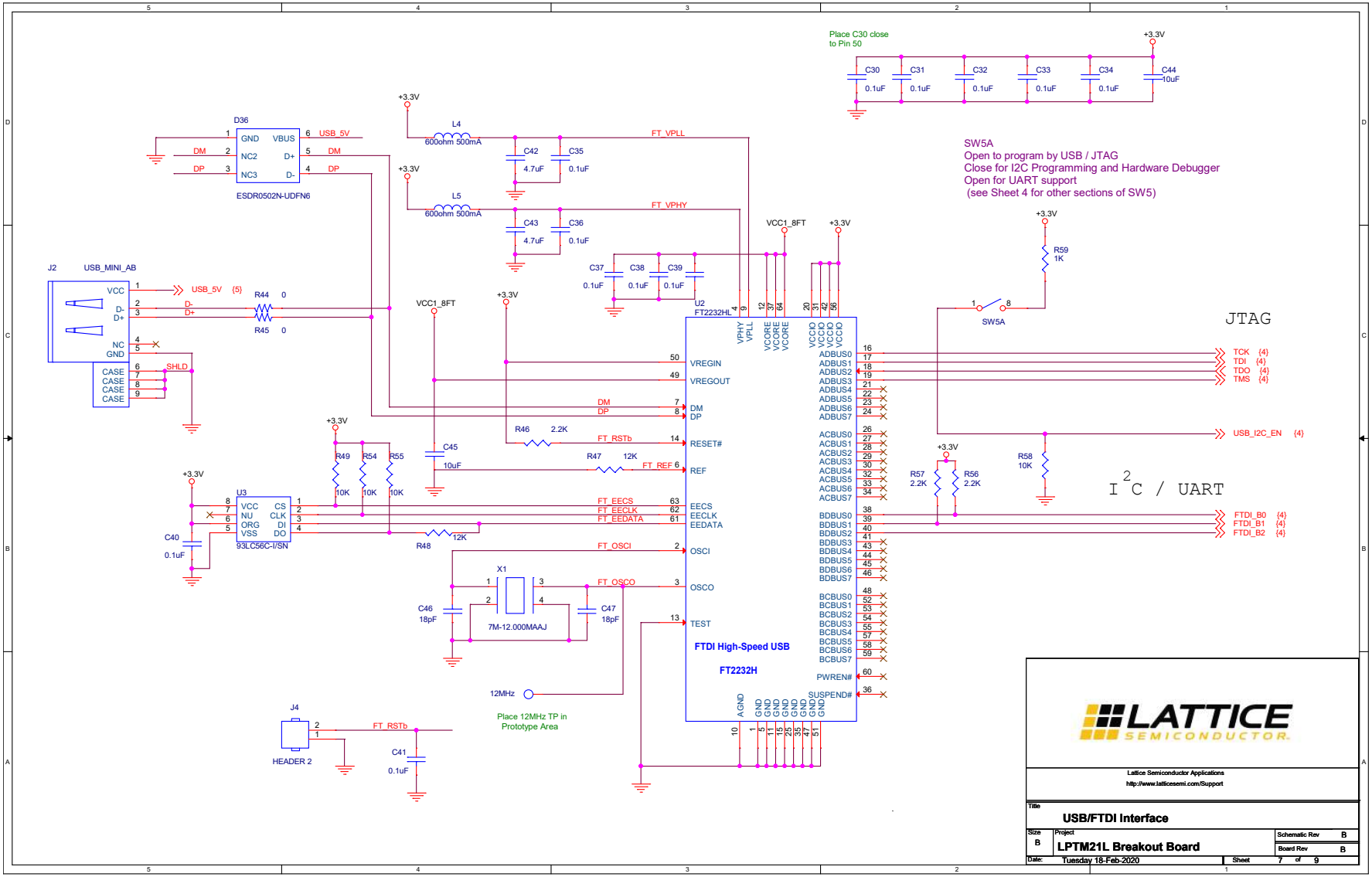

Figure A.7. USB/FTDI Interface

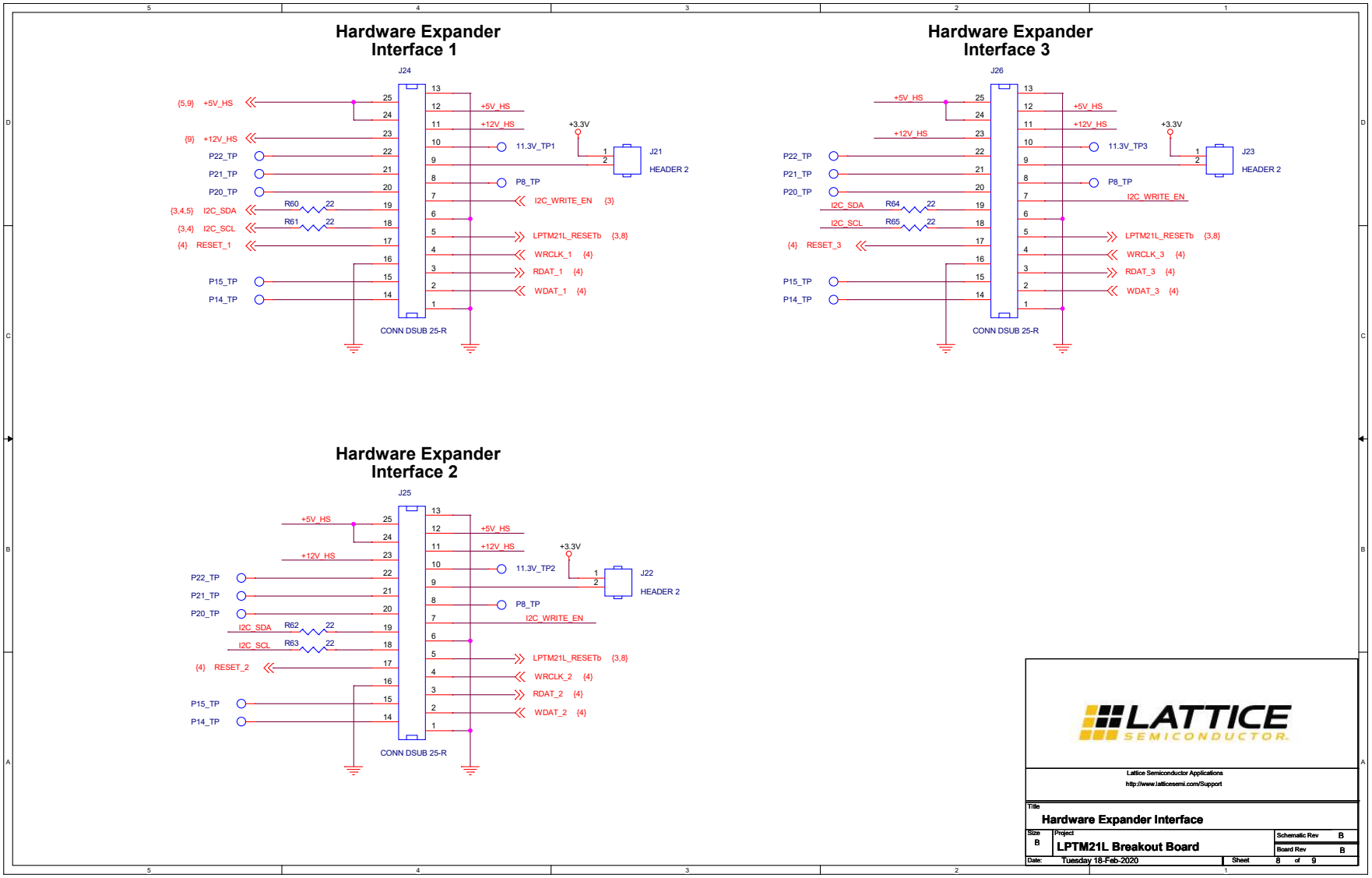

Figure A.8. Hardware Expander Interface

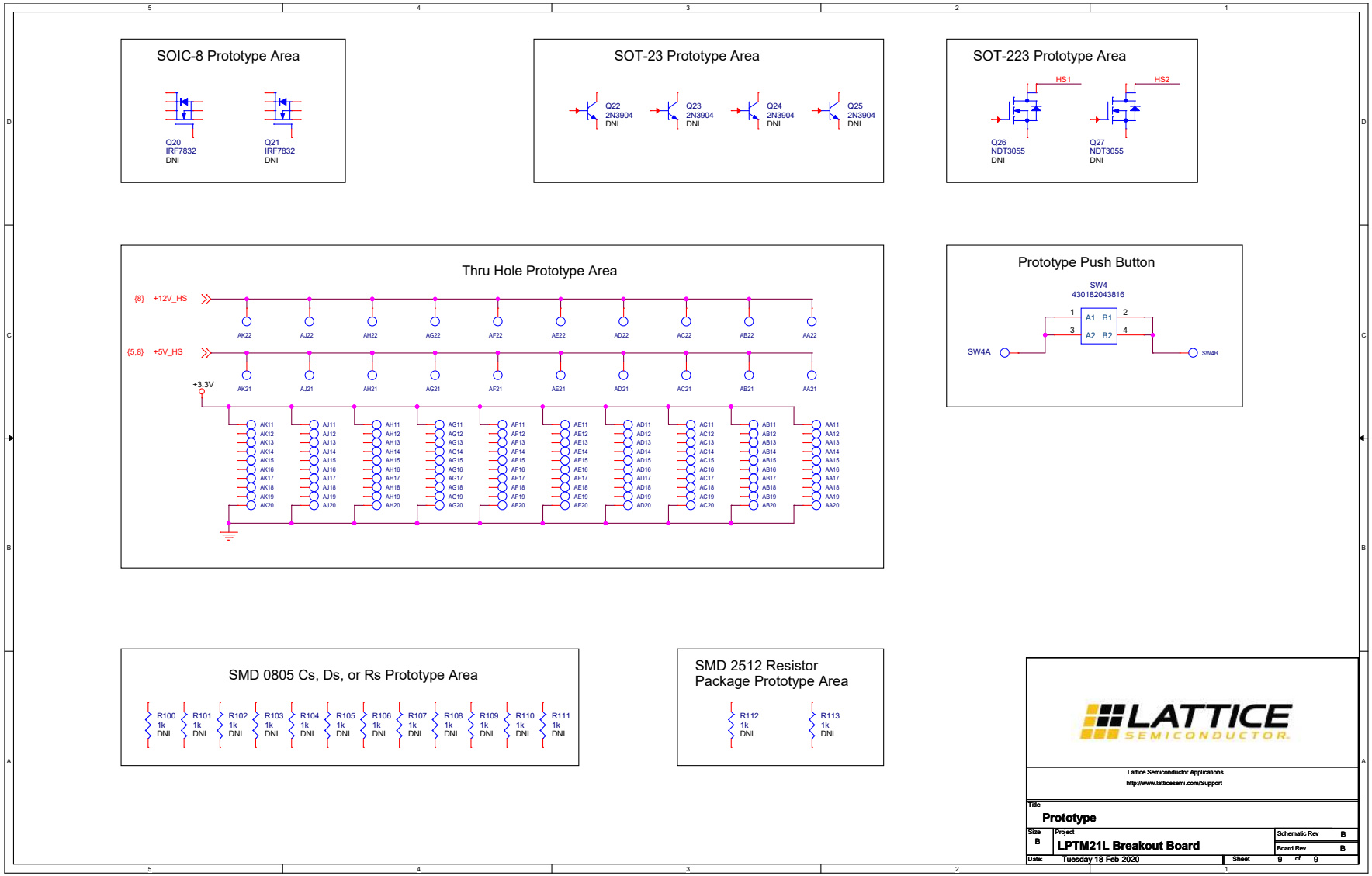

Figure A.9. Prototype

Appendix B. Bill of Materials

Table B.1. LPTM21L Evaluation Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Comments	Manufacturer Part Number	Manufacturer	Description
1	C1,C2	2	50pF	C0603	—	CL10C500JC81PNC	Samsung	CAP CER 50PF 100V C0G/NP0 0603
2	C3,C4	2	150pF	C0603	—	CL10B151KB8NNNC	Samsung	CAP CER 150PF 50V X7R 0603
3	C5,C22,C23,C24, C25,C44,C45	7	10uF	C0603	—	LMK107BJ106MALT D	Taiyo Yuden	CAP CER 10UF 10V 20% X5R 0603
4	C6,C19,C30,C31, C32,C33,C34,C35, C36,C37,C38,C39, C40,C41	14	0.1uF	C0603	—	CL10B104KO8WPNC	Samsung	CAP CER 0.1UF 25V X7R 0603
5	C7	1	50pF	C0603	DNL	CL10C500JC81PNC	Samsung	CAP CER 50PF 100V C0G/NP0 0603
6	C8,C9,C10,C11, C12,C13,C14,C15, C16,C17,C18	11	0.1uF	C0402	—	CL05B104KA5NNNC	Samsung	CAP CER 0.1UF 25V X7R 0402
7	C20,C21	2	10uF	C0402	—	0402ZD106MAT2A	AVX Corporation	CAP CER 10UF 10V X5R 0402
8	C26	1	47uF	UKL1C470KED ANA	—	UKL1C470KEDANA	Nichicon	CAP 47UF 16VFC 10-% TOL10+% RADI
9	C27	1	100uF	UFW1A101MD D1TD	—	UFW1A101MDD1TD	Nichicon	CAP ALUM 100UF 20% 10V RADIAL
10	C28,C29	2	330uF	UVR1A331ME D1TD	—	UVR1A331MED1TD	Nichicon	CAP ALUM 330UF 20% 10V RADIAL
11	C42,C43	2	4.7uF	C0603	—	CL10A475KA8NQNC	Samsung	CAP CER 4.7UF 25V X5R 0603
12	C46,C47	2	18pF	C0402	—	CL05C180JB5NNNC	Samsung	CAP CER 18PF 50V C0G/NP0 0402
13	C48	1	33 nF	C0603	—	—	—	—
14	D1,D2,D3,D4,D5, D6,D7,D8,D9,D10, D43	11	LED_RED_0603	APT1608	—	LTST-C190KRKT	Lite-On Inc.	LED RED CLEAR CHIP SMD
15	D11,D12,D13, D14,D15,D16, D17,D18,D19, D20,D21,D22, D23,D24,D25, D26,D27,D28, D29,D30,D31, D32,D33,D34, D35	25	LED_ORANGE_060 3	APT1608	—	LTST-C190KFKT	Lite-On Inc.	LED ORANGE CLEAR CHIP SMD
16	D36	1	ESDR0502N-UDFN6	UDFN6_040	—	ESDR0502NMUTBG	ON Semiconductor	TVS DIODE 5.5V 6UDFN
17	D37,D38,D40	3	LED_GREEN_0603	APT1608	—	LTST-C190KGKT	Lite-On Inc.	LED GREEN CLEAR CHIP SMD
18	D39,D42,D44	3	NSR0530P2T5G	SM_SOD_923	—	NSR0530P2T5G	ON Semiconductor	DIODE SCHOTTKY 30V 500MA SOD923
19	D41	1	LED_BLUE_0603	APT1608	—	LTST-C190TBKT	Lite-On Inc.	LED BLUE CLEAR CHIP SMD
20	J1,J4,J11,J20,J21, J22,J23	7	HEADER 2	22284024	—	22284024	Molex, LLC	CONN HEADER 2POS .100 VERT GOLD
21	J2	1	USB_MINI_AB	usb2-0-rec-240-0001-9	—	UX60-MB-5ST	Hirose Electric Co Ltd	CONN RECEPT MINI USB2.0 5POS
22	J5,J9	2	HEADER 6X2	Header_2x6	Regular 100 Mil Header	—	—	—

Item	Reference	Qty	Part	PCB Footprint	Comments	Manufacturer Part Number	Manufacturer	Description
23	J6,J7,J8	3	HEADER 3X2	Header_2x3	Regular 100 Mil Header	—	—	—
24	J10	1	CONN DSUB 25-P	5745783-4	—	5745783-4	TE Connectivity	CONN D-SUB RCPT 25POS R/A SOLDER
25	J12,J14,J17,J18, J19	5	HEADER 3	22284034	—	22284034	Molex, LLC	CONN HEADER 3POS .100 VERT GOLD
26	J13	1	JTAG Disable	22284024	—	22284024	Molex, LLC	CONN HEADER 2POS .100 VERT GOLD
27	J15	1	Dual Boot Delay	22284024	—	22284024	Molex, LLC	CONN HEADER 2POS .100 VERT GOLD
28	J16	1	Aardvark	Header_2x5	Regular 100 Mil Header	—	—	—
29	J24,J25,J26	3	CONN DSUB 25-R	5747842-3	—	5747842-3	TE Connectivity	CONN D-SUB PLUG 25POS R/A SOLDER
30	L1,L2,L3,L4,L5	5	600ohm 500mA	fb0603	—	BLM18AG601SN1D	Murata	FERRITE CHIP 600 OHM 500MA 0603
31	Q4	1	2N3904	SOT-23	—	MMBT3904	ON Semiconductor	Trans NPN 40 V 0.2 A SOT-23
32	Q1,Q2,Q3	3	2N3906	SOT-23	—	MMBT3906	ON Semiconductor	TRANS PNP 40V 0.2A SOT-23
33	Q20,Q21	2	IRF7832	SOG_050_8_ WG_244_L_200	DNL	IRF7832TRPBF	Infineon Technologies	MOSFET N-CH 30V 20A 8-SOIC
34	Q22,Q23,Q24,Q25	4	2N3904	SOT-23	DNL	MMBT3904	ON Semiconductor	TRANS NPN 40V 0.2A SOT-23
35	Q26,Q27	2	NDT3055	SOT-223	DNL	NDT3055	ON Semiconductor	MOSFET N-CH 60V 4A SOT-223-4
36	RN1,RN2,RN3,RN4	4	745C101102JP	EXB-2HV	—	745C101102JP	CTS Resistor Products	RES ARRAY 8 RES 1K OHM 2512
37	RN5,RN6,RN7	3	745C101222JP	EXB-2HV	—	745C101222JP	CTS Resistor Products	RES ARRAY 8 RES 2.2K OHM 2512
38	R1,R2,R17,R18, R28,R35,R36,R37, R60,R61,R62,R63, R64,R65,R67,R68	16	22	R0603	—	ERJ-3GEYJ220V	Panasonic	RES SMD 22 OHM 5% 1/10W 0603
39	R3,R26,R30,R49, R54,R55, R58, R78	8	10K	R0603	—	ERJ-3GEYJ103V	Panasonic	RES SMD 10K OHM 5% 1/10W 0603
40	R4,R7,R8,R16, R69,R70,R71	7	100	R0603	—	ERJ-3GEYJ101V	Panasonic	RES SMD 100 OHM 5% 1/10W 0603
41	R5,R6	2	270	R0603	—	ERJ-3GEYJ271V	Panasonic	RES SMD 270 OHM 5% 1/10W 0603
42	R25,R79	2	470	R0603	—	ERJ-3GEYJ471V	Panasonic	RES SMD 470 OHMS 5% 1/10 W 0603
43	R9,R27,R29,R38, R39,R40,R41,R51, R53,R59, R80	11	1K	R0603	—	ERJ-3GEYJ102V	Panasonic	RES SMD 1K OHM 5% 1/10W 0603
44	R10	1	17.8k	R0603	—	ERJ-3EKF1782V	Panasonic	RES SMD 17.8K OHM 1% 1/10W 0603
45	R11	1	13.7k	R0603	—	ERJ-3EKF1372V	Panasonic	RES SMD 13.7K OHM 1% 1/10W 0603
46	R12	1	10.0K	R0603	—	ERJ-3EKF1002V	Panasonic	RES SMD 10K OHM 1% 1/10W 0603
47	R13	1	6.98K	R0603	—	ERJ-PB3B6981V	Panasonic	RES SMD 6.98K OHM 0.1% 1/10W 0603
48	R14	1	4.42K	R0603	—	ERA-3AEB4421V	Panasonic	RES SMD 4.42K OHM 0.1% 1/10W 0603

Item	Reference	Qty	Part	PCB Footprint	Comments	Manufacturer Part Number	Manufacturer	Description
49	R15	1	2.20K	R0603	—	ERJ-3EKF2201V	Panasonic	RES SMD 2.2K OHM 1% 1/10W 0603
50	R19,R20,R21,R22, R23	5	4.7K	R0603	—	ERJ-3GEYJ472V	Panasonic	RES SMD 4.7K OHM 5% 1/10W 0603
51	R24	1	100K	R0603	—	ERJ-3GEYJ104V	Panasonic	RES SMD 100K OHM 5% 1/10W 0603
52	R31,R32,R33,R34, R72,R73,R74	7	0	R0603	—	ERJ-3GEY0R00V	Panasonic	RES SMD 0 OHM JUMPER 1/10W 0603
53	R42	1	0.1	SM_R_0805	—	RUT2012FR100CS	Samsung	RES 0.1 OHM 1% 1/4W 0805
54	R43,R46,R56,R57	4	2.2K	R0603	—	ERJ-3EKF2201V	Panasonic	RES SMD 2.2K OHM 1% 1/10W 0603
55	R44,R45	2	0	R0402	—	ERJ-2GE0R00X	Panasonic	RES SMD 0 OHM JUMPER 1/10W 0402
56	R47,R48	2	12K	R0603	—	ERJ-3GEYJ123V	Panasonic	RES SMD 12K OHM 5% 1/10W 0603
57	R50,R52	2	1k	TH_SLIDEPOT_ 4_25MM	—	RA2043F-20-10EB1-B1K	Alpha (Taiwan)	Slide Potentiometers 20mm TVL LINEAR 1K PC Mount
58	R66	1	50	R0603	—	ERJ-3EKF49R9V	Panasonic	RES SMD 49.9 OHM 1% 1/10W 0603
59	R100,R101,R102, R103,R104,R105, R106,R107,R108, R109,R110,R111	12	1k	R0805	DNL	—	—	—
60	R112,R113	2	1k	R2512	DNL	—	—	—
61	SW1,SW5	2	SW_SPST_4	195-4MST	—	195-4MST	CTS Electrocomponents	SWITCH TACTILE SPST-NO 0.05A 12V
62	SW2,SW4	2	430182043816	sw_sp_st_ck_ pts645_sm	—	430182043816	Wurth Electronics Inc.	SWITCH TACTILE SPST-NO 0.05A 12V
63	SW3	1	SW_SPST_8	195-8MST	—	195-8MST	CTS Electrocomponents	SWITCH PIANO DIP SPST 50MA 24V
64	U1	1	LPTM21L-1A BG100C	caBGA100	Customer Supplied	LPTM21L-1A BG100C	Lattice	Platform Manager 2
65	U2	1	FT2232HL	tqfp64_0p5_12 p2x12p2_h1p6	—	FT2232HL-REEL	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP
66	U3	1	93LC56C-I/SN	so8_50_244	—	93LC56C-I/SN	Microchip	IC EEPROM 2K SPI 3MHZ 8SOIC
67	U4	1	XC6227C331PR-G	SOT-89-5	—	XC6227C331PR-G	Torex Semiconductor Ltd	IC REG LINEAR 3.3V 700MA SOT89-5
68	U5	1	NCP1117	SM_SOT223_ 1234	—	NCP1117ST33T3G	ON Semiconductor	IC REG LINEAR 3.3V 1A SOT223
69	U6	1	SPI_FLASH	SOIC-8	—	S25FL116K0XMFI043	Cypress Semiconductor	IC FLASH 16MBIT 108MHZ 8SOIC
70	U7,U8,U9	3	Analog Switch	6-TSSOP	—	FSA4157P6X	Fairchild	Dual Analog Switch 6-TSSOP
71	X1	1	7M-12.000MAAJ	xtal_4p_7m	—	7M-12.000MAAJ-T	TXC	CRYSTAL 12MHZ 18PF SMD
72	LPTM21L Evaluation Board RevA PCB	1	—	—	—	305-PD-18-0XXX	PACTRON	—

Appendix C. Preference File Listing

```
// The following names are generated by the software and can be copied into
// the preference file when Hardware Expanders are added to the platform
// Hardware Expander 1 connections
LOCATE COMP "rdat_1"  SITE "D3" ;
LOCATE COMP "wdat_1"  SITE "H2" ;
LOCATE COMP "wrclk_1" SITE "C2" ;
// Optional Reset connection
LOCATE COMP "ASC1_RSTN_I" SITE "K5" ;

// Hardware Expander 2 connections
LOCATE COMP "rdat_2"  SITE "E1" ;
LOCATE COMP "wdat_2"  SITE "F1" ;
LOCATE COMP "wrclk_2" SITE "D1" ;
// Optional Reset connection
LOCATE COMP "ASC2_RSTN_I" SITE "K2" ;

// Hardware Expander 3 connections
LOCATE COMP "rdat_3"  SITE "B2" ;
LOCATE COMP "wdat_3"  SITE "A2" ;
LOCATE COMP "wrclk_3" SITE "B1" ;
// Optional Reset connection
LOCATE COMP "ASC3_RSTN_I" SITE "J2" ;



// The following names match the LPTM21L Evaluation Board schematic but,
// they may be re-defined by the user. Thus, they can be copied into
// the preference file and edited to match a different naming convention
// if needed.

// DIO LED connections
LOCATE COMP "DIO1_LED"   SITE "K3" ;
LOCATE COMP "DIO2_LED"   SITE "K4" ;
LOCATE COMP "DIO3_LED"   SITE "J4" ;
LOCATE COMP "DIO4_LED"   SITE "H3" ;
LOCATE COMP "DIO5_LED"   SITE "G3" ;
LOCATE COMP "DIO6_LED"   SITE "F3" ;
LOCATE COMP "DIO7_LED"   SITE "E4" ;
LOCATE COMP "DIO8_LED"   SITE "A5" ;
LOCATE COMP "DIO9_LED"   SITE "B5" ;
LOCATE COMP "DIO10_LED"  SITE "D4" ;
```

```
// The following LED Connections can only be used if the their dual function
// is not being used in the design (such as ASC-I/F, SPI, and JTAG)
LOCATE COMP "DIO11_LED"  SITE "C2" ;
LOCATE COMP "DIO12_LED"  SITE "H2" ;
LOCATE COMP "DIO13_LED"  SITE "D1" ;
LOCATE COMP "DIO14_LED"  SITE "F1" ;
LOCATE COMP "DIO15_LED"  SITE "B1" ;
LOCATE COMP "DIO16_LED"  SITE "A2" ;
LOCATE COMP "DIO17_LED"  SITE "K5" ;
LOCATE COMP "DIO18_LED"  SITE "K2" ;
LOCATE COMP "DIO19_LED"  SITE "J2" ;
LOCATE COMP "DIO20_LED"  SITE "J3" ;
LOCATE COMP "DIO21_LED"  SITE "J5" ;
LOCATE COMP "DIO22_LED"  SITE "A3" ;
LOCATE COMP "DIO23_LED"  SITE "A4" ;
LOCATE COMP "DIO24_LED"  SITE "B4" ;
LOCATE COMP "DIO25_LED"  SITE "B3" ;
```

Appendix D. Rev A Known Issues

The resistor R72 (see Figure D.1) is removed from the Rev A version of the board and blue wires are used to put DIP SW5 – section A in its place. Thus, to use the secondary FTDI port as a USB to I²C interface, the switch must be closed (down position) and the J3 jumpers in place.

Note that if the switch is closed or the J3 jumpers are in place, then other I²C masters may not be able to drive the I²C bus because, the FTDI outputs are not open drain. This includes Diamond Programmer, which uses the JTAG to I²C EFB within the LPTM21L.

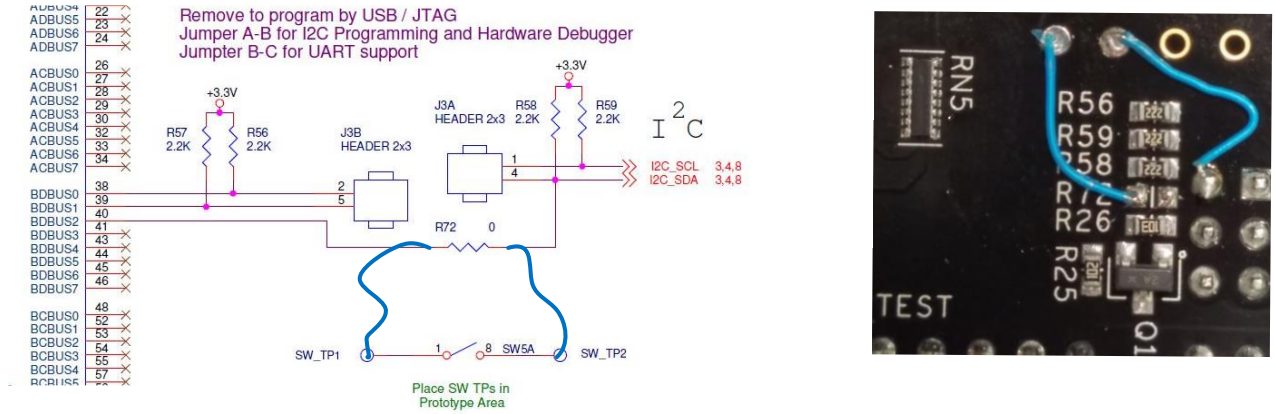

Figure D.1. Rev A Known Issue - Replace R72 with SW5-A

Routing and labeling errors exist on the Rev A board. The connections to the VMON1 and VMON3 test-points are swapped and mis-labeled. The actual Rev A connections are shown in Figure D.2.

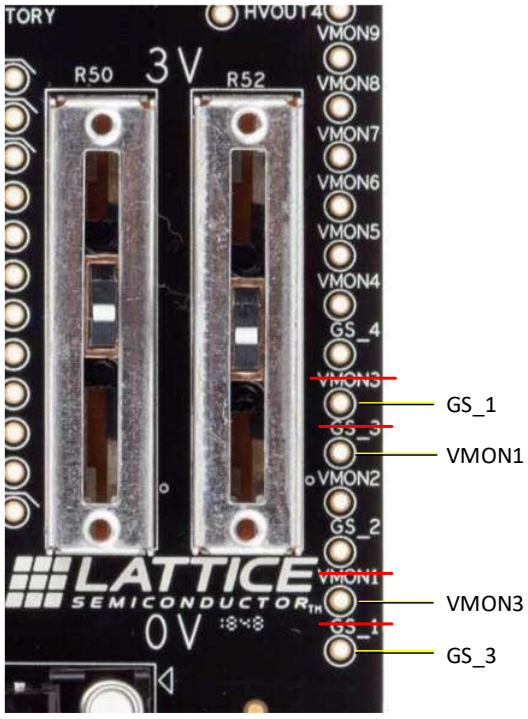

Figure D.2. Rev A Known Issue – VMON1 and VMON3 Connections

References

For more information, refer to:

- Platform Manager 2 Data Sheet (FPGA-DS-02036)
- ASC Breakout Board User Guide (FPGA_EB_02023)
- L-ASC10 Data Sheet (FPGA_DS_02038)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 2.0, June 2020

Section	Change Summary
All	Several changes in the Rev B board.

Revision 1.1, May 2020

Section	Change Summary
Appendix D. Known Issues	Added VMON known issue.

Revision 1.0, May 2019

Section	Change Summary
All	First release.

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