subLVDS to MIPI CSI-2 Image Sensor Bridge with CrossLink-NX

Reference Design

FPGA-RD-02217-1.0

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AP	Application Processor
CMOS	Complementary Metal Oxide Semiconductor
CSI-2	Camera Serial Interface 2
DDR	Double Data Rate
EAV	End of Active Video
FV	Frame Valid
GPLL	General Purpose PLL
HS	High Speed
I^2C	Inter-Integrated Circuit
IP	Intellectual Property
ISP	Image Signal Processor
LP	Low Power
LV	Line Valid
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
OSCI	Internal Oscillator
PLL	Phase Locked Loop
RD	Reference Design
RX	Receiver
SAV	Start of Active Video
TX	Transmitter
WC	Word Count
XHS	Horizontal Sync Pulse
XVS	Vertical Sync Pulse

1. Introduction

Many Image Signal Processors (ISP) or Application Processors (AP) use the Mobile Industry Processor Interface (MIPI®) Camera Serial Interface 2 (CSI-2) standard for image sensor inputs. However, some high-resolution CMOS image sensors use a proprietary subLVDS output format.

The Lattice Semiconductor subLVDS to MIPI CSI-2 Image Sensor Bridge reference design for CrossLink™-NX devices solves the mismatch between subLVDS output image sensor and an ISP/AP using CSI-2 interface.

1.1. Supported Device, IP, and Software

This reference design supports the CrossLink-NX device with IP and software versions shown below.

Table 1.1. Supported Device, IP, and Software

Device Family	Part Number	Compatible IP	Lattice Radiant™ Version
CrossLink-NX	LIFCL-17 and LIFCL-40	• subLVDS Receiver IP version 1.0.4 • Pixel-to-Byte Converter IP version 1.1.1 • D-PHY Transmitter IP version 1.1.4	2.2.1

1.2. Features

- Supports 4-, 6-, 8-, or 10-lane subLVDS input to 1-, 2-, or 4-lane MIPI CSI-2 output
- Supports input lane bandwidth of up to 1.25 Gbps and output lane bandwidth of up to 2.5 Gbps
- Image cropping option
- VSYNC and HSYNC can be generated to control sensor timing
- Dynamic parameter setting through I^2C

1.3. Block Diagram and Clock Distribution

Figure 1.1 shows the block level diagram of the subLVDS to MIPI CSI-2 Image Sensor Bridge reference design. It contains three major IPs and interfacing modules between them. Image data from the sensor come in along with the subLVDS clock in double data rate (DDR) fashion. This clock is divided by 4 or 8 to generate pixel clock according to RX Gear. Pixel clock is fed to trim_ctrl and Pixel-to-Byte IP modules. In addition, pixel clock is fed to TX D-PHY IP as a reference clock and the TX D-PHY IP creates the MIPI clock using its internal PLL. MIPI clock is divided by 8 or 16 to generate the byte clock and the byte clock is fed to Pixel-to-Byte IP and lane_ctrl module. In some configurations, the data bus going to TX D-PHY is half of the data bus coming out from Pixel-to-Byte IP. In that case, the byte clock generated by TX D-PHY must be 2x of the byte clock used in Pixel-to-Byte IP and the original byte clock (hs_byte_clk) is divided by two and fed to Pixel-to-Byte IP and lane_ctrl. The lane_ctrl module takes care of bus width differences. When the image sensor is in slave mode, FPGA has to feed the sync signals to the sensor. In that case, the sensor_sync module takes the clock from the sensor to generate sync signals. I^2C slave module is optional to change the configurations on the fly.

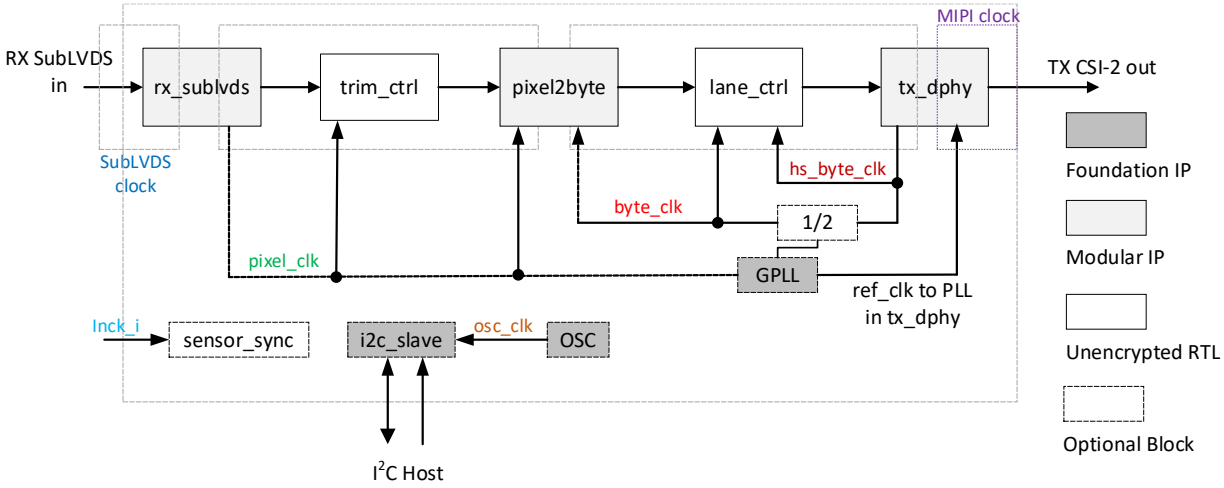

Figure 1.1. subLVDS to MIPI CSI-2 Image Sensor Bridge Block Diagram

1.4. RX and TX Permutations

Table 1.2 shows the available permutations of RX and TX configurations. Same permutations apply to both RAW10 and RAW12. In addition, Pixel-to-Byte IP supports only four lanes on TX. To overcome these limitations, a different TX Gear setting is applied in D-PHY TX IP to handle 1-lane or 2-lane outputs, which require faster byte clock (hs_byte_clk = 2x or 4x of byte_clk). Currently, permutations that require 4x of byte_clk (grayed out in Table 1.2) are not supported due to the unknown necessity.

Also, RX Gear 16 can be applied for RX lane count = 4. However, it does not provide any benefits against RX Gear 8. As such, this is excluded in the design even though the parameter itself remains available for potential future use.

Table 1.2. RX and TX Permutations

Data Type	RX Lane Count	RX Gear	RX Max. Lane Bandwidth (Mbps)	TX Gear Setting in Pixel-to-Byte IP	TX Lane Count	TX Gear	hs_byte_clk Ratio Against byte_clk
RAW10 RAW12	4	8	1250	8	4	8	—
			1250		2	16	—
			625		1	16	2x
		16	1250	16	4	16	—
			1250		2	16	2x
			625		1	16	4x
	6	8	~1000*	8	4	8	—
			833.3		2	16	—
			416.6		1	16	2x
	8	8	1250	16	4	16	—
			625		2	16	2x
			312.5		1	16	4x
	10	8	1000	16	4	16	—
			500		2	16	2x
			250		1	16	4x

The Excel file (*sublvds2csi2_clock_NX.xlsx*) is provided to calculate the pixel clock, byte clock, and others, from RX bandwidth and other information. This sheet can be useful to configure IPs. A sample entry is shown in Figure 1.2. By setting four rows shown in the table, pixel clock, byte clock, and TX bandwidth are automatically calculated. Those can be used to configure D-PHY TX IP. In the following situations, the byte clock that comes out from D-PHY TX IP is hs_byte_clk and half of this clock is byte_clk fed to Pixel-to-Byte IP (and lane_ctrl):

2 x (*TX Gear setting in Pixel-to-Byte IP*) = (*Number of TX Lanes in D-PHY TX) x (TX Gear in D-PHY TX*).

SubLVDS to MIPI CSI-2 Image Sensor Bridge RD with CrossLink-NX Frequency Calculator

SubLVDS RX	Data Type	RAW10		
	Number of RX Lanes	4		
	RX Gear	8	fixed to 8	
	RX Line Rate (per lane)	1250	Mbps	(max 1250)
	SubLVDS Clock Frequency	625	MHz	
	Pixel Clock Frequency	156.25	MHz	
Pixel2Byte	Number of TX Lanes	4	always 4	
	Number of Input Pixel Per Clock	4		
	TX Gear	8		
D-PHY TX	TX Line Rate (total)	5000	Mbps	
	Number of TX Lanes	2		
	TX Line Rate (per lane)	2500	Mbps	(max 2500)
	TX Gear	16		
	Byte Clock Frequency	156.25	MHz	
	Reference Clock Frequency	156.25	MHz	
	hs_byte_clk is not necessary			

set by user

Figure 1.2. Bandwidth and Clock Frequency Calculator

2. Parameters and Port List

There are two directive files for this reference design:

- synthesis_directives.v – used for design compilation by Lattice Radiant and for simulation.
- simulation_directives.v – used for simulation.

You can modify these directives according to your own configuration. The settings in these files must match subLVDS RX IP, Byte-to-Pixel IP, and TX D-PHY IP settings created in the Lattice Radiant software.

2.1. Synthesis Directives

Table 2.1 shows the synthesis directives that affect this reference design. These are used for both synthesis and simulation. Some parameter selections are restricted by other parameter settings.

Table 2.1. Synthesis Directives

Category	Directive	Remarks
Image Sensor control[1]	SENSOR_MODE_MASTER	Use *SLAVE* when sync signals (xvs_o/xhs_o) must be sent from FPGA to the image sensor. Only one of these two directives must be defined.
	SENSOR_MODE_SLAVE	
Image Sensor Sync Polarity[1]	SENSOR_SYNC_NEG	Polarity setting for sync signals to the image sensor. Only effective when SENSOR_MODE_SLAVE is defined. Only one of these two directives must be defined.
	SENSOR_SYNC_POS	
XVS (Vertical Sync) assertion period[1]	XVS_LENGTH_XHS	Select the active pulse length of xvs_o between xhs_o and one horizontal line. Only applicable in case of SENSOR_MODE_MASTER. Only one of these two directives must be defined.
	XVS_LENGTH_LINE	
Total line count[1]	V_TOTAL {value}	Total line count for one frame including blanking. Only effective when SENSOR_MODE_SLAVE is defined. Value must be 12'd10 – 12'd4095.
Total horizontal cycle[1]	H_TOTAL {value}	Total cycle count for one line including blanking in the unit of inck_i. Only effective when SENSOR_MODE_SLAVE is defined. Value must be 12'd10 – 12'd4095.
XHS (Horizontal Sync) pulse cycle[1]	XHS_LENGTH {value}	Active pulse width of xhs_o. Only effective when SENSOR_MODE_SLAVE is defined. Value must be 8'd1 – 8'd255.
RX Data Type	RAW10	Define the data type on RX channel. Only one of these two directives must be defined.
	RAW12	
RX channel lane count	NUM_RX_LANE_4	Number of lanes in RX channel. Only one of these four directives must be defined.
	NUM_RX_LANE_6	
	NUM_RX_LANE_8	
	NUM_RX_LANE_10	
RX subLVDS Clock Gear	RX_GEAR_8	RX subLVDS Clock Gear. Use only Gear 8.
RX subLVDS Dropped Line Mode	RX_DATA_DROPPED_LINE_MODE	Define only if the RX Dropped Line Mode is Dynamic.
RX subLVDS Dropped Pixel Mode	RX_DATA_DROPPED_PIXEL_MODE	Define only if the RX Dropped Pixel Mode is Dynamic.
RX subLVDS Word Count Mode	RX_DATA_WORD_COUNT_MODE	Define only if the RX Word Count Mode is Dynamic.
TX D-PHY Clock mode[2]	TX_CLK_MODE_HS_LP	TX D-PHY Clock mode. Only one of these two directives must be defined. TX_CLK_MODE_HS_LP – Non-Continuous Clock Mode TX_CLK_MODE_HS_ONLY – Continuous Clock Mode
	TX_CLK_MODE_HS_ONLY	
TX channel lane count	NUM_TX_LANE_1	Number of lanes in TX channel. Only one of these three directives must be defined.
	NUM_TX_LANE_2	
	NUM_TX_LANE_4	

Category	Directive	Remarks
TX D-PHY Clock Gear	TX_GEAR_8	Number of TX Clock Gear on RX channel. Only one of these directives must be defined.
	TX_GEAR_16	
Use GPLL[10]	USE_GPLL	Use GPLL to create a reference clock to be fed to PLL of TX DPHY IP.
Parameter set by I²C	USE_I2C	Define this to use I²C I/F to configure the image sensor from FPGA.
Software Reset Register[3]	SW_RST_N {value}	Default value of the software reset register of I²C Slave module. Value must be 1'b0 or 1'b1. Applicable only when USE_I2C is defined. Active low.
Top Line Trimming[4, 5]	TOP_TRIM {value}	Define the number of lines to be trimmed before TX. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 6'd0 – 6'd63.
Vertical Active Lines on TX[5]	V_ACTIVE {value}	Define the number of active lines to be sent on TX. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 12'd1 – 12'd4095.
Left Pixel Unit Trimming[6, 8]	LEFT_TRIM_UNIT {value}	Define the number of pixel units to be trimmed before TX. 1 pixel unit = number of RX lanes. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 6'd0 – 6'd63.
Left Pixel Trimming[6, 8]	LEFT_TRIM_LANE {value}	Define the number of pixels to be trimmed before TX. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 4'd0 – 4'd9 and less than the RX lane count.
Horizontal Active Pixel units on TX[7, 8]	H_ACTIVE_UNIT {value}	Define the number of active pixels to be sent on TX. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 10'd1 – 10'd1023. The value must be even in case of TX_GEAR_16 or NUM_TX_CH_2.
Active Word Count[9]	WC {value}	Define the number of byte count of active pixels to be sent to TX. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 16'd5 – 16'd65535.
Virtual Channel ID	VC {value}	Define the virtual Channel ID. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. Value must be 2'd0 – 2'd3.
KEEP clock lane in HS mode	KEEP_HS	When defined, clock lane is kept in HS mode during active line periods even if TX clock lane is in non-continuous clock mode. This value is used as a fixed value when USE_I2C is not defined and used as the default value of the I²C register when USE_I2C is defined. The value is 1'b1 when defined and 1'b0 when not defined.

Notes:

1. Refer to the image sensor data sheet for proper settings.
2. HS_LP mode means non-continuous clock mode and HS_ONLY means continuous clock mode.
3. Logical OR between this register and system reset (reset_n_i) is used to reset modules other than I²C slave module.
4. Value = 0 is not allowed when no line is trimmed by SubLVDS RX IP.
5. (TOP_TRIM + V_ACTIVE) cannot exceed the vertical active line count of the incoming RX data. It is your responsibility to manage this.
6. Number of pixels trimmed from the left edge is ((LEFT_TRIM_UNIT x number of RX lanes x (RX_GEAR / 8)) + LEFT_TRIM_LANE).
7. Active pixel count sent to TX is (H_ACTIVE_UNIT x number of RX lanes x (RX_GEAR / 8)).
8. ((LEFT_TRIM_UNIT + H_ACTIVE_UNIT) x number of RX lanes x (RX_GEAR / 8) + LEFT_TRIM_LANE) cannot exceed the horizontal active pixel count of the incoming RX data. It is your responsibility to manage this.
9. WC ≤ (H_ACTIVE_UNIT x number of RX lanes x (RX_GEAR / 8)) x (RAW number (10 or 12)) / 8. Refer to the trim_ctrl section for details.
10. Refer to the int_gpll section for details.

2.2. Simulation Directives

Table 2.2 shows the simulation directives for this reference design. Some parameter selections are restricted by other parameter settings including Table 2.1.

Table 2.2. Simulation Directives

Category	Directive	Remarks
RX subLVDS clock period	PIX_CLK {value}	RX subLVDS clock period in ps.
INCK clock period	INCK_PERIOD {value}	INCK clock period in ps. Applicable only when SENSOR_MODE_SLAVE is defined.
Number of frames to run	NUM_FRAMES {value}	Number of video frames fed by testbench.
Number of active lines[1]	NUM_LINES {value}	Number of RX active video lines per frame.
Number of active pixels[2]	NUM_PIXELS {value}	Number of RX active video pixels per line.
Vertical Blanking from XVS to active line[1]	VFRONT_BLNK {value}	Number of blanking lines before the active video line.
Vertical Blanking after active line[1]	VREAR_BLNK {value}	Number of blanking lines after the active video line.
Horizontal Blanking period[2]	HB_PERIOD {value}	Horizontal Blanking period in SubLVDS clock cycles.
I^{2}C Slave Address	I2C_SLAVE_ADR {value}	Define 7-bit of I2C Slave Address. Value must match the one set for i2c_s module in Lattice Radiant. Applicable only when USE_I2C is defined.
Software Reset Register[3]	I2C_SW_RST_N {value}	Write value to the software reset register of I2C Slave module. Value must be 1'b0 or 1'b1. Applicable only when USE_I2C is defined. Active low.
Top Line Trimming[4, 5]	I2C_TOP_TRIM {value}	Write value to the top trim register of I2C Slave module. Value must be 6'd0 – 6'd63. Applicable only when USE_I2C is defined.
Vertical Active Lines on TX[5]	I2C_V_ACTIVE {value}	Write value to the vertical active line register of I2C Slave module. Value must be 12'd1 – 12'd4095. Applicable only when USE_I2C is defined.
Left Pixel Unit Trimming[6, 8]	I2C_LEFT_TRIM_UNIT {value}	Write value to the pixel unit trim register of I2C Slave module. Value must be 6'd0 – 6'd63. Applicable only when USE_I2C is defined.
Left Pixel Trimming[6, 8]	I2C_LEFT_TRIM_LANE {value}	Write value to the pixel trim register of I2C Slave module. Value must be 4'd0 – 4'd9 and less than the RX lane count. Applicable only when USE_I2C is defined.
Horizontal Active Pixel units on TX[7, 8]	I2C_H_ACTIVE_UNIT {value}	Write value to the horizontal active pixel unit register of I^{2}C Slave module. Value must be 10'd1 – 10'd1023. Applicable only when USE_I2C is defined.
Active Word Count[9]	I2C_WC {value}	Write value to the word count register of I2C Slave module. Value must be 16'd5 – 16'd65535. Applicable only when USE_I2C is defined.
Virtual Channel ID	I2C_VC {value}	Write value to the virtual channel ID register of I2C Slave module. Value must be 2'd0 – 2'd3. Applicable only when USE_I2C is defined.
KEEP HS mode	I2C_KEEP_HS {value}	Write value to the keep HS mode register of I2C Slave module. Value must be 1'b0 or 1'b1. Applicable only when USE_I2C is defined.
Total line count[10]	I2C_V_TOTAL {value}	Write value to the total line count register of I2C Slave module. Value must be 12'd10 – 12'd4095. Applicable only when USE_I2C and SENSOR_MODE_SLAVE are defined.
Total horizontal cycle[10]	I2C_H_TOTAL {value}	Write value to the total horizontal cycle count register of I2C Slave module. Value must be 12'd10 – 12'd4095. Applicable only when USE_I2C and SENSOR_MODE_SLAVE are defined.

Category	Directive	Remarks
XHS (Horizontal Sync) pulse cycle[10]	I2C_XHS_LENGTH {value}	Write value to the XHS pulse length register of I2C Slave module. Value must be 8'd1 – 8'd255. Applicable only when USE_I2C and SENSOR_MODE_SLAVE are defined.

Notes:

1. Total number of lines per frame is (NUM_LINES + VFRONT_BLNK + VREAR_BLNK).
2. In the case of SENSOR_MODE_MASTER, total number of subLVDS clock cycles per line is (((NUM_PIXELS/NUM_RX_LANE) + 8) x (RAW number (10 or 12)) / 2) + HB_PERIOD).
3. Logical OR between this register and system reset (reset_n_i) is used to reset modules other than I^2C slave module.
4. Value = 0 is not allowed when no line is trimmed by subLVDS RX IP.
5. (I2C_TOP_TRIM + I2C_V_ACTIVE) cannot exceed the vertical active line count of the incoming RX data. It is your responsibility to manage this.
6. Number of pixels trimmed from the left edge is ((I2C_LEFT_TRIM_UNIT x number of RX lanes x (RX_GEAR / 8)) + I2C_LEFT_TRIM_LANE).
7. Active pixel count sent to TX is (I2C_H_ACTIVE_UNIT x number of RX lanes x (RX_GEAR / 8)).
8. ((I2C_LEFT_TRIM_UNIT + I2C_H_ACTIVE_UNIT) x number of RX lanes x (RX_GEAR / 8) + I2C_LEFT_TRIM_LANE) cannot exceed the horizontal active pixel count of the incoming RX data. It is your responsibility to manage this.
9. I2C_WC ≤ (I2C_H_ACTIVE_UNIT x number of RX lanes x (RX_GEAR / 8)) x (RAW number (10 or 12)) / 8. Refer to the trim_ctrl section for details.
10. Refer to the image sensor data sheet for proper settings.

2.3. Top-Level I/O

Table 2.3 shows the top level I/O of this reference design. Actual I/O depend on the customer's channel and lane configurations. All necessary I/O ports are automatically declared by compiler directives.

Table 2.3. SubLVDS to MIPI CSI2 Top-Level I/O

Port Name	Direction	Description
Reset		
reset_n_i	I	Asynchronous active low system reset
Control Interface (conditional)		
inck_i	I	Clock to control XVS and XHS. Only used in case of SENSOR_MODE_SLAVE.
xvs_o	O	Vertical Sync signal to the image sensor. Only used in case of SENSOR_MODE_SLAVE.
xhs_o	O	Horizontal Sync signal to the image sensor. Only used in case of SENSOR_MODE_SLAVE.
Control Interface (optional)		
scl	I/O	I^2C clock. Only used in case of USE_I2C.
sda	I/O	I^2C data Only used in case of USE_I2C.
SubLVDS RX Interface		
clk_p_i	I	Positive differential RX subLVDS input clock
clk_n_i	I	Negative differential RX subLVDS input clock
d0_p_i	I	Positive differential RX subLVDS input data 0
d0_n_i	I	Negative differential RX subLVDS input data 0
d1_p_i	I	Positive differential RX subLVDS input data 1
d1_n_i	I	Negative differential RX subLVDS input data 1
d2_p_i	I	Positive differential RX subLVDS input data 2
d2_n_i	I	Negative differential RX subLVDS input data 2
d3_p_i	I	Positive differential RX subLVDS input data 3
d3_n_i	I	Negative differential RX subLVDS input data 3
d4_p_i	I	Positive differential RX subLVDS input data 4 (in case of 6/8/10-lane configuration)
d4_n_i	I	Negative differential RX subLVDS input data 4 (in case of 6/8/10-lane configuration)
d5_p_i	I	Positive differential RX subLVDS input data 5 (in case of 6/8/10-lane configuration)
d5_n_i	I	Negative differential RX subLVDS input data 5 (in case of 6/8/10-lane configuration)

Port Name	Direction	Description
d6_p_i	I	Positive differential RX subLVDS input data 6 (in case of 8/10-lane configuration)
d6_n_i	I	Negative differential RX subLVDS input data 6 (in case of 8/10-lane configuration)
d7_p_i	I	Positive differential RX subLVDS input data 7 (in case of 8/10-lane configuration)
d7_n_i	I	Negative differential RX subLVDS input data 7 (in case of 8/10-lane configuration)
d8_p_i	I	Positive differential RX subLVDS input data 8 (in case of 10-lane configuration)
d8_n_i	I	Negative differential RX subLVDS input data 8 (in case of 10-lane configuration)
d9_p_i	I	Positive differential RX subLVDS input data 9 (in case of 10-lane configuration)
d9_n_i	I	Negative differential RX subLVDS input data 9 (in case of 10-lane configuration)
CSI-2 TX Interface		
clk_p_o	O	Positive differential TX CSI-2 output clock
clk_n_o	O	Negative differential TX CSI-2 output clock
d0_p_o	O	Positive differential TX CSI-2 output data 0 (in case of 1-lane configuration)
d0_n_o	O	Negative differential TX CSI-2 output data 0 (in case of 1-lane configuration)
d1_p_o	O	Positive differential TX CSI-2 output data 1 (in case of 2/4-lane configuration)
d1_n_o	O	Negative differential TX CSI-2 output data 1 (in case of 2/4-lane configuration)
d2_p_o	O	Positive differential TX CSI-2 output data 2 (in case of 4-lane configuration)
d2_n_o	O	Negative differential TX CSI-2 output data 2 (in case of 4-lane configuration)
d3_p_o	O	Positive differential TX CSI-2 output data 3 (in case of 4-lane configuration)
d3_n_o	O	Negative differential TX CSI-2 output data 3 (in case of 4-lane configuration)

3. Design and Module Description

The top-level design (sublvds2csi2_NX.v) consists of the following modules:

- sensor_sync (conditional)
- rx_sublvds
- trim_ctrl
- pix2byte
- lane_ctrl
- tx_dphy
- int_gpll (conditional)
- i2c_slave (optional)
- int_osc (conditional)

The top-level design has a reset synchronization logic.

3.1. sensor_sync

This module is instantiated when SENSOR_MODE_SLAVE is defined to feed the horizontal and vertical sync signals (xhs_o, xvs_o) to the image sensor using the external clock (inck_i). Sync pulse polarity and interval can be changed by directives described in the Synthesis Directives and Simulation Directives sections. Figure 5.4 shows xvs_o having one line length of active pulse by XVS_LENGTH_LINE directive. This module has no interaction with other modules except for i2c_slave. The following parameters are taken as input data:

- v_total_i[11:0] – Total number of lines per frame including blanking lines.
- h_total_i[11:0] – Total number of clock cycles per line including blanking period.
- xhs_length[7:0] – Pulse length of xhs_o. In case that XVS_LENGTH_XHS is defined, this value also applies to xvs_o active pulse length.

3.2. rx_sublvds

This module must be created for the RX channel according to channel conditions, such as the number of lanes, bandwidth, and others. Figure 3.1 and Figure 3.2 show an example of the IP interface settings in the Lattice Radiant software for the subLVDS Image Sensor Receiver IP Core. You can use the ipx file (rx_sublvds/rx_sublvds.ipx) included in the sample project and re-configure according to your needs. Refer to SubLVDS Image Sensor Receiver IP Core User Guide (FPGA-IPUG-02093) for details.

The following shows guidelines and parameter settings required for this reference design.

- Number of RX Lanes – Set according to channel configuration. The value must match NUM_RX_LANE_* setting (4, 6, 8, or 10).
- RX Gear – Always Select 8.
- RX Line Rate – Set according to channel configuration. The following are the maximum values for different lane configurations:
  - 4-Lane, Gear 8 – 1250 Mbps
  - 6-Lane, Gear 8 – 1250 Mbps
  - 8-Lane, Gear 8 – 1250 Mbps
  - 10-Lane, Gear 8 – 1000 Mbps
- Dropped Line Mode – Can be set as Dynamic or Static according to the channel configuration.
- Dropped Line Count – Set 0. This value must not be 0 when TOP_TRIM / I2C_TOP_TRIM are set to 0.
- Dropped Pixel Mode – Can be set as Dynamic or Static according to the channel configuration.
- Dropped Pixel Count – Set 0.
- Word Count Mode – Can be set as Dynamic or Static according to the channel configuration.
- Word Count – Set 0.
- Video Packet Data Type – Select RAW10 or RAW12.
- Image Sensor Mode – Always select Master. Slave mode is handled by sensor_sync module.

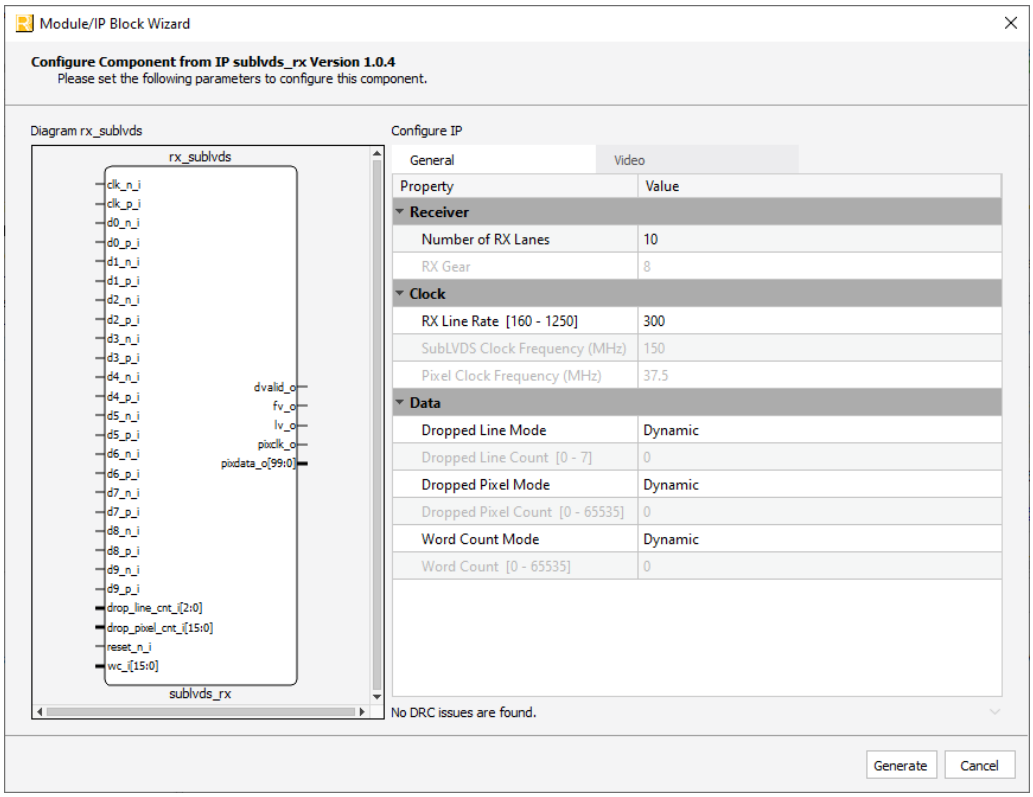

Figure 3.1. rx_sublvds IP Creation #1

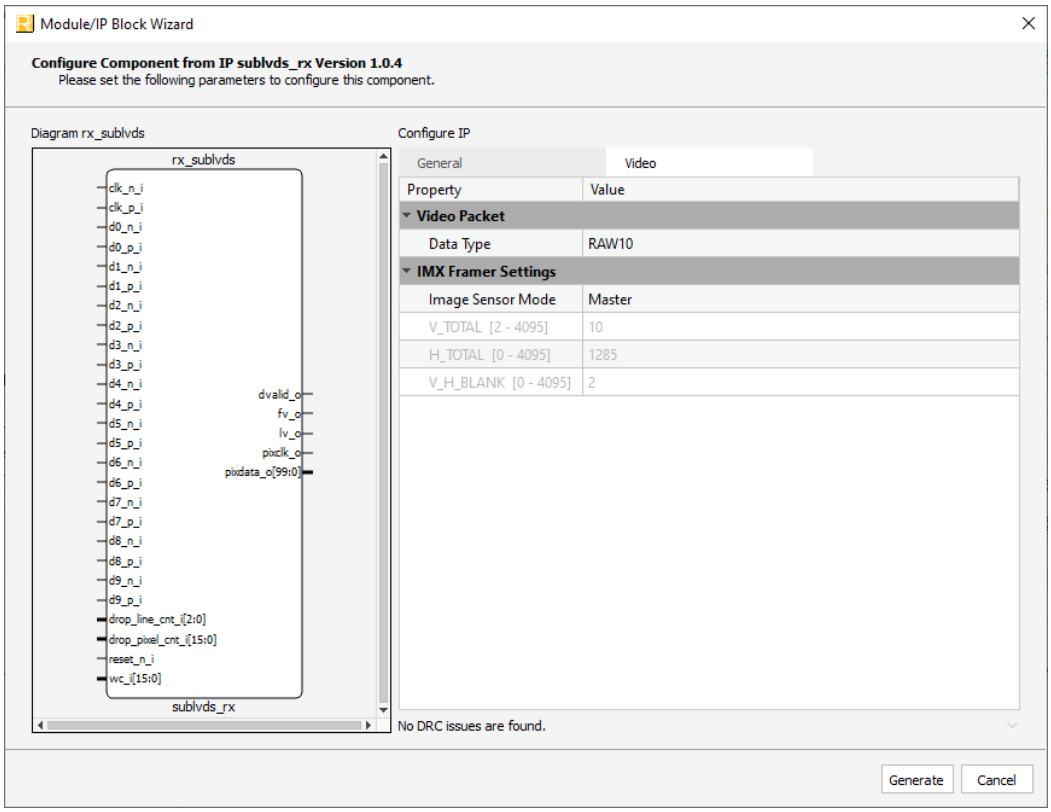

Figure 3.2. rx_sublvds IP Creation #2

This module takes serial subLVDS data from the image sensor and outputs pixel data after de-serialization. In case that you generate this IP from scratch, it is recommended to set the module name to *rx_sublvds* so that you do not need to modify the instance name of this IP in the top-level design as well as the simulation setup file. Otherwise, you have to modify the names accordingly.

Figure 3.3 shows a global timing example of RAW10 in 10-lane configuration. This IP takes data between SAV (Start of Active Video) and EAV (End of Active Video) as active video data and outputs along with the assertion of dvalid. In case of Gear 8, the pixel clock frequency is ¼ of the incoming subLVDS clock. Incoming data is DDR, which means 8 bits of data are de-serialized every pixel clock cycle. In both RAW10 and RAW12 cases, a single pixel clock cycle is not enough to retrieve one pixel data on each lane. Therefore, dvalid has on and off cycles. In case of RAW10, dvalid is asserted 4 out of every 5 pixel clock cycles (8 bits x 5 = 40 bits: 4 pixel data). In case of RAW12, dvalid is asserted 2 out of every 3 pixel clock cycles (8 bits x 3 = 24 bits: 2 pixel data).

Table 3.1 shows the sync code details. Both SAV and EAV comes from four words of data. The first word is always all *1* and second and third words are always all *0*. The fourth word determines the type of the sync codes.

As you can see by Table 3.1, there are only blanking lines and non-blanking lines and no concept of front porch or back porch against vertical sync. As shown in Figure 3.3, XVS (Vertical sync) belongs to the first non-blanking lines in a frame. In case of Figure 3.3, more than 18 lines exist from the first non-blanking line to the active video line. Therefore top line trimming is effective to process all necessary lines. On the other hand, it will require a special attention if we need to process the very first line since we don't have enough time to process frame start packet transaction in CSI-2 which requires low power to high speed mode transition while acquiring the payload data of the first line. To avoid that condition, this design doesn't process the first line payload data. In other words, this design mandate the first line is always skipped. This is guaranteed by "Dropped line in subLVDS RX IP GUI" + "TOP_TRIM/I2C_TOP_TRIM set in synthesis_directives/simulation_directives" > 0.

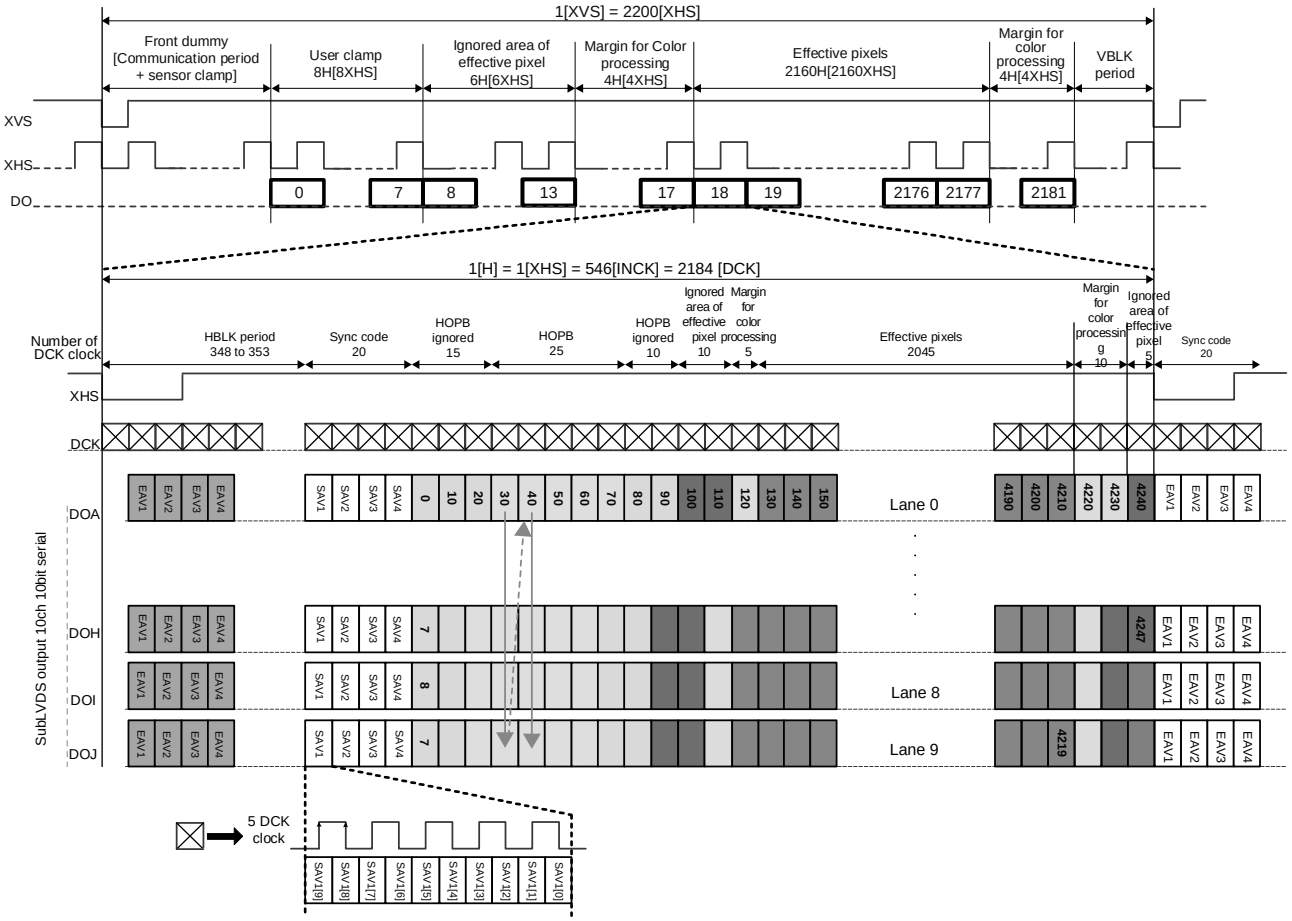

Figure 3.3. subLVDS Input Global Timing (RAW10, 10 Lanes)

Table 3.1. Sync Code Details

LVDS Output Bit No.		Sync Code				
12-Bit Output	10-Bit Output	First Word	Second Word	Third Word	Fourth Word	
11	9	1	0	0	1	
10	8	1	0	0	0	
9	7	1	0	0	V	1: Blanking line 0: Except blanking line
8	6	1	0	0	H	1: End sync code 0: Start sync code
7	5	1	0	0	P3	Protection bits
6	4	1	0	0	P2	
5	3	1	0	0	P1	
4	2	1	0	0	P0	
3	1	1	0	0	0	
2	0	1	0	0	0	
1	—	1	0	0	0	
0	—	1	0	0	0	

		Protection Bits			
V	H	P3	P2	P1	P0
0	0	0	0	0	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

3.3. trim_ctrl

In many cases, the data that comes out from rx_sublvds includes unnecessary data and is discarded by the downstream devices. This module enables the trimming of the edge data based on the given parameters. The following parameters are taken as input data:

- top_trim_i[5:0] – Number of top lines to be trimmed. This value doesn't include the dropped lines by subLVDS RX IP. When the number of dropped line by subLVDS RX IP is 0, top_trim_i cannot be 0.
- v_active_i[11:0] – Number of active lines to be sent to TX module.
- left_trim_unit_i[5:0] – Number of unit pixels to be trimmed. One unit is pixels equal to RX lane count in case of RX Gear 8 and 2x of RX lane count in case of RX Gear 16.
- left_trim_lane_i[3:0] – Number of pixels to be trimmed after unit trimming. Total number of pixels to be trimmed is (left_trim_unit_i) x (RX lane count) x (RX Gear / 8) + (left_trim_lane_i).
- h_active_unit_i[9:0] – Number of unit pixels to be sent to TX module. One unit is equal to RX lane count in case of RX Gear 8 and 2x of RX lane count in case of RX Gear 16.

Figure 3.4 shows a global timing example of trim_ctrl. In this case, the first and last lines are trimmed by trim_ctrl. Note that the original first line is already trimmed by rx_sublvds.

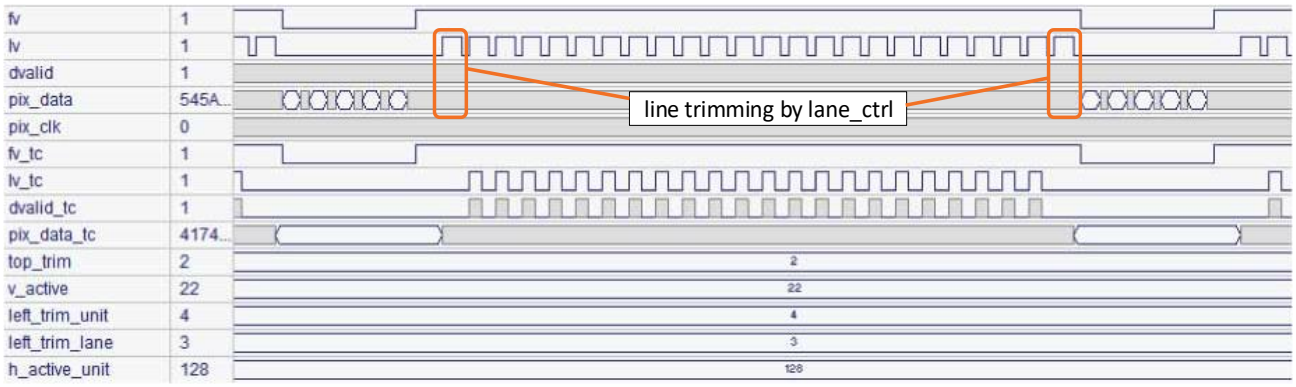

Figure 3.4. trim_ctrl Global Timing (RAW10, 10 Lanes)

Figure 3.5 shows the close-up of the above focusing the beginning of the line. In this case, the pixel counts to be trimmed is 4 (left_trim_unit) x 10 (RX lane count) + 3 (left_trim_lane) = 43. That means 4 unit data are trimmed from the beginning and 3 pixel data (LSB 30 bits) are trimmed from the fifth unit data (pix_data_A). The rest of the fifth unit data are shifted down towards LSB and LSB 30 bits of the next data (pix_data_B) are placed at the MSB 30 bits. The result is the first output data from lane_ctrl (pix_data_tc_A). This means pix_data_tc_A[99:0] = {pix_data_B[29:0], pix_data_A[99:30]}.

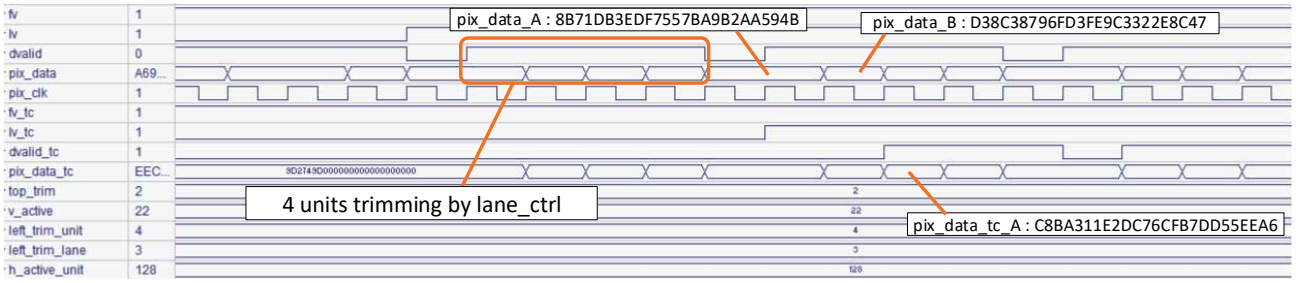

Figure 3.5. Trimming in the Beginning of the Line (RAW10, 10 Lanes)

The number of lines and pixels to be trimmed can be set in the unit of 1 line or 1 pixel as well as number of active lines to be cropped. However, there exist some limitations on the number of pixels to be cropped. Pixel cropping has to be in the unit of RX lane count as a parameter h_active_unit. In addition to this, the number of active pixels must be a multiple of 4 in case of RAW10 and a multiple of 2 in case of RAW12 according to CSI-2 spec. Moreover, due to the FIFO data width in rx_sublvds, another restriction has to be applied. Table 3.2 shows the unit value (granularity) of h_active_unit for all cases considering all of limitations mentioned above. In most cases, cropping with finer granularity is possible through WC setting. This WC is fed to lane_ctrl as the second stage cropping.

Example: RAW10, 10 RX lane, 4 TX lane with cropping 1920 pixels from 2400 active pixel input
The unit value of h_active_unit for RAW10, 10 RX lane is 16.
Since 1920 / (10 lanes x 16 units) = 12.
set h_active_unit = 16 x 12 = 192 to cover 1920 pixels.
WC = 1920 x 5/4 = 2400.

Table 3.2. Granularity of h_active_unit and WC

Data Type	RX Lane Count	RX Gear	TX Lane Count	TX Gear	Unit Value of h_active_unit	Granularity of WC
RAW10	4	8	1	16	4 (= 16 pixels)	10 (= 8 pixels)
			2	16	4 (= 16 pixels)	20 (= 16 pixels)
			4	8	4 (= 16 pixels)	20 (= 16 pixels)
		16	2	16	2 (= 16 pixels)	20 (= 16 pixels)
			4	16	4 (= 32 pixels)	40 (= 32 pixels)
	6	8	1	16	8 (= 48 pixels)	10 (= 8 pixels)
			2	16	8 (= 48 pixels)	20 (= 16 pixels)
			4	8	8 (= 48 pixels)	20 (= 16 pixels)
	8	8	2	16	4 (= 32 pixels)	20 (= 16 pixels)
			4	16	4 (= 32 pixels)	40 (= 32 pixels)
	10	8	2	16	16 (= 160 pixels)	20 (= 16 pixels)
			4	16	16 (= 160 pixels)	40 (= 32 pixels)
RAW12	4	8	1	16	2 (= 8 pixels)	6 (= 4 pixels)
			2	16	2 (= 8 pixels)	12 (= 8 pixels)
			4	8	2 (= 8 pixels)	12 (= 8 pixels)
		16	2	16	2 (= 16 pixels)	12 (= 8 pixels)
			4	16	2 (= 16 pixels)	24 (= 16 pixels)
	6	8	1	16	4 (= 24 pixels)	6 (= 4 pixels)
			2	16	4 (= 24 pixels)	12 (= 8 pixels)
			4	8	4 (= 24 pixels)	12 (= 8 pixels)
	8	8	2	16	2 (= 16 pixels)	12 (= 8 pixels)
			4	16	2 (= 16 pixels)	24 (= 16 pixels)
	10	8	2	16	8 (= 80 pixels)	12 (= 8 pixels)
			4	16	8 (= 80 pixels)	24 (= 16 pixels)

Note: RX Gear 16 is shown for reference only and not used in this design.

3.4. pixel2byte

This module must be created for RX channel according to data type, the number of RX lanes, RX Gear, and others. Figure 3.6 shows an example of IP interface settings in Radiant Software for the pixel2byte IP. You can use the ipx file (pix2byte/pix2byte.ipx) included in the sample project and re-configure according to your needs. Refer to Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094) for details.

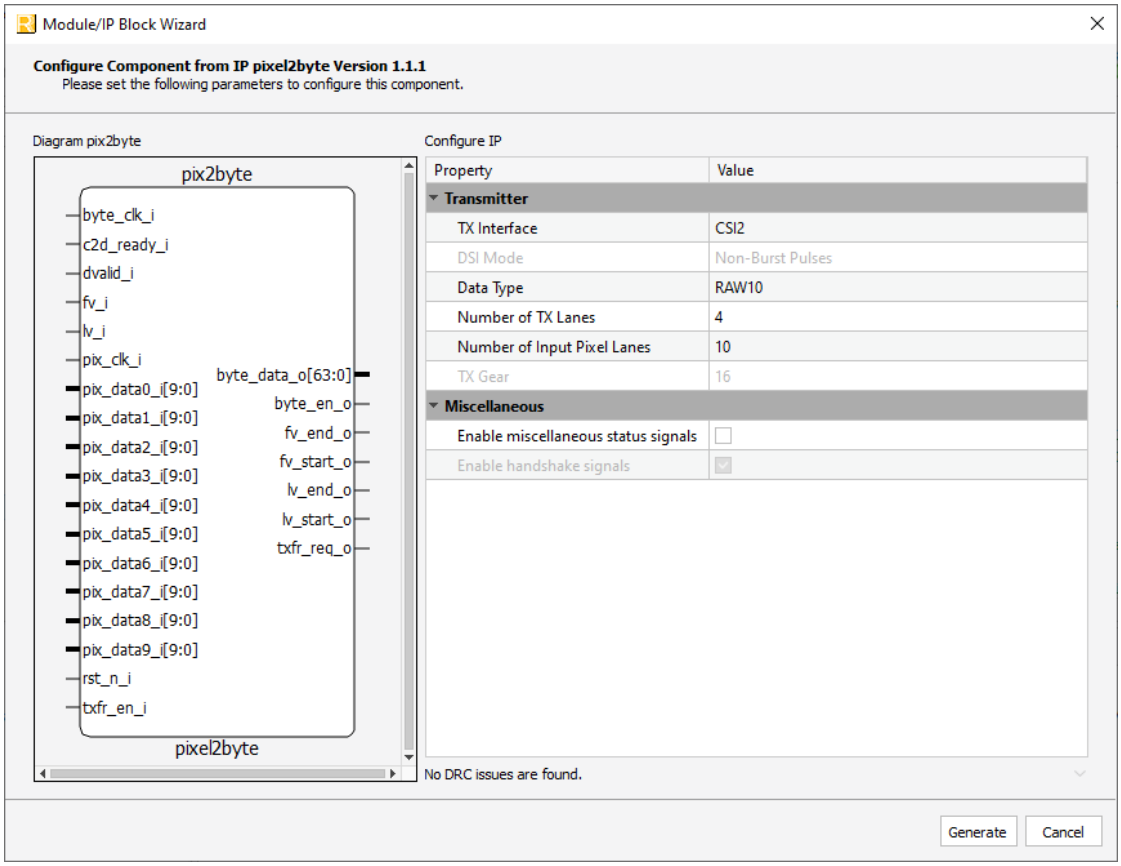

Figure 3.6. pixel2byte IP Creation

The following shows guidelines and parameter settings required for this reference design.

- TX Interface – Select CSI-2.
- Data Type – Select RAW10 or RAW12. Others are not supported by RX SubLVDS IP.
- Number of TX Lanes – Always set 4.
- Number of Input Pixel Per Clock – Set the value equal to (RX lane count) x (RX Gear / 8).
- TX Gear – automatically set in case of Number of Pixel per Clock = 6, 8, or 10. 8 or 16 can be selected in case of Number of Input Pixel per Clock = 4 (refer to Table 1.2).
- Enable miscellaneous status signals – unchecked.

In case that you generate this IP from scratch, it is recommended to set the module name to pix2byte so that you do not need to modify the instance name of this IP in the top-level design as well as the simulation setup file. Otherwise, you have to modify the names accordingly.

This module receives pixel data (pix_data_tc) from trim_ctrl along with fv_tc, lv_tc, and dvalid_tc (frame valid, line valid and data valid) and re-organizes the data to form the byte data via FIFO according to the data type specified. FIFO is used as a data buffer as well as a clock domain bridge. Pixel data are written to FIFO in pixel clock domain and read in byte clock domain. Byte clock is provided from TX D-PHY module. Figure 3.7 shows the global timing of pixel2byte in the case of RX 10-lane with RX Gear 8.

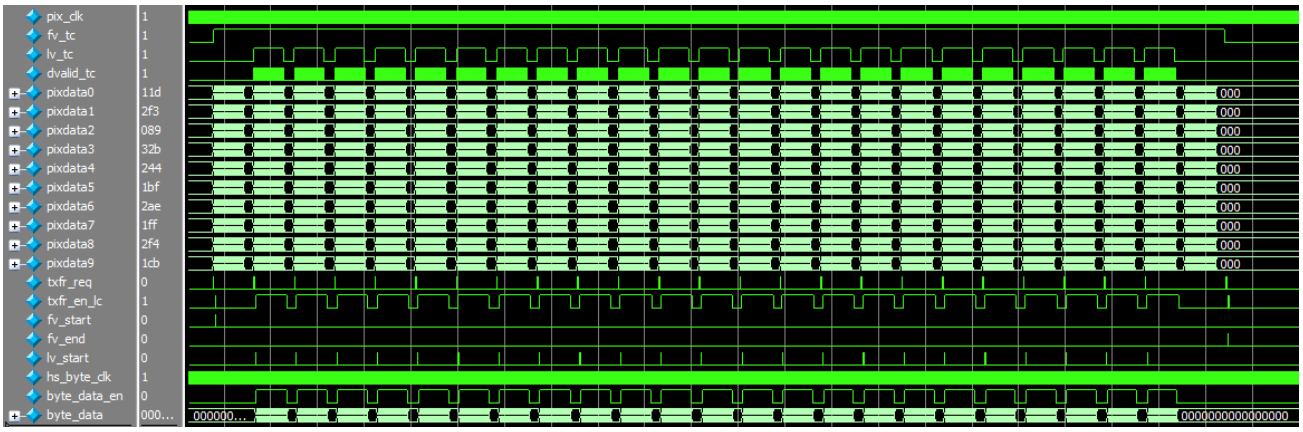

Figure 3.7. Global Timing of pixel2byte

Figure 3.8 shows line transactions. pixel2byte asserts txfr_req after receiving the valid line data and start sending byte based data following lv_start assertion. At the end of one-line valid data, txfr_req is asserted again. This assertion is redundant and masked by lane_ctrl and does not affect the system operation.

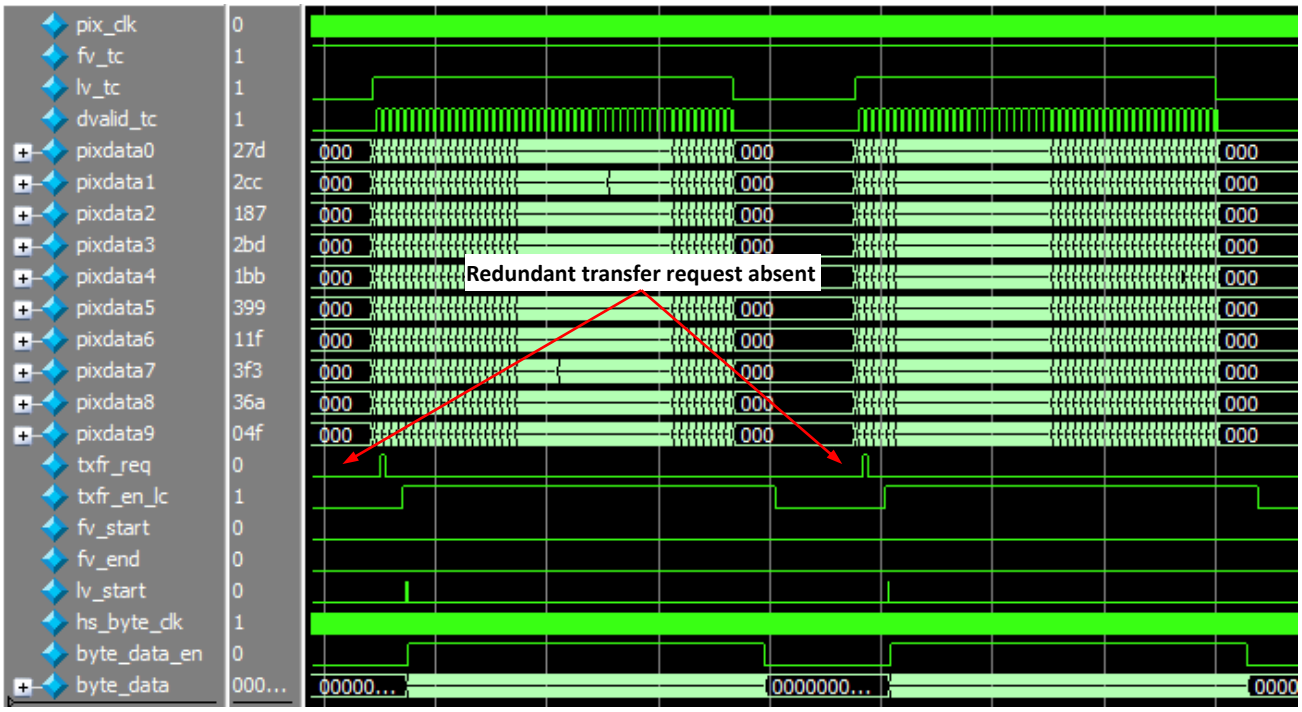

Figure 3.8. Line Transactions of pixel2byte

3.5. lane_ctrl

This module resides between pixel2byte and tx_dphy. It has two major functions:

- Communication control between pixel2byte and tx_dphy
- Bus width and Lane assignment conversion between pixel2byte and tx_dphy

3.5.1. Communication Control

pixel2byte and tx_dphy have handshake signals to request and grant data transfer from pixel2byte to tx_dphy, but current version of IP cannot handle a certain condition (Frame End event happens just after the valid data transmission of the last line) when those signals are directly connected. lane_ctrl holds the assertion of sp_en when txfr_en is high and waits for txfr_req_lc assertion until txfr_en goes low. Figure 3.9 shows the global timing of lane_ctrl in case of RAW10, RX lane count = 10 with RX Gear 8, TX lane count = 4 with TX Gear 8. In this case, byte data that comes from pixel2byte is 64 bits and active data input of TX D-PHY is 32 bits. Therefore hs_byte_clk (= 2x byte_clk) is used to match the input and output bandwidths. As described in the pixel2byte section, txfr_req assertion around the end of valid data transmission is masked by this module and is not transmitted to tx_dphy. This module also handles the clock domain crossing in case that hs_byte_clk is used. A compiler directive of HS_BYTE_CLK is automatically defined in the top-level RTL when hs_byte_clk is required.

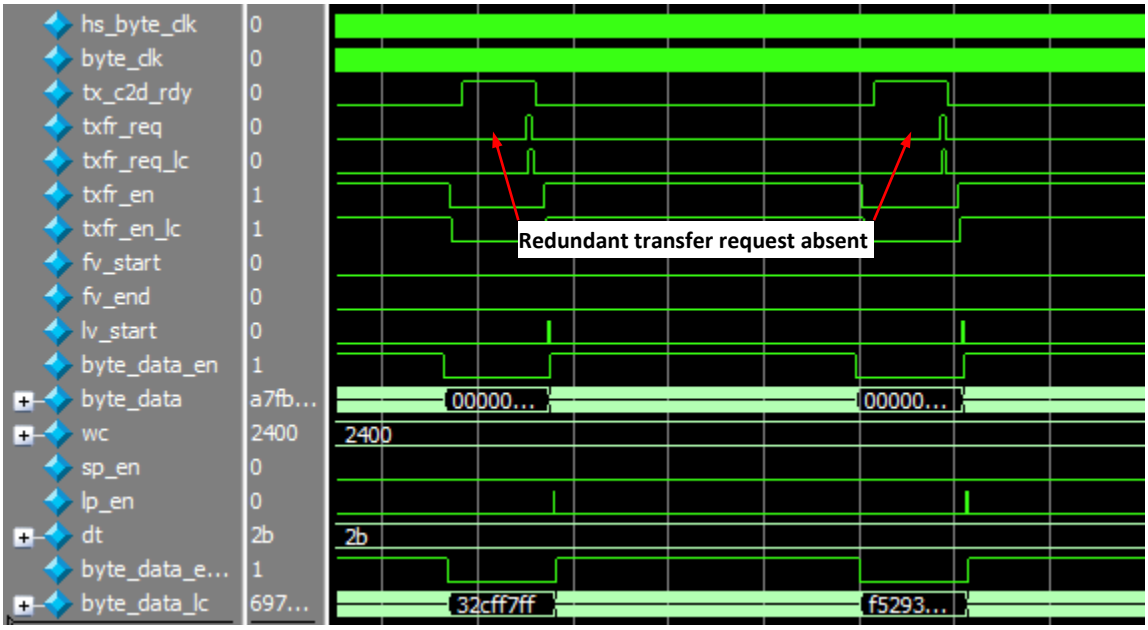

Figure 3.9. Global Timing of lane_ctrl

3.5.2. LP-HS Control in Continuous Clock Mode

Figure 3.10 shows the handshake flow from trim_ctrl to tx_dphy to send Frame Start short packet. fv_tc from trim_ctrl lets pixel2byte asserts txfr_req. Then txfr_req is forwarded as txfr_req_lc when tx_c2d_rdy = 1, which means tx_dphy is ready to begin a new HS transmission. After tx_dphy goes in to HS mode, txfr_en goes 1 and that was transferred as txfr_en_lc to pixel2byte. That lets pixel2byte assert fv_start and lane_ctrl asserts sp_en, which results in short packet transmission by tx_dphy.

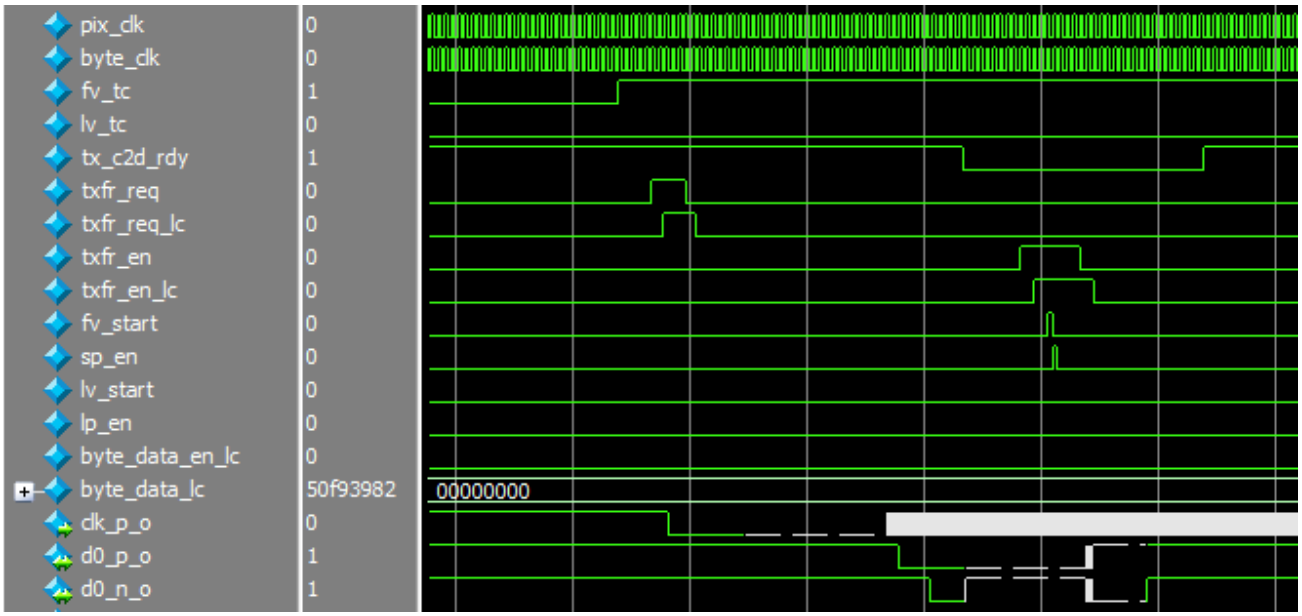

Figure 3.10. LP-HS Transition in Continuous clock mode (Short Packet)

Figure 3.11 shows an example of the handshake for Long Packet transmission. As mentioned earlier, txfr_req while txfr_en = 1 is masked by lane_ctrl and is not transferred to tx_dphy.

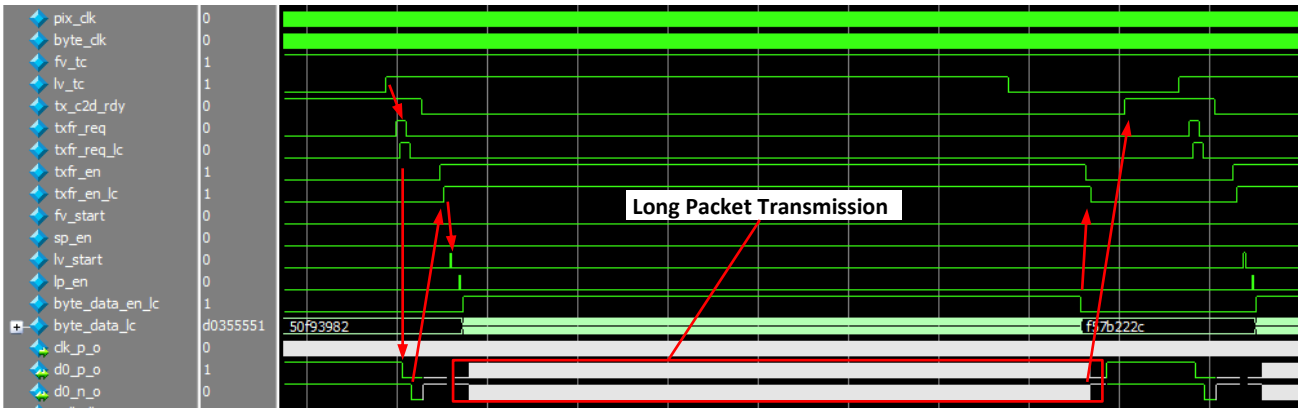

Figure 3.11. LP-HS Transition in Continuous clock mode (Long Packet)

3.5.3. LP-HS Control in Non-Continuous Clock Mode

This module controls LP-HS transition of tx_dphy module as shown in Figure 3.12 and Figure 3.13 with the following sequence in case of non-continuous clock mode.

1. Check tx_c2d_rdy = 1, clk_hs_en_lc = 1 and assert txfr_req (at least one tx_clk_byte cycle).
2. Clock lane goes into HS mode.
3. Data lane goes into HS mode.
4. Wait for txfr_en = 1, then assert tx_sp_en or tx_lp_en for one tx_clk_byte cycle.
5. In case of Long Packet data, assert tx_bd_en along with tx_bd two cycles after ld_pyld = 1.
6. HS data transmission.
7. After HS data transmission is done, txfr_en goes 0 and data lane goes to LP mode. Then clock lane goes to LP mode.
8. After all HS transaction ends, tx_c2d_rdy becomes 1, which means tx_dphy is ready to handle the next HS transaction.

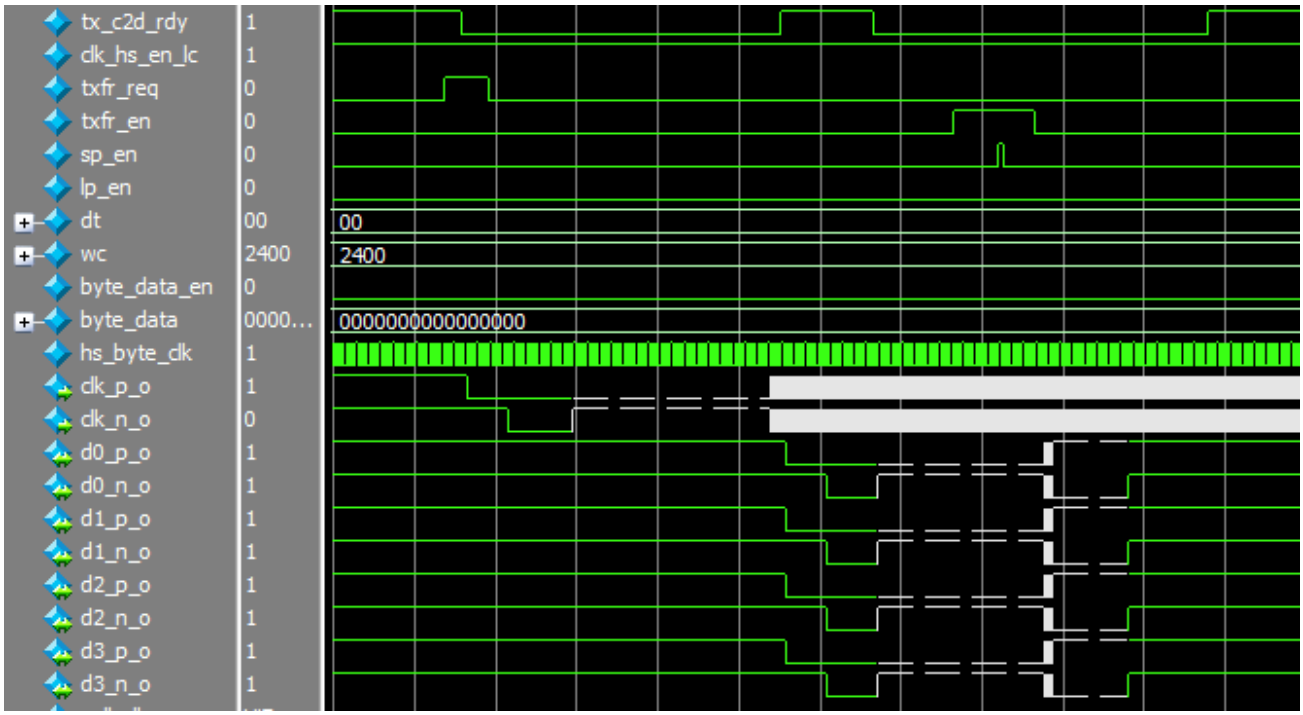

Figure 3.12. LP-HS Transition in Non-Continuous clock mode (Short Packet)

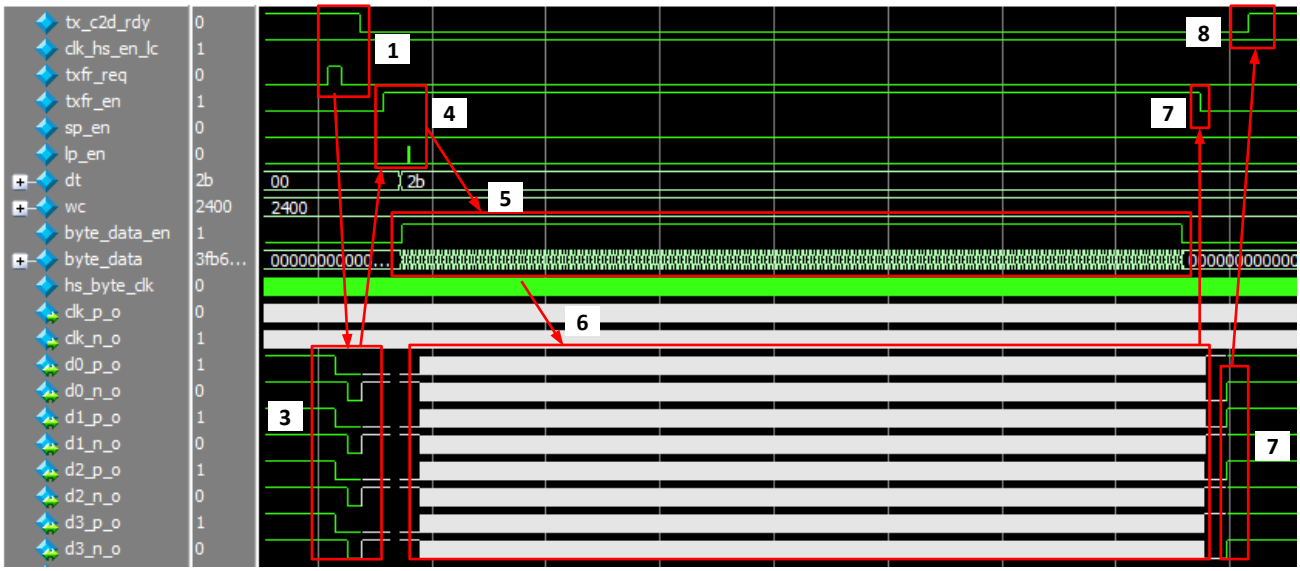

Figure 3.13. LP-HS Transition in Non-Continuous clock mode (Long Packet)

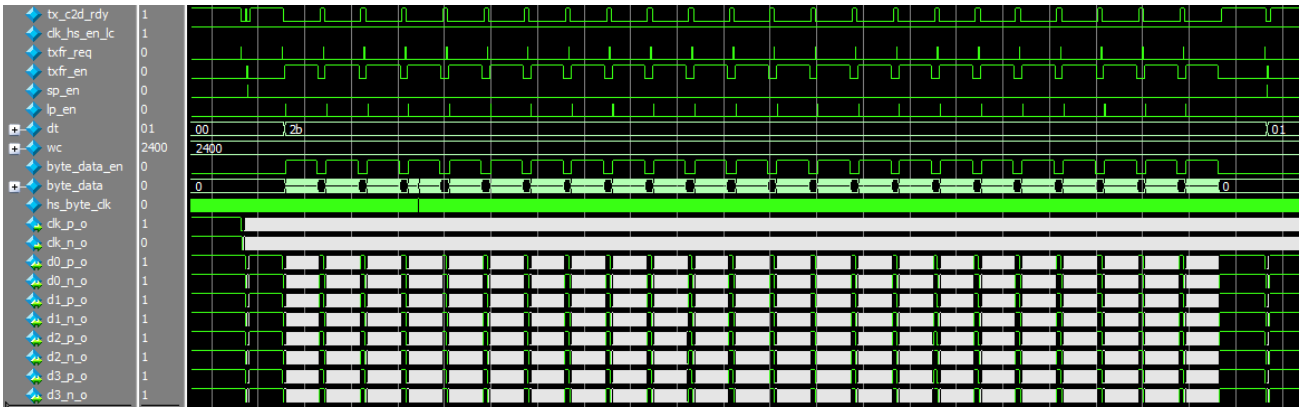

Figure 3.14. LP-HS Transition in Non-Continuous clock mode with KEEP_HS

3.5.4. Bus Width Conversion

Since pixel2byte configuration is always with 4 TX lanes, bus width conversion is necessary when TX lane count is 1 or 2. Figure 3.15 shows the example in case of RAW10, RX lane count = 10 with RX Gear 8, TX lane count = 4 with TX Gear 8. 64-bit data are stored into the internal FIFO using byte_clk and read back using hs_byte_clk in every other cycles and sent to tx_dphy.

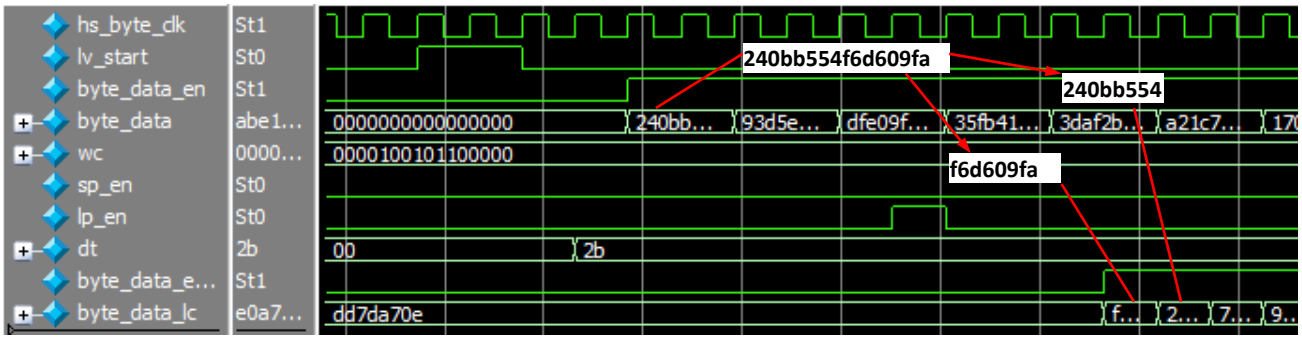

Figure 3.15. Bus Width Conversion by lane_ctrl

3.6. tx_dphy

This module must be created for TX channel according to the number of TX lanes, TX Line Rate, and others. Figure 3.16 shows an example of IP interface settings in the Lattice Radiant software for the TX D-PHY IP. You can use the ipx file (tx_dphy/tx_dphy.ipx) included in the sample project and re-configure according to your needs. Refer to CSI-2/DSI D-PHY Transmitter IP Core User Guide (FPGA-IPUG-02080) for details.

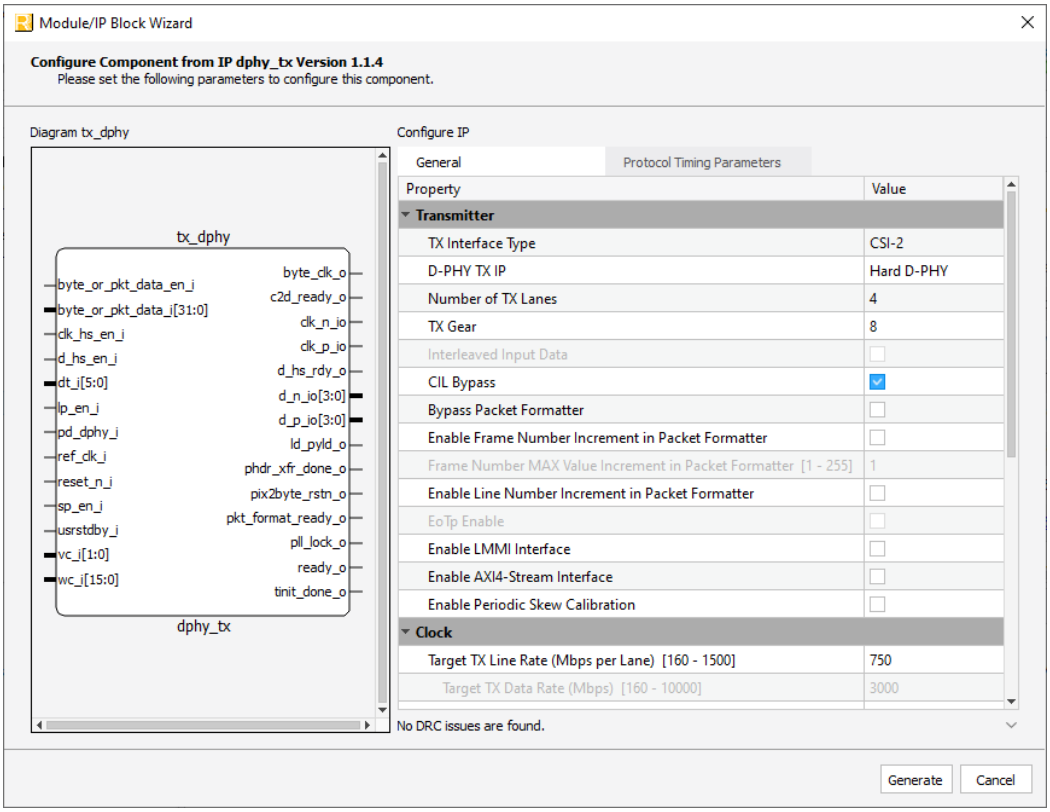

Figure 3.16. tx_dphy IP Creation #1

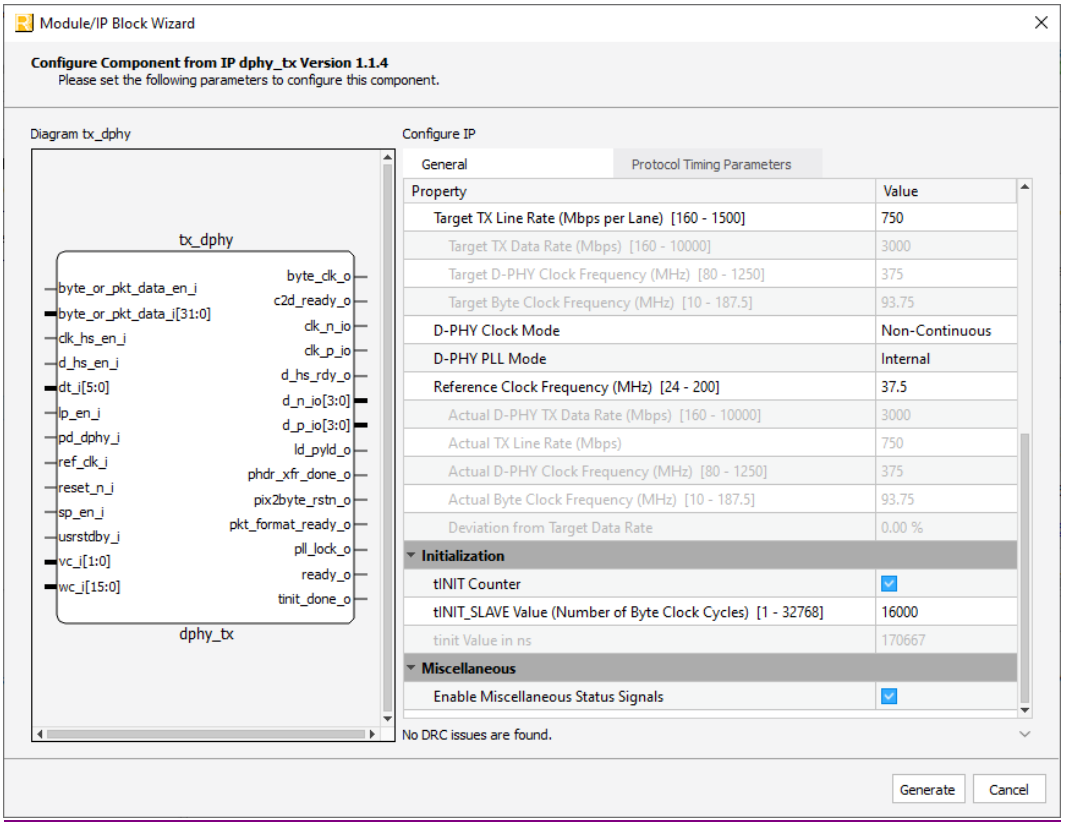

Figure 3.17. tx_dphy IP Creation #2

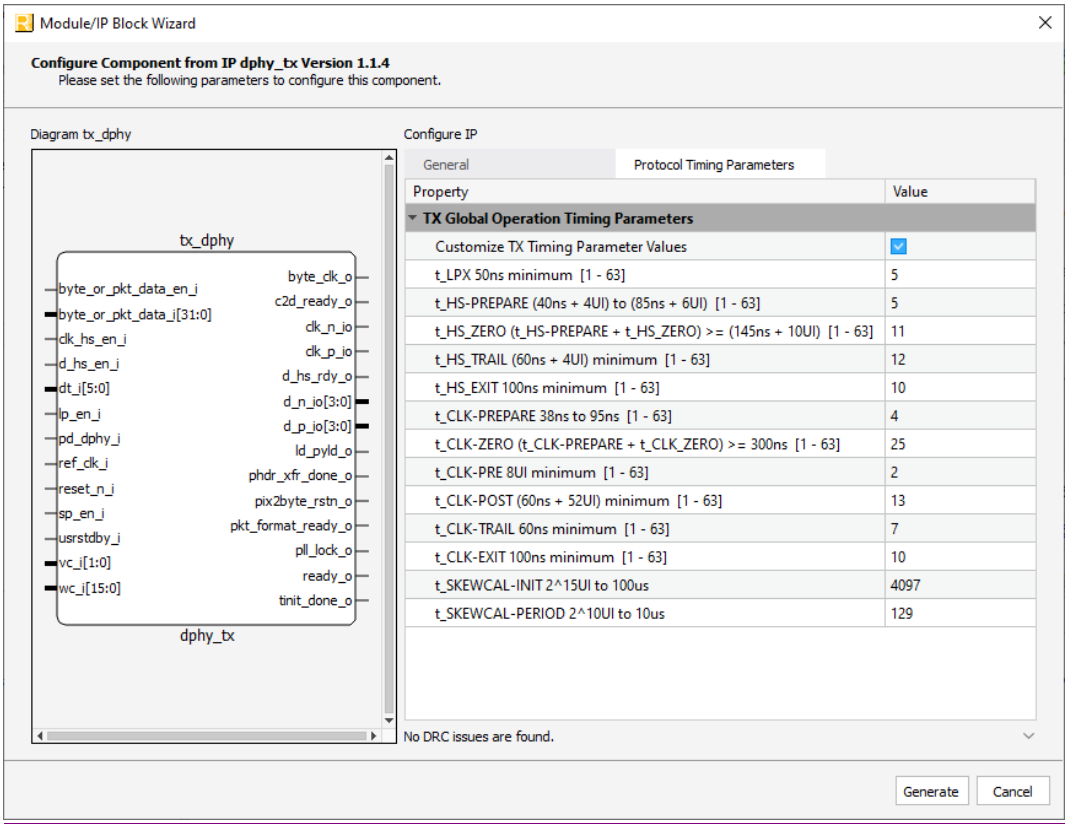

Figure 3.18. tx_dphy IP Creation #3

The following shows guidelines and parameter settings required for this reference design.

- TX Interface type – Select CSI-2.
- DPHY TX IP – Select Hard DPHY.
- Number of TX Lanes – Set according to TX lane configuration. Must match NUM_TX_LANE_* setting.
- TX Gear – Automatically set according to TX Line Rate.
- Interleaved Input Data – Must be disabled (unchecked).
- CIL Bypass – Must be enabled (checked).
- Bypass packet formatter – Must be disabled (unchecked).
- Enable frame number increment in Packet Formatter – Must be disabled (unchecked).
- Enable line number increment in Packet Formatter – Must be disabled (unchecked).
- TX Line Rate per Lane – Use the value specified in the Excel sheet.
- DPHY Clock Mode – Set according to TX channel configuration. Continuous is recommended when the length of the horizontal blanking period is unknown.
- DPHY PLL Mode – Always set Internal.
- Reference Clock Frequency – Set the appropriate value which can be obtained by pix_clk or GPLL output. This clock frequency must be 24 – 200 MHz.
- tINIT counter – Enabled (checked) is recommended.
- tINIT_SLAVE Value – Value to make tINIT Value more than 100 µs is recommended.
- Enable miscellaneous status signals – Must be set to enabled (checked).
- Protocol Timing Parameters tab – Default values are recommended.

This module takes the byte data and outputs CSI-2 data after serialization in CSI-2 High Speed mode. In case that you generate this IP from scratch, it is recommended to set the design name to tx and module name to tx_dphy so that you do not need to modify the instance name of this IP in the top level design as well as simulation setup file. Otherwise, you need to modify the names accordingly.

TX Line Rate is derived from the following equation:

$$TX\_lane\_bandwidth = \frac{RX\_lane\_bandwidth * number\_of\_RX\_lane}{number\_of\_TX\_lane}$$

Example #1: RAW10 RX with 10-lane at RX lane bandwidth = 600 Mbps with 4 TX lanes
TX lane bandwidth = (600 x 10) / 4 = 1500 Mbps.

Example #2: RAW12 RX with 4-lane at RX lane bandwidth = 1200 Mbps with 4 TX lanes
TX lane bandwidth = (1200 x 4) / 4 = 1200 Mbps.

3.7. int_gpll

Create the GPLL module to generate the reference clock for TX DPHY IP when pix_clk frequency is not in the range of 24 -200 MHz. You can use the ipx file (int_gpll/int_gpll.ipx) included in the sample project and reconfigure according to your needs. In case you generate this IP from scratch, it is recommended to set the design name to int_gpll so that you do not need to modify the instance name of this IP in the top level design as well as in the simulation setup file. Otherwise, you need to modify the names accordingly.

You have to define USE_GPLL directive in synthesis_directives.v.

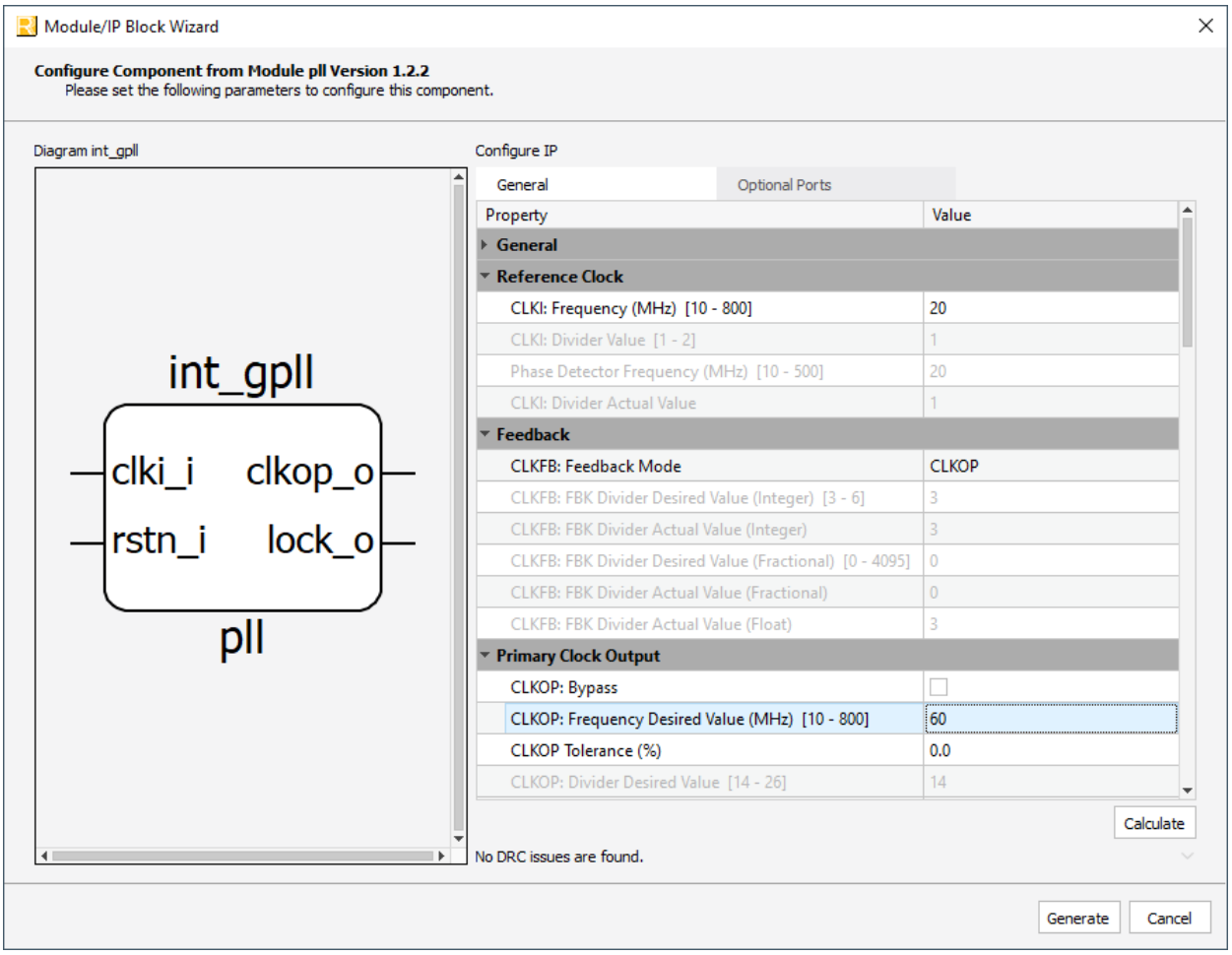

Figure 3.19. GPLL IP Creation

3.8. i2c_slave

This module is instantiated when USE_I2C is defined and enables you to change parameters on the fly through I²C connections. I²C Hard IP is instantiated and used as an I²C slave device. You can use the ipx file (i2c_s/i2c_s.ipx) included in the sample project and re-configure. In case that you generate this IP from scratch, it is recommended to set the module name to i2c_s so that you do not need to modify the instance name of this IP in i2c_slave as well as simulation setup file. Otherwise, you need to modify the names accordingly. Refer to I²C Slave IP Core User Guide (FPGA-IPUG-02072) for details. Figure 3.20 shows basic settings of I²C Slave IP. The following shows guidelines and parameter settings required for this reference design.

- APB Mode Enable – Recommended to be disabled (unchecked).
- Addressing Mode – 7-bit is recommended.
- I2C Slave Address – Set the value of your selection.
- System Clock Frequency – Set the appropriate frequency.
- FIFO Depth – 16 is recommended.
- Implementation of FIFO – LUT is recommended.
- TX FIFO Almost Empty Flag – Set the value of your selection (unused).
- TX FIFO Almost Full Flag – Set the value of your selection (unused).

In the current design, I²C data written from the external host device is stored in the FIFO and those data are read when I²C write transaction is completed. Since the first write data is for I²C sub address, total 17 data must be stored in case of consecutive full 16 data write. The current FIFO depth setting is 16 and FIFO overflow happens. To avoid that, consecutive data must be up to 15 data. Alternately, you can increase the FIFO depth to 32 if you want to write all 16 data in a single write transaction. In the sample design, 45 MHz clock generated by the on-chip oscillator is fed as a system clock.

One typical usage of this module is changing parameters during the system development and/or debugging stages so that you can try many cases without updating FPGA bit files as long as I²C registers cover what you would like to change. After that you can recreate a bit file using the finalized parameters without USE_I2C directive for the product.

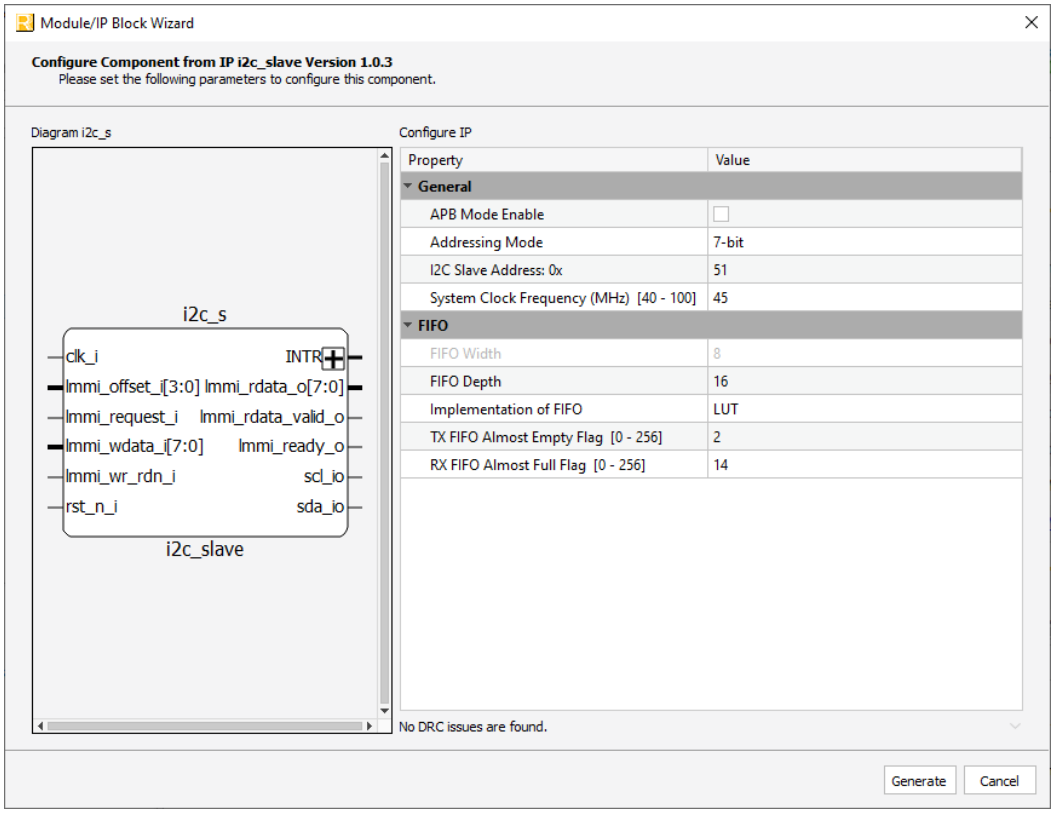

Figure 3.20. I²C Slave IP Creation

This module is equipped with parameter registers of 4-bit address area of I²C sub-address shown in Table 3.3.

Table 3.3. I²C Slave Register Map

Sub Address	Name	Bit assignment	Description
0	SW Reset	[0]	Software reset register. When this is active, all modules except for i2c_slave are in reset condition. Active low.
1	TOP_TRIM	[5:0]	Top edge trim register. The value must be 6'd1 – 6'd63.
2	V_ACTIVE[7:0]	[7:0]	Vertical active line register. The value must be 12'd1 – 12'd4095.
3	V_ACTIVE[11:8]	[3:0]	
4	LEFT_TRIM_UNIT	[5:0]	Left edge trim register by the unit. The value must be 6'd0 – 6'd63.
5	LEFT_TRIM_LANE	[3:0]	Left edge trim register within the lanes. The value must be 4'd0 – 4'd9.
6	H_ACTIVE_UNIT[7:0]	[7:0]	Horizontal Active Pixel register by the unit. The value must be 10'd1 – 10'd1023.
7	H_ACTIVE_UNIT[9:8]	[1:0]	
8	WC[7:0]	[7:0]	Word count register. The value must be 16'd1 – 16'd65535.
9	WC[15:8]	[15:8]	
10	VC	[1:0]	Virtual channel ID register. The value must be 2'd0 – 2'd3.
	KEEP_HS	[7]	Force clock lane in HS mode during active lines regardless of TX clock mode.
11	V_TOTAL[7:0]	[7:0]	Total line count register used in Sensor Slave Mode. The value must be 12'd10 – 12'd4095.
12	V_TOTAL[11:8]	[3:0]	
13	H_TOTAL[7:0]	[7:0]	Total horizontal cycle count register used in Sensor Slave Mode. The value must be 12'd10 – 12'd4095.
14	H_TOTAL[11:8]	[3:0]	
15	XHS_LENGTH	[7:0]	XHS pulse length register. Used in Sensor Slave Mode. The value must be 8'd1 -8'd255.

All registers are set to the default values specified by corresponding directives defined in synthesis_directives.v.

Software reset works as the system reset (reset_n_i) for all modules other than i2c_slave, therefore you can assert this while updating other I²C registers, then release Software reset upon completing the register update to avoid an unexpected operation during register update. Refer to the Simulation Directives and trim_ctrl sections for register details.

3.9. int_osc

In the sample design, a 45 MHz clock is generated by the on-chip oscillator and fed to i2c_slave module. You can use the ipx file (int_osc/int_osc.ipx) included in the sample project and re-configure according to your needs. In case you generate this IP from scratch, it is recommended to set the module name to int_osc so that you do not need to modify the instance name of this IP in the top level design as well as simulation setup file. Otherwise, you need to modify the names accordingly. This module is not necessary when i2c_slave is not used.

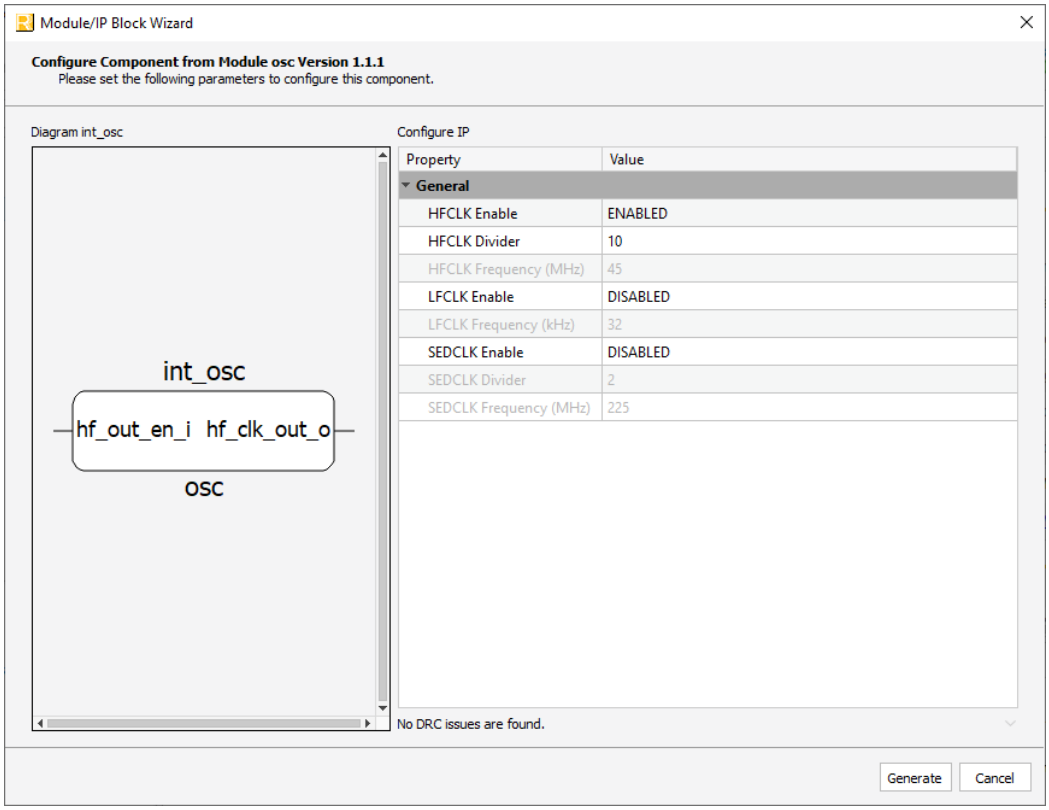

Figure 3.21. OSC IP Creation

4. Design and File Modification by User

This reference design is based on version 1.0.4 of the subLVDS Image Sensor Receiver IP, version 1.1.1 of the Pixel-to-Byte Converter IP, and version 1.1.4 of the CSI-2/DSI D-PHY Transmitter IP.

4.1. Top-level RTL

You have to change IP instance names if you generate IPs created in Radiant Software with different instance names in the sample project.

If you use I^2C Slave module with a clock other than the internal oscillator clock, you will have to disable the int_osc (internal oscillator) instantiation and connect an appropriate clock to clk_i port of i2c_slave.

5. Design Simulation

The script file (sublvds2csi2_NX_msim.do) and testbench files are provided to run the functional simulation by ModelSim Lattice FPGA Edition 2020.3. If you follow the naming recommendations regarding design names and instance names when RX subLVDS, Pixel-to-Byte, TX D-PHY, GPLL, and I²C IPs are created by Radiant Software, the following will be the only change required in the script file.

- User Project directory shown by red box.

```
### Set Customer's simulation directory ###
set sim_dir C:/Users/Desktop/SubLVDS_MIPI_CSI2_Crosslink_NX/simulation/lifcl
```

Figure 5.1. Script File Modification

You need to modify simulation_directives.v according to your configuration (refer to Simulation Directives for details). By executing the script in ModelSim, compilation and simulation are executed automatically. The testbench takes all data comparison between the expected data and output data from the RD. It shows the following statements while running and doing data comparison:

```
### unit_cnt = 203, after lane_no = 7, payload_cnt = 2039, payload_LSBs = c6
# [920939920][CSI-2_CHK] Frame 3, Line 23, Byte Count 1625 - 1628, payload data = c3 43 2b 84 --- Data matches : c3 43 2b 84
# [920945632][CSI-2_CHK] Frame 3, Line 23, Byte Count 1629 - 1632, payload data = 53 75 8c 37 --- Data matches : 53 75 8c 37
# [920951344][CSI-2_CHK] Frame 3, Line 23, Byte Count 1633 - 1636, payload data = 47 af b7 f1 --- Data matches : 47 af b7 f1
# h_lane_on = 1, pixel_cnt = 1632
# unit_cnt = 204, lane_no = 0, payload_cnt = 2040, payload[9:2] = a4 by rx_dat[1632] = 291
# h_lane_on = 1, pixel_cnt = 1633
# unit_cnt = 204, lane_no = 1, payload_cnt = 2041, payload[9:2] = e5 by rx_dat[1633] = 394
# h_lane_on = 1, pixel_cnt = 1634
# unit_cnt = 204, lane_no = 2, payload_cnt = 2042, payload[9:2] = df by rx_dat[1634] = 37e
# h_lane_on = 1, pixel_cnt = 1635
# unit_cnt = 204, lane_no = 3, payload_cnt = 2043, payload[9:2] = 25 by rx_dat[1635] = 097
### unit_cnt = 204, after lane_no = 3, payload_cnt = 2044, payload_LSBs = e1
# h_lane_on = 1, pixel_cnt = 1636
# unit_cnt = 204, lane_no = 4, payload_cnt = 2045, payload[9:2] = 76 by rx_dat[1636] = 1d9
# h_lane_on = 1, pixel_cnt = 1637
# unit_cnt = 204, lane_no = 5, payload_cnt = 2046, payload[9:2] = 80 by rx_dat[1637] = 200
# h_lane_on = 1, pixel_cnt = 1638
# unit_cnt = 204, lane_no = 6, payload_cnt = 2047, payload[9:2] = e4 by rx_dat[1638] = 392
# h_lane_on = 1, pixel_cnt = 1639
# unit_cnt = 204, lane_no = 7, payload_cnt = 2048, payload[9:2] = 20 by rx_dat[1639] = 083
### unit_cnt = 204, after lane_no = 7, payload_cnt = 2049, payload_LSBs = e1
# [920957056][CSI-2_CHK] Frame 3, Line 23, Byte Count 1637 - 1640, payload data = 02 40 57 7c --- Data matches : 02 40 57 7c
# [920962768][CSI-2_CHK] Frame 3, Line 23, Byte Count 1641 - 1644, payload data = 36 1a 0e f7 --- Data matches : 36 1a 0e f7
# h_lane_on = 1, pixel_cnt = 1640
# unit_cnt = 205, lane_no = 0, payload_cnt = 2050, payload[9:2] = 3a by rx_dat[1640] = 0eb
# h_lane_on = 1, pixel_cnt = 1641
```

Data Comparison

Simulation halts when data comparison fails. The following statements are shown when simulation is completed.

```
# [927019630][DPHY_LP_HS_CHK] LP11 to LP01 Transition on D0 lane
# [927071038][DPHY_LP_HS_CHK] LP01 to LP00 Transition on D0 lane with LP01 period = 51 ns
# [927133870][DPHY_LP_HS_CHK] LP00 to HS00 Transition on D0 lane with LP00 period = 62 ns
# [927339145][DPHY_LP_HS_CHK] HS00 to HS Transition on D0 lane with LP00+HS00 period = 268 ns
# [927348784][CSI-2_CHK] Short Packet detected : Data type = 01 --- Frame End
# [927442318][DPHY_LP_HS_CHK] HS to LP11 Transition on D0 lane with HS-TRAIL period = 93 ns
#            930249180 : ### EAV Insertion ###
#
#            931163100 : ### SAV Insertion ###
#
#            934647420 : ### EAV Insertion ###
#
#            935561340 : ### SAV Insertion ###
#
#            939045660 : ### EAV Insertion ###
#
#            939102780 : End of frame :          2
#
# Total payload bytes checked were 165600 = 3 Frames x 2400 bytes (1920 pixels) x 23 lines : all matched !!!!!
# Simulation Succeeded !!!!!
# TEST END!!!
```

The above shows results after running three frames.

Figure 5.2 shows the global timing of 10-lane RX and 4-lane TX. In this case, the first and the last lines are trimmed.

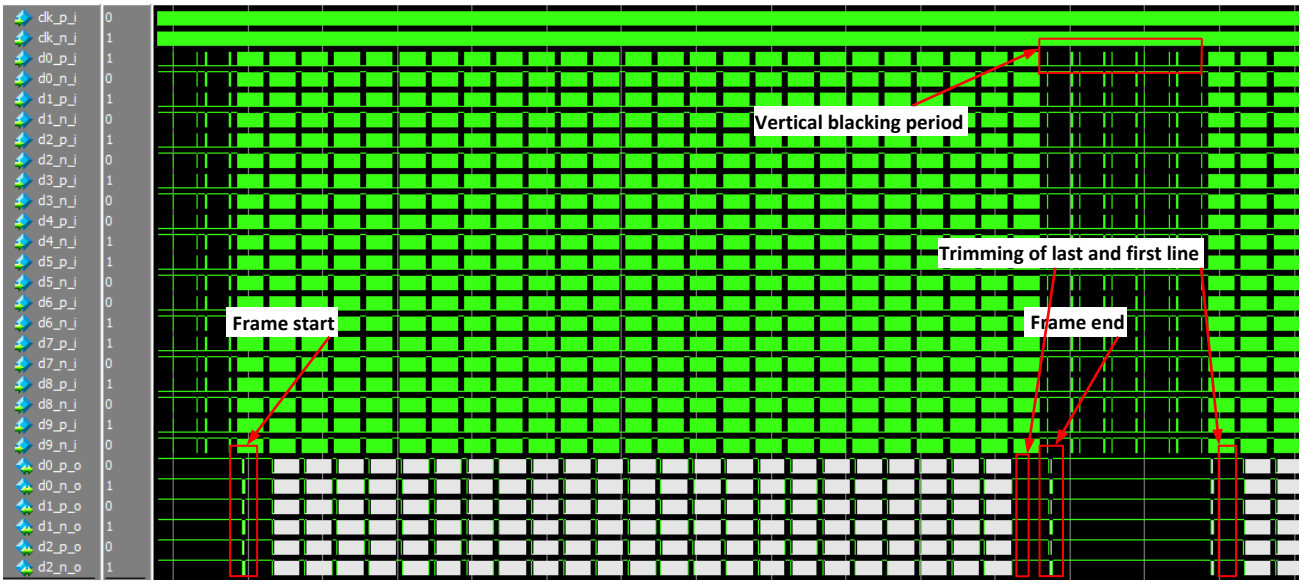

Figure 5.2. Global Timing of 10-Lane RX and 4-Lane TX

Figure 5.3 shows the close-up of the above waveform of one line period. Non-continuous clock mode is selected in TX D-PHY in this case so that CSI-2 TX clock lane goes into LP (Low Power) mode after the data lanes go into LP mode, then comes back to HS (High Speed) mode followed by the data lane transition to HS mode.

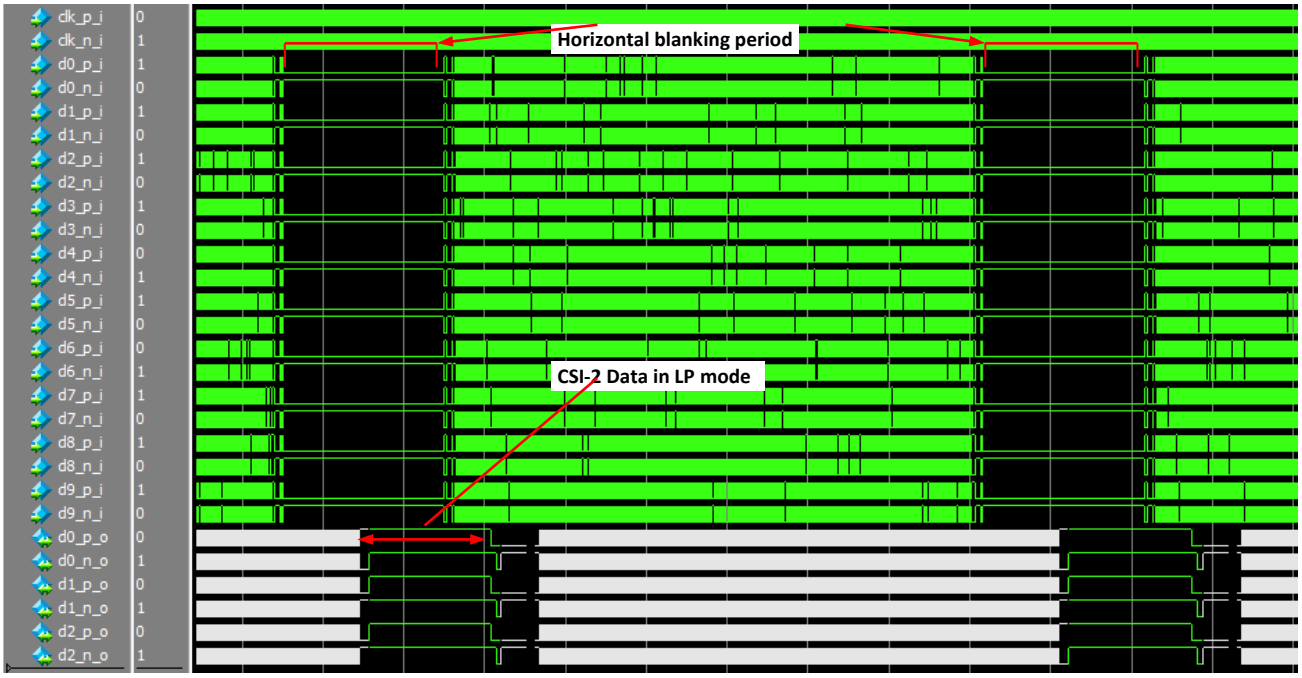

Figure 5.3. CSI-2 LP/HS Mode Transitions

Figure 5.4 shows the global timing of RAW12, 6-lane RX to 2-lane TX with Sensor Slave Mode. FPGA generates xvs_o and xhs_o as vertical and horizontal sync signals.

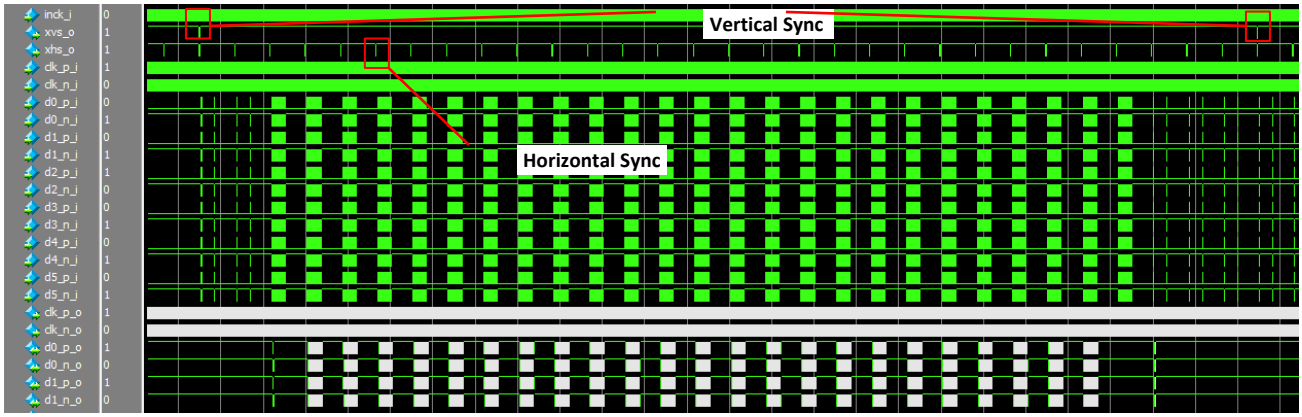

Figure 5.4. Global Timing with Sensor Slave Mode

6. Design Debug on Hardware

Hardware debug of a MIPI related design is a challenge when the system is not working and there is no clue to the area of the MIPI path that is causing the problem. This section shows some guidelines to try to isolate the cause of the problem.

Note that what is described here only provides some ideas on how to debug the system including FPGA functionality, but is not a comprehensive list that covers all possible scenarios.

6.1. Top-Level

The following is essential points you should check first:

- Power Supply or any board related issues
- Pin assignments / Signal Connections
- Reset Signals
- Clock Signals including PLL outputs
- Parameter and/or Mode mismatch

6.2. D-PHY TX Control

At least two scenarios exist in case that the system doesn't work related to D-PHY TX IP.

[Continuous Clock Mode Operation]

Some downstream devices need LP to HS transition on clock lane even though stating to support Continuous clock mode. Using Non-Continuous clock mode is a way to eliminate this potential issue. Along with Non-Continuous clock mode you can enable `define KEEP_HS in synthesis_directives.v as described in lane_ctrl section in case that you cannot allow the clock lane to go into LP mode during the horizontal blanking period.

[Timing Parameter Modification]

The simulation testbench includes the timing checker and issues an error when outgoing MIPI signals violates the MIPI timing specs, but you might want to give some more timing margins when the timing is close to the minimum or maximum values specified by the spec. In that case, you can modify the timing parameters shown in Figure 3.18. These values are based on the byte clock cycles.

7. Known Limitations

The following are the limitations of this reference design.

- The first line must be always trimmed by either rx_sublvds or trim_ctrl.
- Granularity of CSI-2 output video data is coarser than CSI-2 specification for both RAW10 and RAW12 as described in the trim_ctrl section.
- The design does not support RX Gear 16. It also does not support hs_byte_clk ratio of 0.5x and above 4x.
- The simulation may fail for configurations where D-PHY Tx Line rate is greater than 1500 Mbps and in non-continuous mode. This will be addressed in the next revision of the CSI-2/DSI D-PHY Transmitter IP.
- Simulation may fail for some LEFT_TRIM_UNIT and LEFT_TRIM_LANE configurations.

8. Design Package and Project Setup

The SubLVDS to MIPI CSI-2 Image Sensor Bridge Reference Design with CrossLink-NX is available on the Lattice website at www.latticesemi.com. Figure 8.1 shows the directory structure. The design is targeted for LIFCL-40. synthesis_directives.v and simulation_directives.v are set to configure an example shown below:

- RX – RAW10, 10 lanes, Gear 8, I2C enabled
- TX – 4 lanes with Gear 8

You can modify the directives for own configuration.

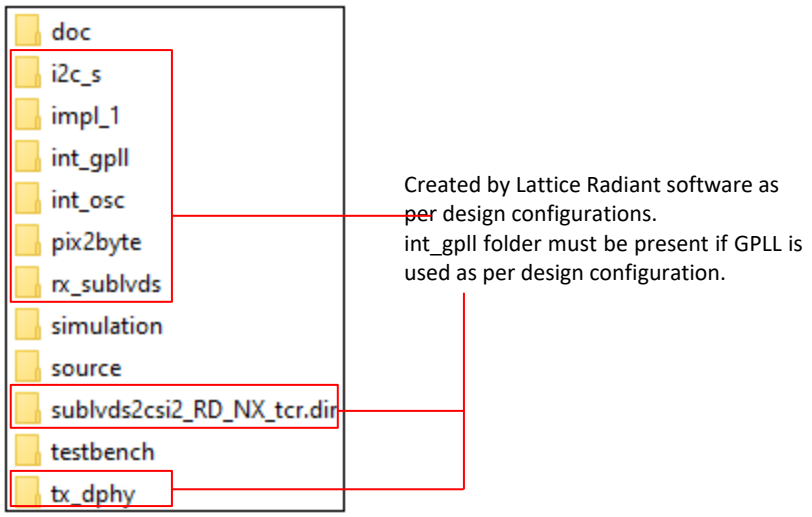

Figure 8.1. Directory Structure

Folders i2c_s, int_osc, pix2byte, rx_sublvds, and tx_dphy are created by the Lattice Radiant software for corresponding IPs. Figure 8.2 shows design files used in the Lattice Radiant software project. The Lattice Radiant software creates five .ipx files. Folder of int_gpll must be available in the directory structure to enable USE_GPLL directive as per design requirements. If not available then you must create one from Lattice Radiant Software IP Catalog.

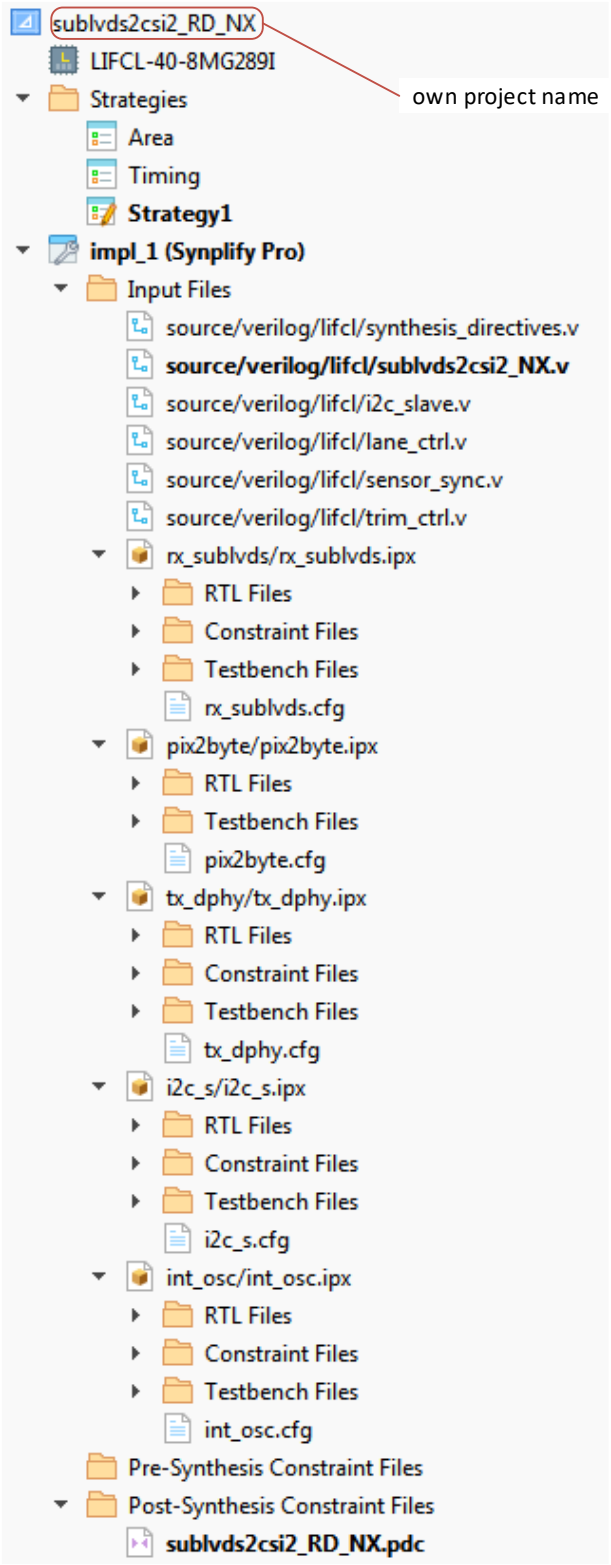

Figure 8.2. Project Files

9. Resource Utilization

Resource utilization depends on the configurations. Table 9.1 shows resource utilization examples under certain configurations. Actual usage may vary.

Table 9.1. Resource Utilization Examples

Configuration	LUT (Utilization/Total)	FF (Utilization/Total)	EBR (Utilization/Total)	I/O (Utilization/Total)
RAW12 RX 4 lanes, Gear 8 to TX 2 lanes with I^2C, Sensor Master Mode	2221/32256	1465/32775	4/84	8/173
RAW12 RX 4 lanes, Gear 8 to TX 1 lanes with I^2C, Sensor Master Mode	2174/32256	1482/32775	5/84	8/173
RAW10 RX 6 lanes, Gear 8 to TX 2 lanes with I^2C, Sensor Master Mode	2570/32256	1546/32775	5/84	10/173
RAW12 RX 8 lanes, Gear 8 to TX 4 lanes with I^2C, Sensor Master Mode	3910/32256	1987/32775	6/84	12/173
RAW10 RX 10 lanes, Gear 8 to TX 4 lanes with I^2C, Sensor Slave Mode	3886/32256	2008/32775	8/84	14/173

References

- MIPI® Alliance Specification for D-PHY Version 1.2
- MIPI® Alliance Specification for Camera Serial Interface 2 (CSI-2) Version 1.2
- SubLVDS Image Sensor Receiver IP Core User Guide (FPGA-IPUG-02093)
- Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094)
- CSI-2/DSI D-PHY Transmitter IP Core User Guide (FPGA-IPUG-02080)
- I^2C Slave IP Core User Guide (FPGA-IPUG-02072)

For more information on the CrossLink FPGA device, visit http://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX.

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow, Tasks, and Simulation Flow, see the Lattice Radiant User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, April 2021

Section	Change Summary
All	Initial release

www.latticesemi.com