Parallel to MIPI CSI-2 and DSI with CertusPro-NX

Reference Design

FPGA-RD-02239-1.2

May 2023

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CSI-2	Camera Serial Interface 2
DPI	Display Pixel Interface
DSI	Display Serial Interface
EBR	Embedded Block RAM
ECC	Error Correction Code
GPLL	General Purpose PLL
HS	High Speed
LP	Low Power
LUT	Look Up Table
MIPI	Mobile Industry Processor Interface
PLL	Phase Locked Loop
P2B	Pixel2Byte
RX	Receiver
TX	Transmitter

1. Introduction

The Mobile Industry Processor Interface (MIPI®) D-PHY was developed primarily to support camera and display interconnections in mobile devices, and it has become the industry's primary high-speed PHY solution for these applications in smartphones. It is typically used in conjunction with MIPI Camera Serial Interface-2 (CSI-2) and MIPI Display Serial Interface (DSI) protocol specifications. It meets the demanding requirements of low power, low noise generation, and high noise immunity that mobile phone designs demand.

MIPI D-PHY is a practical PHY for typical camera and display applications. It is designed to replace traditional parallel bus based on LVCMOS or LVDS. However, many processors and displays/cameras still use RGB, CMOS, or MIPI Display Pixel Interface (DPI) as interface.

The Parallel to MIPI reference design allows the quick interface for a processor with an RGB interface to a display with a MIPI DSI interface or a camera with a CMOS interface to a processor with CSI-2 interface. The Lattice Semiconductor Parallel to MIPI D-PHY Interface reference design provides this conversion for Lattice Semiconductor CertusPro-NX devices. This is useful for wearable, tablet, human machine interfacing, medical equipment and many other applications.

1.1. Supported Device and IP

This reference design supports the following devices with IP versions.

Device Family	Part Number	Compatible IP
CertusPro™-NX	LFCPNX-100	Pixel-to-Byte Converter IP version 1.4.0 D-PHY Transmitter IP version 1.7.2

The IPs above are supported by Lattice Radiant™ software version 2022.1 or later.

1.2. Features List

The key features of the Parallel to MIPI Reference Design are:

- Compliant with MIPI D-PHY version 1.2, MIPI DSI version 1.2, and MIPI CSI-2 version 1.2 Specifications
- Supports MIPI DSI and MIPI CSI-2 interfacing up to 6 Gb/s for Soft D-PHY
- Supports 1, 2, or 4 MIPI D-PHY data lanes
- Supports non-burst mode with sync pulses for transmission of DSI packets only
- Supports low-power (LP) mode during vertical and horizontal blanking
- Supports common MIPI DSI compatible video formats (RGB888, RGB666)
- Supports common MIPI CSI-2 compatible video formats (RGB888, RAW8, RAW10, RAW12, RAW14)

1.3. Block Diagram

Figure 1.1 shows the block level diagram of the Parallel to MIPI Reference Design.

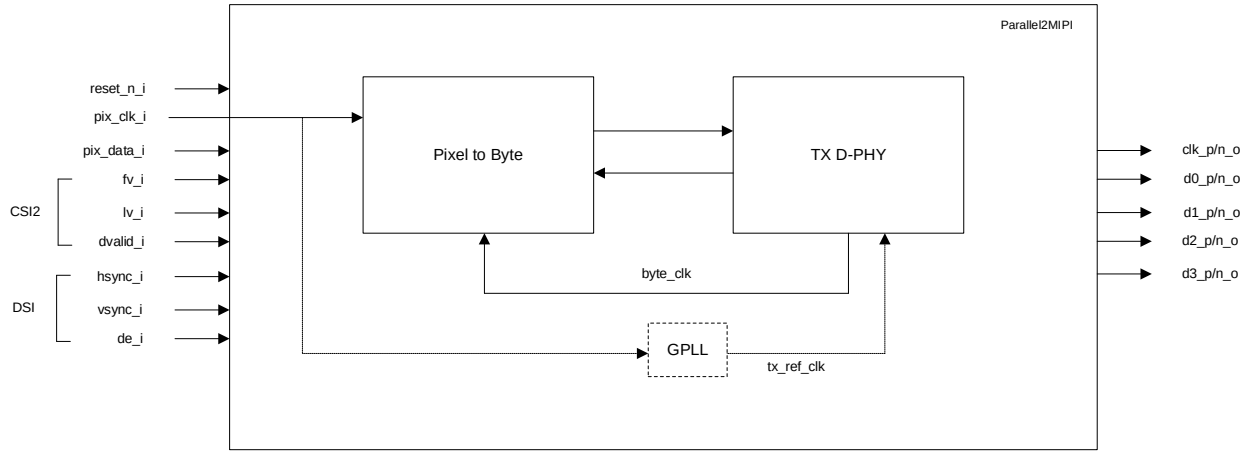

Figure 1.1. Parallel to MIPI Reference Design Block Diagram

Figure 1.1 shows the block level diagram of the Parallel to MIPI reference design mainly consists of the Pixel to Byte and TX D-PHY IPs. Since TX D-PHY PLL has an input clock frequency requirement of between 24 MHz and 200 MHz, another on-chip GPLL may have to be used to create an appropriate clock.

1.4. Functional Description

The Parallel to MIPI D-PHY Reference Design converts a standard parallel video interface into either DSI or CSI-2 byte packets. The input interface for the design consists of a pixel bus (RGB888, RGB666), vertical and horizontal sync flags, a data enable and a clock for DSI and pixel bus (RGB888, RAW8, RAW10, RAW12, and RAW14), frame and line valid flags and a clock for CSI-2.

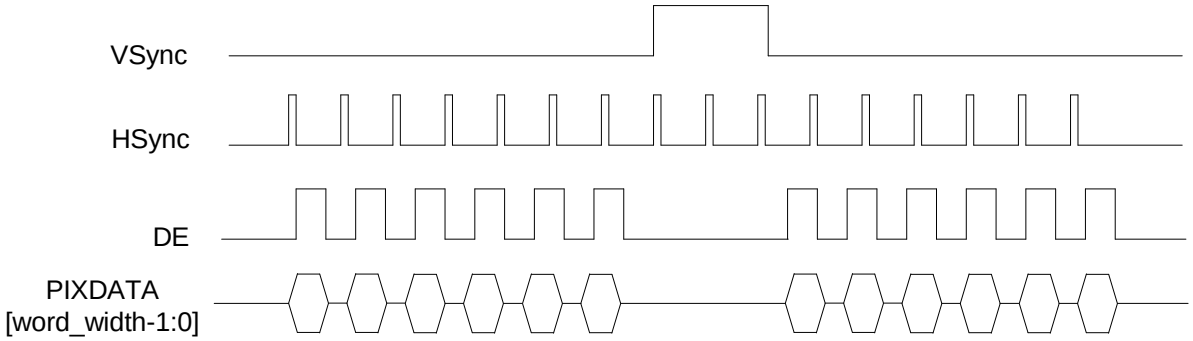

Figure 1.2. Display Parallel Input Bus Waveform

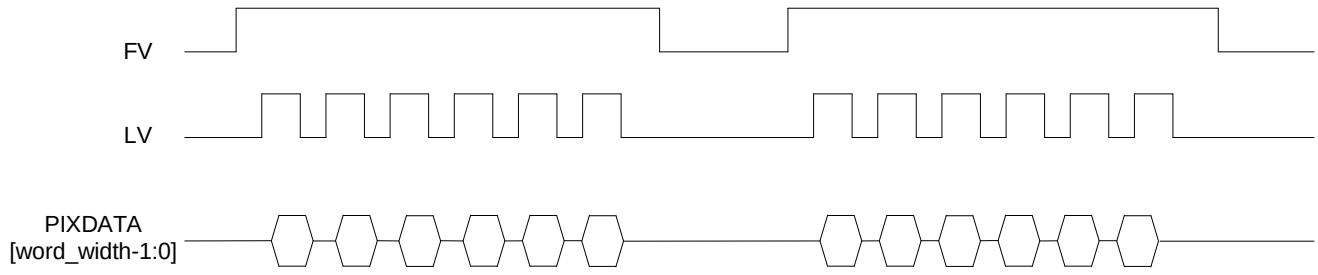

Figure 1.3. Camera Sensor Parallel Input Bus Waveform

This parallel bus in Figure 1.2 and Figure 1.3 is converted to the appropriate DSI or CSI-2 output format. The DSI/CSI-2 output serializes HS (High Speed) data and controls LP (Low Power) data and transfers them through MIPI D-PHY IP. MIPI D-PHY also has a maximum of five lanes per channel. It consists of one clock lane and up to four data lanes. The maximum Soft D-PHY data rate is 1.5 Gbp/s per lane (depending on the package). Refer to CertusPro-NX Family Datasheet (FPGA-DS-02086).

1.5. Conventions

1.5.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL. This includes radix indications and logical operators.

1.5.2. Data Ordering and Data Types

The highest bit within a data bus is the most significant bit. 8-bit parallel data is serialized to 1-bit data stream on each MIPI D-PHY data lane where bit 0 is the first transmitted bit.

Table 1.1 lists pixel data order coming from core module.

Table 1.1. Pixel Data Order

Data Type	Format
RGB	{Red[MSB:0], Green[MSB:0], Blue[MSB:0]}
RAW	RAW[MSB:0]

1.5.3. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
  Some signals are declared as bidirectional (I/O) but are only used as input. Hence, _*i* identifier is used.
- _*o* are output signals
  Some signals are declared as bidirectional (I/O) but are only used as output. Hence, _*o* identifier is used.
- _io are bidirectional signals

2. Parameters and Port List

There are two directive files for this reference design:

- synthesis_directives.v – used for design compilation by Lattice Radiant software and for simulation.
- simulation_directives.v – used for simulation.

The user can modify these directives according to user's own configuration. The settings in these files must match Pixel to Byte and TX D-PHY IP settings created by Lattice Radiant.

2.1. Synthesis Directives

Table 2.1 shows the synthesis directives that affect this reference design. These are used for both synthesis and simulation. Some parameter selections are restricted by other parameter settings as shown in Table 2.1 and Table 2.2.

Table 2.1. Synthesis Directives

Category	Directive	Remarks
D-PHY Type	TX_DSI	Only one of these two directives must be defined. Used for DSI or CSI-2 transmission.
	TX_CSI2	
Video Data Type	RGB888	Only one of these six directives must be defined. Type of video data to convert from pixel format to byte format for Pixel to Byte converter.
	RGB666	
	RAW8	
	RAW10	
	RAW12	
	RAW14	
Number of TX Lane	NUM_TX_LANE_1	Only one of these directives must be selected
	NUM_TX_LANE_2	
	NUM_TX_LANE_4	
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_1	Only one of these four directives must be defined. Number of pixels per pixel clock is used for the input to the Pixel to Byte converter.
	NUM_PIX_LANE_2	
	NUM_PIX_LANE_4	
	NUM_PIX_LANE_6	
TX D-PHY Clock Gear	TX_GEAR_8	TX D-PHY Clock Gear.
Miscellaneous	MISC_ON	Enables internal signals monitored by test-bench. Only one of these two directives must be defined.
	MISC_OFF	
Number of Pixels	NUM_PIXELS {value}	Number of active Pixels per Line
Clock Mode[1]	CLK_MODE_HS_ONLY	TX D-PHY Clock mode. Only one of these two directives must be defined.
	CLK_MODE_HS_LP	

Note:

1. HS_LP mode means *non-continuous clock mode* and HS_ONLY means *continuous clock mode* for the TX D-PHY.

2.2. Simulation Directives

Table 2.2 shows the simulation directives for this reference design.

Table 2.2. Simulation Directives

Category	Directive	Remarks
Pixel clock period	PIX_CLK {value}	Pixel clock period in ns
Number of video frames	NUM_FRAMES {value}	Number of video frames to be transmitted
Number of lines per frame	NUM_LINES {value}	Number of active lines per frame
Horizontal Front Porch	HFRONT {value}	Number of blanking cycles before HSYNC signal is asserted
Number of cycles HSYNC signal asserted	HPULSE {value}	Number of cycles for which HSYNC signal is asserted
Horizontal Back Porch	HBACK {value}	Number of blanking cycles after HSYNC signal is de-asserted
Vertical Front Porch	VFRONT {value}	Number of blanking lines before VSYNC signal is asserted
Number of lines VSYNC signal asserted	VPULSE {value}	Number of lines for which VSYNC signal is asserted
Vertical Back Porch	VBACK {value}	Number of blanking lines after VSYNC signal is de-asserted

2.3. Top-Level I/O

Table 2.3 shows the top level I/O of this reference design. Actual I/O depends on the customer's configurations. All necessary I/O ports are automatically declared by compiler directives.

Table 2.3. Parallel to MIPI Top Level I/O

Port Name	Direction	Description
Clocks and Resets		
pix_clk_i	I	Input pixel/reference clock. Period of pixel clock is defined in simulation_directives.v
reset_n_i	I	Asynchronous active low system reset
DSI Input Interface		
vsync_i[1]	I	Input vertical sync for parallel interface
hsync_i[1]	I	Input horizontal sync for parallel interface
de_i[1]	I	Input data enable for parallel interface
CSI-2 Input Interface		
fv_i[2]	I	Input frame valid for parallel interface
lv_i[2]	I	Input line valid sync for parallel interface
dvalid_i[2]	I	Input data enable for parallel interface
Input Data		
pixdata_i	I	Input pixel data. Data Bus width depends on the data type selected and Number of pixels per clock. RGB888 : 24-bit bus width × Number of Pixel per clock RGB666[1] : 18-bit bus width × Number of Pixel per clock RAW14[2] : 14-bit bus width × Number of Pixel per clock RAW12[2] : 12-bit bus width × Number of Pixel per clock RAW10[2] : 10-bit bus width × Number of Pixel per clock RAW8[2] : 8-bit bus width × Number of Pixel per clock
Debug Interface		
pll_lock_o[3]	O	D-PHY PLL lock signal
TX Output Interface		
d_p_io[NUM_TX_LANE -1:0][4]	I/O	Positive differential TX D-PHY data lanes
d_n_io[NUM_TX_LANE -1:0][4]	I/O	Negative differential TX D-PHY data lanes

Port Name	Direction	Description
clk_p_io	I/O	Positive differential TX D-PHY clock lane
clk_n_io	I/O	Negative differential TX D-PHY clock lane

Notes:

1. Available only if data interface is DSI.
2. Available only if data interface is CSI-2.
3. Turned-on if Enable miscellaneous status signals attribute is selected.
4. NUM_TX_LANE = Number of TX D-PHY Lanes: 1, 2, 4 (available on user interface).

3. Design and Module Description

The top-level design (parallel2mipi_LFCPNX.v) consists of the following modules:

- p2b
- tx_dphy
- int_pll

The top-level design has external PLL support, which is used when USE_GPLL is defined in the synthesis_directives.v file.

Figure 3.1 shows the timing diagram for the D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface.

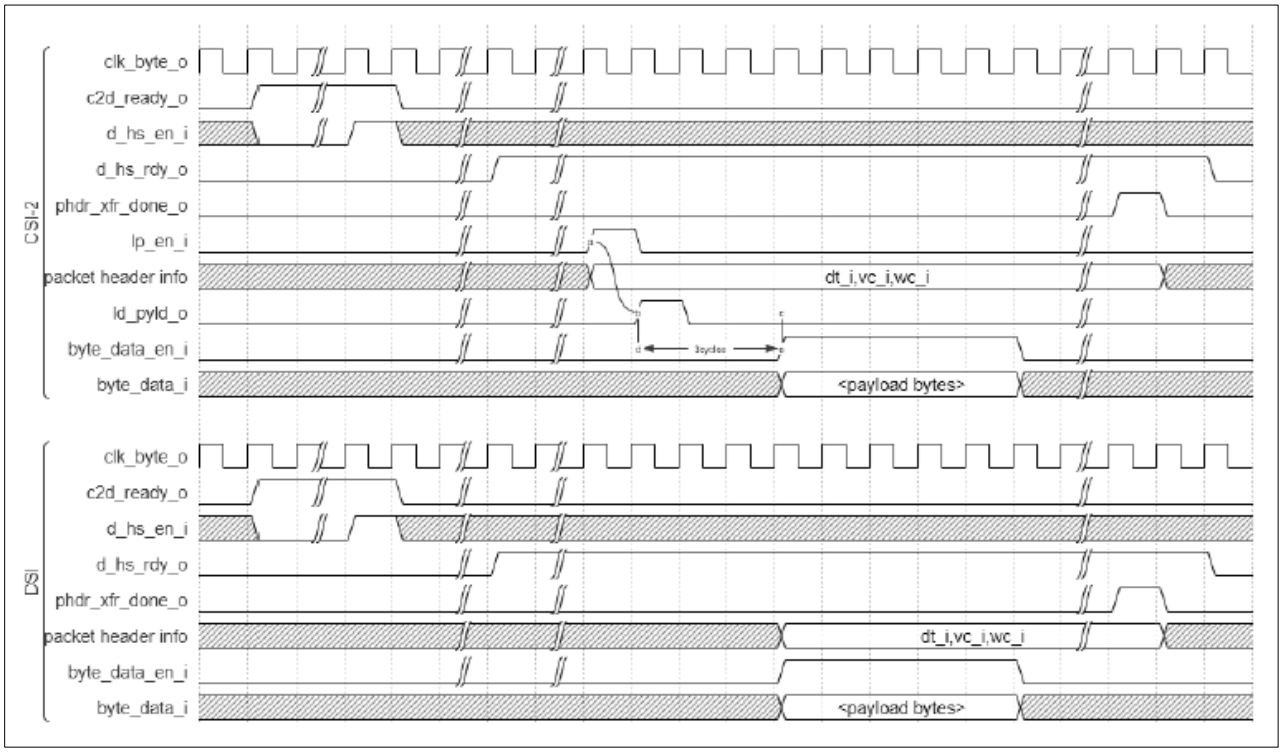

Figure 3.1. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface

When the protocol type selected is CSI-2, there is no internal buffer to save the incoming payload data before the creation of the header packet. Because of this, the D-PHY TX IP requires 3 cycles from the assertion of the ld_pyld_o to the arrival of the valid payload data. The ld_pyld_o asserts the next cycle after the detection of the lp_en_i. Hence little glue logic is added in the top-level design to take care of this timing requirement for the required signals for the D-PHY TX IP as shown in Figure 3.1.

3.1. p2b

This module must be created to convert Pixel data into Byte data output according to configurations, such as TX Interface, Data Type, number of TX Lanes, and others. Figure 3.2 shows an example of IP interface settings in Lattice Radiant for the Pixel to Byte Submodule IP. Refer to Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094) for details.

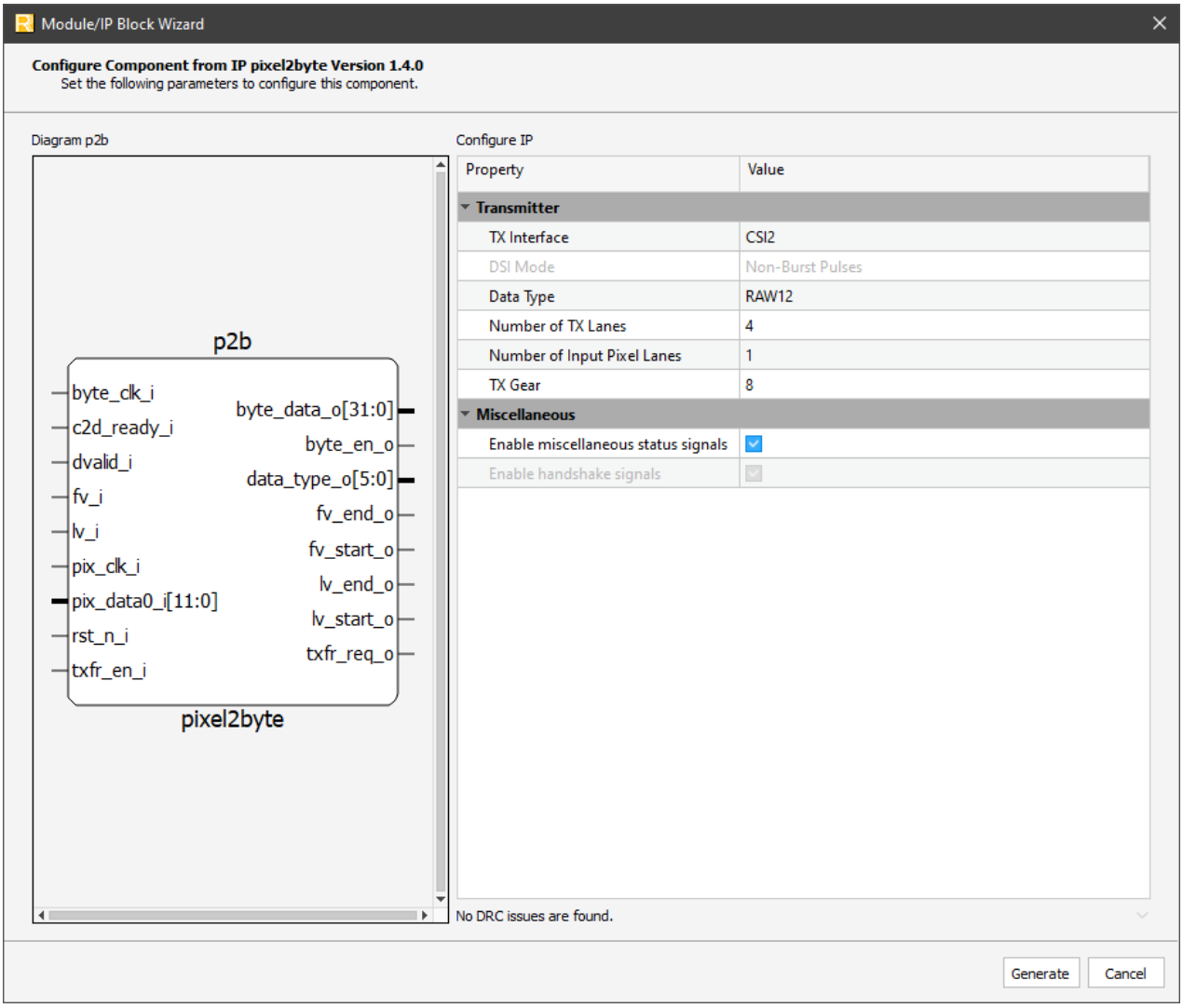

Figure 3.2. p2b IP Creation in Lattice Radiant

The following shows the guidelines and parameter settings required for this reference design:

- TX Interface – Select DSI or CSI-2. Set the same type as TX D-PHY IP.
- Data Type – Select RGB888 or RGB666 for DSI and RGB888, RAW8, RAW10, RAW12, or RAW14 for CSI-2. Others are not supported in this reference design.
- Number of TX Lanes – Select 1, 2, or 4. Set the same value as TX D-PHY IP.
- Number of Input Pixel Lanes – Select 1, 2, 4, and 6 for input Pixel per clock. Number of Input Pixel per Clock 6 is only supported for CSI-2, RAW10, and RAW12.
- TX Gear – Select 8. Only Gear 8 is supported in this reference design.
- Enable miscellaneous status signals – Select checkbox to enable (checked).

The Pixel-to-Byte Converter IP converts the standard pixel data format to the D-PHY CSI-2/DSI standard based byte data stream. The *.ipx* file included in the project (p2b/p2b.ipx) can be used to reconfigure the IP as per the user configuration requirements. If user creating this IP from scratch, it is recommended to set the design name to *p2b* so that user do not need to modify the instance name of this IP in the top-level design as well as in the simulation setup file. Otherwise, user need to modify the names accordingly.

3.2. tx_dphy

The user must create this module according to the channel conditions, such as number of lanes, bandwidth, and others. Figure 3.3 and Figure 3.4 show an example IP interface setting in Lattice Radiant for the CSI-2/DSI D-PHY Transmitter Submodule IP. Refer to CSI-2/DSI D-PHY Tx IP Core User Guide (FPGA-IPUG-02080) for details.

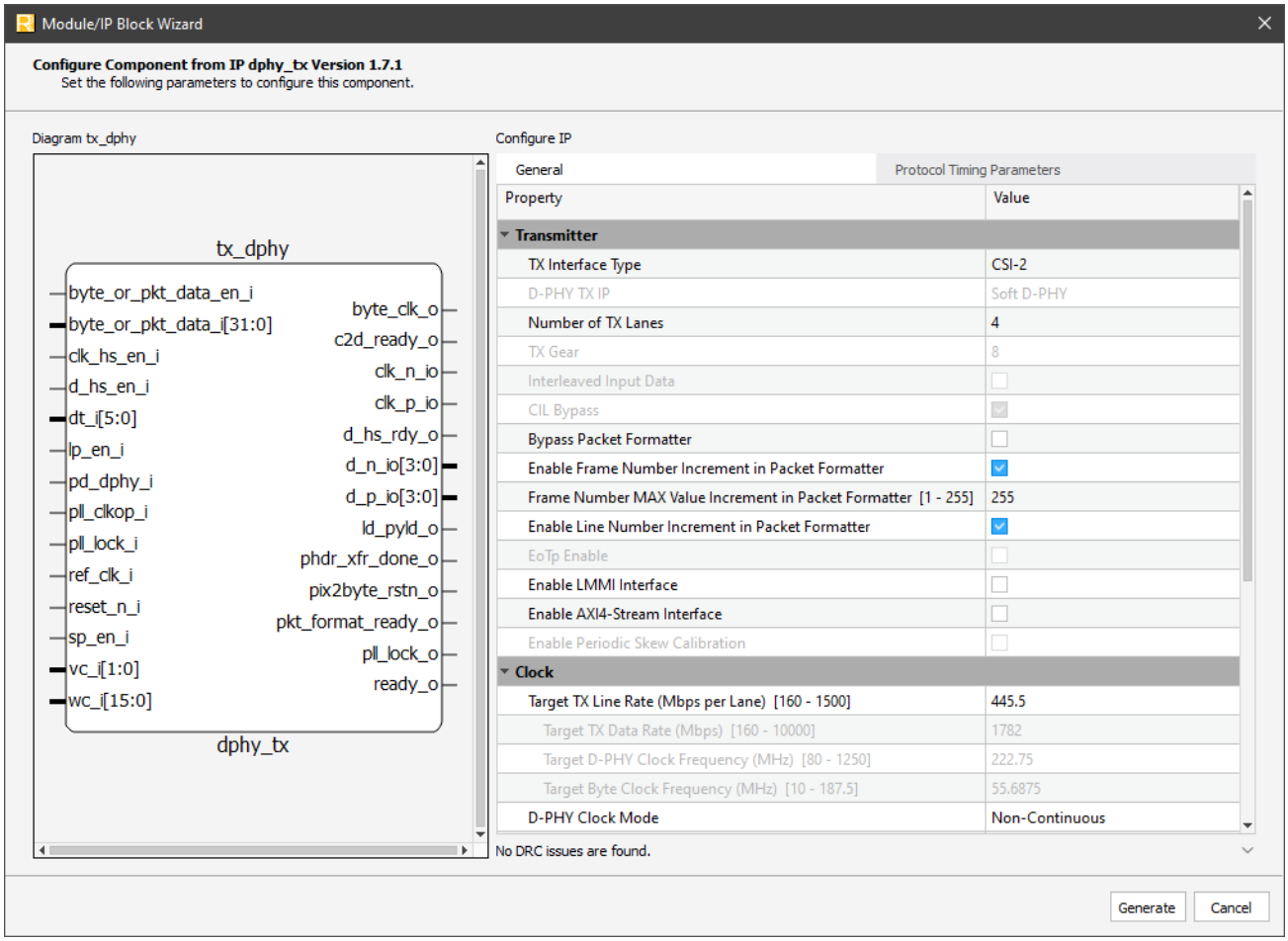

Figure 3.3. tx_dphy IP Creation in Lattice Radiant (1/2)

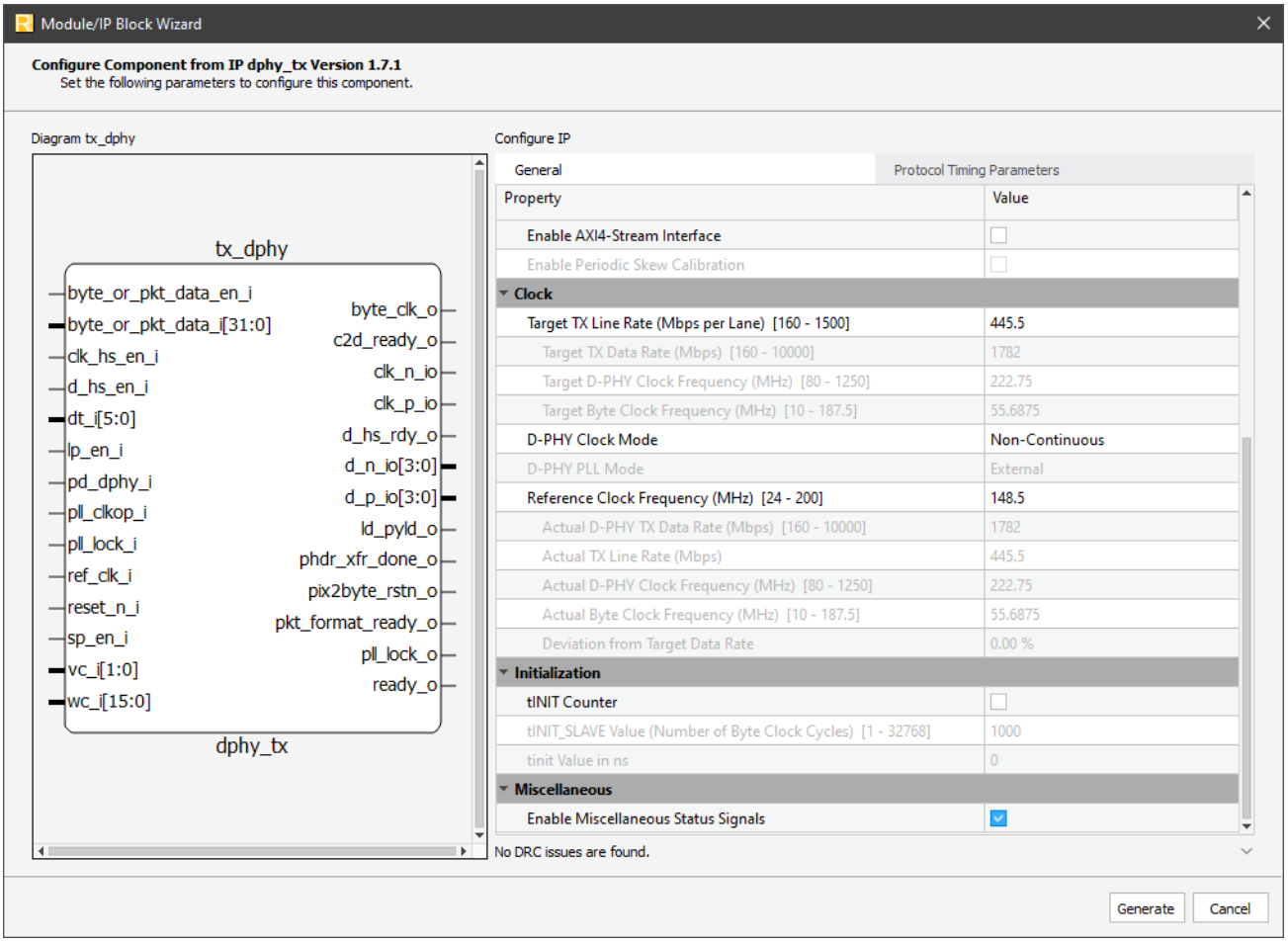

Figure 3.4. tx_dphy IP Creation in Lattice Radiant (2/2)

The following shows the guidelines and parameter settings required for this reference design:

- TX Interface Type – Select DSI or CSI-2 (set according to the required configuration).
- D-PHY TX IP – CertusPro-NX Supports only Soft DPHY type.
- Number of TX Lanes – Select 1, 2, or 4 (set according to the required configuration).
- TX Gear – Select 8. When the D-PHY TX IP is Soft D-PHY selected, then TX Gear is 8. TX Gear 8 is also automatically selected by Lattice Radiant when the lane bandwidth is less than 1500 Mbps, which means TX byte clock could be ~187.5 MHz.
- Interleaved Input Data – Select disabled (unchecked).
- CIL Bypass – Select checkbox to enable (checked).
- Bypass Packet Formatter – Select disabled (unchecked).
- Enable Frame Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2.
- Frame Number MAX Value Increment in Packet Formatter [1–255] – Numerical value between 1 to 255, only for CSI-2.
- Enable Line Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2.
- EoTp Enable – Select checkbox to enable (checked) EoTp insertion, only for DSI. This option is not mandatory.
- Enable LMMI Interface – Select disabled (unchecked).
- Enable AXI4-Stream Interface – Select disabled (unchecked).
- Enable Periodic Skew Calibration – Select disabled (unchecked).
- TX Line Rate per Lane (Mbps) [160–1500] (Soft D-PHY) – Set according to the required configuration.
- D-PHY Clock Mode – Set according to the required configuration.

- D-PHY PLL Mode – Select External for Soft D-PHY IP.
- Reference Clock Frequency (MHz) [24–200] – Set the same value as pixel clock frequency.
- tINIT Counter – Select disabled (unchecked).
- Enable Miscellaneous Status Signals – Select checkbox to enable (checked).
- Protocol Timing Parameters tab – Default values are recommended (Change timing values if required).

This module takes the byte data and outputs DSI/CSI-2 data after serialization in DSI/CSI-2 High Speed mode. The .ipx file included in the project (tx_dphy/tx_dphy.ipx) can be used to reconfigure the IP as per the user configuration requirements. If user creating this IP from scratch, it is recommended to set the design name to *tx_dphy* so that user do not need to modify the instance name of this IP in the top-level design as well as simulation setup file. Otherwise, user need to modify the names accordingly.

3.3. int_pll

This module generates the required clkop for TX D-PHY module when Soft D-PHY IP is used. Figure 3.5 shows an example IP interface setting in Lattice Radiant for the PLL Submodule IP. Refer to PLL Module User Guide (FPGA-IPUG-02063) for details.

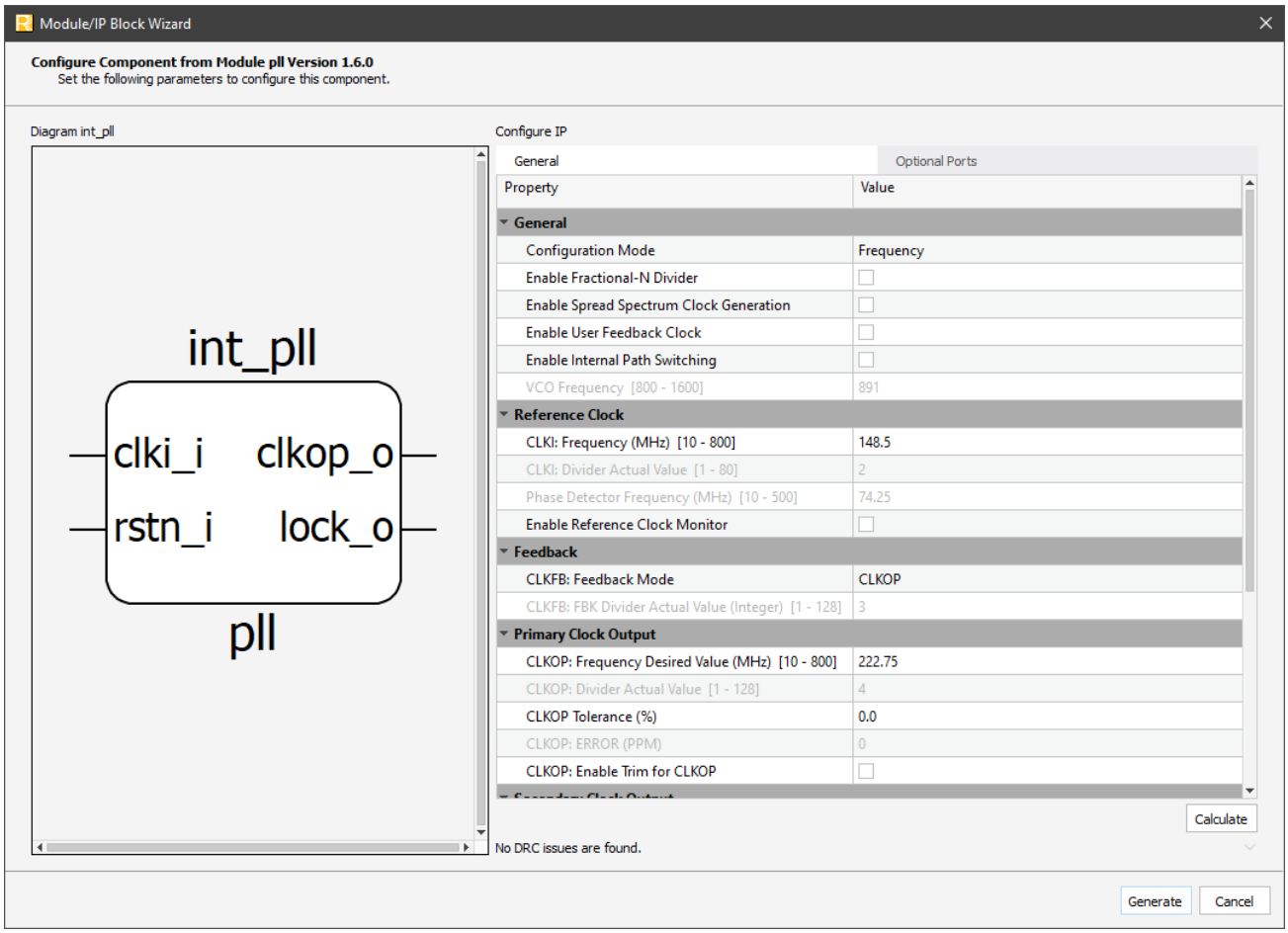

Figure 3.5. int_pll IP Creation in Lattice Radiant

The user need to modify the reference clock frequency and the clkop frequency as per the required configuration. For Soft D-PHY TX IP, clkop frequency is half of the TX Line Rate per Lane. The design also requires the external PLL to be used. The .ipx file included in the project (int_pll/int_pll.ipx) can be used to reconfigure the IP as per the user configuration requirements. If user creating this IP from scratch, it is recommended to set the design name to int_pll so that user do not need to modify the instance names of these IPs in the top-level design file. Otherwise, user need to modify the name accordingly.

4. Design and File Modifications

This reference design is based on version 1.4.0 of the Pixel2Byte IP and version 1.7.2 of the TX D-PHY IP. Some modifications are required depending on user configuration in addition to two directive files (synthesis_directives.v and simulation_directives.v).

5. Design Simulation

The script file (parallel_to_mipi_LFCPNX_msim.do) and testbench files are provided to run the functional simulation by Modelsim. If user follow the naming recommendations regarding design name and instance name when the Pixel2Byte and TX D-PHY IPs are created by Lattice Radiant, the following are the only changes required in the script file:

- User project directory

```
### Set Customer's project/simulation directory ###
set radiant_dir C:/lscc/radiant/3.1
set project_dir C:/Users/gquiriad/Documents/User_Guide/Done/Parallel_to_MIPI_CertusPro_NX/FPGA-RD-02239/FPGA-RD-02239
set sim_dir     $project_dir/simulation/lifcl/
```

Own Project Directory

Figure 5.1. Script Modification #1

```
set num_frames 3
set num_lines  3

cd $sim_dir

if {![file exists work]} {
    vlib work
}

transcript file "$sim_dir/simulation.log"

### Compiling modules ###
vlog \
+incdir+"$project_dir/int_pll/rtl/" \
+incdir+"$project_dir/p2b/rtl/" \
+incdir+"$project_dir/tx_dphy/rtl/" \
+incdir+"$project_dir/source/verilog/lfcpnx/" \
+incdir+"$project_dir/testbench/verilog/tb_include/" \
+incdir+"$project_dir/testbench/verilog/" \
$project_dir/source/verilog/lfcpnx/synthesis_directives.v \
$project_dir/testbench/verilog/simulation_directives.v \
$project_dir/int_pll/rtl/int_pll.v \
$project_dir/p2b/rtl/p2b.v \
$project_dir/tx_dphy/rtl/tx_dphy.v \
$project_dir/source/verilog/lfcpnx/parallel2mipi_LFCPNX.v \
$project_dir/testbench/verilog/vid_timing_gen_driver.v \
$project_dir/testbench/verilog/dphy_checker.v \
$project_dir/testbench/verilog/parallel2mipi_LFCPNX_tb.v \
+define+NUM_FRAMES=$num_frames+NUM_LINES=$num_lines \

vsim -voptargs=+acc=ap work.parallel2mipi_LFCPNX_tb -L pmi_work -L ovi_lfcpnx -c -do
"add wave -r parallel2mipi_LFCPNX_tb/* ;run -all; quit" -t fs -suppress 3085
```

Figure 5.2. Script Modification #2

The user need to modify simulation_directives.v according to the configuration (refer to the Simulation Directives section for details). By executing the script in Modelsim, compilation and simulation are executed automatically.

The testbench parallel2mipi_LFCPNX_tb.v instantiates the top level design module, generates the stimulus video data and does the data comparison between the expected data and output data from the RD, including Frame Number, EoT Packet check, CRC check, EoTp (Long Packet and Short Packet), ECC, and timing parameters of TX D-PHY. It shows the following statements while running the simulation.

```
#                    0   ============================
#                    0   D-PHY Type     = CSI2
#                    0   Data Type      = RAW12
#                    0   No of TX LANE = 4
#                    0   No of PIX/CLK = 1
#                    0   TX Gear        = 8
#                    0   Clock Mode     = HS_LP
#                    0   D-PHY_IP       = LATTICE
#                    0   ============================
#                    0   TEST START
#                    0   Num of Frames          : 3
#                    0   Num of Lines per Frame : 3
#                    0   ============================
#                  438   test_hsync_front_porch : 480
#                  438   test_hsync_width       : 288
#                  438   test_hsync_back_porch  : 672
#                  438   test_h_width           : 1920
#                  438   test_v_height          : 3
#                  438   test_vsync_front_porch : 1
#                  438   test_vsync_width       : 3
#                  438   test_vsync_back_porch  : 36
#                  438   test_number_of_bytes   : 2880
#
#                814979   FRAME #1 START
#                856989   LINE #1 Transmitted
#                879615   LINE #2 Transmitted
#                902242   LINE #3 Transmitted
#                928110   FRAME #1 END
#
#
#                995989   FRAME #2 START
#               1829917   LINE #1 Transmitted
#               1852544   LINE #2 Transmitted
#               1875170   LINE #3 Transmitted
#               1901039   FRAME #2 END
#
#
#               1968917   FRAME #3 START
#               2802846   LINE #1 Transmitted
#               2825472   LINE #2 Transmitted
#               2848098   LINE #3 Transmitted
#               2873967   FRAME #3 END
```

When the simulation is finished, the following statements are displayed:

```
2941841      TEST DONE for CSI2 :: DATA_TYPE is RAW12
#              2941941   ------------------------------------------
#              2941941   ##### DATA COMPARING IS STARTED #####
#              2941941   ------------------------------------------
#              2941941   ***PASS : EOT PACKET CHECK***
#              2941941   ***PASS : SYNC CHECK
#              2941941   ***PASS : ECC
#              2941941   ***PASS : FRAME NO
#              2941941   ***PASS : TIMING PARAMETERS***
#              2941941   ***PASS : CRC***
#              2941941   Test fail count : 0
#
#              2941941  ------------------------------------------------------
#              2941941  ----------------- SIMULATION PASSED ------------------
#              2941941  ------------------------------------------------------
#              2946941   TEST END
```

The test-bench generates other debug files during simulation like, *input_data.log*, *output_data.log* and *dphy_checker_timing.log* for debugging purpose. The *input_data.log* file stores the data transmitted by the test-bench. The *output_data.log* file stores the data received to the test-bench. The testbench compares both of these files. The *dphy_checker_timing.log* file stores all the timing parameters (such as LP-11, TLPX, HS-prepare, HS-0, and HS-Trail) and gives error if any timing parameter fails. The same file also saves timing of Header Packet received and Header Packet values like DT, VC, WC, and ECC.

Calculation for DSI – RGB888 :
1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Non-continuous Mode

Total Horizontal Samples **= 2200** Total Vertical Lines **= 1125**	Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format
Pixel Clock Frequency PCF = 2200 x 1125 x 60 **= 148.5 MHz**	Input this frequency at reference clock in your int_pll & tx_dphy
Bandwidth (Total Data Rate) B = 148.5 MHz x 24-bit **= 3.564 Gbps**	RGB888 uses 24 bits.
Line Rate (Data Rate per Lane) LR = 3.564 Gbps/4-lane **= 891 Mbps**	Input this tx line rate at tx_dphy. Maximum TX bandwidth is 1.5 Gbps/lane using D-PHY Soft IP. Only Soft D-PHY in CertusPro-NX.
MIPI Bit Clock Frequency MBCF = 891/2 **= 445.5 MHz**	Input this frequency at primary clock output in your int_pll.

For DSI Simulation, Eotp enable (tx_dphy) is needed to be enabled.

Figure 5.3. Calculation for DSI: RGB888

Figure 5.4 shows the simulation waveform of the full view of three lines and three frames for the DSI interface. Figure 5.6 shows the zoom view of the simulation waveform shown in Figure 5.4 for DSI interface. The waveform shows all the top-level I/O and few other signals.

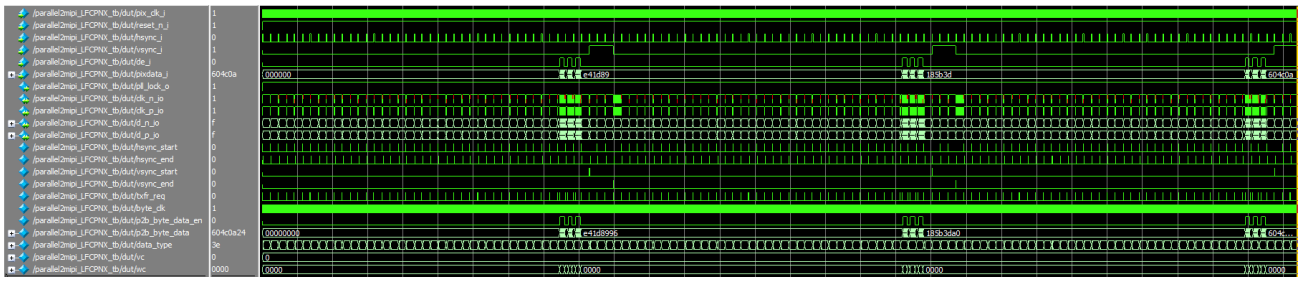

Figure 5.4. Simulation Waveform for DSI: RGB888

Calculation for DSI – RGB666 :
1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Non-continuous Mode

Total Horizontal Samples **= 2200** Total Vertical Lines **= 1125**	Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format
Pixel Clock Frequency PCF = 2200 x 1125 x 60 **= 148.5 MHz**	Input this frequency at reference clock in your int_pll & tx_dphy
Bandwidth (Total Data Rate) B = 148.5 MHz x 18-bit **= 2.673 Gbps**	RGB666 uses 18 bits.
Line Rate (Data Rate per Lane) LR = 2.673 Gbps/4-lane **= 668.250 Mbps**	Input this tx line rate at tx_dphy. Maximum TX bandwidth is 1.5 Gbps/lane using D-PHY Soft IP. Only Soft D-PHY in CertusPro-NX.
MIPI Bit Clock Frequency MBCF = 668.250/2 **= 334.125 MHz**	Input this frequency at primary clock output in your int_pll.

For DSI Simulation, Eotp enable (tx_dphy) is needed to be enabled.

Figure 5.5. Calculation for DSI: RGB666

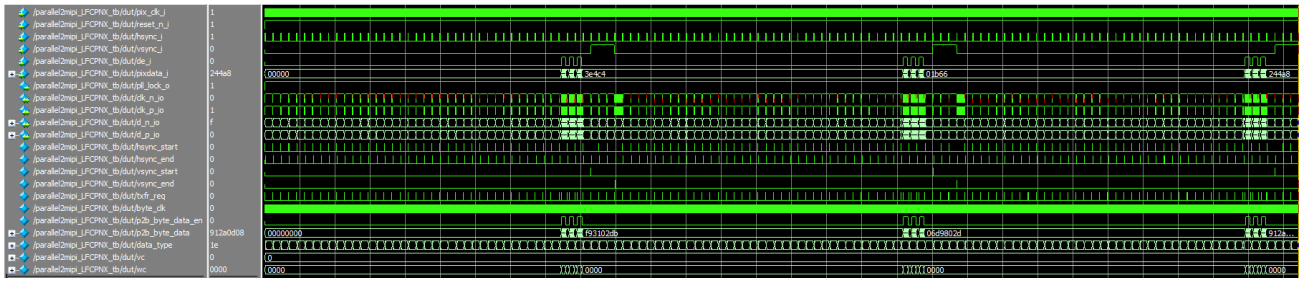

Figure 5.6. Simulation Waveform for DSI: RGB666

Figure 5.8 shows the simulation waveform of the full view of three lines and three frames for the CSI-2 RAW10 interface. Figure 5.10 shows the simulation waveform of the full view of three lines and three frames for the CSI-2 RAW12 interface. The waveform shows all the top level I/O and few other signals.

Calculation for CSI-2 : RAW10
1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Non-continuous Mode

Total Horizontal Samples = **2200** Total Vertical Lines = **1125**	Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format
Pixel Clock Frequency PCF = 2200 x 1125 x 60 = **148.5 MHz**	Input this frequency at reference clock in your int_pll & tx_dphy
Bandwidth (Total Data Rate) B = 148.5 MHz x 10-bit = **1.485 Gbps**	RAW10 uses 10 bits.
Line Rate (Data Rate per Lane) LR = 1.485 Gbps/4-lane = **371.25 Mbps**	Input this tx line rate at tx_dphy. Maximum TX bandwidth is 1.5 Gbps/lane using D-PHY Soft IP. Only Soft D-PHY in CertusPro-NX.
MIPI Bit Clock Frequency MBCF = 371.25/2 = **185.625 MHz**	Input this frequency at primary clock output in your int_pll.

For CSI-2 Simulation, configure the following parameters in tx_dphy.

Enable Frame Number Increment in Packet	Enabled
Frame Number MAX Value Increment in Packet Formatter	255
Enable Line Number Increment in Packet Formatter	Enabled

Figure 5.7. Calculation for CSI-2: RAW10

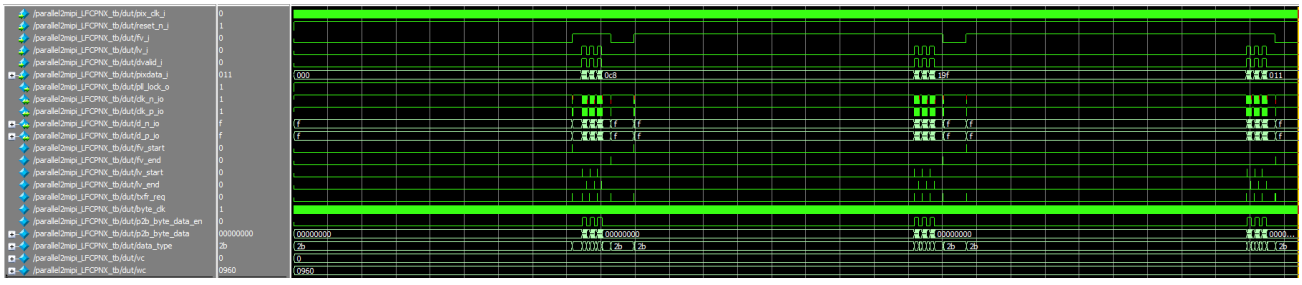

Figure 5.8. Simulation Waveform for CSI-2: RAW10

Calculation for CSI-2 : RAW12
1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Non-continuous Mode

Total Horizontal Samples **= 2200** Total Vertical Lines **= 1125**	Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format
Pixel Clock Frequency PCF = 2200 x 1125 x 60 **= 148.5 MHz**	Input this frequency at reference clock in your int_pll & tx_dphy
Bandwidth (Total Data Rate) B = 148.5 MHz x 12-bit **= 1.782 Gbps**	RAW12 uses 12 bits.
Line Rate (Data Rate per Lane) LR = 1.782 Gbps/4-lane **= 445.5 Mbps**	Input this tx line rate at tx_dphy. Maximum TX bandwidth is 1.5 Gbps/lane using D-PHY Soft IP. Only Soft D-PHY in CertusPro-NX.
MIPI Bit Clock Frequency MBCF = 455.5/2 **= 222.750 MHz**	Input this frequency at primary clock output in your int_pll.

For CSI-2 Simulation, configure the following parameters in tx_dphy.

Enable Frame Number Increment in Packet	Enabled
Frame Number MAX Value Increment in Packet Formatter	255
Enable Line Number Increment in Packet Formatter	Enabled

Figure 5.9. Calculation for CSI-2: RAW12

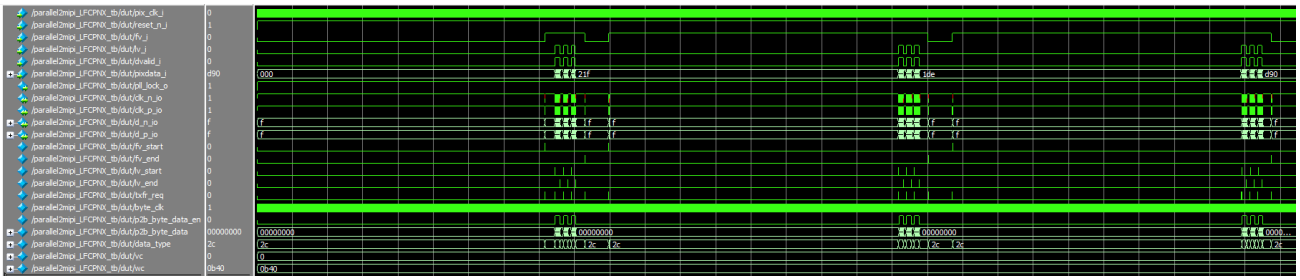

Figure 5.10. Simulation Waveform for CSI-2: RAW12

The simulation waveform can be accessed by opening the vsim.wlf file in the Modelsim from the simulation directory. More signals of a module can be added to the waveform as required.

6. Known Limitations

The following are the limitations of this reference design:

- Only following data types are supported for MIPI DSI interface: RGB888, RGB666
- Only following data types are supported for MIPI CSI-2 interface: RGB888, RAW8, RAW10, RAW12, and RAW14

7. Design Package and Project Setup

The Parallel to MIPI with CertusPro-NX Reference Design is available on www.latticesemi.com. Figure 7.1 shows the directory structure. The design is targeted for LFCPNX-100-7LFG672I. synthesis_directives.v and simulation_directives.v are set to configure the design with following configuration:

- RX – CSI-2, RAW12 parallel data with 1 pixel/clock
- TX – 4-lanes, Gear 8 with Soft D-PHY in non-continuous clock mode

The user can modify the directives for user's own configuration.

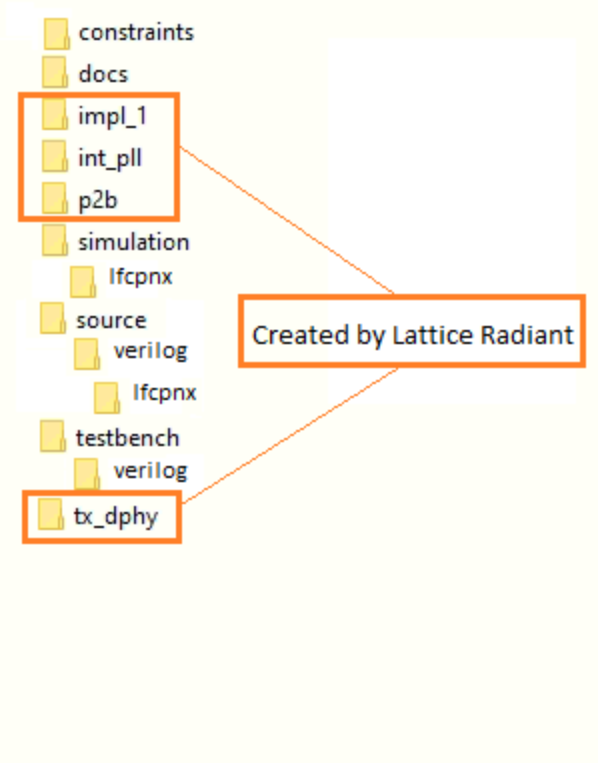

Figure 7.1. Directory Structure

Figure 7.2 shows the design files used in the Lattice Radiant project. Including PLL, Lattice Radiant creates three .ipx files. By specifying parallel2mipi_LFCPNX as a top-level design, all unnecessary files are ignored. Constraint file (parallel_to_mipi_LFCPNX.pdc) is also included in the project for reference. The user can modify it according to user's own configuration.

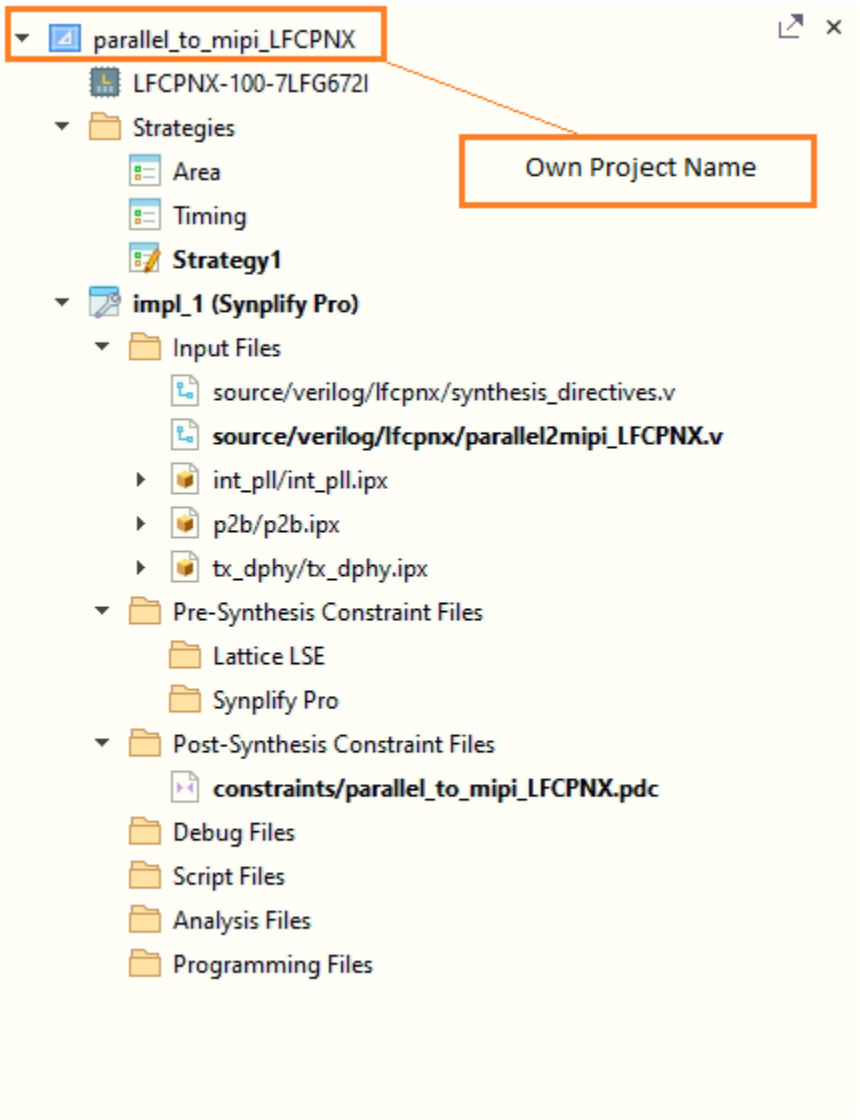

Figure 7.2. Project Files

8. Resource Utilization

Resource utilization depends on the configuration used. Table 8.1 shows the resource utilization examples under certain configurations targeting LFCPNX-100. This is just a reference and actual usage varies.

Table 8.1. Resource Utilization Examples

Configuration	LUT (Utilization/Total)	FF (Utilization/Total)	EBR (Utilization/Total)	I/O (Utilization/Total)
2-lane, Gear 8, Soft D-PHY, CSI-2, RAW14, 1 Pixels/clock	763/79872	602/80769	1/208	25/299
4-lane, Gear 8, Soft D-PHY, CSI-2, RAW12, 6 Pixels/clock	1109/79872	754/80769	4/208	88/299
4-lane, Gear 8, Soft D-PHY, DSI, RGB888, 2 Pixels/clock	803/79872	857/80769	3/208	64/299
4-lane, Gear 8, Soft D-PHY, DSI, RGB666, 2 Pixels/clock	929/79872	829/80769	2/208	52/299

References

- MIPI Alliance Specification for D-PHY Version 1.2
- MIPI Alliance Specification for Display Serial Interface 2 (DSI) Version 1.2
- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) Version 1.2
- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) Version 2.0
- Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094)
- CSI-2/DSI D-PHY Tx IP Core User Guide (FPGA-IPUG-02080)
- PLL Module User Guide (FPGA-IPUG-02063)
- MIPI D-PHY Bandwidth Matrix and Implementation (FPGA-TN-02090)

For more information on the CertusPro-NX FPGA device, visit https://www.latticesemi.com/Products/FPGAandCPLD/CertusPro-NX.

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow, Tasks, and Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.2, May 2023

Section	Change Summary
References	Added reference to the MIPI D-PHY Bandwidth Matrix and Implementation technical note.
All	Minor adjustments in format and style.

Revision 1.1, February 2023

Section	Change Summary
Introduction	Updated the document title from “Parallel to MIPI with CertusPro-NX” to “Parallel to MIPI CSI-2 and DSI with CertusPro-NX”.
Introduction	Updated Supported Device and IP section for below changes: • Changed Pixel-to-Byte Converter IP version from 1.3.0 to 1.4.0. • Changed D-PHY Transmitter IP version from *1.2.0* to *1.7.2.* • Changed Radiant software version from 3.1 to 2022.1.
Design and Module Description	Updated the figures below: • Figure 3.2. p2b IP Creation in Lattice Radiant • Figure 3.3. tx_dphy IP Creation in Lattice Radiant (1/2) • Figure 3.4. tx_dphy IP Creation in Lattice Radiant (2/2) • Figure 3.5. int_pll IP Creation in Lattice Radiant
Design and File Modifications	Changed Pixel2Byte IP version from *1.3.0* to *1.4.0* and TX D-PHY IP version from *1.2.0* to *1.7.2.*

Design Simulation	• Updated the figures below:
	  • Figure 5.1. Script Modification #1
	  • Figure 5.2. Script Modification #2
	  • Figure 5.4. Simulation Waveform for DSI: RGB888
	  • Figure 5.6. Simulation Waveform for DSI: RGB666
	  • Figure 5.8. Simulation Waveform for CSI-2: RAW10
	  • Figure 5.10. Simulation Waveform for CSI-2: RAW12
	• Added the figures below:
	  • Figure 5.3. Calculation for DSI: RGB888
	  • Figure 5.5. Calculation for DSI: RGB666
	  • Figure 5.7. Calculation for CSI-2: RAW10
	  • Figure 5.9. Calculation for CSI-2: RAW12

Technical Support Assistance	Added FAQ website link in Technical Support Assistance section.

Revision 1.0, September 2021

Section	Change Summary
All	Initial release.

www.latticesemi.com