CertusPro-NX Hardware Checklist

Technical Note

FPGA-TN-02255-1.7

October 2025

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ADC	Analog-to-Digital Converter
BGA	Ball Grid Array
CML	Current-Mode Logic
FB	Ferrite Bead
FPGA	Field-Programmable Gate Array
GND	Ground
HCSL	High-Speed Current Steering Logic
HPIO	High-Performance I/O
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
JTAG	Joint Test Action Group
LPDDR2/3/4	Low-Power Double Data Rate (2/3/4)
LVDS	Low-Voltage Differential Signaling
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LUT	Look Up Table
LVSTL	Low-Voltage Stub Series Terminated Logic
MCLK	Master Clock
MDx	Mode Data
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSPI	Master Serial Peripheral Interface
PLL	Phase-Locked Loop
PCLK	Primary Clock
SCL	Serial Clock Line
SCSN	Slave Chip Select Not
SDx	SERDES Data Channel
SERDES	Serializer/Deserializer
SI/SO	Serial In/Serial Out
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SSPI	Secondary Serial Peripheral Interface
SSTL	Stub Series Terminated Logic
sysCLOCK	System Clock
sysCONFIG	System Configuration
sysDSP	System Digital Signal Processing
sysI/O	System Input/Output
WRIO	Wide-Range I/O

1. Introduction

When designing complex hardware using the CertusPro™-NX device, you must pay close attention to critical hardware configuration requirements. This technical note outlines these critical hardware implementation items specific to the CertusPro-NX device. It does not provide detailed step-by-step instructions but offers a high-level checklist to support the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that you are familiar with the CertusPro-NX device features as described in CertusPro-NX Family Data Sheet (FPGA-DS-02086). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to CertusPro-NX Family Data Sheet (FPGA-DS-02086) for details. The critical hardware areas covered in this technical note are:

- Power supplies, as they relate to the CertusPro-NX power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Thermal Management (FPGA-TN-02044)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SERDES Jitter (TN1084)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- Related pinout information can be found on the CertusPro-NX web page.
- ADC User Guide for Nexus Platform (FPGA-TN-02129)

2. Power Supplies

The V_{CC}, V_{CCAUXA}, and V_{CCIOX} power supplies are monitored to determine the CertusPro-NX internal Power Good condition during power-up. These supplies must reach valid and stable levels before the device becomes operational. All other supplies are not monitored during power-up, but must also be at valid and stable levels before device configuration is complete, and the device enters user mode.

Several other supplies are used in conjunction with onboard SERDES blocks and ADCs on CertusPro-NX devices.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Single-Ended I/O Standards

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCECLK}	1.0 V	FPGA core clock power supply. Required for Power Good condition.
V_{CCAUX}	1.8 V	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. Used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	1.8 V	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. Used for generating stable current for the differential input comparators and stable drive current for the I/O.
V_{CCAUXA}	1.8 V	Auxiliary supply voltage for internal analog circuitry. Required for Power Good condition.
$V_{CCIO[7:0]}$	Banks 0, 1, 2, 6, 7: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	Bank I/O driver supply voltage. Each bank has its own V_{CCIO} supply: V_{CCIO0} and V_{CCIO1} are used in conjunction with pins dedicated and shared with device configuration, and are required to reach a proper level for Power Good condition.
$V_{CCADC18}$	1.8 V	ADC block power supply. Should be isolated from excessive noise.
ADC_REFP[1:0]	1.0 V to 1.8 V Typical	ADC external reference. Should be isolated from excessive noise and have high accuracy (< 0.1%).
V_{CCSDx}	1.0 V	SERDES block core power supply voltage. Should be isolated from excessive noise.
V_{CCSDCK}	1.0 V	SERDES block clock buffer supply voltage. Should be isolated from excessive noise.
$V_{CCPLLSDx}$	1.8 V	SERDES block PLL power supply voltage. Should be isolated from excessive noise.
$V_{CCAUXSDQx}$	1.8 V	SERDES block auxiliary power supply voltage. Should be isolated from excessive noise.

The CertusPro-NX FPGA device has a power-on-reset state machine that depends on several of the power supplies.

These supplies must rise monotonically. Initialization of the device does not proceed until all monitored power supplies have reached their minimum operating voltages.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator's feedback pin, which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR × expected current draw
- Expected voltage drops due to current measuring resistor's ESR × expected current draw

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is particularly sensitive to noise, as every 10 mV represents 1% of the rail voltage. For SERDES power rails, it is recommended to target a maximum 1% peak noise. For PLLs, they target less than 0.5% peak noise to minimize jitter.

3. CertusPro-NX SERDES and ADC Power Supplies

Providing a quiet, filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB-related crosstalk with sensitive blocks are related to FPGA outputs found in close proximity to the sensitive power supplies. These supplies require a cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCECLK}	10 µF x 2 + 100 nF per pin	Core and clock logic. Tie V_{CC} and V_{CCECLK} pins together. 1.0 V
V_{CCAUX}, $V_{CCAUXHx}$ (Single Ended)	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pins. Tie V_{CCAUX} and $V_{CCAUXHx}$ pins together for banks without high-speed differential pair I/O. 1.8 V
$V_{CCAUXHx}$ (Fast Differential)	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. Use separate FB + Capacitor filter for banks with high-speed differential I/O. 1.8 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for internal analog circuitry 1.8 V
$V_{CCIO[7:0]}$	10 µF + 100 nF per pin	Bank I/O. Unused banks can use a single 1.0 µF. For banks with lots of outputs or large capacitive loading replace the 10 µF with a 22 µF (or use two 10 µF). Banks 0, 1, 2, 6, 7 = 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4, 5 = 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.
$V_{CCADC18}$	220 Ω or 120 Ω FB + 10 µF + 100 nF per pin	ADC Block. If ADC block is not used, leave it open. 1.8 V
ADC_REFP[1:0]	220 Ω or 120 Ω FB + 1.0 µF + 100 nF per pin	ADC Block External Reference. Must have very low noise and high accuracy (< 0.1%). Voltage source/regulator should be filtered by 220 Ω or 120 Ω FB + 1 µF If ADC block is not used, connect to board ground. 1.0 V to 1.8 V Typical
V_{CCSDx}	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Core. If SERDES block is not used, leave it open. 1.0 V
V_{CCSDCK}	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Clock buffer. If both SERDES blocks are not used, leave open. 1.0 V

Power Input	Recommended Filter	Notes
$V_{CCPLLSDx}$	220 Ω FB + 47 µF + 470 nF per pin IMPORTANT: Connect capacitor grounds only to FPGA pin SDx_REFRET	SERDES Block PLL. If SERDES block is not used, leave it open. Route bypass capacitor grounds only to SDx_REFRET 1.8 V
$V_{CCAUXSDQx}$	120 Ω FB + (10 µF and 100 nF to each channel's SDx_REFRET)	SERDES Block Auxiliary. If SERDES block is not used, leave it open. Route bypass capacitor grounds only to SDx_REFRET 1.8 V

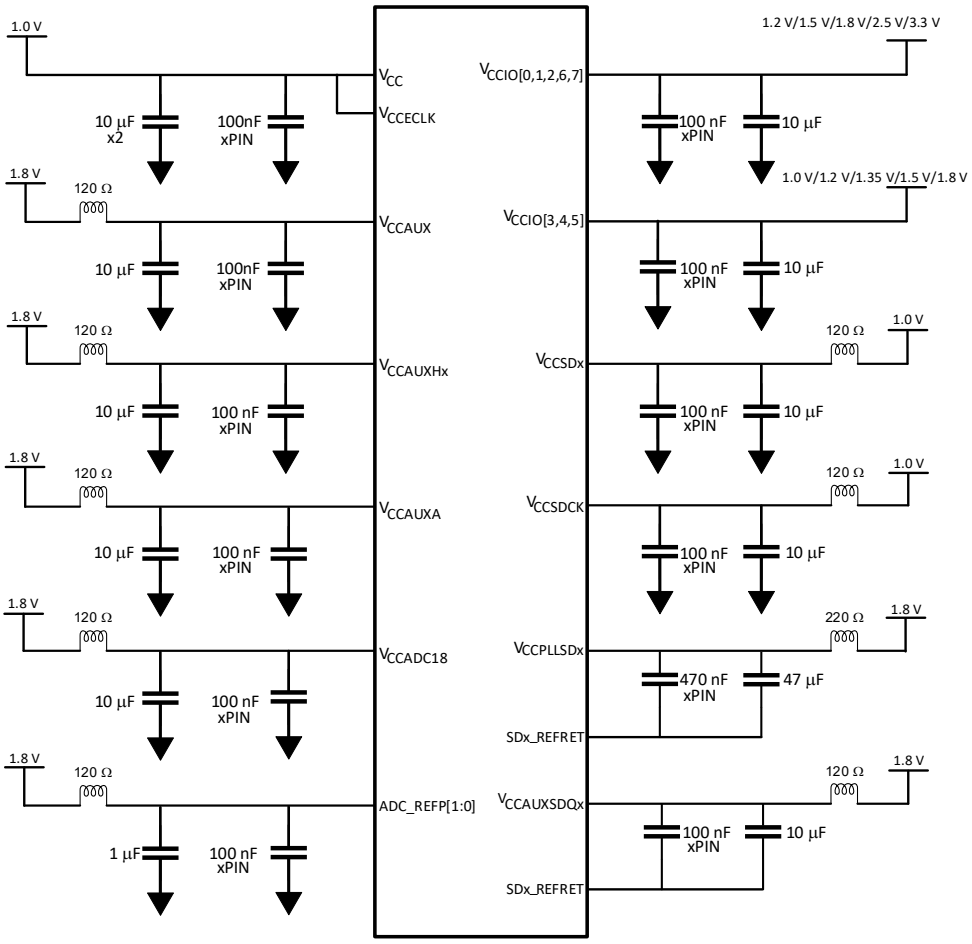

Figure 3.1. Recommended Power Filters

3.2. Ground Pins

- All ground pins need to be connected to the board ground plane.
- V_{SSSDx} and V_{SSADC} pins are sensitive to noise and should be isolated from fast switching high current pathways on the ground plane. Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.
- SDx_REFRET — Input SERDES Reference Return Input. This pin should be AC coupled (bypassed) to the $V_{CCPLLSDx}$ supply.

3.3. Unused Bank V_{CCIOx}

Connect unused V_{CCIO} pins to a power rail, do not leave them open.

3.4. Unused ADC Blocks

Connect V_{SSADC}, ADC_REFPx, ADC_DPx, and ADC_DNx pins to board ground. Leave $V_{CCADC18}$ unconnected.

3.5. Unused SERDES Quads

- Connect V_{SSSDQ}, and the Rx differential inputs: SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET, SDx_REXT to board ground.
- Leave $V_{CCAUXSDQx}$ [x=0,1], V_{CCSDx} [x= 0-7], $V_{CCPLLSDx}$ [x = 0-7], and Tx differential pair outputs open.
- If both SERDES Quads are not in use, leave V_{CCSDCK} open.

3.6. Unused SERDES Channels in a Quad

- Connect all V_{SSSDQ} pins to board ground.
- Channel 1 of the used quad must be supplied with filtered power, regardless of whether it is in use. Connect $V_{CCAUXSDQx}$ [x=0,1], V_{CCSDx} [x= 1,5], and $V_{CCPLLSDx}$ [x = 1,5] pins to filtered power rails.
- Connect to board ground the Rx differential inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET, and SDx_REXT.
- Leave V_{CCSDx} [x= 0-7], $V_{CCPLLSDx}$ [x = 0-7], and Tx differential pair outputs open.

3.7. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-end or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator are recommended.

When specifying components, choose good-quality ceramic capacitors in small packages and place them as close to the clock oscillator supply pins as possible. Good quality capacitors for bypassing generally meet the following requirements.

3.8. Ferrite Bead Selection Notes

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR × CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.025 Ω and 0.10 Ω depending on current load.
- PLL rails draw low current, which allows ferrite beads with an ESR ≤ 0.3 Ω.
- Small package size ferrite beads have a higher ESR than large package size ferrite beads of the same impedance.
- High impedance ferrite beads have a higher ESR than low impedance ferrite beads in the same package size.

3.9. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the power supply pins as possible. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.9.1. Dielectric

Use dielectrics such as X5R, X7R and similar dielectrics which have good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U and similarly poor capacitance-controlled dielectrics.

3.9.2. Voltage Rating

A capacitor's working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor's voltage rating should target at least 80% higher than the maximum voltage rail. For example, bypass capacitors for a 3.3 V rail should use the commonly available 6.3 V rating as a minimum.

3.9.3. Size

Smaller-body capacitors have lower inductance, operate at higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger-body capacitors. To balance market pricing with size-related inductance benefits, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0603
4.7 µF	0603	0402
10 µF	0603	0805
22 µF	0805	1206

4. Power Sequencing

There is no power-up sequence required for the CertusPro-NX device.

5. Power Estimation

Once the CertusPro-NX device density, package, and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant™ design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current and maximum DC and AC current for the given system environmental conditions.
- The ability for the system environment and CertusPro-NX device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, the CertusPro-NX device power requirements can be taken into consideration early in the design phase.

6. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024). WLCSP packages are similar to other BGA (ball grid array) packages with regard to the PCBs the packages are to be mounted on. For application-specific assembly guidance, consult the design guidelines of the assembly service provider.

The CertusPro-NX device includes provisions to configure the FPGA via the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 6.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI/SI	4.7 kΩ pull-up to V_{CCIO1}
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
TDO/SO	4.7 kΩ pull-up to V_{CCIO1}
TCK/SCLK	2.2 kΩ pull-down to GND

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with the corresponding V_{CCIO1} and ground.

External resistors are necessary for configuration signals when they are used to handshaking with other devices. However, external pull-resistors are not required on individual configuration pins if the signal pin is not persisted Recommended pull-up resistors to the appropriate bank V_{CCIO} and pull-down resistors to board ground should be used on the pins listed in Table 6.2.

Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO0}
INITN	4.7 kΩ pull-up to V_{CCIO0}
DONE	4.7 kΩ pull-up to V_{CCIO0}
MCLK	1.0 kΩ to GND (Not installed by default) 1.0 kΩ to V_{CCIO0} (Not installed by default)
MCSN	4.7 kΩ pull-up to V_{CCIO0}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
SCL/SDA[1]	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO1}

Note:

1. Pull-up resistors are not required in target I3C configuration mode.

Table 6.3. Configuration Pins Needed per Programming Mode[1]

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
MSPI	0	(Default)	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
JTAG	1	JTAG_EN pin[2]	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key[2]	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

Notes:

1. Leave unused configuration ports open.
2. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

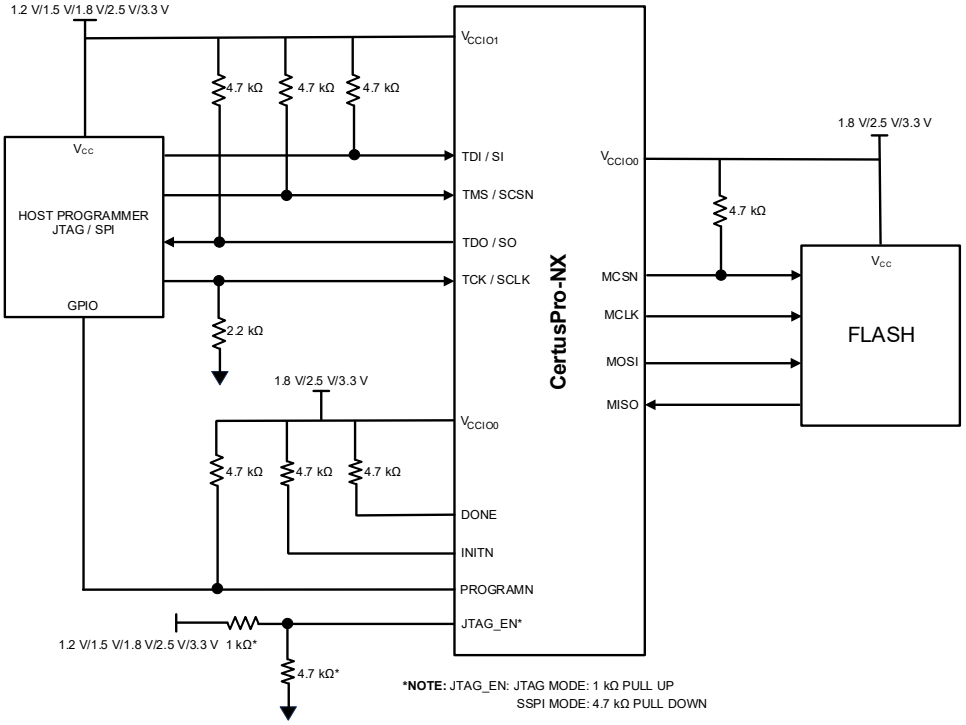

Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI

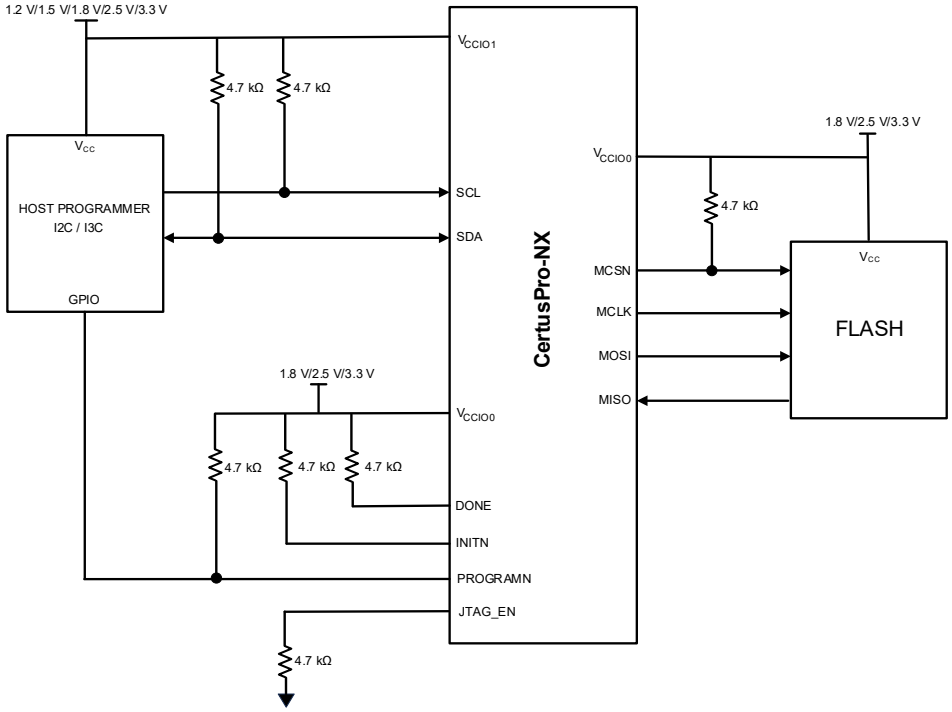

Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C

Some architectures require Bank 0 and Bank 1 to operate at different bank voltages. One such architecture is illustrated in Figure 6.3. When the control signal— such as PROGRAMN—originates in one voltage domain but terminates in another, a voltage translation device or circuit must be implemented to prevent excess current leakage or potential device damage. Figure 6.3 shows a voltage translator used for PROGRAMN, allowing a 3.3 V driver to drive the 1.8 V Bank 0 input buffer safely and efficiently.

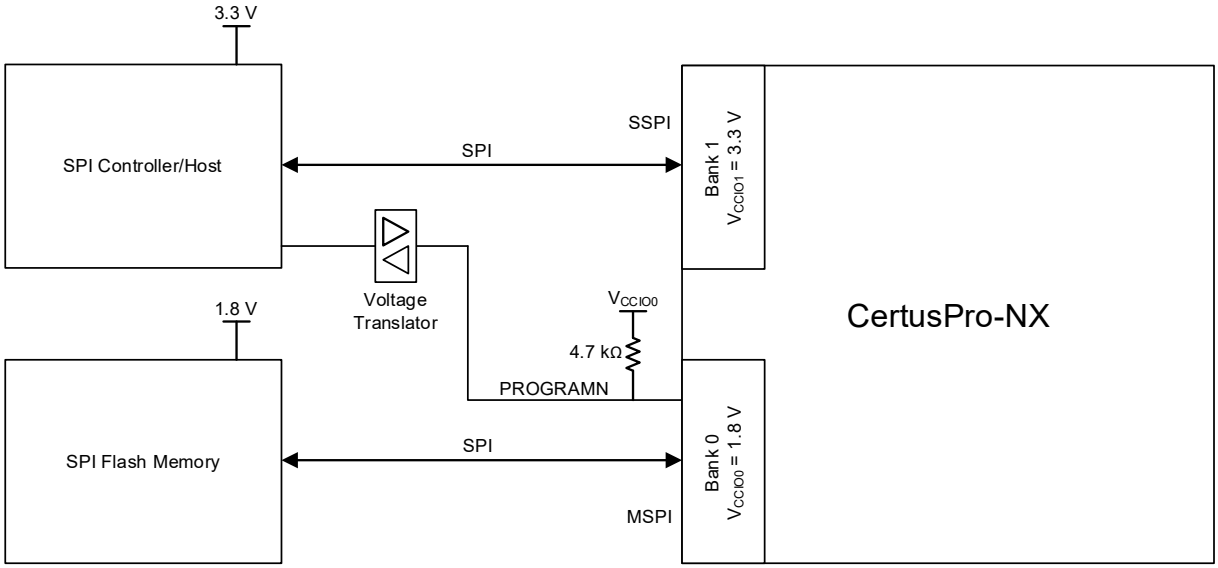

Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks

7. External SPI Flash

The SPI Flash voltage should match the CertusPro-NX bank's V_{CCIO0} voltage.

It is recommended to use SPI Flash devices that are supported by the Radiant Programmer.

You can view the list of supported devices by searching for *SPI Flash support* in the Lattice Radiant Programmer Help menu. For SPI Flash devices that are not listed in the *SPI Flash support*, using the custom flash option may allow non-supported devices to work.

8. I/O Pin Assignments

Assembly and rework parameters for WLCSP packages are similar to other BGA packages. Refer to Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041), which outlines the reflow parameters for all the various package styles offered, including WLCSP.

The V_{CCSDCK}, $V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ provide *quiet* supplies for the SERDES blocks. For optimal jitter performance, careful pin assignment is essential to keep noisy I/O pins away from sensitive ones. A leading cause of PCB-related SERDES crosstalk is the placement of FPGA outputs in close proximity to the sensitive SERDES power supplies. These supplies require meticulous board layout to ensure immunity to switching noise generated by FPGA outputs. While guidelines are provided to help build quiet, filtered supplies, robust PCB layout practice are still necessary to prevent noise from infiltrating these analog supplies.

Although coupling has been reduced in the device packages of CertusPro-NX devices—resulting in minimal crosstalk—the PCB can still introduce significant noise injection from any I/O pin located adjacent to SERDES data, reference clock, and power pins, or other critical I/O signals such as clocks. The Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing hardware to reduce the likelihood of crosstalk affecting the analog supplies. PCB traces that run in parallel over long distances require careful analysis. Use a PCB crosstalk simulation tool to evaluate any suspect traces and determine whether they pose a risk.

It is common practice for designers to select pinouts early in the design cycle. This requires FPGA designer to have a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/Os. Lattice Semiconductor provides detailed pinout information, available for download in.csv format from its website, which designers can use as a resource when creating pinout configuration. For example, by accessing the pinout.csv file, users can obtain pinout details for all package variants within a device family, including I/O banking, differential pairing, dual-function pins, and input/output characteristics.

9. sys I/O

The CertusPro-NX device offers flexibility to configure each I/O according to your design requirements. Pins can be set as input, output, or tri-state. You can also configure attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH.

For the PULLMODE, both pull-up and pull-down resistors can be enabled. These resistors are implemented using a constant current source, with values specified in Table 9.1.

Table 9.1. Weak Pull Up/Down Current Specifications

	Parameter	Condition	Min	Max	Unit
Pull-up	I/O weak pull-up resistor current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	–30	–150	µA
Pull-down	I/O weak pull-down resistor current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	150	µA

The CertusPro-NX device also provides special I/O like, HPIO and WRIO that can be used for high-speed communication. Figure 9.1 shows the block diagram for HPIO and Figure 9.2 shows the block diagram for WRIO.

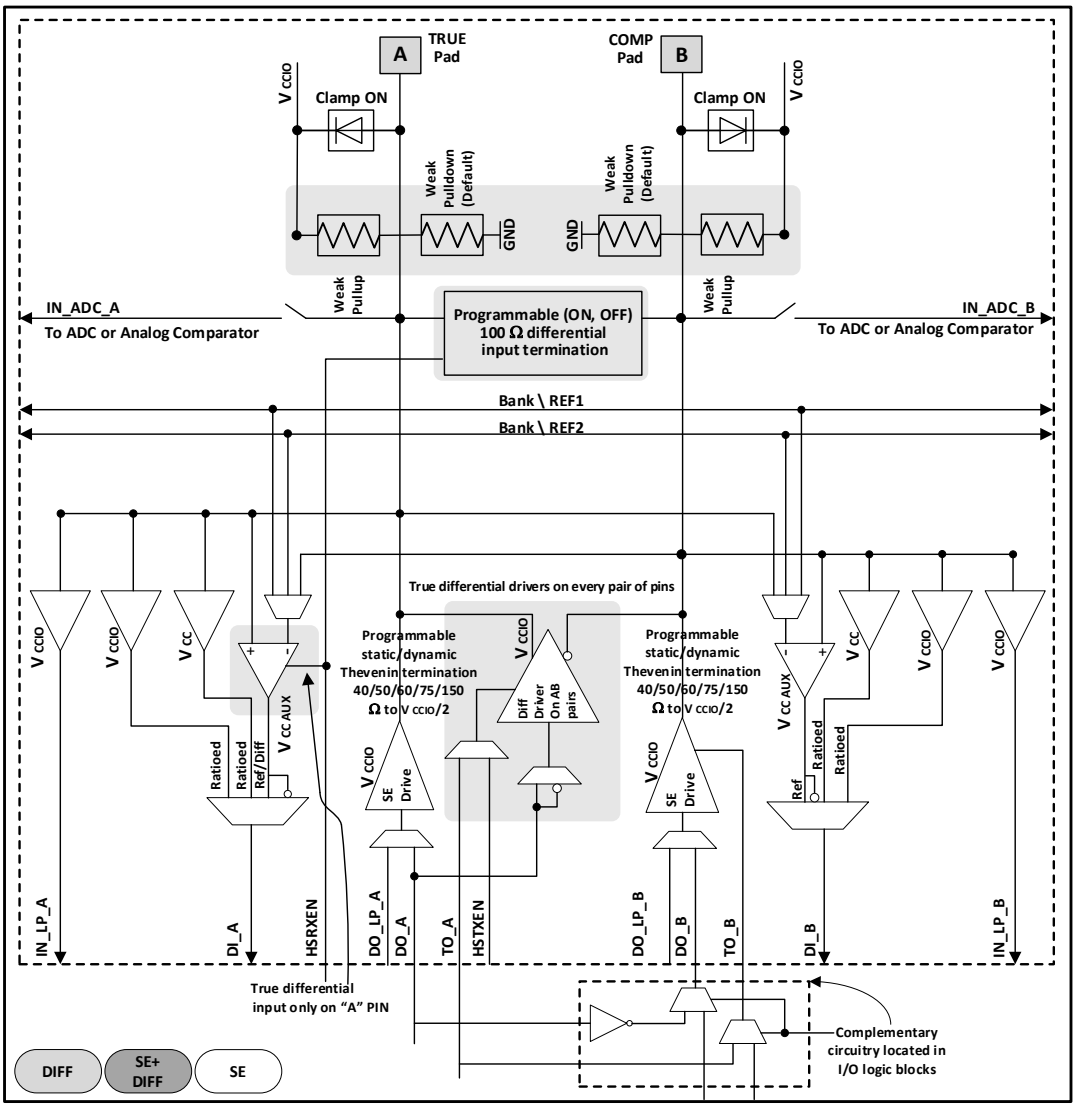

Figure 9.1. High Performance sysI/O Buffer Pair for Bottom Side

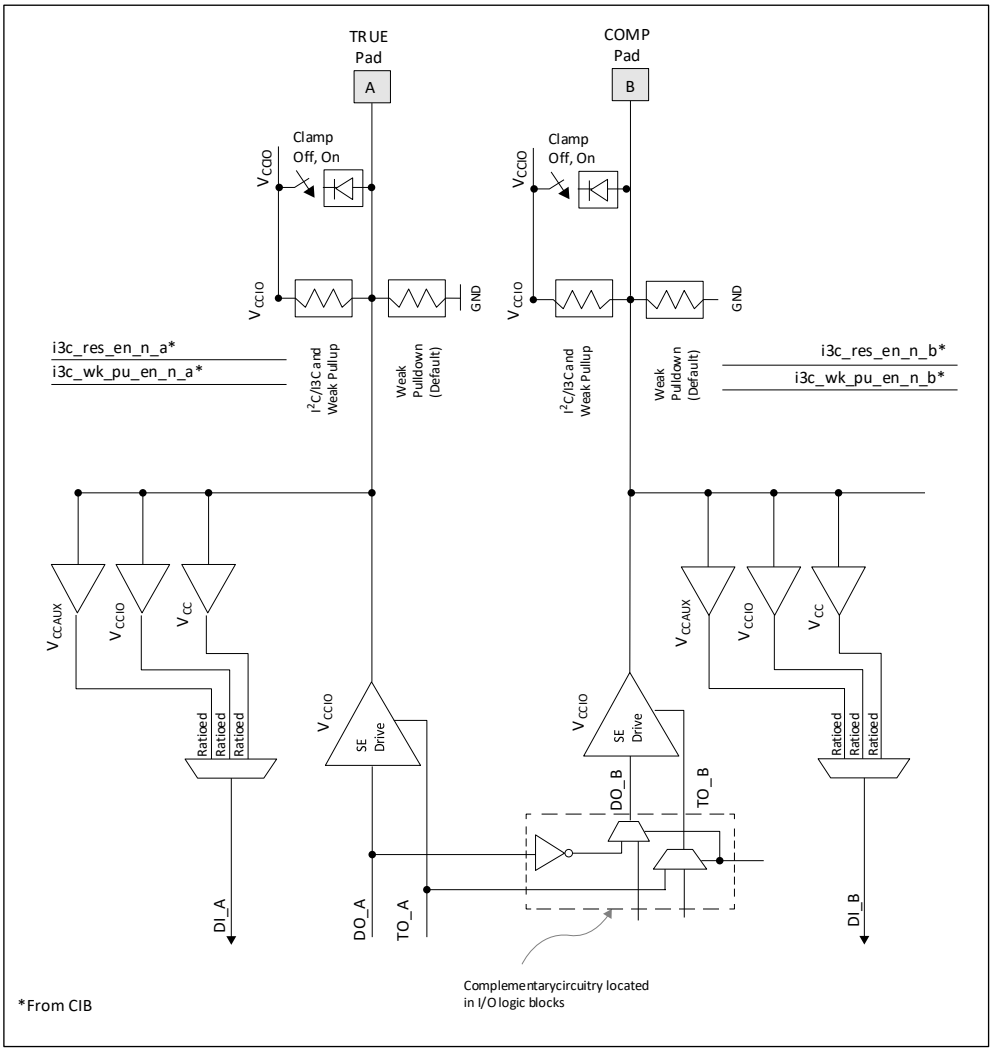

Figure 9.2. Wide Range sysI/O Buffer for Top, Left/Right Side

10. Clock Inputs

The CertusPro-NX device provides dedicated pins in each /O bank that can be used as clock inputs. These pins are shared and may alternately function as general-purpose I/Os. When they are for clocking purposes, it is important to minimize signal noise on these pins. For detailed guidance, refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244).

These shared clock input pins, typically labeled GPLL and PCLK, are listed under the *Dual Function* column of the pinlist.csv file. High-speed differential interfaces (such as MIPI) must route their differential clock pairs into inputs that support differential clocking, specifically labeled as PCLKTx_y (+true) and PCLKCx_y (-complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage does not exceed the voltage level of the target I/O bank. Proper power supply decoupling of the clock oscillator is also essential to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

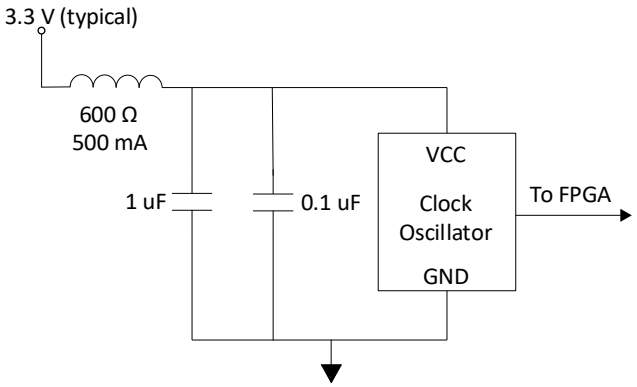

Figure 10.1. Clock Oscillator Bypassing

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to ensure the clock voltage remains less than or equal to the bank's V_{CCIO}. An LVDS oscillator may also be used if AC-coupled and then DC-biased to half the V_{CCIO} voltage. An example of a dual-footprint design that supports both HCSL and LVDS oscillators is as shown in Figure 10.2.

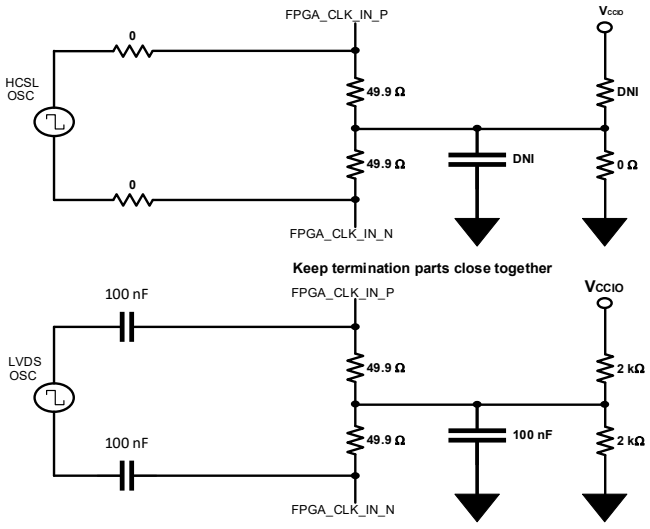

Figure 10.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

10.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enabled pin is shown in Figure 10.3.

Note: External board oscillators typically require 5 to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

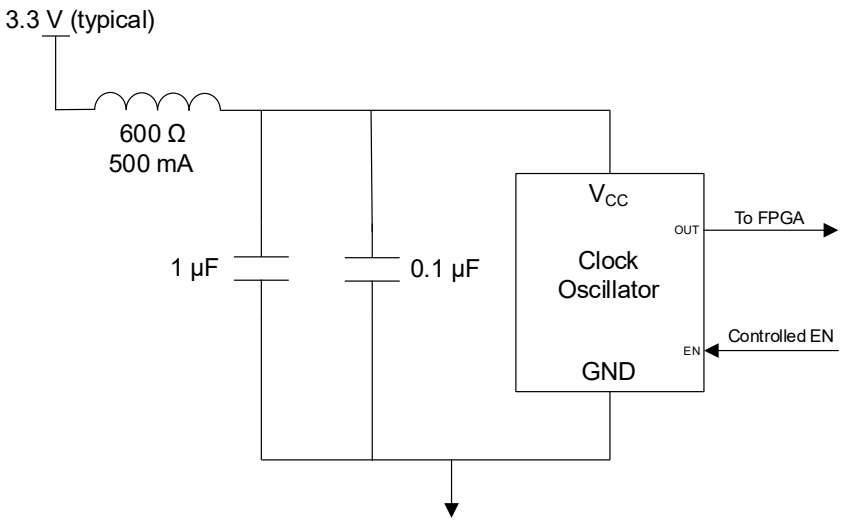

Figure 10.3. Clock Oscillator with Controlled Enable Pin

11. Pinout Considerations

The CertusPro-NX device supports a wide range of high-speed interface applications. These interfaces often require rule-based pinouts that must be understood before beginning PCB design. Pinout selection should be done with a clear understanding of the interface building blocks implemented in the FPGA fabric. These include I/O LOGIC blocks such as DDR, clock resource connectivity, and the use of PLLs and DLLs. For detailed guidelines on these interface types, refer to the CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244).

11.1. LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins on the device's bottom banks 3, 4, and 5 only . The top, left, and right side I/O banks do not support True LVDS standard but can support emulated LVDS outputs. True LVDS input pairings on bottom banks are listed under the High-Speed column in the pinlist .csv file.

Emulated LVDS outputs are available in pairs across all banks; however, they require external termination resistors. This implementation is described in sysI/O User Guide for Nexus Platform (FPGA-TN-02067).

11.2. HSUL, SSTL and LVSTL Pin Assignments

The HSUL, SSTL and LVSTL interfaces are referenced I/O standards that require an external reference voltage. These standards are supported only on the device's bottom banks 3, 4, and 5 only.

When assigning pins on the PCB, give high priority to the V_{REF} pins. These pins can be identified in the Dual Function column of the pinlist .csv file, labeled as V_{REF}. Each I/O bank has a dedicated reference (V_{REF}), which sets the threshold for the referenced input buffers. Individual I/Os are configurable based on the bank's supply and reference voltages.

12. DPHY and SERDES Pin Considerations

High-speed signaling requires careful PCB design to maintain proper transmission line characteristics, A continuous ground reference should be preserved along high-speed routing paths. Differential pairs must be tightly length-matched, with a mismatch no greater than ±4 mil, and should have minimal discontinuities.

The DPHY clock input must use a PCLK pin to ensure direct routing to the edge clock tree. For recommended methods and design guidance, refer to High-Speed PCB Design Considerations (FPGA-TN-02178).

13. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

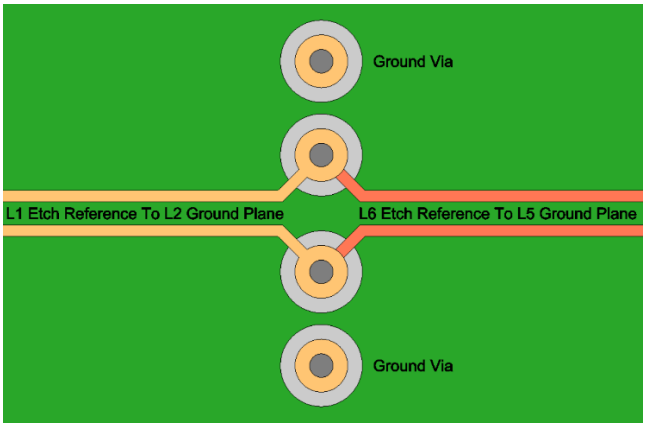

Figure 13.1. Ground Vias Implementation

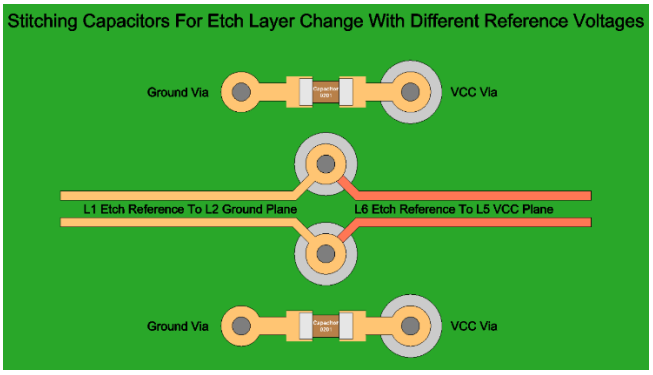

Figure 13.2. Stitching Vias Implementation

6. High-speed signals have a corresponding impedance requirement. Calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

14. Simulation and Board Measurement of Critical Signals

To ensure design reliability and high manufacturing yield, critical signals should be simulated during the design phase and subsequently measured on the assembled PCB to verify proper functionality.

14.1. Critical Signals

Signals that are sensitive to Signal Integrity (SI) degradation are considered critical signals and require additional design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

14.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often require recurring subscription fees. These premium tools can import board design files and provide accurate simulations that include crosstalk and other signal integrity (SI) degrading effects.

Free IBIS-based tools (like Micro-cap) can offer useful basic simulations, but they require more manual effort to set up SI effects—especially when dealing with multiple signals, varying transmission line lengths, lossy lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

14.3. Board Measurements

Critical signals should be measured on the assembled PCB using an oscilloscope to verify proper signaling behavior and signal integrity (like eye diagrams and other SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (for example output series termination resistor value).
- Adjust the setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (for example USB, MIPI).

15. Checklist

Table 15.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{CC} and V_{CCECLK} core at 1.0 V ±5%		
1.1.2	Use a PCB plane for V_{CC} core with proper decoupling		
1.1.3	V_{CC} and V_{CCECLK} core sized to meet power requirement calculation from software		
1.1.4	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} at 1.8 V –3%/+5%		
1.1.5	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} Must be *quiet* and isolated from other switching noises.		
1.1.6	V_{CCAUX} pins and $V_{CCAUXHx}$ pins for banks without high-speed differential pair I/O ganged together. Solid PCB plane is recommended.		
1.1.7	$V_{CCAUXHx}$ banks with high-speed differential pair I/O should use separate FB + Capacitor filter. Solid PCB plane is recommended.		
1.1.8	V_{CCAUXA} pins should be ganged together, and a solid PCB plane is recommended.		
1.2	I/O Supplies		
1.2.1	All *Wide Range* V_{CCIO} (Banks 0,1,2,6,7) are between 1.2 V to 3.3 V		
1.2.2	All *High Performance* (Bank 3,4,5) V_{CCIO} are between 1.0 V to 1.8 V		
1.2.3	All Configuration V_{CCIO} (Banks 0,1), when used with configuration interfaces (for example, memory devices), need to match specifications.		
1.2.4	$V_{CCIO[7:2]}$ used based on user design		
1.3	ADC power supplies		
1.3.1	$V_{CCADC18}$ is 1.8 V +5%		
1.3.2	$V_{CCADC18}$ *quiet* and *isolated*		
1.4	SERDES Power Supplies		
1.4.1	V_{CCSDx} and V_{CCSDCK} are at 1.0 V ±5%		
1.4.2	V_{CCSDx} and V_{CCSDCK} *quiet* and *isolated* from each other and other 1.0 V supplies		
1.4.3	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ are 1.8 V +5%		
1.4.4	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ *quiet* and *isolated* from each other and other 1.8 V supplies		
1.4.5	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ bypass capacitor grounds go only to SDx_REFRET		
2	**JTAG**		
2.1	Apply a pull-up or pull-down resistor to the JTAG_EN pin, as specified in Table 6.2.		
2.2	Ensure the JTAG_EN pin remains accessible on the PCB to allow JTAG port recovery, particularly during development.		
2.3	Ensure the JTAG port pins remain accessible on the PCB, particularly during development.		
2.4	Pull-down on TCK as specified in Table 6.1.		
2.5	Pull-up on TMS, TDI, and TDO as specified in Table 6.1.		
3	**Configuration**		
3.1	Apply pull-up or pull-down resistors on persisted configuration-specific pins as specified in Table 6.1 and Table 6.2		
3.2	V_{CCIO0}, V_{CCIO1} bank voltage must match the sysCONFIG peripheral devices such as SPI Flash.		
4	**Special Pin Assignments**		
4.1	V_{REF} assignments must be applied for single-ended SSTL inputs		
4.2	Properly decouple the V_{REF} source.		
5	**Critical Pinout Selection**		
5.1	The pinout is selected to align FPGA resource connections with I/O logic and clock resources, in accordance with the CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244).		
5.2	Shared general-purpose I/Os are used as inputs for the FPGA PLL and clock inputs signals.		
5.3	The DPHY clock input must be assigned to PCLK pins to enable direct routing to the edge clock tree.		
5.4	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		

	Item	OK	NA
6	**DDR3, DDR3L, LPDDR2, and LPDDR4 Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed as a data group with similar trace lengths and matched via counts. It is recommended to use no more than three vias between the FPGA controller and the memory device.		
6.2	Maintain trace length matching to a maximum of ±20 mil between each DQ/DM signal and its associated DQS strobe in a DQ group. Use precise serpentine routing technique to achieve this requirement.		
6.3	Each data group must reference a continuous ground plane within the PCB stack-up.		
6.4	DDR trace must reference a solid, uninterrupted ground plane, with no slots or breaks, along the entire path between the FPGA and the memory device.		
6.5	Maintain a minimum spacing of 3 W between each data group and any unrelated signals to minimize crosstalk. For all DDR traces—excluding differential CK and DQS pairs—use a minimum of 2 W spacing (W refers to the minimum trace width allowed).		
6.6	FPGA I/O assignments within a data group may be swapped to optimize layout, except for DQS signals, which must remain fixed.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched at ±10 mil.		
6.8	Placing resistor terminations (DQ) in a fly-by configuration at the FPGA is highly recommended. If stub-style terminations are used, ensure that stub lengths do not exceed 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
6.10	Address and control signals, along with associated CK and CK_N differential clock pair, should be routed with trace length matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched within ±10 mil.		
6.12	Address and control signals may reference a power plane if a ground plane is unavailable; however, a ground reference is preferred.		
6.13	Route address and control signals on a separate layer from DQ, DQS, and DM signals to minimize crosstalk.		
6.14	The differential termination for the CLK/CLKN pair must be placed as close as possible to the memory device.		
6.15	Using a fly-by termination technique—placing address and control terminations after the memory component is highly recommended. If stub-style terminations are used, stub lengths must not exceed 600 mils.		
7	**External Flash**		
7.1	Flash voltage should match V_{CCIO0} voltage		
8	**SERDES**		
8.1	The dedicated reference clock input from the clock source must meet both DC and AC electrical requirements.		
8.2	External AC coupling capacitors may be required to ensure compatibility with common-mode voltage levels of connected devices.		
8.3	Reference clock termination resistors may be required to ensure compatible signaling levels.		
8.4	Maintain good high-speed transmission line route with at least 60 mil spacing to other signals.		
8.5	Continuous ground reference plane to serial channels.		
8.6	Tightly length matched differential traces, ±4 mils maximum		
8.7	Do not route other signals on the PCB layers directly above or below high-speed SERDES without isolation.		
8.8	Avoid routing non-SERDES signal traces above or below the V_{CCSDCK}, $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ power plane without isolation.		
9	**ADC**		
9.1	When using the ADC function, route the clock through the lower-right corner PLL.		

	Item	OK	NA
10	**Clock Inputs**		
10.1	External clock source must be connected to PCLK or GPLL pins.		
10.2	PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the PLL Reference Clock Locking section for more details.		

References

For more information refer to:

- CertusPro-NX web page
- CertusPro-NX Family Data Sheet (FPGA-DS-02086)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- Thermal Management (FPGA-TN-02044)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SERDES Jitter (TN1084)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.7, October 2025

Section	Change Summary
All	Minor editorial fixes.
Introduction	The statement, *The device family consists of FPGA densities ranging from 50K to 100K Logic Cells,* has been removed as of revision 1.6.
Clock Inputs	• Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*. • Added the PLL Reference Clock Locking section.
Checklist	• Added item 5.4, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*. • Added *Clock Inputs* under *item 10*.

Revision 1.6, August 2025

Section	Change Summary
All	Minor editorial fixes.
Abbreviations in This Document	Updated section contents.
Introduction	Added, *Hardware Checklists are developed after Evaluation boards and incorporate optimized designs that supersede the circuitry of Evaluation boards. Customers copying circuits from Evaluation boards should optimize their designs according to the Hardware Checklists,* after the first paragraph of this section.
Power Supplies	Replaced *0.25% peak noise* with *0.50% peak noise* in the last sentence of the Power Source section.
CertusPro-NX SERDES and ADC Power Supplies	• Rearranged subsections 3.2 to 3.9. • Updated the ADC_REFP[1:0] notes from *If ADC Block not used, leave open* to *If ADC Block not used, connect to board ground* in Table 3.1. Recommended Power Filtering Groups and Components. • Updated the Unused SERDES Quads section and the Unused SERDES Channels in a Quad section. • Moved *SDx_REXT* to bullet, *Connect to board ground VSSSDQ, and the Rx differential inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET, and SDx_REXT*.
Pinout Considerations	Added LVDS Pin Assignment and HSUL, SSTL, and LVSTL Pin Assignments as subsections.
LVDS Pin Assignments	Removed this section and moved its content under the Pinout Considerations.
HSUL, SSTL, and LVSTL Pin Assignments	Removed this section and moved its content under the Pinout Considerations.
Layout Recommendations	Replaced Figure 15.1 Recommended Layout with Figure 13.1. Ground Vias Implementation and Figure 13.2. Stitching Vias Implementation.
Simulation and Board Measurement of Critical Signals	Added this section.

Revision 1.5, May 2025

Section	Change Summary
All	• Minor editorial fixes. • Changed *SerDes* to *SERDES*.
Abbreviations in This Document	Replaced *Acronyms* with *Abbreviations*.

Section	Change Summary

CertusPro-NX SerDes and ADC Power Supplies	• Changed paragraph style of the Unused SERDES Quads section.
	• Added the following to Unused SERDES Channels in a Quad section.
	  • Connect to board ground the Rx differential inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET.
	  • Leave V_{CCSDx} [x= 0-7], $V_{CCPLLSDx}$ [x = 0-7], SDx_REXT, and Tx differential pair outputs open.

Revision 1.4, June 2024

Section	Change Summary
All	• Minor editorial fixes. • Changed *I²C to I2C*. • Changed *Master to Controller*. • Changed *Slave to Target*.
Inclusive Language	Added this section.
CertusPro-NX SerDes and ADC Power Supplies	• Updated the recommended filter of VCCPLLSDx *to 220 Ω FB + 47 µF + 470 nF per pin* in Table 3.1. Recommended Power Filtering Groups and Components. • Updated Figure 3.1. Recommended Power Filters to align with the changes of VCCPLLSDx in Table 3.1. Recommended Power Filtering Groups and Components.

Revision 1.3, April 2024

Section	Change Summary
All	Minor editorial fixes.
CertusPro-NX SerDes and ADC Power Supplies	Updated the Unused ADC Blocks to *Connect VSSADC, ADC_REFx, ADC_DPx, and ADC_DNx pins to board ground. Leave VCCADC18 floating (not connected)*.

Revision 1.2, January 2024

Section	Change Summary
Disclaimer	Updated this section.
Introduction	Added ADC User Guide for Nexus Platform (FPGA-TN-02129).
Power Supplies	Table 2.1. Single-Ended I/O Standards : Updated the nominal voltage value of ADC_REFP[1:0] from 1.2 V to 1.8 V Typical to *1.0 V to 1.8 V Typical*.

CertusPro-NX SerDes and ADC Power Supplies	• Table 3.1. Recommended Power Filtering Groups and Components:
	  • Updated the notes of ADC_REFP[1:0] from 1.2 V to 1.8 V Typical to *1.0 V to 1.8 V Typical.*
	  • Updated the notes of VCCSDCK from If SerDes Block not used, leave open, to *If both SerDes blocks are not used, leave open*.
	• Added Figure 3.1. Recommended Power Filters.
	• Added subsection 3.5 Capacitor Selection.
	• Removed Figure 3.2. Clock Oscillator Bypassing (formerly figure 3.1) under subsection Clock Oscillator Supply Filtering formerly subsection 3.4.
	• Update subsection 3.7 Unused ADC Blocks to: *Connect VSSADC pins to board ground. Leave VCCADC18 and ADC I/O floating (not connected)*.
	• Updated subsection 3.8 Unused SerDes Quads to: *Connect to board ground VSSSDQ, Rx Differential Inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET. Leave open VCCAUXSDQx [x=0,1], VCCSDx [x= 0-7], VCCPLLSDx [x = 0-7], SDx_REXT, and Tx Differential pair outputs. If both SerDes Quads are not used, then leave open VCCSDCK*.

Section	Change Summary
Configuration Considerations	• Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins: Updated MCLK pin to 1.0 kΩ to V_{CCIO0}. • Table 6.3. Configuration Pins Needed per Programming Mode2: Added note no.2 – Leave unused configuration ports open. • Added Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI and Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C.
External SPI Flash	Added this main section.
sysI/O	Added this main section.
Clock Inputs	Reworked section contents.
Layout Recommendations	Added this main section.

Checklist	Added the following items:
	• No. 7 – External Flash
	  • No. 7.1. Flash voltage should match VCCIO0 voltage
	• No. 9 – ADC
	  • No. 9.1 When using ADC function, use the lower right corner PLL.

References	Added this section.

Revision 1.1, April 2023

Section	Change Summary
Checklist	Updated Table 13.1. Hardware Checklist to change row 6 from 'LPDDR3 and DDR3 Interface Requirements' to 'DDR3, DDR3L, LPDDR2, and LPDDR4 Interface Requirements'.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Revision 1.0, October 2022

Section	Change Summary
All	• Changing document status to Production Release. • Minor adjustments in formatting across the document.
Configuration Considerations	Updated Figure 6.1. Accommodation for Mixed Voltage Across Configuration Banks to change to CertusPro-NX.

Revision 0.83, June 2022

Section	Change Summary
All	Changed SERDES to SerDes across the document.
CertusPro-NX SerDes and ADC Power Supplies	• Added Unused SerDes Quads and Unused SerDes Channels in a Quad sections. • Updated SerDes power filtering for VCCPLLSDx and VCCAUXSDQx in Table 3.1. Recommended Power Filtering Groups and Components.
Configuration Considerations	Updated Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins to add 1.0 kΩ to V_{CCIO1} (not installed by default) for JTAG_EN.
Checklist	• Added $V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ bypass capacitor ground go only to SDx_REFRET. • Updated item 2.5 in JTAG group to change from TMS to TMS, TDI, and TDO.

Revision 0.82, February 2022

Section	Change Summary
DPHY and SerDes Pin Considerations	• Renamed section 12 SerDes Pin Considerations to DPHY and SerDes Pin Considerations. • Added a line to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.
Checklist	Added a row in Table 13.1 to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.

Revision 0.81, August 2021

Section	Change Summary
Configuration Considerations	Added note for Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins.

Revision 0.80, June 2021

Section	Change Summary
All	Preliminary release.

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