CrossLink-NX PCIe Bridge Board Hardware

Evaluation Board User Guide

FPGA-EB-02040-1.1

July 2021

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
caBGA	Chip Array Ball Grid Array
CMOS	Complementary Metal-Oxide Semiconductor
DIP	Dual Inline Package
DNI	Do Not Install
ESD	Electrostatic Discharge
FPGA	Field Programmable Logic Array
FTDI	Future Technology Devices International
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid crystal display
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile industry processor interface
PCIe	Peripheral Component Interconnect Express
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Synchronous Bus

1. Introduction

The Lattice Semiconductor CrossLink™-NX PCI Express® (PCIe) Bridge Board allows you to investigate and experiment with the features of the CrossLink-NX Field Programmable Gate Array (FPGA). The features of the CrossLink-NX PCIe Bridge Board assist you with the rapid prototyping and testing of your specific designs.

The CrossLink-NX PCIe Bridge Board is a feature-rich board with many different interfaces to help you develop system-level applications. The primary function of this board is to support PCIe applications, enabling both Endpoint and Root Port PCIe configurations. This board also supports interfaces such as MIPI CSI-2, RGMII, SGMII and USB3.

- The CrossLink-NX PCIe Bridge Board supports RISC-V Embedded Development platform having DDR3, Ethernet, UART, ADC and SPI Flash as key components. It has power measurement resistors to help manage the power consumption of the entire FPGA.
- The CrossLink-NX PCIe Bridge Board supports embedded vision type applications since it provides you the flexibility to interface with the hardened MIPI of CrossLink-NX. It supports an onboard camera, which is connected to one hard PHY over CSI-2. This board provides flexibility of connecting to the other hard DPHY over FPC for faster prototyping.
- The CrossLink-NX PCIe Bridge Board can be used for a number of end applications. As the name suggests, this board can be used for various bridging functions. A few use cases are:
  - MIPI to PCIe bridging
  - SGMII to PCIe bridging
  - RGMII to PCIe bridging

This board can also be used for a number of other low-level control functions over PCIe such as GPIO, I^2C, and MDIO.

The contents of this user guide include top-level function descriptions for the various sections of the PCIe bridge board, descriptions of the onboard interfaces (SFP, PCIe connector), headers, LEDs and switches, and a complete set of schematics.

2. CrossLink-NX PCIe Bridge Board

The CrossLink-NX PCIe Bridge Board features the CrossLink-NX FPGA in the 400-ball caBGA package (LIFCL-408BG400C). The board has the ability to expand the usability of the CrossLink-NX with SFP, PCIe, CSI, DSI, Ethernet PHY, USB3 controller, and DDR3.

Figure 2.1 and Figure 2.3 show the top view and bottom view of the CrossLink-NX PCIe Bridge Board. Figure 3.1 shows the jumper locations.

2.1. Features

The CrossLink-NX PCIe Bridge board includes the following features:

- CrossLink-NX FPGA (LIFCL-40-8BG400C/ES2)
- PCIe x1 Gen2 supports:
  - Endpoint configuration
  - Root port configuration
- MIPI CSI-2 Camera connector
- One SFP port on SGMII
- One 1 Gbit DDR3 Memory
- One USB 3.0 connector
- D-PHY connector
- USB-B connection for device programming and Inter-Integrated Circuit (I^2C) utility
- One RJ45 on Ethernet RGMII PHY
- Seven user LEDs, three Digit 7-SEG Displays, and five input DIP Switches for demo purpose
- Variable potentiometer and Header for ADC
- Onboard Boot Flash – 512 Mbit Serial Peripheral Interface (SPI) Flash with Quad mode support
- Multiple reference clock sources
- Lattice Radiant™ software programming support

Caution: The CrossLink-NX PCIe Bridge Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

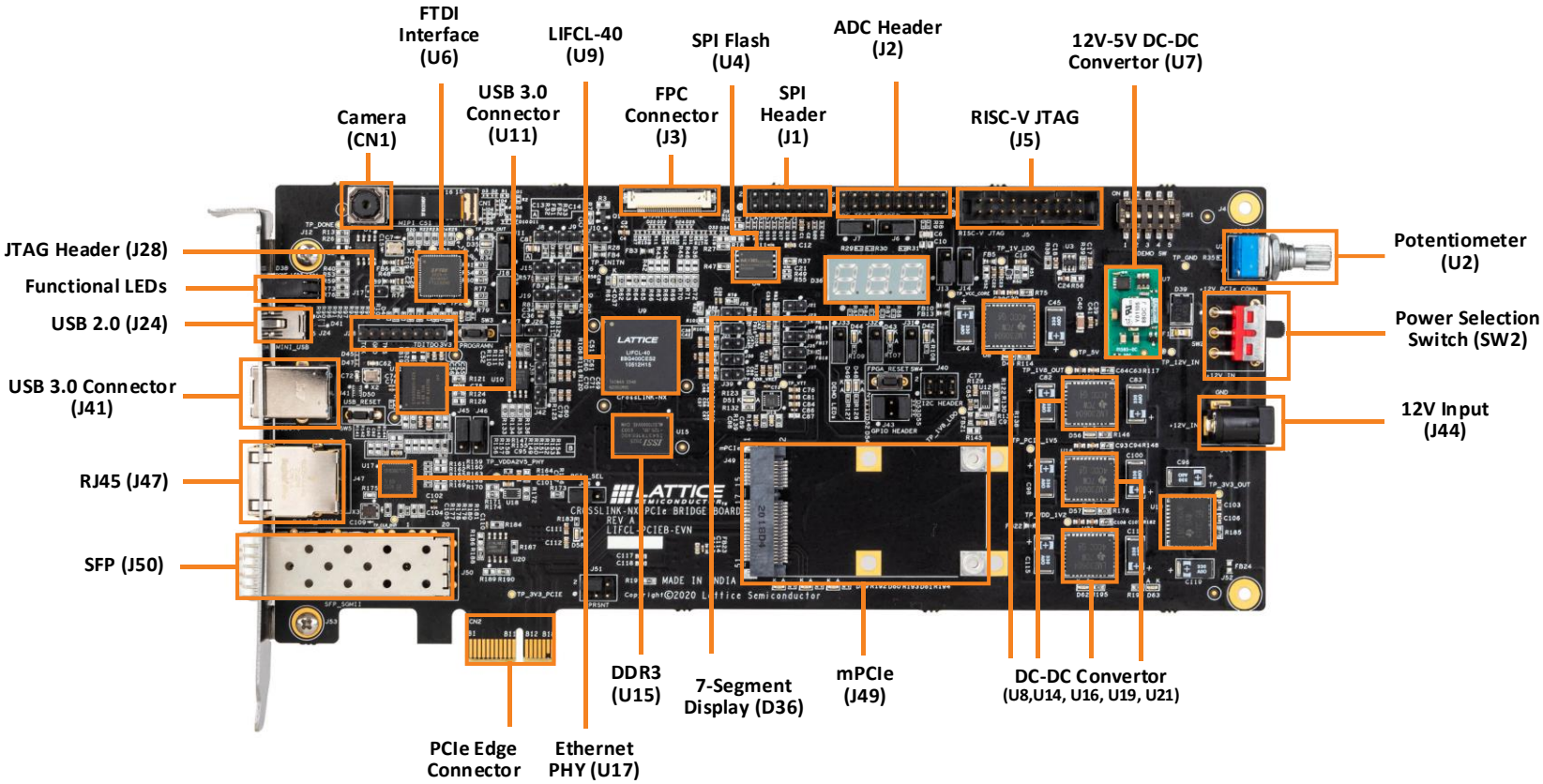

Figure 2.1. Top View of CrossLink-NX PCIe Bridge Board

Figure 2.2. Front View of CrossLink-NX PCIe Bridge Board

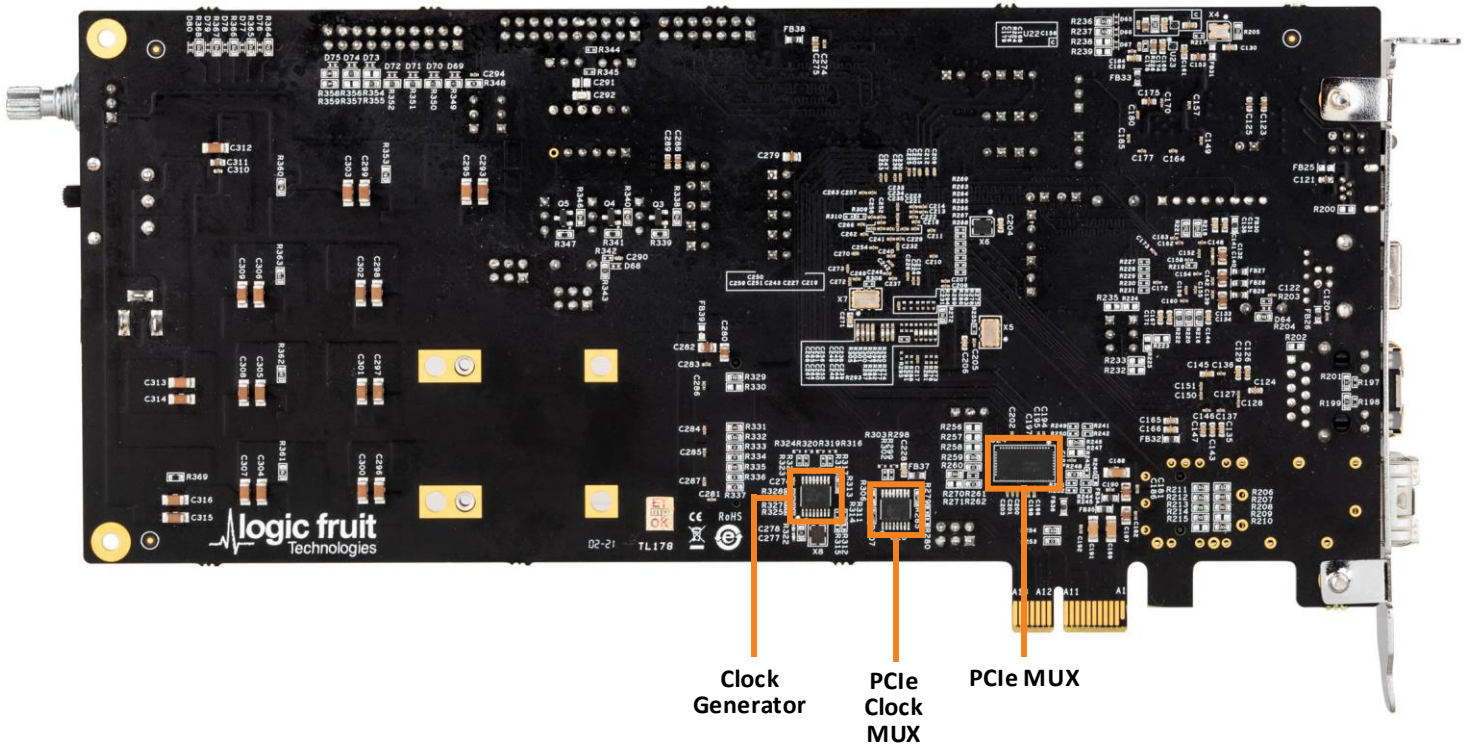

Figure 2.3. Bottom View of CrossLink-NX PCIe Bridge Board

2.2. CrossLink-NX Device

The CrossLink-NX PCIe Bridge Board features the CrossLink-NX device in a 400-ball caBGA package. Also referred to as LIFCL-408BG400C/ES2, it offers a variety of features and programmability. For more information on the capabilities of CrossLink-NX, refer to the CrossLink-NX Family Data Sheet (FPGA-DS-02049).

2.3. Applying Power to the Board

Power is applied to CL-NX PCIe Bridge Board by 12 V adaptor or from PCIe Edge connector. Select the Power adapter or PCIe edge connector by Power Selection Switch (SW2) (Figure 2.4).

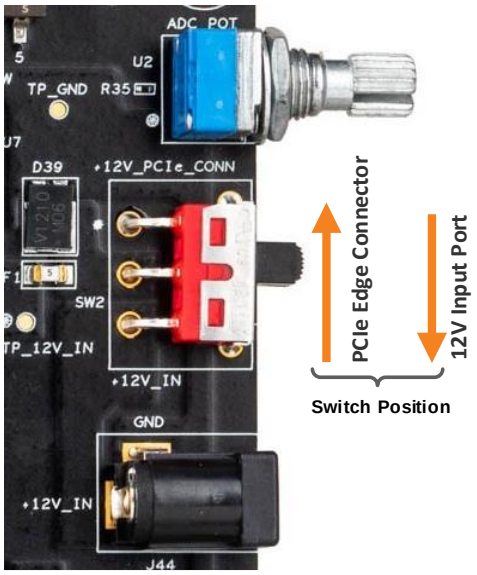

Figure 2.4. Board Power Supply

Table 2.1. Board Power Supply

Part Designator	Description
J44	12 V DC input DC jack
F1	12 V DC Input Supply Fuse
SW2	Power Selection Switch

3. Jumpers and Test Connection

Jumper locations in the card is shown in Figure 3.1. Jumper descriptions and settings are provided in Table 3.1.

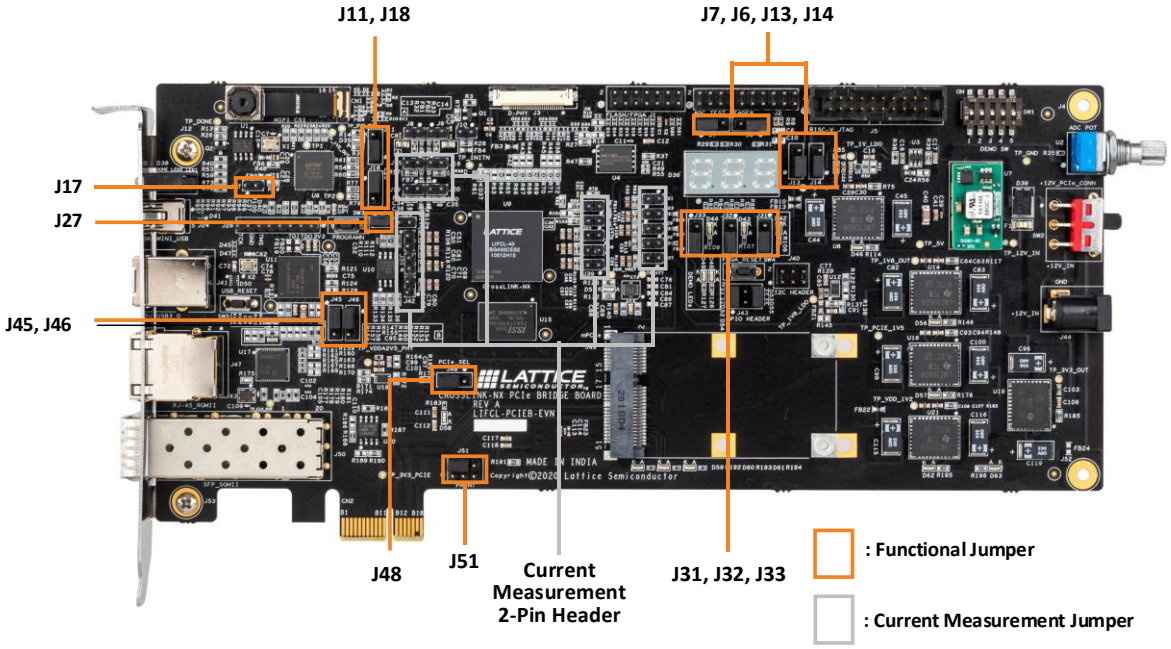

Figure 3.1. Jumper Location

Table 3.1. Jumper Details

Serial No.	Part	Description	Settings
1	J11, J18	FTDI UART/ I2C Select	Default 1-2 Short (1-2 Short FTDI UART/2-3 Short for FTDI I2C)
2	J7	ADC_DP0 Selection Jumper	Default 1–2 (POT)/2-3 (connector)
	J6	ADC_DN0 Selection Jumper	Default 1–2 (GND)/2-3 (connector)
	J13	ADC_REFP1 Selection Jumper	Default 1–2 (ADC_Vref)/2-3 (connector Input Voltage)
	J14	ADC_REFP0 Selection Jumper	Default 1–2 (ADC_Vref)/2-3 (connector Input Voltage)
3	J31	LED and 7 SEGMENT display DIGIT jumper	Default 2-3 Short (2-3 Short for 7SEG Digit 3 control / 1-2 Short for using LED2)
	J32	LED and 7 SEGMENT display DIGIT jumper	Default 2-3 Short (2-3 Short for 7SEG Digit 1 control / 1-2 Short for using LED0)
	J33	LED and 7 SEGMENT display DIGIT jumper	Default 2-3 Short (2-3 Short for 7SEG Digit 2 control / 1-2 Short for using LED1)
4	J8,J9,J10,J15, J16,J19,J20, J21,J22 J23,J25, J26,J29,J30, J34,J35, J36,J37, J38,J39 and J42	Current Measurement 2 Pin Header	—
5	J51	PCIe End Point Reset	Default 2-4 Short
6	J48	PCIe Data Multiplier SEL0	Default 2-3 Short (2-3 Short for PCIe Edge Connector/1-2 Short for mPCIe)
7	J27	USB3 Controller SPI MOSI Jumper	Default Short (Short SPI_MISO connected/Open SPI_MISO unconnected)
8	J45,J46	Ethernet PHY Configuration strap LED_1, LED_2	Default 1-2
9	J17	FTDI RESET Jumper	Default OPEN (Active FTDI)/Short (Reset FTDI)

4. Programming and I²C

The JTAG/SPI programming architecture and I²C interface of the CrossLink-NX PCIe Bridge Board are shown in Figure 4.1.

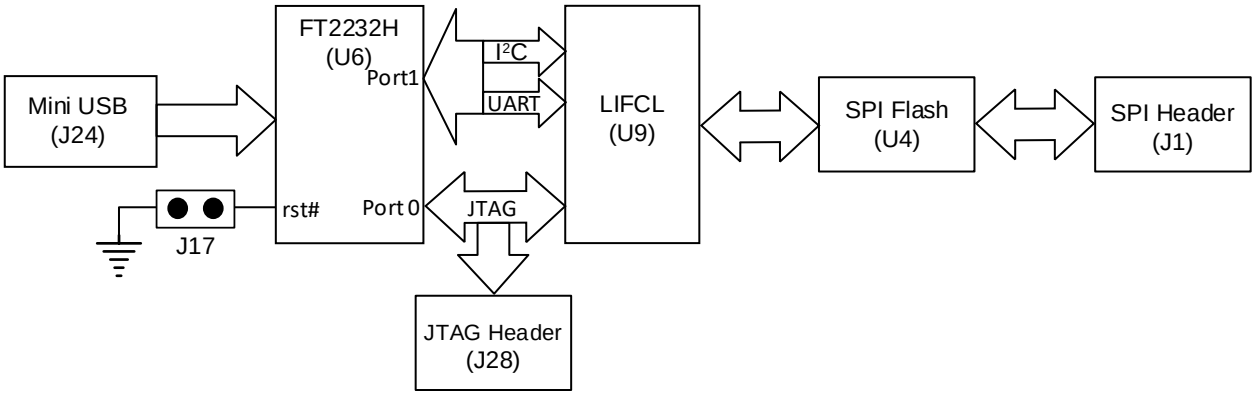

Figure 4.1. Configuration Architecture

4.1. JTAG Download interface

The CrossLink-NX PCIe Bridge Board has a built-in download controller for programming the CrossLink-NX device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download cable, connect the USB cable from a PC with Radiant Programmer tool installed to the mini USB connector on the board. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in cable available for use with the Radiant programming software.

4.2. Alternate JTAG Download Interface

J28 is an 8-pin standalone JTAG header used with an external Lattice download cable that is available separately, when the FTDI part is disabled from the JTAG chain after resetting FTDI. A USB download cable can be attached to the board using this JTAG Header to interface with the CrossLink-NX device. For details on the connection between the USB download cable and J28, refer to Programming Cables User Guide (FPGA-UG-02042).

JTAG Header can also be used as test point when USB to JTAG is working. The JTAG connection is shown in Table 4.1.

Table 4.1. JTAG Connection

J28 Pin Number	Signal Name	CrossLink-NX Ball
1	3V3_OUT	—
2	TDO	F19
3	TDI	F17
4	—	—
5	—	—
6	TMS	F15
7	GND	—
8	TCK	G18

4.3. JTAG to MSPI Pass through Interface

The download controller can also access the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Radiant Programmer. For details about programming the SPI Flash, refer to the Default Demo section.

4.4. Other FPGA Configuration Pins

The CrossLink-NX PCIe Bridge Board provides test points for other FPGA configuration pins as shown in Table 4.2.

Table 4.2. Other JTAG Signals

Signal Name	CrossLink-NX Ball Location	Test Point	Push Button
PROGRAMN	E11	—	SW3
INITN	D11	TP_INITN	—
DONE	D12	TP_DONE	—

For more information on CrossLink-NX JTAG and SPI programming, refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

5. CrossLink-NX Clock Sources

The CrossLink-NX PCIe Bridge Board has three clock sources for the CrossLink-NX FPGA. Refer to Table 5.1 for more details regarding the clock sources.

Table 5.1. Clock Sources

Clock Frequency	Signal Name	Clock Sources	CrossLink-NX Ball	Type
125 MHz	F_CLKIN_125Mhz	X6	K3	Single Ended
100 MHz	F_100Mhz_P	X7	W14	Differential
—	F_100Mhz_N	—	W15	—
125 MHz	F_125Mhz_P	X5	R5	Differential
—	F_125Mhz_N	—	R6	—

6. Default Demo

The CrossLink-NX PCIe Bridge Board is programmed with a default demo. This section provides details about this default demo as well as steps to program the Crosslink-NX FPGA.

The default demo tests the following interfaces on the CrossLink-NX PCIe Bridge Board:

- DIP Switches and onboard user LEDs — There are total five DIP switches and five LEDs on the bridge board. LED1, LED2, LED3 are multiplexed with the three seven-segment displays present onboard. The remaining two LEDs (LED4, LED5) are connected to DIPSWITCH4 and DIPSWITCH5 respectively.
- Seven-segment Display — There are three-digit seven-segment displays on the bridge board.
- Front Facial LEDs — There are three front facial LEDs onboard. LED1 represents the heartbeat signal. LED2 indicates PCIe Linkup status. DONE LED represents successful programming of FPGA. It indicates whether the FPGA booting is successful or not.

6.1. Programming the FPGA

This section guides you through the process of uploading the bit file in SPI Flash. Follow the instructions below.

For programing the .bit file, you need to install the Lattice Radiant 2.2 or later version.

Note: The software programs are available at www.latticesemi.com/en/Products/DesignSoftwareAndIP.
The software programs are available for download only if you log in at www.latticesemi.com.

1. Connect the 12 V power adapter to J44 connector of the Crosslink NX PCIe Bridge Board.
2. Connect the USB Cable to J24 connector of the Crosslink NX PCIe Bridge Board.
3. If the Radiant project is already opened in Lattice Radiant software, click the Radiant Programmer icon from the toolbar. If the project is not opened, click the Windows Start menu and choose *Radiant Programmer* to open the stand-alone Radiant Programmer. The Radiant Programmer - Getting Started dialog pops up (Figure 6.1). The default project name is *Untitled*. Enter a desired project name and browse to settle the project location from the Project Location area. Click **OK**.

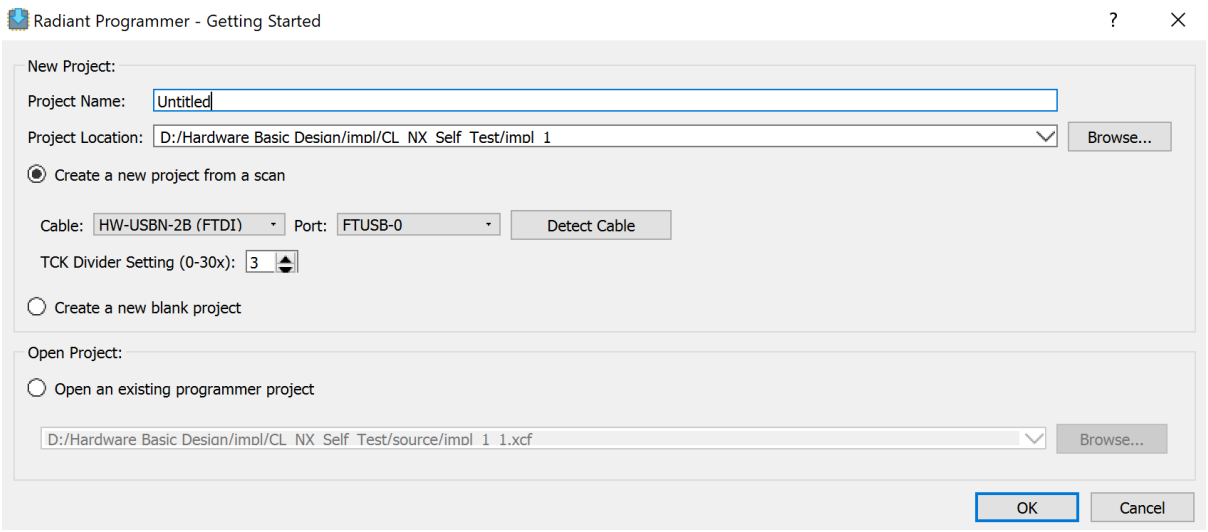

Figure 6.1. Stand-alone Radiant Programmer Opened from Windows Start Menu

4. You can see the selected project opened in the Programmer (Figure 6.2).

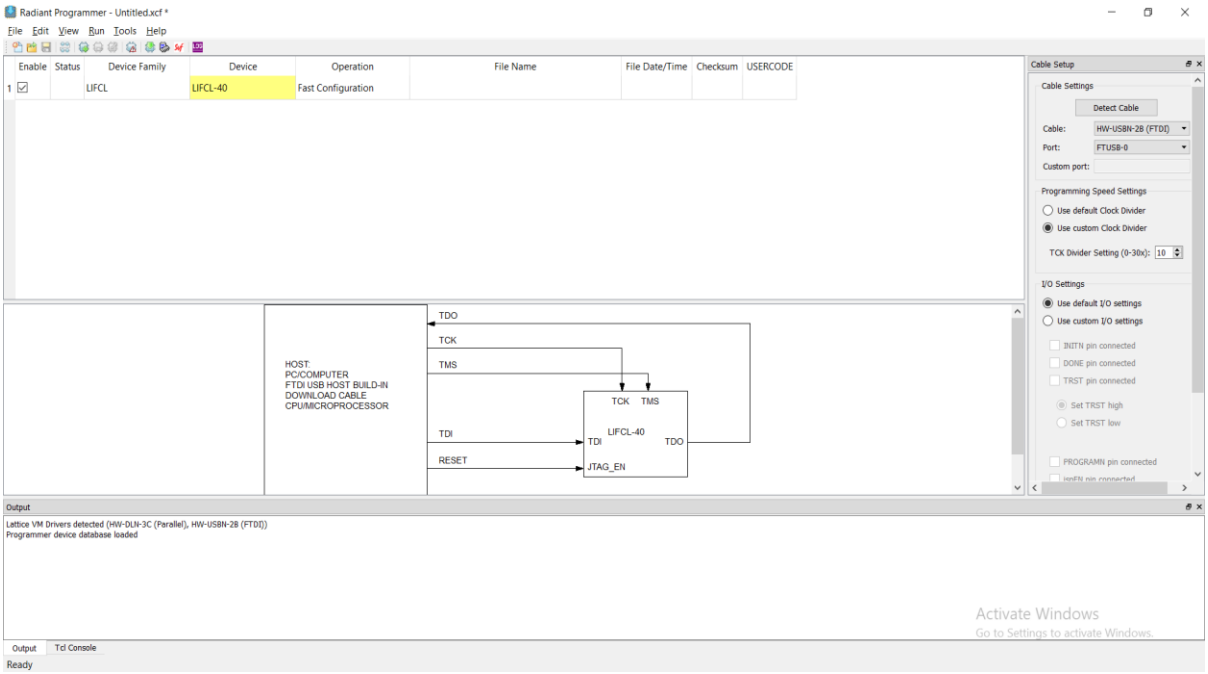

Figure 6.2. Radiant Programmer Window with a Selected Project Opened

5. If the settings you see are not the same as that shown in Figure 6.1, manually make changes and make settings (device family, device, and so on) the same as those shown in Figure 6.3.

	Enable	Status	Device Family	Device	Operation	File Name	File Date/Time	Checksum	USERCODE
1	☑		LIFCL	LIFCL-40	Fast Configuration				

Figure 6.3. FPGA Device Settings

6. Click on *Fast Configuration* from the Operation column (Figure 6.3). The Device Properties dialog pops up (Figure 6.4). Change the Target Memory settings using the drop-down menu, and then you can see the device properties settings exactly as those shown in Figure 6.4.

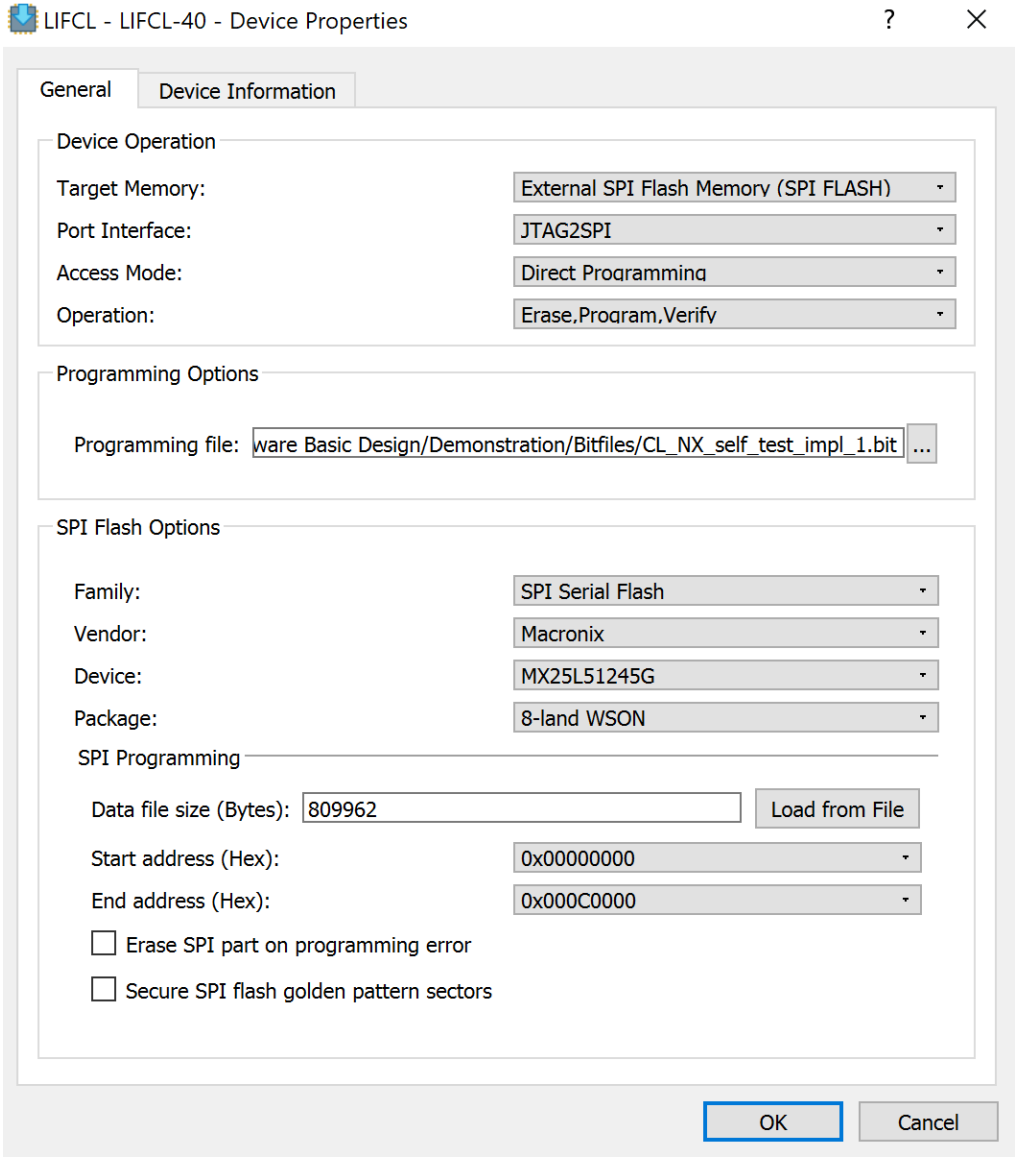

Figure 6.4. Device Properties Dialog for SPI Flash Programming

7. Browse to choose the programming file <*Drive*>://<*Project_Folder*>/*Hardware Basic Design/Demonstration*/Bitstream CL_NX_self_test_impl_1.bit (Figure 6.4).
8. Click **OK**.
9. Click the Program Device icon from the toolbar (Figure 6.5) to start the programming.

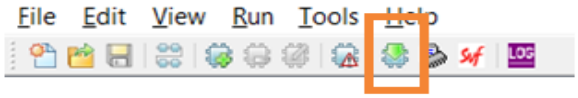

Figure 6.5. Programmer Toolbar

10. Check the Output console for the status of the programming. You should see **Operation: Successful** as shown in Figure 6.6.

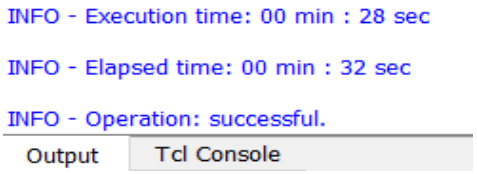

Figure 6.6. Programmer Output Window

11. If there is any issue or problem, refer to the Troubleshooting section for more details.
12. After programming, power cycle the board.

6.1.1. Troubleshooting

This section guides you about the troubleshooting while testing the design.

- If you get verification error while dumping the .bit file, try changing the TCK frequency to be greater than 4. The TCK Divider setting option can be got from the right-click menu of the Radiant Programmer Window (Figure 6.7). Restart programming by clicking .

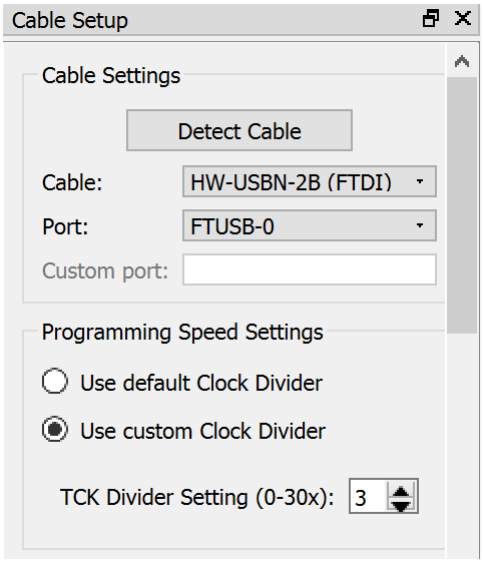

Figure 6.7. TCK Frequency Setting

- If the device is not detected on port FTUSB-0, click on *Detect Cable* and select the port FTUSB-1 (Figure 6.8).

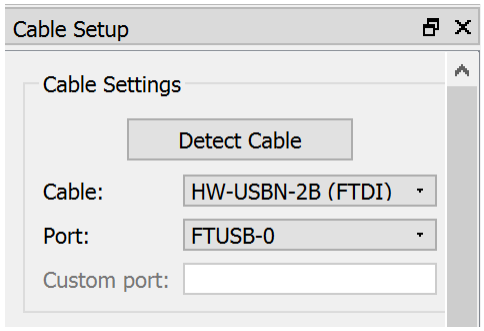

Figure 6.8. Port Selecting

6.2. Observation of Board when Powered by 12 V Supply through Power Adapter

From the following Figure 6.9, you can observe:

- All the power LEDs (D63, D56, D57, D62, D46, D51) glow indicating all the power are Present.
- LED D58 glows indicating that EEPROM for PCIe MUX is Programmed.
- LEDs D48 and D49, which are connected to the DIP Switch 5 and 4 respectively, glow green.
- The 3-digit seven-segment display area displays the Hexadecimal counters starting from 0 to F.

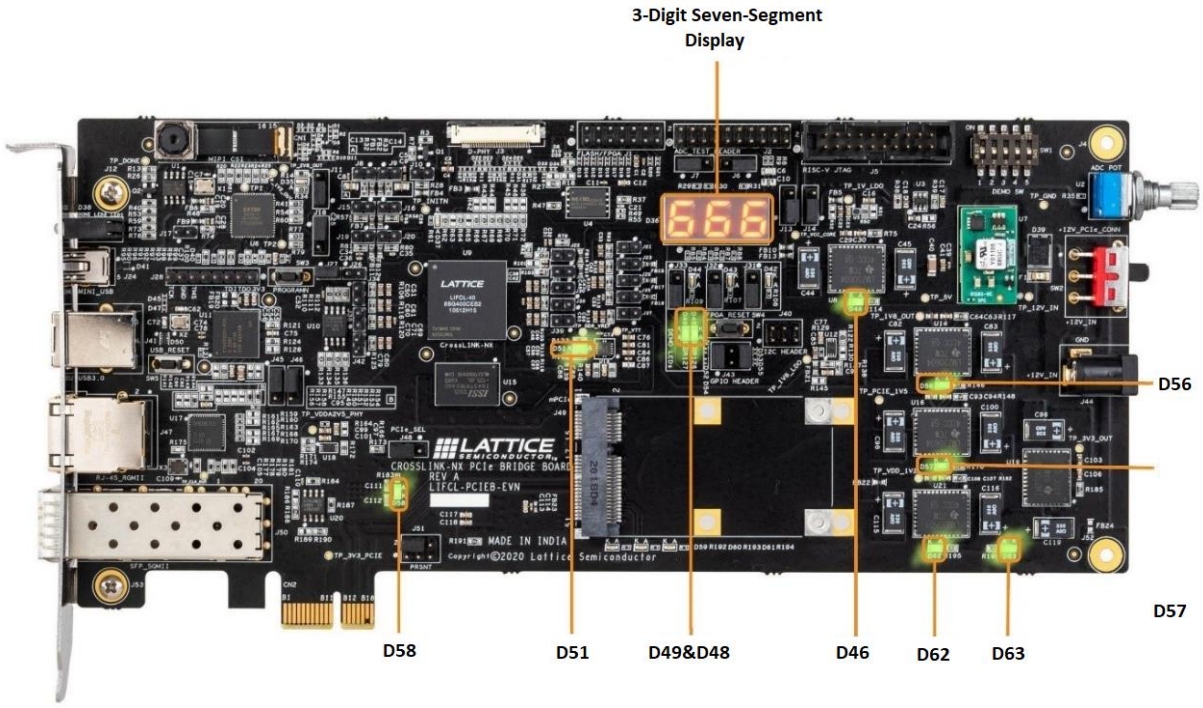

Figure 6.9. Board Status

- The status of the three front facial LEDs (Figure 6.10) should be as follows:
  - The topmost LED (LED 1) should continuously blink green, which is the heartbeat signal.
  - The lower most LED (DONE) shows the status of FPGA being done, no matter the FPGA has been booted from the SPI flash or not. It should glow green, depicting that FPGA has been booted.
  - The middle LED (LED2) indicates PCIe link up status. Its being green indicates the link success, while its being red indicates the link-up failure.

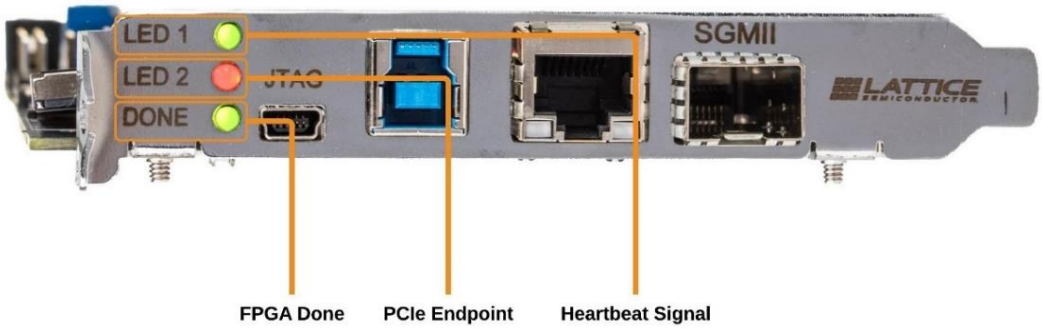

Figure 6.10. Front Facial LEDs Status

Note: Perform the observation procedure below when the board is connected to the PC through the PCIe Endpoint:

1. Connect the board through the PCIe End points by changing the position of the power selection switch (SW2) to the PCIe Edge Connector side, as described in the Applying Power to the Board section.
2. Connect the board to PC through PCIe Pluggable Cable. Alternatively, directly insert the board into the PCIe slot of the CPU in the turn-off condition.
3. Turn on the PC.
4. You can observe the Board status through the three front facial LEDs status (Figure 6.11).
   - The topmost LED (LED 1) should continuously blink green, which is the heartbeat signal.
   - The lower most LED (DONE) shows the status of FPGA being done, no matter the FPGA has been booted from the SPI flash or not. It should glow green, depicting that FPGA has been booted.
   - The middle front facial LED should glow green indicating that PCIe Linkup has been done.

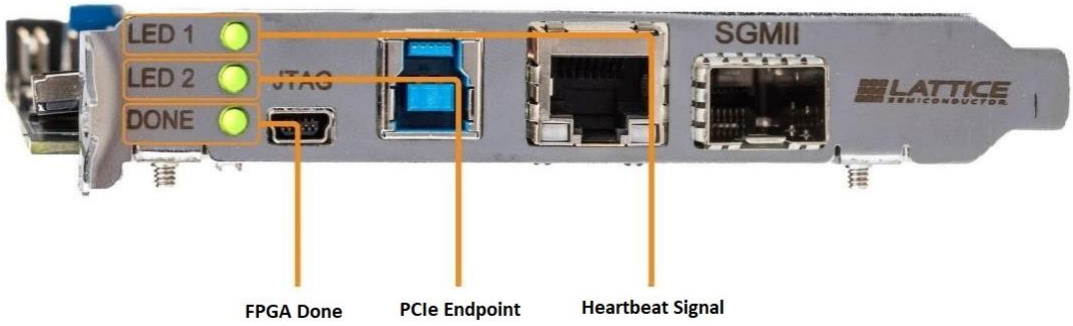

Figure 6.11. Front Facial LEDs Status after PCIe Linkup

7. Control Buses – UART, I²C, and SPI

This section describes the topology of the various configuration and communication buses.

7.1. I²C Topology

The CrossLink-NX PCIe Bridge Board uses the I²C bus to support CrossLink-NX FPGA configuration. The I²C bus has the signal names FTDI_I2C_SCL and FTDI_I2C_SDA. When 2-3 pin of jumpers, J11 and J18 for example, are short, then the I²C bus is connected to a dedicated CrossLink-NX FPGA GPIO (PR11A/E20 and PR11B/F20). The I²C and UART share the same output port B on FTDI chip. Refer to Figure 7.1 for the topology diagram. The I²C connections are summarized in Table 7.1.

Table 7.1. I²C Bus Connection

Signal Name	CrossLink-NX Ball Location	FTDI CHIP Pin	Jumper
FTDI_I2C_SCL	F20	38	J18
FTDI_I2C_SDA	E20	39 &40	J11

7.2. UART Topology

The board provides support for UART configuration by providing an uninstalled connection between the FTDI and CrossLink-NX device. Two Jumpers (J11 and J18) short Pin 1-2 to connect Port 1 to two general purpose I/O (PR3B/E17 and PR4A/F13) in Bank 1. The I²C Architecture and UART option are shown in in Figure 7.1.

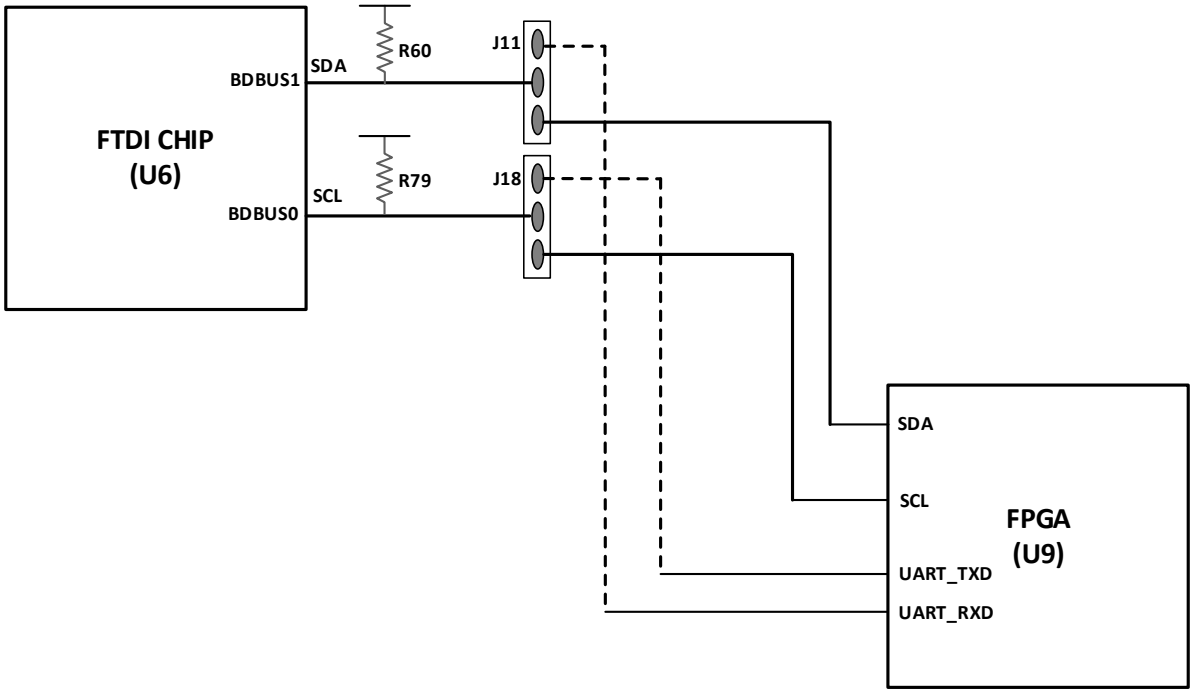

Figure 7.1. I²C Architecture and UART Option

7.3. SPI Topology

One of the major functions of SPI connections on the board is to support CrossLink-NX configuration from the SPI Flash or the Parallel Configuration Header (Table 7.2). The CrossLink-NX PCIe Bridge Board can support both Master SPI (MSPI) and Slave SPI (SSPI) modes for CrossLink-NX configuration.

Table 7.2. CrossLink-NX SPI Connections

Signal Name	CrossLink-NX Ball	Parallel Configuration Header Pin
F_FLASH_MOSI	D13	5
F_FLASH_MISO	D15	7
F_FLASH_DQ2	D14	11
F_FLASH_DQ3	D16	9
F_FLASH_CS#	E13	2
F_FLASH_MCLK	E12	12
MCSNO	E16	3

8. LEDs and Switches

This section describes the CrossLink-NX PCIe Bridge Board LEDs and switches that can be used in demo designs.

8.1. DIP Switch

Five CrossLink-NX pins are connected to the SW1 DIP switch (Figure 8.1) to allow for manually actuated inputs to the FPGA. One side of each switch is connected to the GPIO within the VCCIO4 bank and pulled up through 4.7 kΩ resistors, the other side is grounded. The designated pins are connected as shown in Table 8.1.

Table 8.1. DIP Switch Signals

Signal Name	Silk Screen Pin Number	CrossLink-NX Ball	CrossLink-NX Bank	Logic Level at ON Position
SWITCH1	1	P11	4	0
SWITCH2	2	V10	4	0
SWITCH3	3	U10	4	0
SWITCH4	4	T11	4	0
SWITCH5	5	T10	4	0

Figure 8.1. SW1 DIP SWITCH

8.2. General Purpose Push Button

The CrossLink-NX PCIe Bridge Board provides three push button switches (Figure 8.2, Figure 8.3, and Figure 8.4) for configuration, Reset of which provides ease of use. As listed in Table 8.2, the first two of the buttons control pre-defined functional pins, and the third is for USB3 Controller Reset. Pressing these buttons drives a logic level *0* to the corresponding I/O pins.

Table 8.2. Push Button Signals

Signal Name	CrossLink-NX Ball	Push Button Reference	Logic Level at Button Pressed
PROGRAMN	E11	SW3	0
F_RESET_N	G19	SW4	0
F_USB3.0_RESET#	R4	SW5	0

Figure 8.2. PROGRAMN Button

Figure 8.3. FPGA RESET Button

Figure 8.4. USB3.0_RESET Button

When PROGRAMN (SW3) is asserted LOW, the FPGA exits user mode and starts a device configuration sequence at the Initialization phase. Holding the PROGRAMN pin LOW prevents the CrossLink-NX device from leaving the Initialization phase. SW4 is intended to be used as a global set/reset pin when active LOW, but can be substituted by another function if you desire. SW5 is to reset the USB3 Controller.

8.3. General Purpose LEDs and GPIO

The CrossLink-NX PCIe Bridge Board provides five LEDs (Figure 8.5) that are connected to I/O within Bank 4 and Bank 2. LED1, LED2, LED3 are multiplexed with the 3-digit seven-segment display presented onboard. The remaining two LEDs, LED4 and LED5, are connected to DIPSWITCH4 and DIPSWITCH5 respectively.

Figure 8.5. LEDs

One stacked LED (Figure 8.6) is connected to Bank 0 and Bank 2. The LEDs are lighted when the output is driven HIGH. Four WR GPIO for the user is provided on the header (Figure 8.7). Refer to Table 8.3 for more details.

Figure 8.6. Stack-up LED

Figure 8.7. GPIO Header

Table 8.3. General Purpose LEDs and GPIO

Signal Name	Reference Designator	CrossLink-NX Ball	CrossLink-NX Bank/Color
LED0	D43	R7	4 (Green)
LED1	D44	T7	4 (Green)
LED2	D42	Y9	4 (Green)
LED3	D49	P17	2 (Green)
LED4	D48	R17	2 (Green)
ST_LED1_0, ST_LED1_1	D38_1	D17, E18	0 (Green/Red)
ST_LED2_0, ST_LED2_1	D38_2	W19, Y19	2 (Green/Red)
GPIO 1	J43	N14	2
GPIO 2	J43	N16	2
GPIO 3	J43	T20	2
GPIO 4	J43	W20	2

8.4. Indicator LEDs

Table 8.4 lists various LEDs and describes their purpose.

Table 8.4. Various LED Signals

LEDs	Signal Name	CrossLink-NX Ball	Color	Purpose
D35	UART_ACT	F13	Green	If Installed, Lights in UART mode.
D37	INITN	D11	RED	Lights if configuration error.
D38_1	125Mhz Clock present	R5, R6	Green	Green Blinking when Clock present.
D38_2	PCIe Link up	—	—	Lights up if PCIe link up takes place.
D38_3	DONE	D12	Green	Lights if successful configuration.
D63	+3.3V	—	Green	Lights up if voltage present.
D56	+1.8V	—	Green	Lights up if voltage present.
D57	+1.5V	—	Green	Lights up if voltage present.
D62	+1.2V	—	Green	Lights up if voltage present.
D46	+1V(VCC_Core)	—	Green	Lights up if voltage present.
D51	0.75V	—	Green	Lights up if DDR Reference voltage present.
D58	PCIe MUX EEPROM Programmed	—	Green	Lights up if EEPROM programmed.

9. Connectors Mapping and LIFCL-40 Device Ball Mapping

This section describes the CrossLink-NX PCIe Bridge Board headers/connectors and ball mapping.

9.1. SPI Configuration Header

Table 9.1. SPI Configuration Header

J1 Pin Name	Signal Name	LIFCL-40 Ball
1	CONN_PROGRAMN	E11
2	CONN_FLASH_CS#	—
3	MCSNO	E16
4	DONE	D12
5	CONN_FLASH_MOSI	—
6	CONN_INITN	D11
7	CONN_FLASH_MISO	—
8	—	—
9	CONN_FLASH_DQ3	—
10	3V3_OUT	—
11	CONN_FLASH_DQ2	—
12	CONN_FLASH_MCLK	—
13	GND	—
14	GND	—

9.2. Camera Connector

Table 9.2. Camera Connector

CN1 Pin Name	Signal Name	LIFCL-40
1	No Connect	—
2	CAM_CLK_N	B1
3	CAM_CLK_P	A2
4	GND	—
5	CAM_D3_N	B4
6	CAM_D3_P	A4
7	GND	—
8	CAM_D1_N	B3
9	CAM_D1_P	A3
10	GND	—
11	CAM_D0_N	C1
12	CAM_D0_P	B2
13	GND	—
14	CAM_D2_N	D1
15	CAM_D2_P	C2
16	GND	—
17	GND	—
18	2V8_OUT	—

CN1 Pin Name	Signal Name	LIFCL-40
19	No Connect	—
20	CAM_MCLK	—
21	No Connect	—
22	CAM_I2C_SDA	W5
23	CAM_I2C_SCL	Y5
24	CAM_RESET	W1
25	1V2_OUT	—
26	1V8_OUT	—
27	GND	—
28	GND	—
29	2V8_OUT	—
30	GND	—

9.3. PCIe Edge Connector

Table 9.3. PCIe Edge Connector

CN2 Pin Name	Signal Name	LIFCL-40 Ball	CN2 Pin Name	Signal Name	LIFCL-40 Ball
A1	PCIe_EC_PRSNT#1	—	B1	12V_IN_PCIE	—
A2	12V_IN_PCIE	—	B2	12V_IN_PCIE	—
A3	12V_IN_PCIE	—	B3	12V_IN_PCIE	—
A4	GND	—	B4	GND	—
A5	No Connect	—	B5	No Connect	—
A6	No Connect	—	B6	No Connect	—
A7	No Connect	—	B7	GND	—
A8	No Connect	—	B8	3V3_PCIe	—
A9	3V3_PCIe	—	B9	No Connect	—
A10	3V3_PCIe	—	B10	No Connect	—
A11	F_PCIe_EC_PRSNT#	M15	B11	No Connect	—
A12	GND	—	B12	No Connect	—
A13	F_PCIe_EC_100Mhz_CLK_P	—	B13	GND	—
A14	F_PCIe_EC_100Mhz_CLK_N	—	B14	EP_PCIe_RXD_P	—
A15	GND	—	B15	EP_PCIe_RXD_N	—
A16	EP_PCIe_TXD_P	—	B16	GND	—
A17	EP_PCIe_TXD_N	—	B17	PCIe_EC_PRSNT#3	—
A18	GND	—	B18	GND	—

9.4. mPCIe Connector

Table 9.4. mPCIe Connector

J49 Pin Name	Signal Name	LIFCL-40 Ball	J48 Pin Name	Signal Name	LIFCL-40 Ball
1	3V3_OUT	—	27	GND	—
2	3V3_OUT	—	28	PCIE_1V5	—
3	No Connect	—	29	GND	—
4	GND	—	30	F_PCIe_I2C_SCK	M18
5	No Connect	—	31	RT_PCIe_TXD_N	—
6	PCIE_1V5	—	32	F_PCIe_I2C_SDA	M19
7	F_PCIe_CLKREQ#	M16	33	RT_PCIe_TXD_P	—
8	No Connect	—	34	GND	—
9	GND	—	35	GND	—
10	No Connect	—	36	No Connect	—
11	mPCIE_100Mhz_CLK_N	—	37	No Connect	—
12	No Connect	—	38	No Connect	—
13	mPCIE_100Mhz_CLK_P	—	39	3V3_OUT	—
14	No Connect	—	40	GND	—
15	GND	—	41	3V3_OUT	—
16	No Connect	—	42	LED_WWAN#	—
17	No Connect	—	43	No Connect	—
18	GND	—	44	LED_WWAN#	—
19	No Connect	—	45	No Connect	—
20	No Connect	—	46	LED_WWAN#	—
21	GND	—	47	No Connect	—
22	F_PCIe_RESET#	M14	48	PCIE_1V5	—
23	RT_PCIe_RXD_N	—	49	No Connect	—
24	3V3_OUT	—	50	GND	—
25	RT_PCIe_RXD_P	—	51	No Connect	—
26	GND	—	52	3V3_OUT	—

9.5. SFP Connector

Table 9.5. SFP Connector

J50 Pin Name	Signal Name	LIFCL-40 Ball
1	GND	—
2	F_SFP_TX_FAULT	P20
3	F_SFP_TX_DISABLE	P19
4	F_SFP_I2C_SDA	N20
5	F_SFP_I2C_SCL	N19
6	F_SFP_ABS	M20
7	F_SFP_RS0	—
8	F_SFP_LOS	M17
9	F_SFP_RS1	—

J50 Pin Name	Signal Name	LIFCL-40 Ball
10	GND	—
11	GND	—
12	F_SFP_RX_N	T1
13	F_SFP_RX_P	U1
14	GND	—
15	3V3_OUT	—
16	3V3_OUT	—
17	GND	—
18	F_SFP_TX_P	Y2
19	F_SFP_TX_N	Y3
20	GND	—

9.6. RISC-V JTAG Connector

Table 9.6. RISC-V JTAG

J5 Pin Number	Signal Name	LIFCL-40 Ball
1	3V3_OUT	—
2	3V3_OUT	—
3	RISC_N_TRST	G15
4	GND	—
5	RISC_TDI	L13
6	GND	—
7	RISC_TMS	L14
8	GND	—
9	RISC_TCK	L16
10	GND	—
11	RISC_RTCK	L15
12	GND	—
13	RISC_TDO	L20
14	GND	—
15	RISC_N_SRST	L19
16	GND	—
17	GND	—
18	GND	—
19	GND	—
20	GND	—

9.7. FPC Connector

Table 9.7. FPC Connector

J3 Pin Number	Signal Name	LIFCL-40 Ball
1	CAM_I2C_SDA	W5
2	LCD_VDD_1V8	—
3	LCD_VDD_1V8	—
4	CAM_I2C_SCL	Y5
5	LCD_RESET	W7
6	LCD_PWM_CNTRL	V1
7	GND	—
8	LCD_D0_N	B7
9	LCD_D0_P	A7
10	GND	—
11	LCD_D1_N	B9
12	LCD_D1_P	A9
13	GND	—
14	LCD_CLK_N	B8
15	LCD_CLK_P	A8
16	GND	—
17	LCD_D2_N	B6
18	LCD_D2_P	A6
19	GND	—
20	LCD_D3_N	B10
21	LCD_D3_P	A10
22	GND	—
23	GND	—
24	GND	—
25	GND	—
26	GND	—
27	LCD_5V5	—
28	LCD_5V5	—
29	LCD_5V5	—
30	LCD_5V5	—

9.8. ADC Connector

Table 9.8. ADC Connector

J2 Pin Number	Signal Name	LIFCL-40 Ball
1	GND	—
2	GND	—
3	J7 Pin 3	—
4	GND	—
5	J6 Pin 3	—
6	GND	—
7	GND	—
8	GND	—
9	ADC_DP1	T17
10	GND	—
11	ADC_DN1	U17
12	GND	—
13	GND	—
14	GND	—
15	VREF1_CON	—
16	GND	—
17	GND	—
18	GND	—
19	VREF0_CON	—
20	GND	—

10. Power Scheme

The CrossLink-NX PCIe Bridge Board has most of its power supplied by onboard regulators powered by an external 12 V Adaptor or PCIe Edge Connector. Refer to Appendix A. CrossLink-NX PCIe Bridge Board Schematics to see the details of these power supply options. Figure 10.1 shows the high-level power supply architecture of the board. Table 10.1 shows the voltage options available for the various VCCIO supplies.

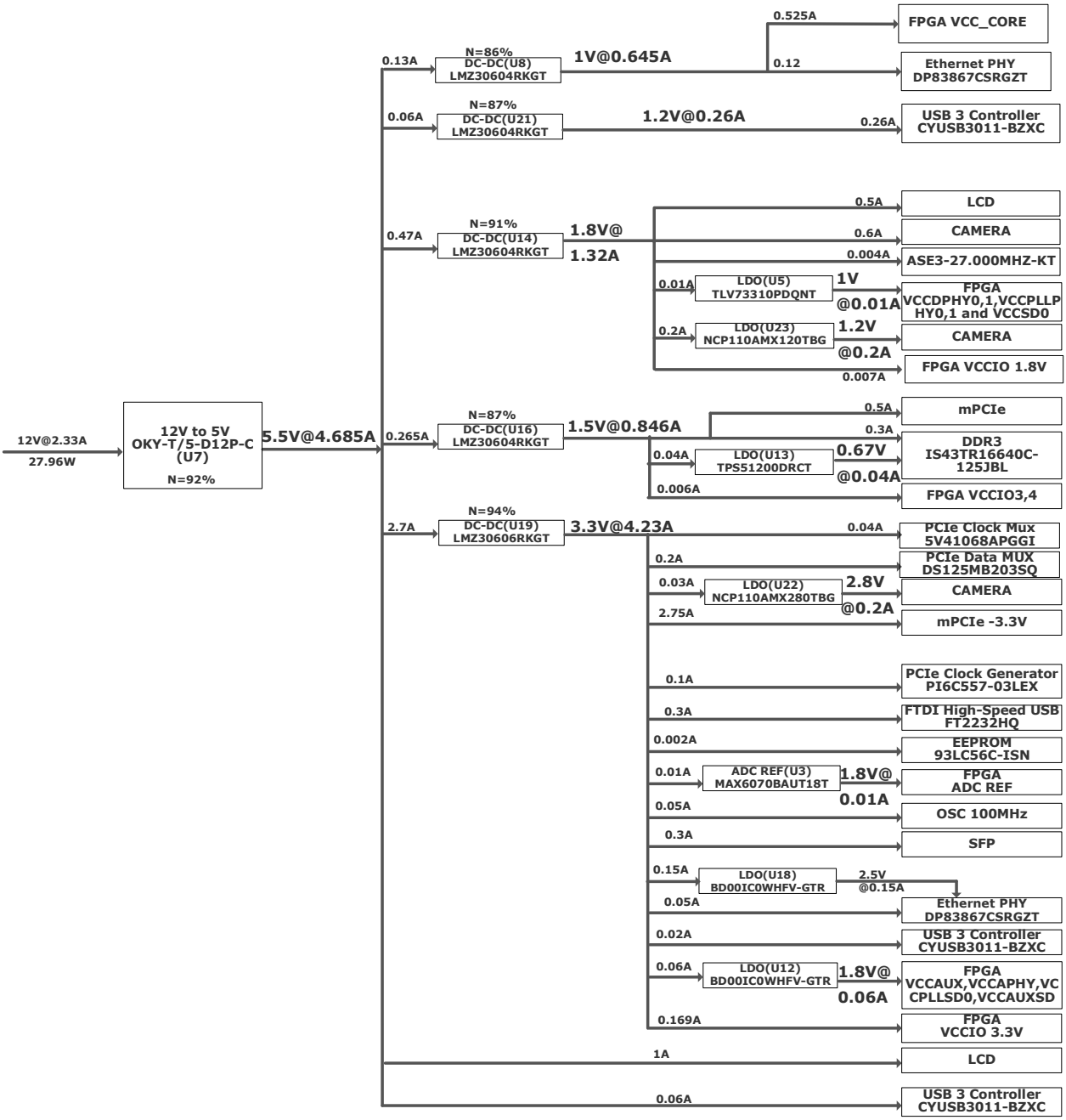

Figure 10.1. Power Diagram

Table 10.1. CrossLink-NX VCCIO Supply

VCCIO Bank	3V3_OUT	1V8_OUT	1V5_DDR
VCCIO0	Fixed	N/A	N/A
VCCIO1	Fixed	N/A	N/A
VCCIO2	Fixed	N/A	N/A
VCCIO3	N/A	N/A	Fixed
VCCIO4	N/A	N/A	Fixed
VCCIO5	N/A	Fixed	N/A
VCCIO6	Fixed	N/A	N/A
VCCIO7	Fixed	N/A	N/A

11. Software Requirements

The following software versions are required to develop designs for the CrossLink-NX PCIe Bridge Board:

- Lattice Radiant Software 2.2 or later
- Lattice Radiant Programmer 2.2 or later

12. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the development board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

13. Ordering Information

Table 13.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EEUP)
CrossLink-NX PCIe Bridge Board	LIFCL-PCIEB-EVN	

Appendix A. CrossLink-NX PCIe Bridge Board Schematics

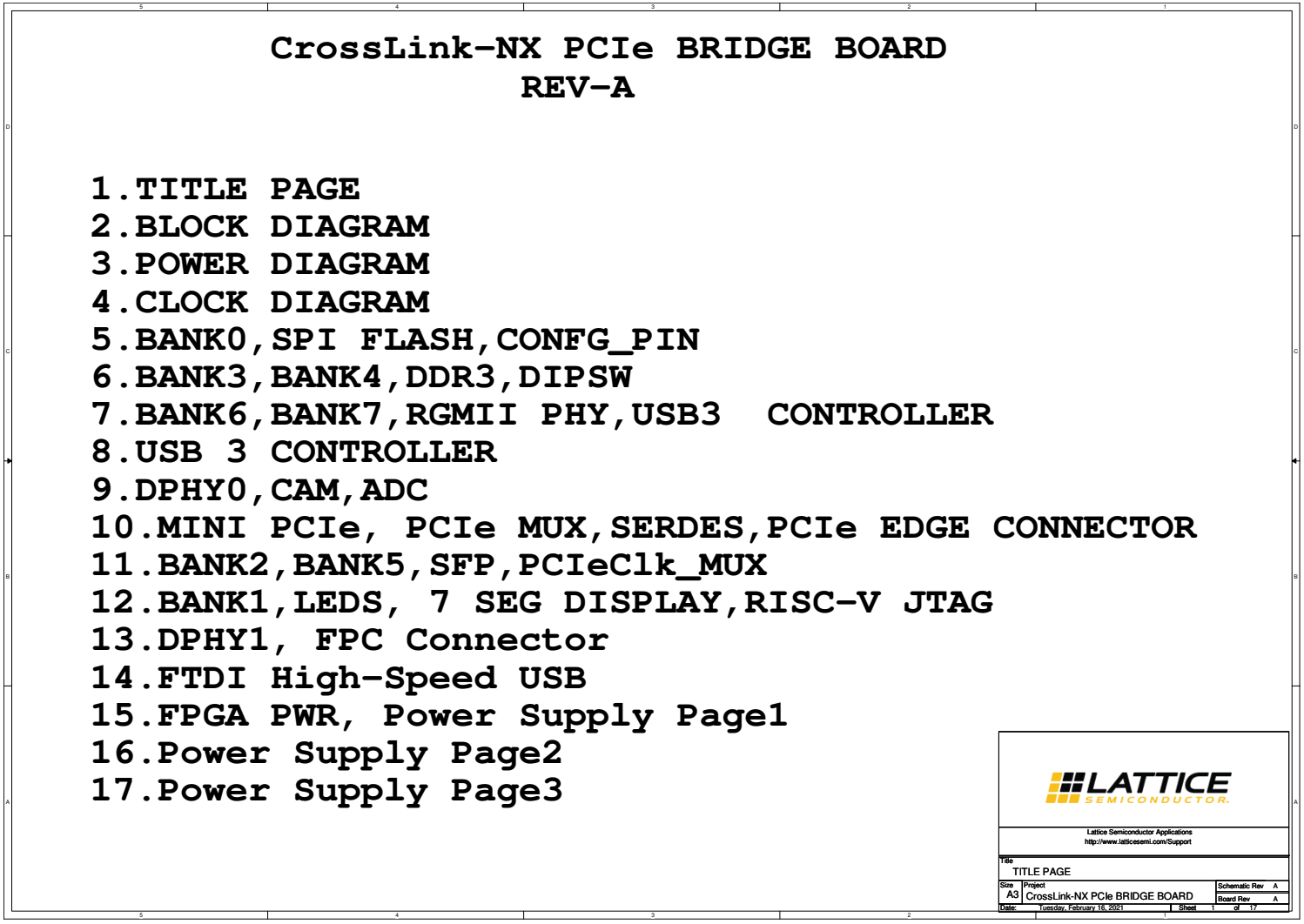

Figure A.1. Title Page

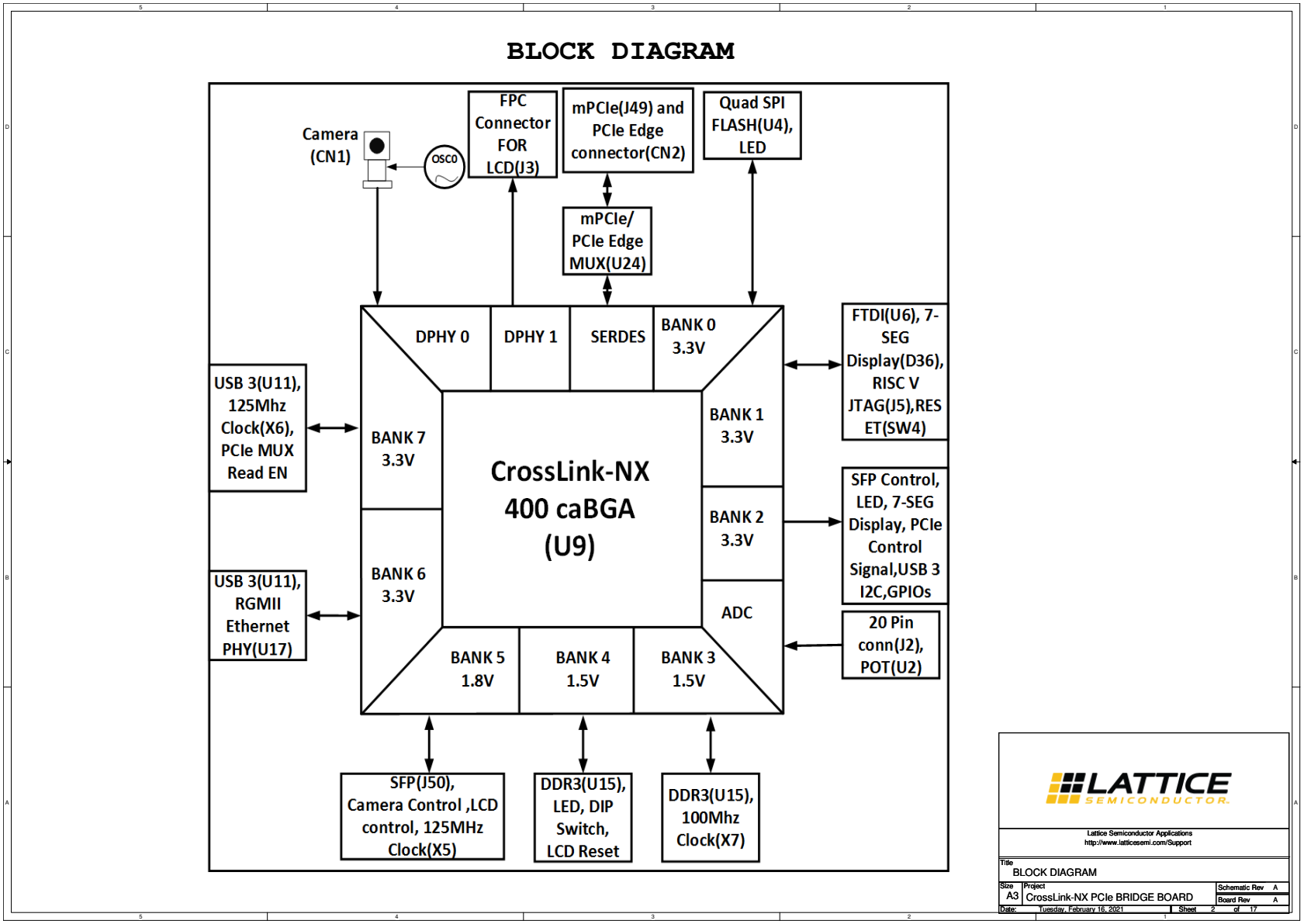

Figure A.2. Block Diagram

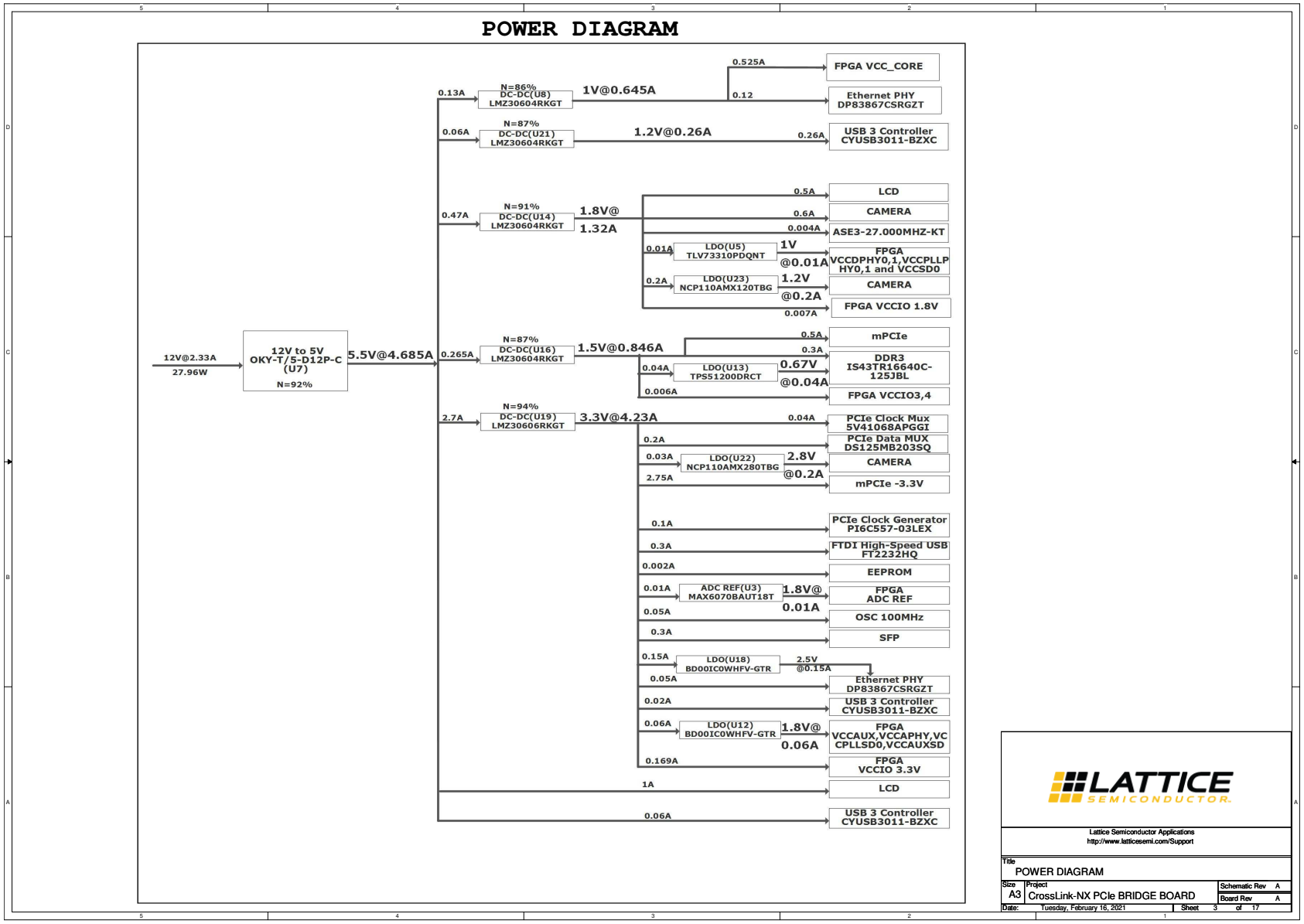

Figure A.3. Power Diagram

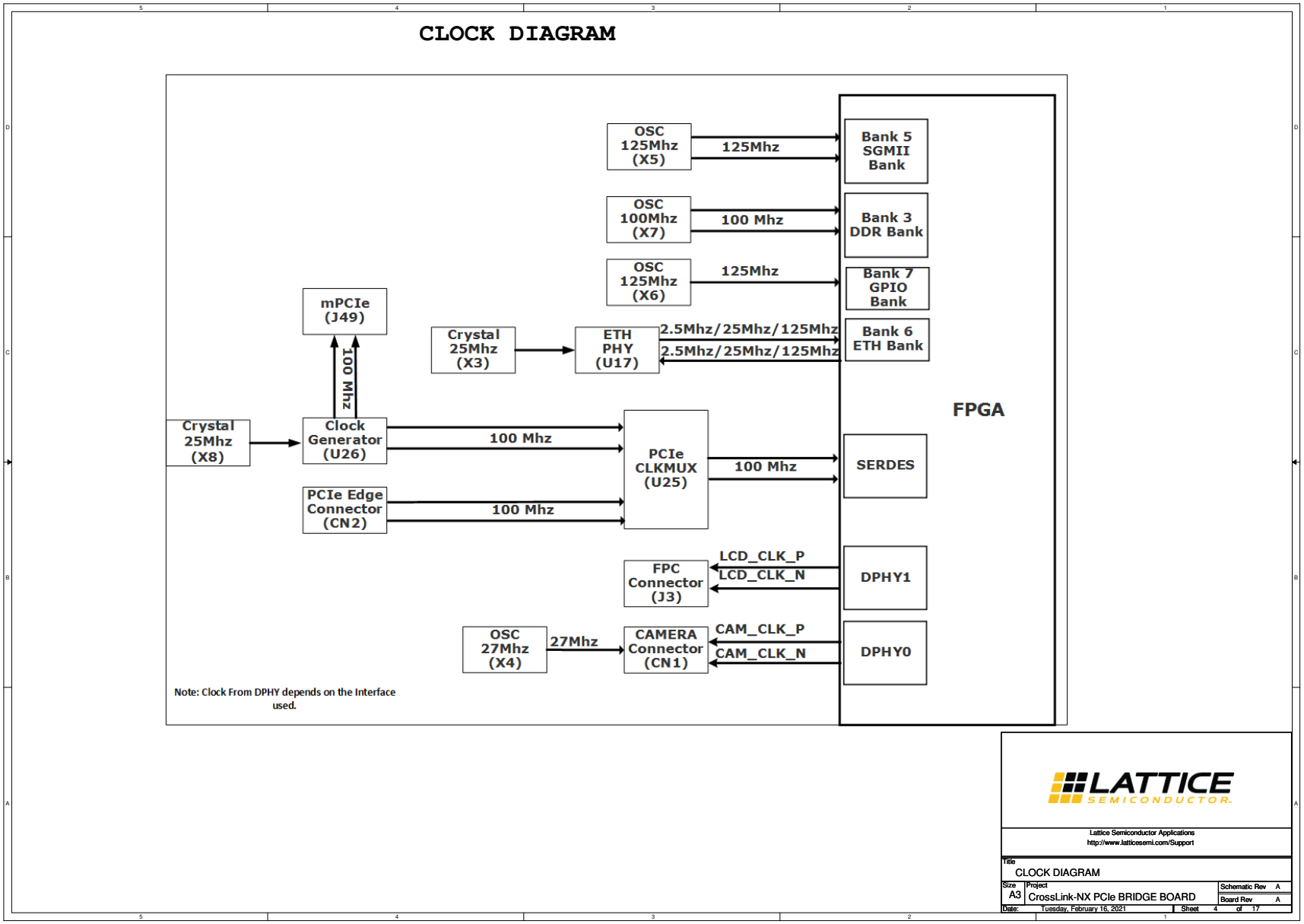

Figure A.4. Clock Diagram

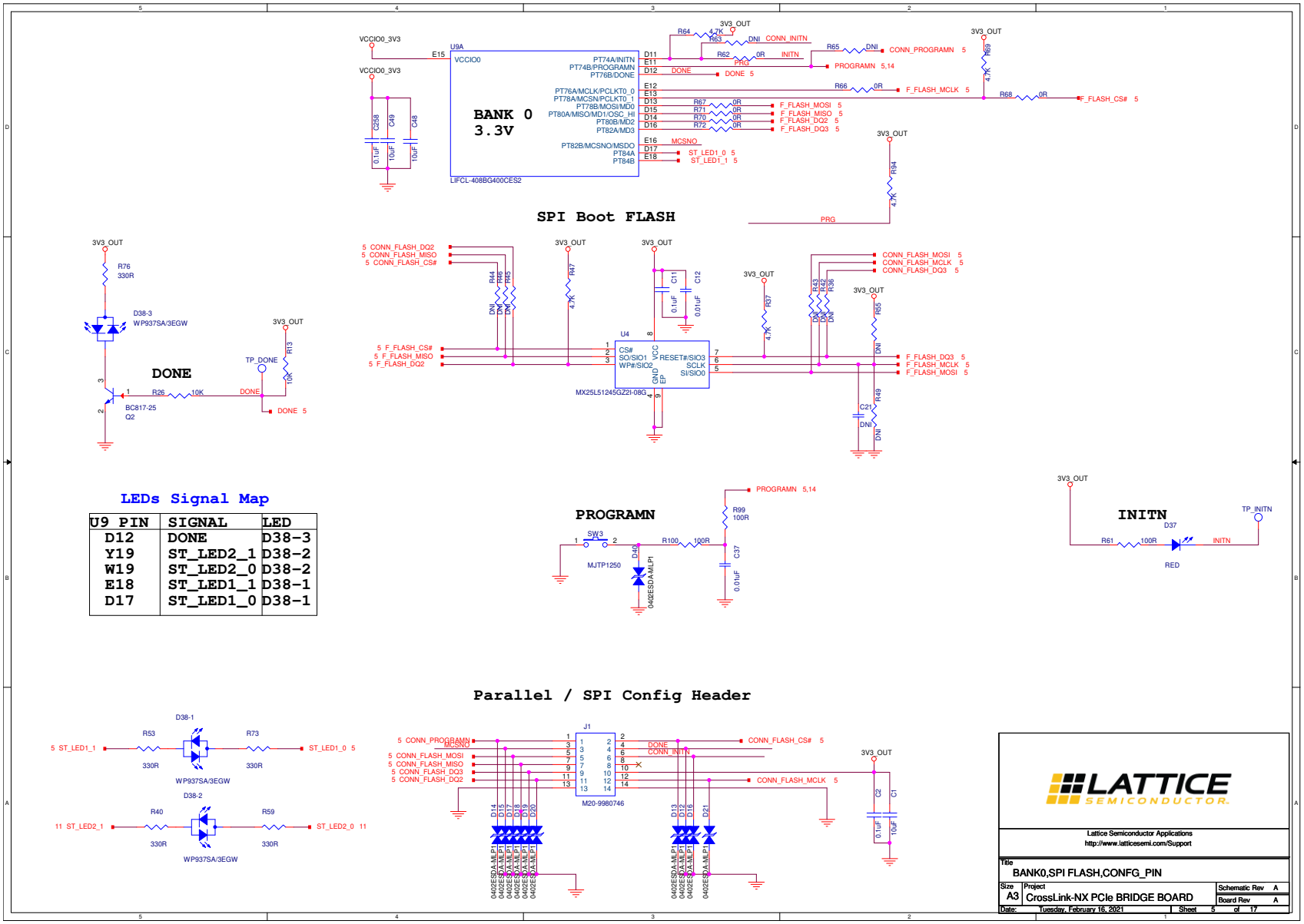

Figure A.5. BANK0, SPI FLASH, CONFG_PIN

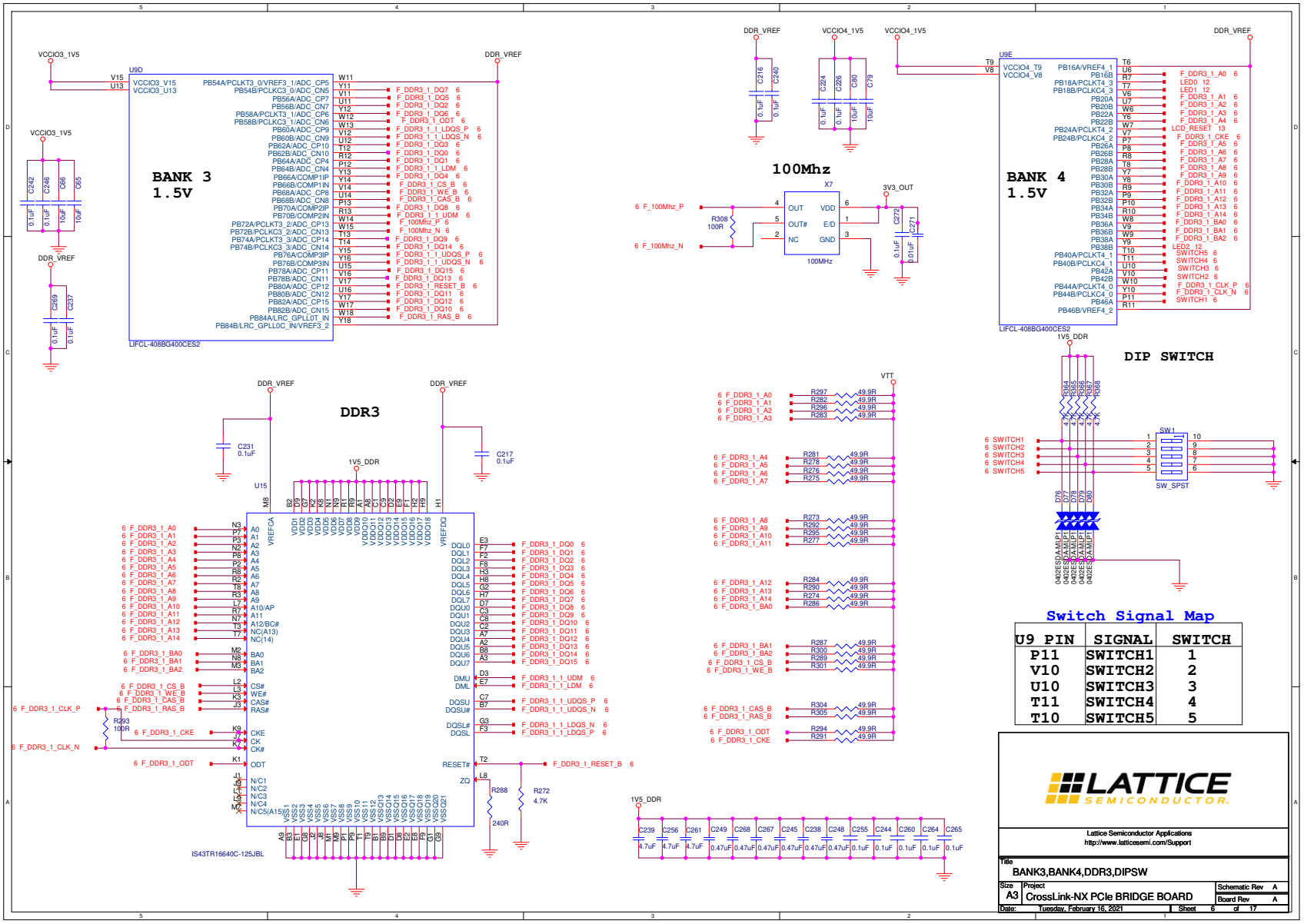

Figure A.6. BANK3, BANK4, DDR3, DIPSW

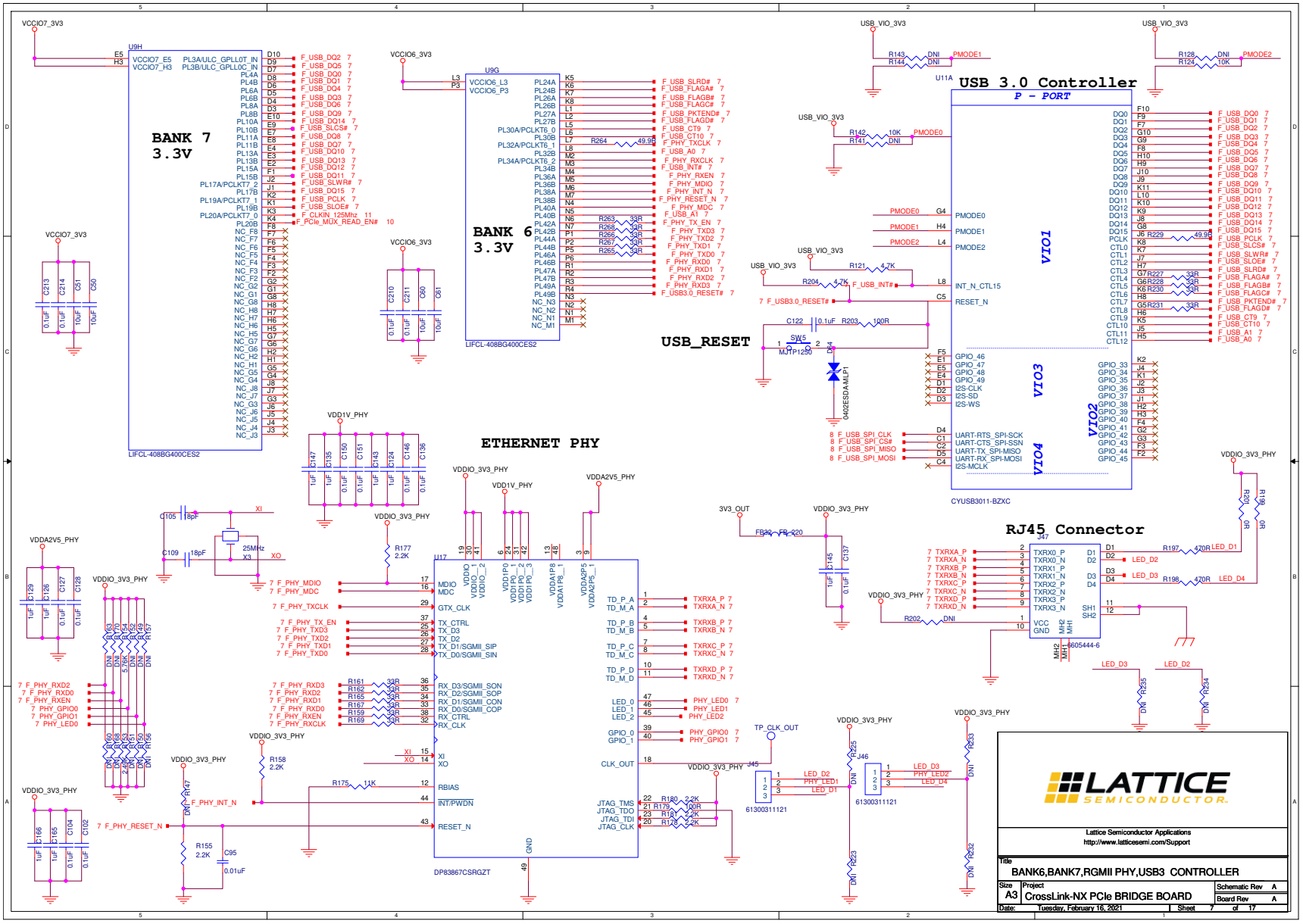

Figure A.7. BANK6, BANK7, RGMII PHY, USB3 CONTROLLER

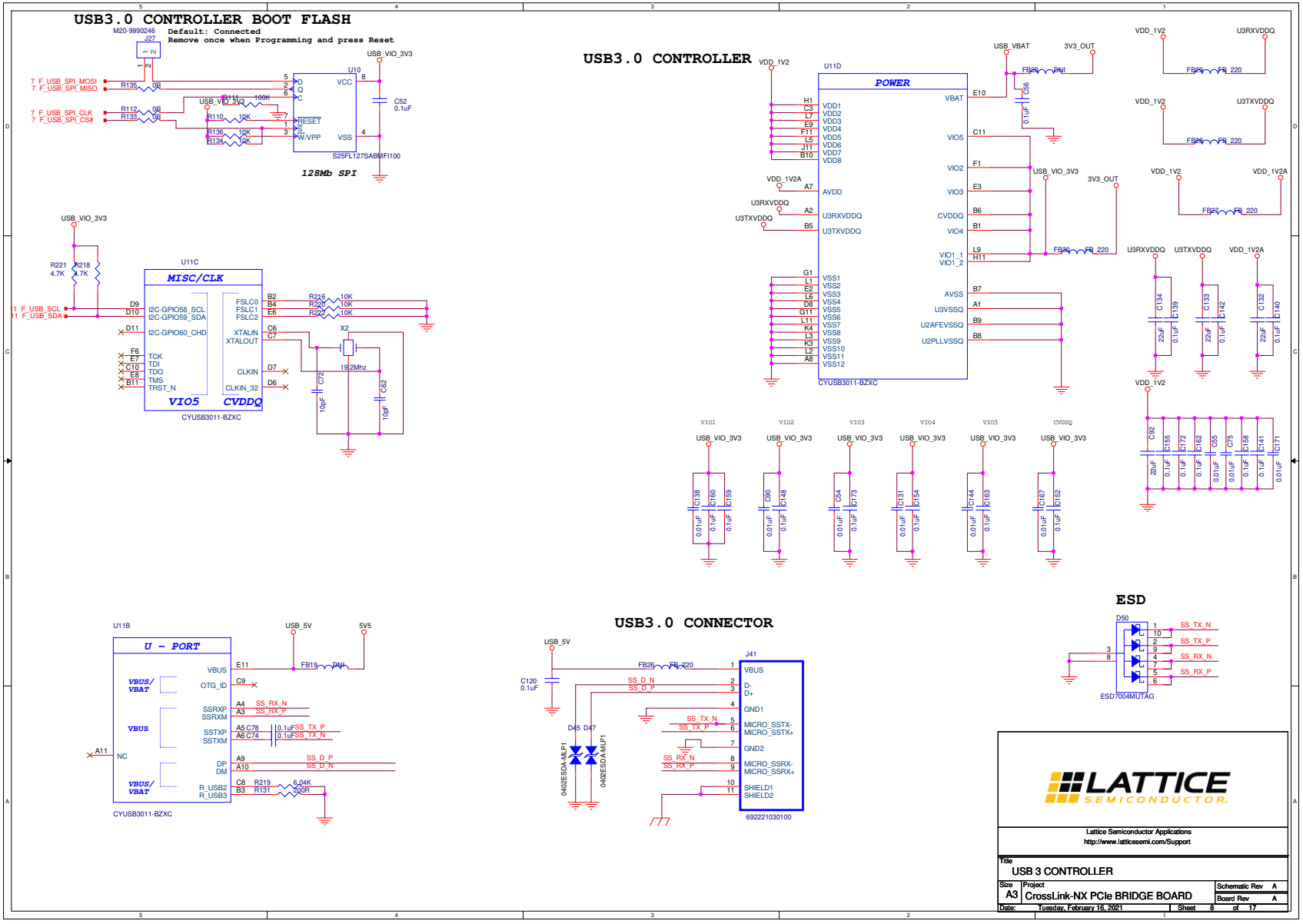

Figure A.8. USB 3 CONTROLLER

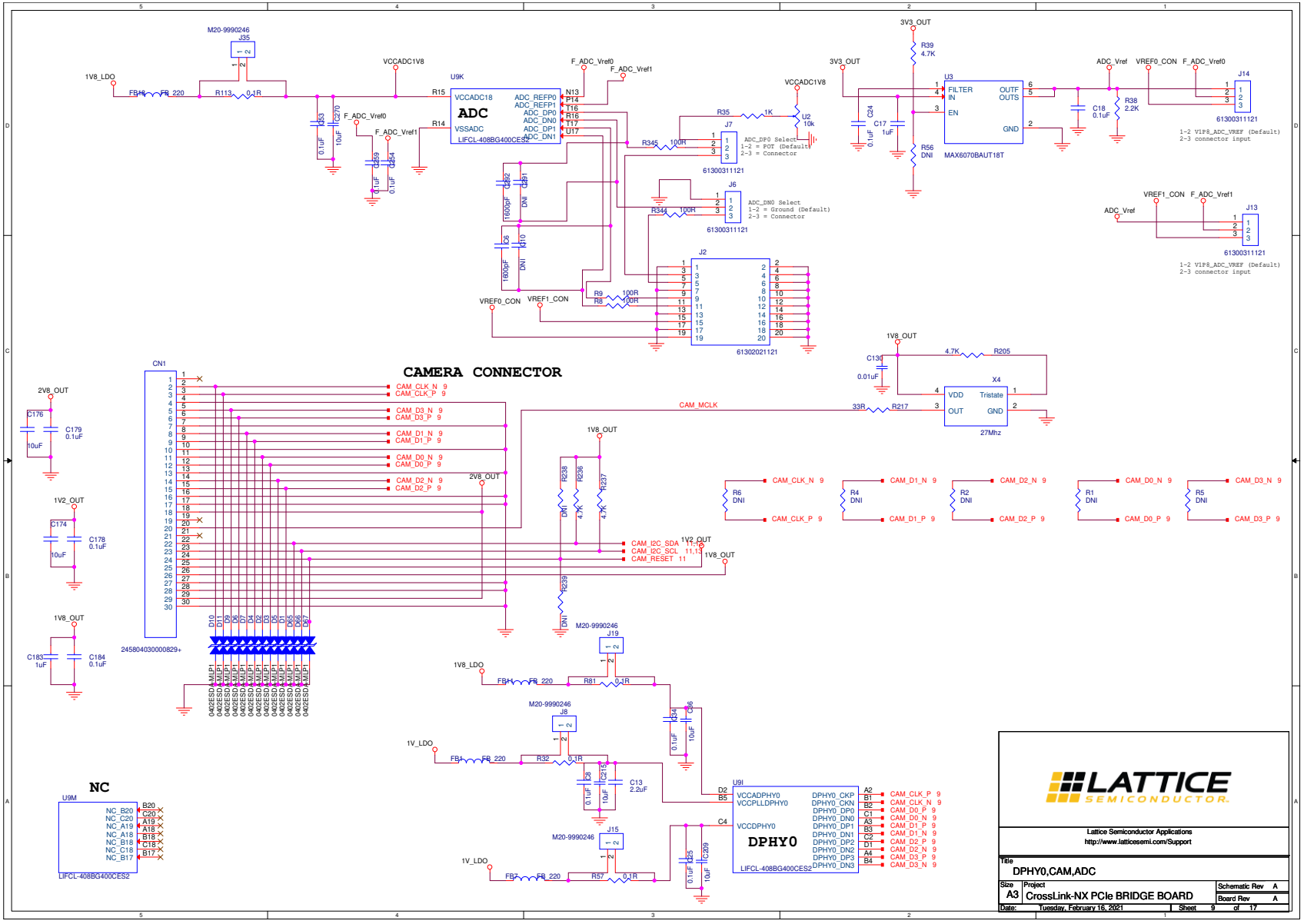

Figure A.9. DPHY0, CAM, ADC

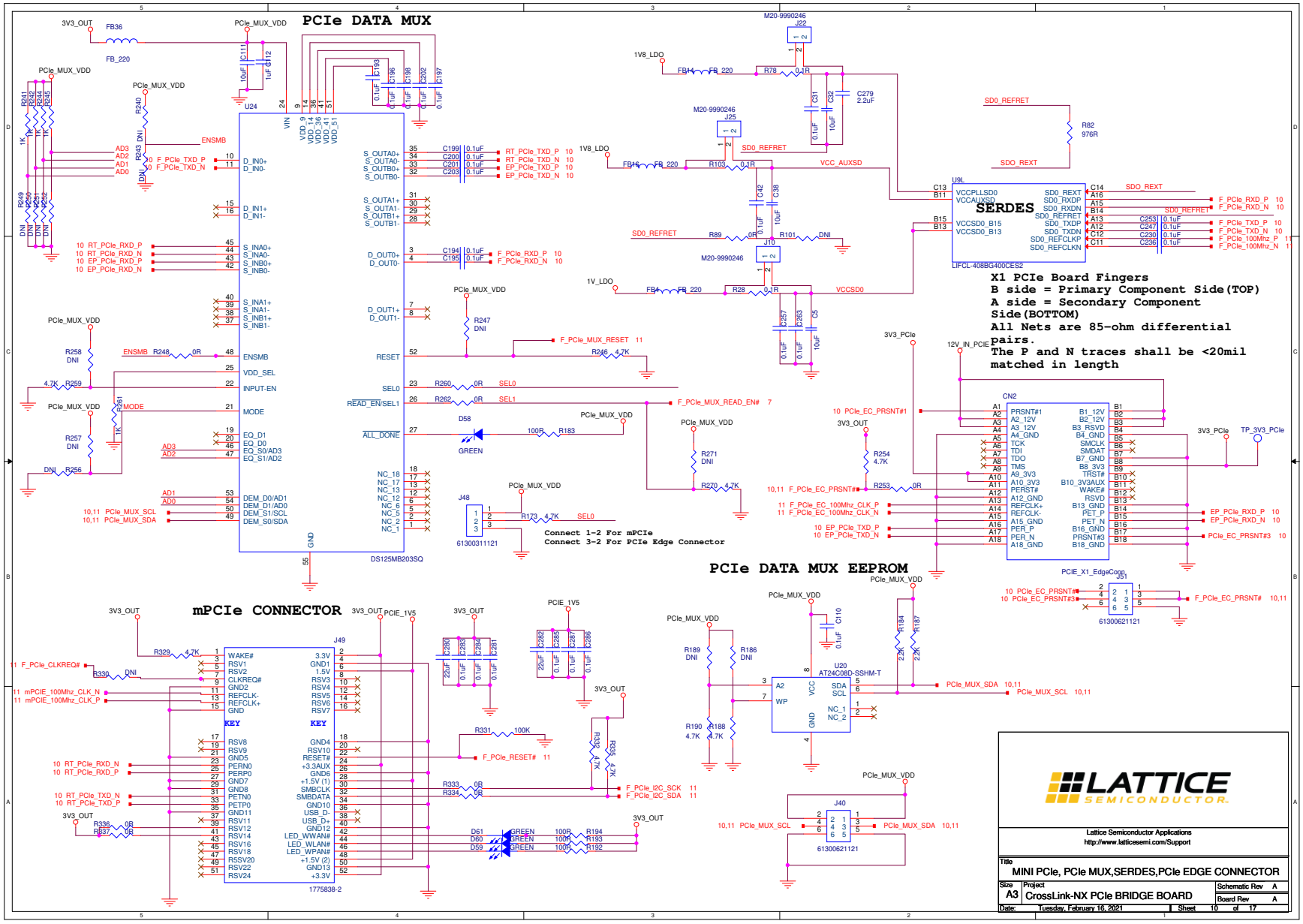

Figure A.10. MINI PCIe, PCIe MUX, SERDES, PCIe EDGE CONNECTOR

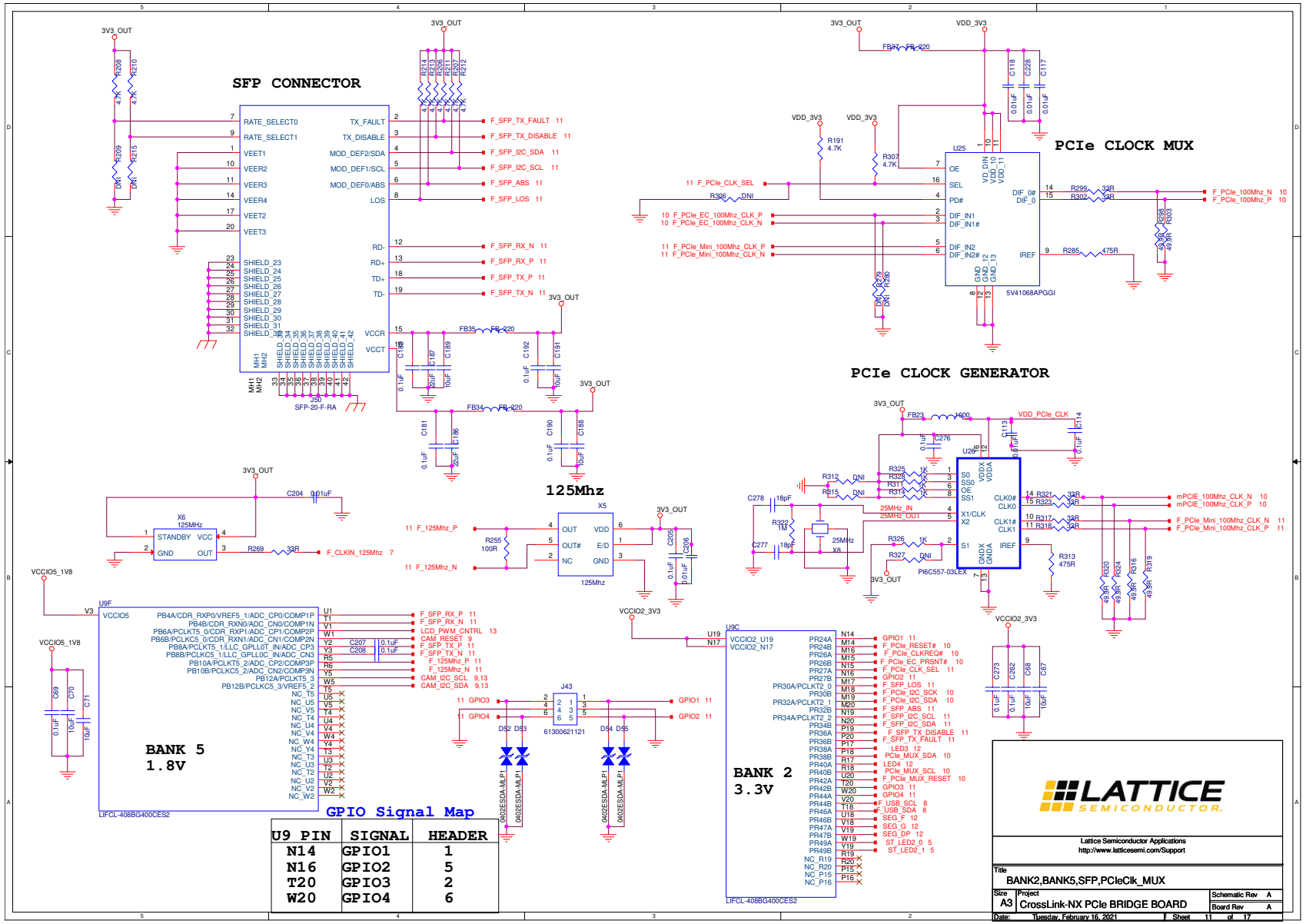

Figure A.11. BANK2, BANK5, SFP, PCIeClk_MUX

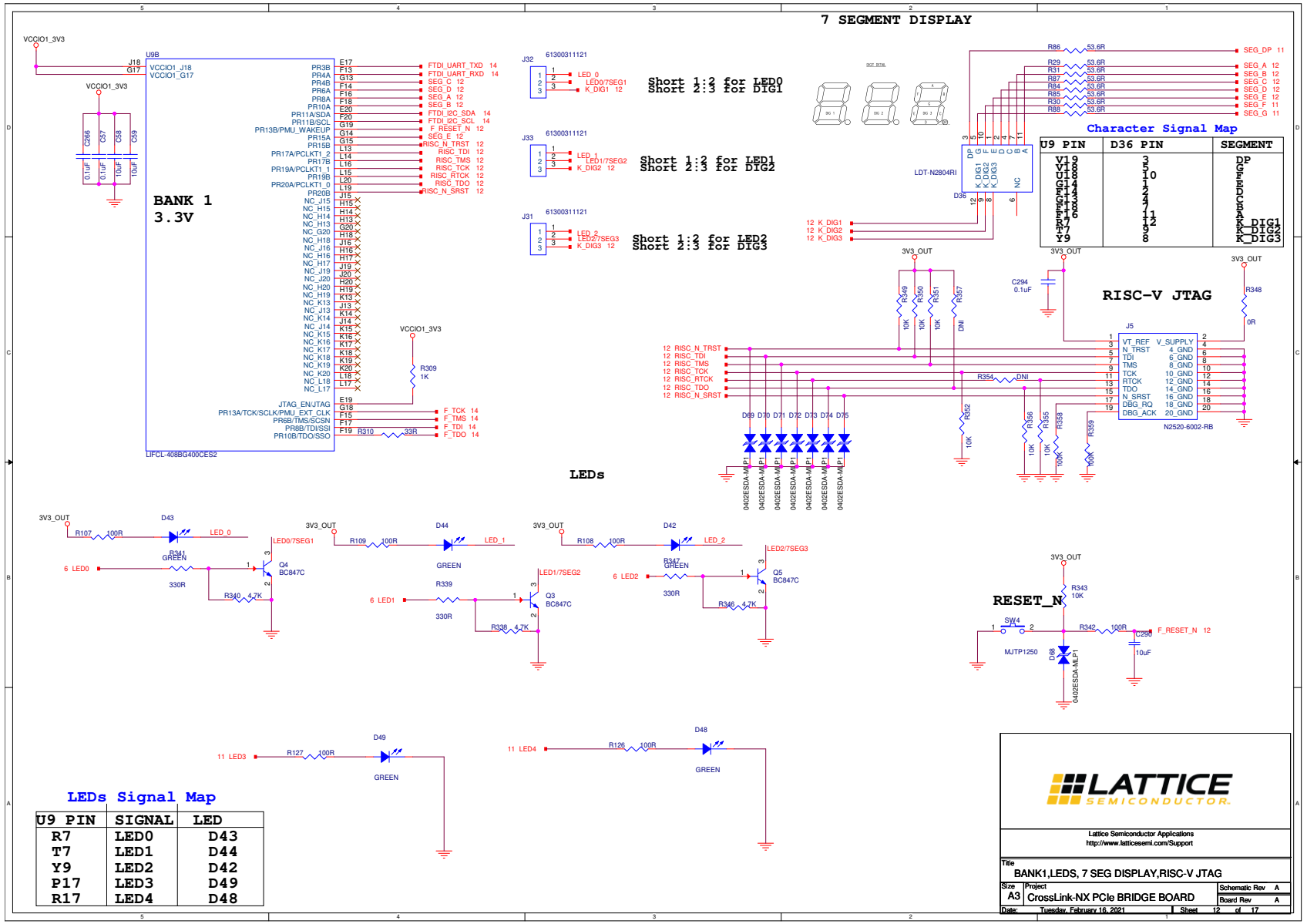

Figure A.12. BANK1, LEDS, 7 SEG DISPLAY, RISC-V JTAG

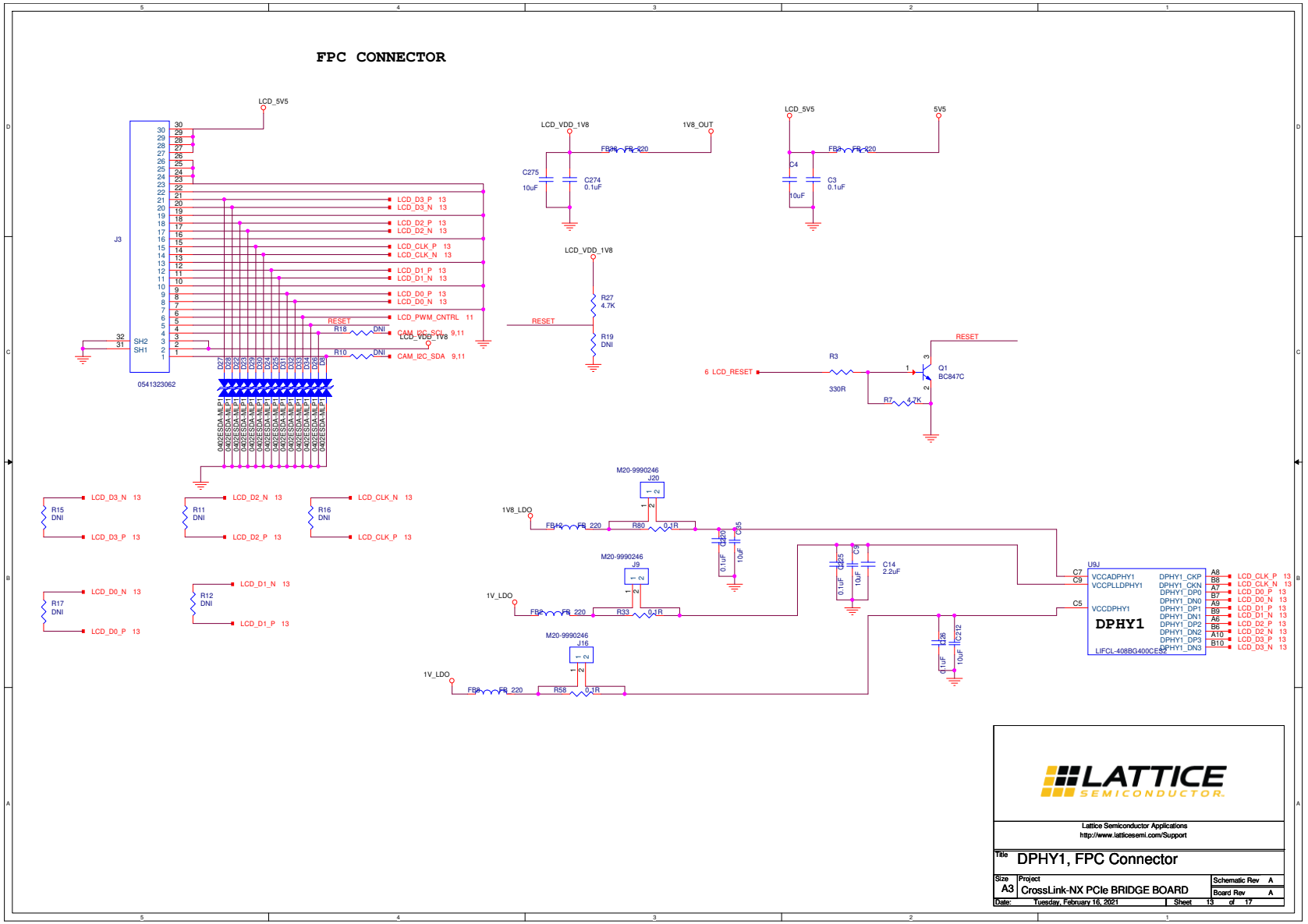

Figure A.13. DPHY1, FPC Connector

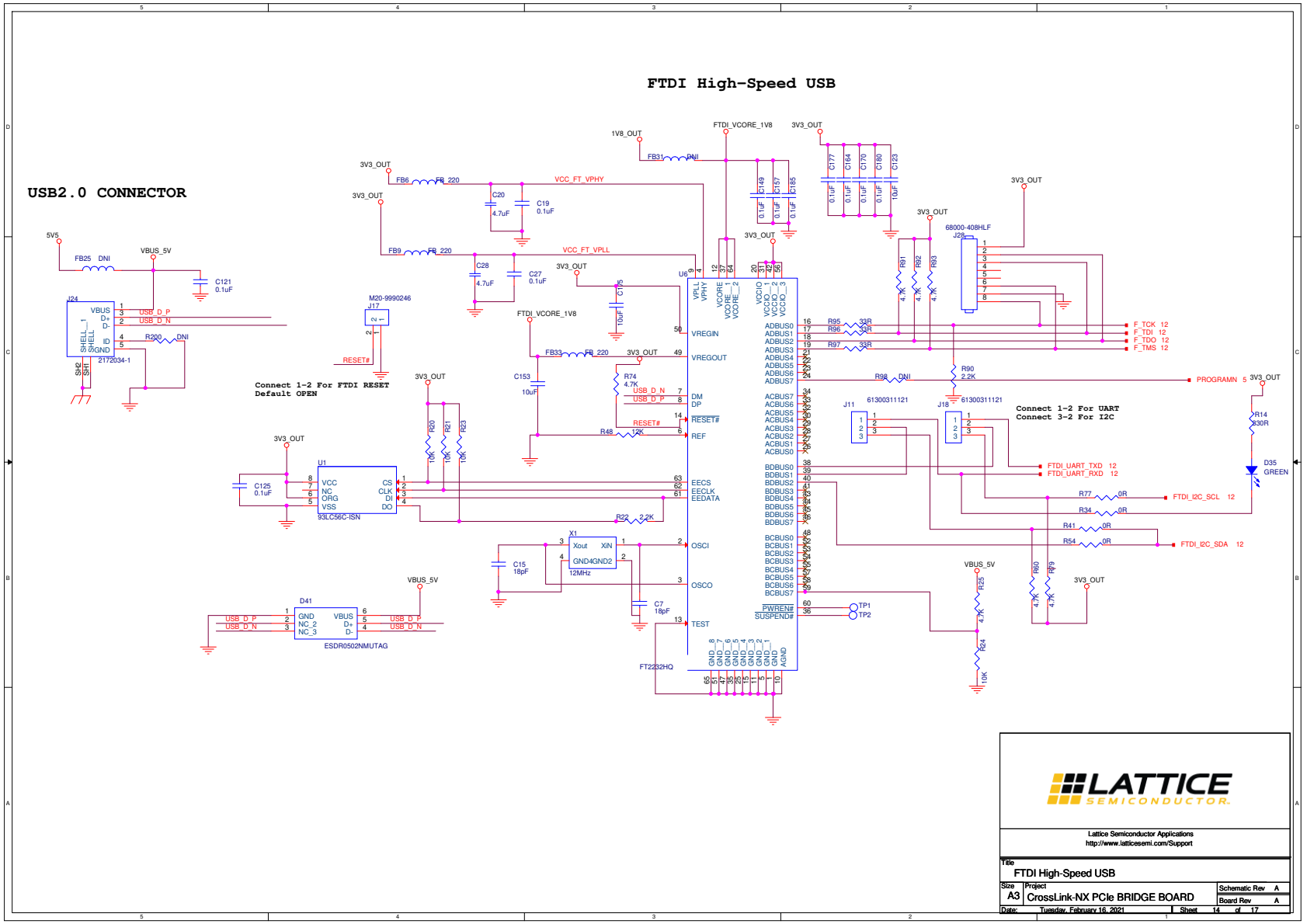

Figure A.14. FTDI High-Speed USB

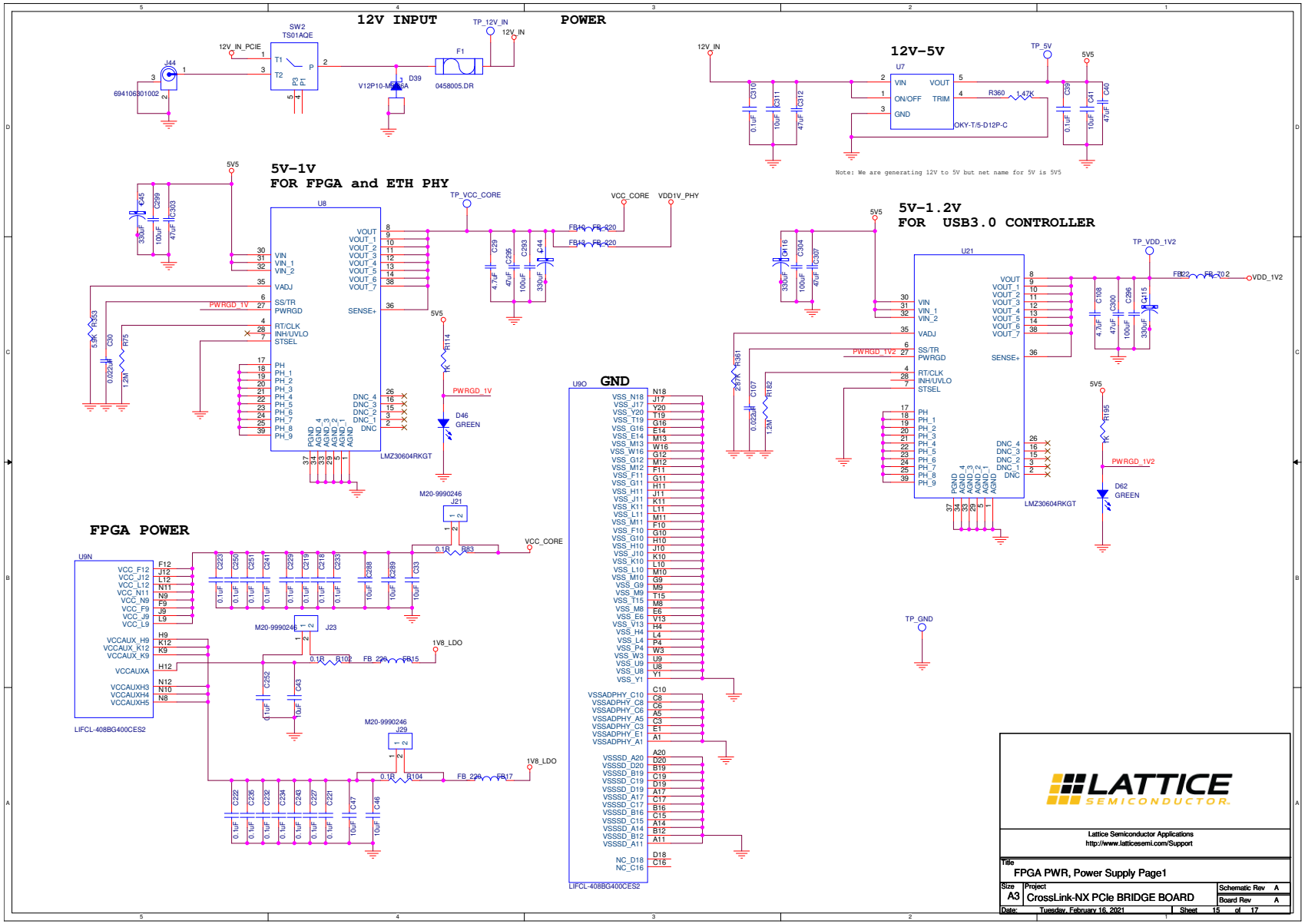

Figure A.15. FPGA PWR, Power Supply Page 1

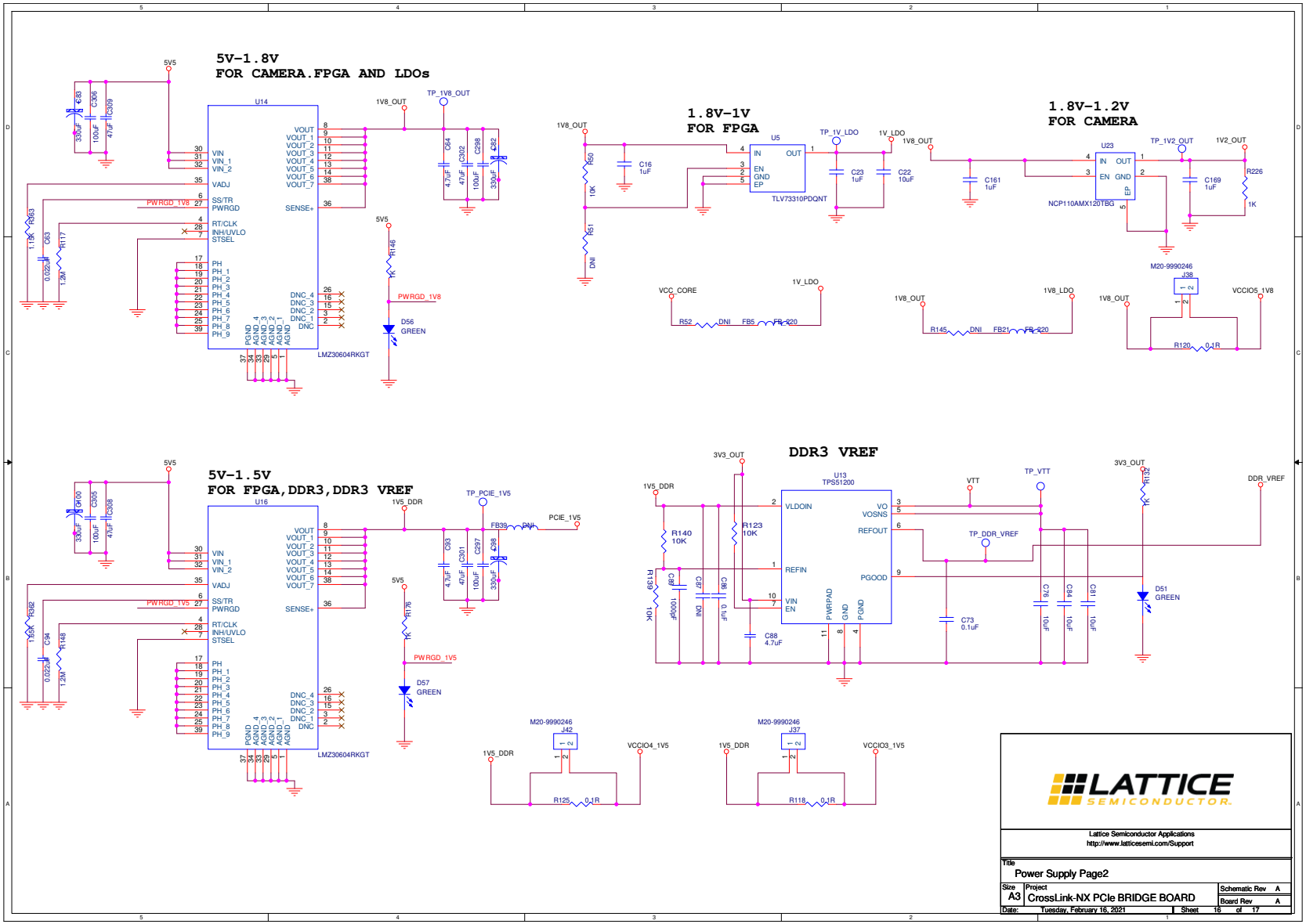

Figure A.16. Power Supply Page 2

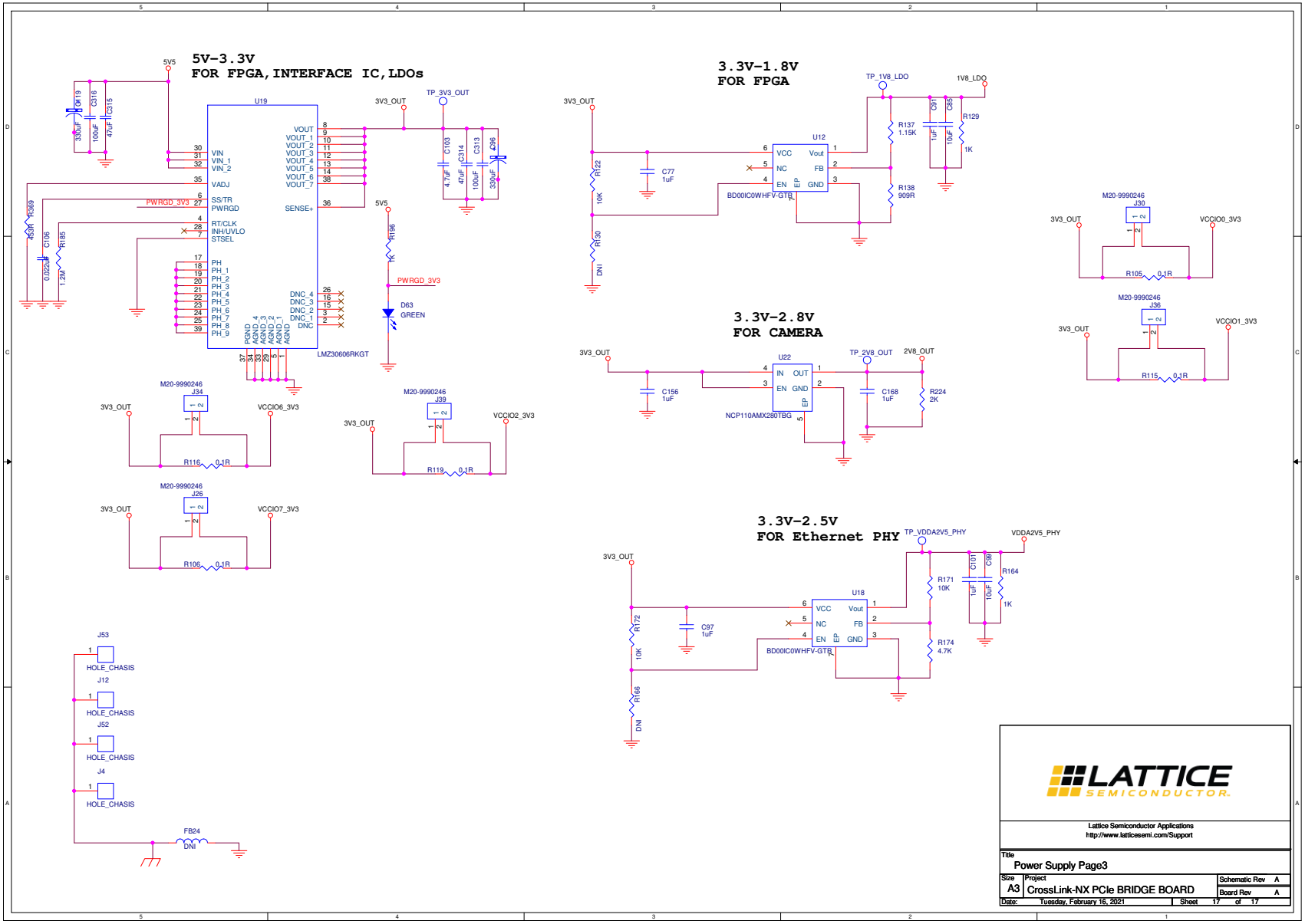

Figure A.17. Power Supply Page 3

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, July 2021

Section	Change Summary
All	Minor adjustments in formatting across the document.
Jumpers and Test Connection	Updated Figure 3.1 to correct J27 and J17 jumper locations.

Revision 1.0, April 2021

Section	Change Summary
All	First release.

www.latticesemi.com