# Parallel to MIPI with CrossLink-NX Devices

# Reference Design

FPGA-RD-02214-1.2

May 2024

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| CSI-2 | Camera Serial Interface 2 |
| DSI | Display Serial Interface |
| EBR | Embedded Block RAM |
| ECC | Error Correction Code |
| GPLL | General Purpose PLL |
| HS | High Speed |
| LP | Low Power |
| LUT | Look Up Table |
| MIPI | Mobile Industry Processor Interface |
| PLL | Phase Locked Loop |
| P2B | Pixel2Byte |
| RX | Receiver |
| TX | Transmitter |

# Supported Device and IP

This reference design supports the following devices with IP versions.

| Device Family | Part Number | Compatible IP |
|---|---|---|
| CrossLink-NX | LIFCL-40<br>LIFCL-17 | Pixel-to-Byte Converter IP version 1.4.0<br>D-PHY Transmitter IP version 1.7.2 |

The IPs above are supported by Lattice Radiant™ software version 2022.1 or later.

# 1. Introduction

The Mobile Industry Processor Interface (MIPI®) D-PHY was developed primarily to support camera and display interconnections in mobile devices, and it has become the industry's primary high-speed PHY solution for these applications in smartphones. It is typically used in conjunction with MIPI Camera Serial Interface-2 (CSI-2) and MIPI Display Serial Interface (DSI) protocol specifications. It meets the demanding requirements of low power, low noise generation, and high noise immunity that mobile phone designs demand.

MIPI D-PHY is a practical PHY for typical camera and display applications. It is designed to replace traditional parallel bus based on LVCMOS or LVDS. However, many processors and displays/cameras still use RGB, CMOS, or MIPI Display Pixel Interface (DPI) as interface.

The Parallel to MIPI reference design allows the quick interface for a processor with an RGB interface to a display with a MIPI DSI interface or a camera with a CMOS interface to a processor with CSI-2 interface. The Lattice Semiconductor Parallel to MIPI D-PHY Interface reference design provides this conversion for Lattice Semiconductor CrossLink™-NX devices. This is useful for wearable, tablet, human machine interfacing, medical equipment and many other applications.

## 1.1. Features List

The key features of the Parallel to MIPI Reference Design are:

- Compliant with MIPI D-PHY v1.2, MIPI DSI v1.2, and MIPI CSI-2 v1.2 Specifications
- Supports MIPI DSI and MIPI CSI-2 interfacing up to 6 Gb/s for Soft D-PHY and up to 10 Gb/s for Hard D-PHY
- Supports 1, 2, or 4 MIPI D-PHY data lanes
- Supports non-burst mode with sync events for transmission of DSI packets only
- Supports low-power (LP) mode during vertical and horizontal blanking
- Supports common MIPI DSI compatible video formats (RGB888, RGB666)
- Supports common MIPI CSI-2 compatible video formats (RGB888, RAW8, RAW10, RAW12)

## 1.2. Block Diagram

Figure 1.1 shows the block level diagram of the Parallel to MIPI Reference Design.

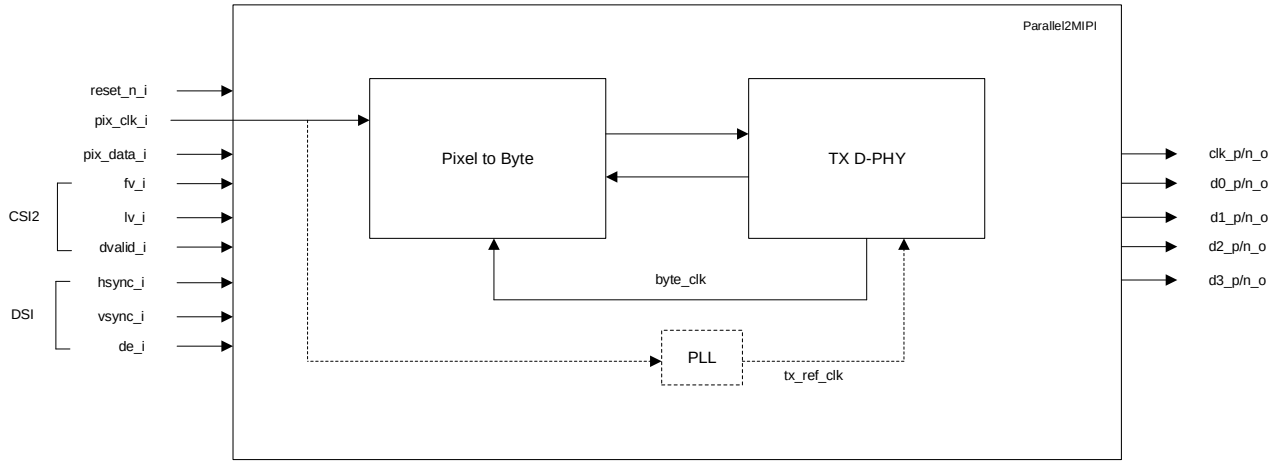


**Figure 1.1. Parallel to MIPI Reference Design Block Diagram**

As shown in the Figure 1.1, the block level diagram of the Parallel to MIPI reference design mainly consists of the Pixel to Byte and TX D-PHY IPs. Since TX D-PHY PLL has an input clock frequency requirement of between 24 MHz and 200 MHz, another on-chip GPLL may have to be used to create an appropriate clock.

## 1.3. Functional Description

The Parallel to MIPI D-PHY Reference Design converts a standard parallel video interface into either DSI or CSI-2 byte packets. The input interface for the design consists of a pixel bus (RGB888, RGB666), vertical and horizontal sync flags, a data enable and a clock for DSI and pixel bus (RGB888, RAW8, RAW10, and RAW12), frame and line valid flags and a clock for CSI-2.

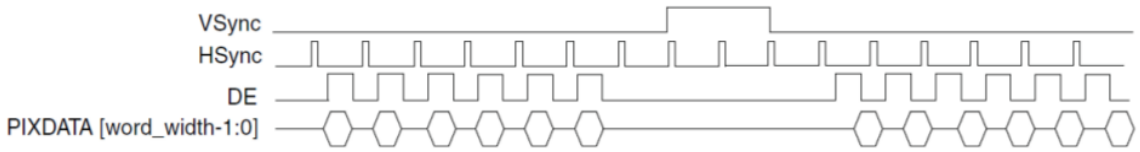


**Figure 1.2. Display Parallel Input Bus Waveform**

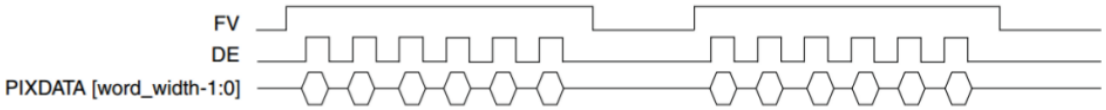


**Figure 1.3. Camera Sensor Parallel Input Bus Waveform**

This parallel bus in Figure 1.2 and Figure 1.3 is converted to the appropriate DSI or CSI-2 output format. The DSI/CSI-2 output serializes HS (High Speed) data and controls LP (Low Power) data and transfers them through MIPI D-PHY IP. MIPI D-PHY also has a maximum of 5 lanes per channel. It consists of one clock lane and up to 4 data lanes. The maximum D-PHY data rate per lane is 1.5 Gb/s by Soft D-PHY IP and 2.5 Gb/s by Hard D-PHY IP.

## 1.4. Conventions

### 1.4.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL. This includes radix indications and logical operators.

### 1.4.2. Data Ordering and Data Types

The highest bit within a data bus is the most significant bit. 8-bit parallel data is serialized to 1-bit data stream on each MIPI D-PHY data lane where bit 0 is the first transmitted bit.

Table 1.1 lists pixel data order coming from core module.

**Table 1.1. Pixel Data Order**

| Data Type | Format |
|---|---|
| RGB | {Red[MSB:0], Green[MSB:0], Blue[MSB:0]} |
| RAW | RAW[MSB:0] |

### 1.4.3. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
  Some signals are declared as bidirectional (I/O) but are only used as input. Hence, *_i* identifier is used.
- *_o* are output signals
  Some signals are declared as bidirectional (I/O) but are only used as output. Hence, *_o* identifier is used.
- *_io are bidirectional signals*

# 2. Parameters and Port List

There are two directive files for this reference design:

- synthesis_directives.v – used for design compilation by Lattice Radiant software and for simulation.
- simulation_directives.v – used for simulation.

Users can modify these directives according to their own configuration. The settings in these files must match Pixel to Byte and TX D-PHY IP settings created by Lattice Radiant.

## 2.1. Synthesis Directives

Table 2.1 shows the synthesis directives that affect this reference design. These are used for both synthesis and simulation. Some parameter selections are restricted by other parameter settings as shown in Table 2.1 and Table 2.2.

**Table 2.1. Synthesis Directives**

| Category | Directive | Remarks |
|---|---|---|
| D-PHY Type | TX_DSI | Only one of these two directives must be defined. Used for DSI or CSI-2 transmission. |
| | TX_CSI2 | |
| Video Data Type | RGB888 | Only one of these five directives must be defined. Type of video data to convert from pixel format to byte format for Pixel to Byte converter. |
| | RGB666 | |
| | RAW8 | |
| | RAW10 | |
| | RAW12 | |
| Number of TX Lane | NUM_TX_LANE_1 | Only one of these directives must be selected |
| | NUM_TX_LANE_2 | |
| | NUM_TX_LANE_4 | |
| Number of Pixels Per Pixel Clock | NUM_PIX_LANE_1 | Only one of these six directives must be defined. Number of pixels per pixel clock is used for the input to the Pixel to Byte converter. |
| | NUM_PIX_LANE_2 | |
| | NUM_PIX_LANE_4 | |
| | NUM_PIX_LANE_6 | |
| | NUM_PIX_LANE_8 | |
| | NUM_PIX_LANE_10 | |
| TX D-PHY Clock Gear | TX_GEAR_8 | TX D-PHY Clock Gear. Only one of these two directives must be defined. |
| | TX_GEAR_16 | |
| Miscellaneous | MISC_ON | Enables internal signals monitored by test-bench. Only one of these two directives must be defined. |
| | MISC_OFF | |
| Number of Pixels | NUM_PIXELS {value} | Number of active Pixels per Line |
| Clock Mode[1] | CLK_MODE_HS_ONLY | TX D-PHY Clock mode. Only one of these two directives must be defined. |
| | CLK_MODE_HS_LP | |
| PLL Mode | PLL_INTERNAL | Internal PLL or External PLL to be used for TX D-PHY. Only one of these directives must be used. |
| | PLL_EXTERNAL | |
| D-PHY IP | DPHY_HARD | Hard and Soft configuration of D-PHY TX IP. Only one of these directives must be used. |
| | DPHY_SOFT | |

**Note**: HS_LP mode means *non-continuous clock mode* and HS_ONLY means *continuous clock mode* for the TX D-PHY.

## 2.2. Simulation Directives

Table 2.2 shows the simulation directives for this reference design.

**Table 2.2. Simulation Directives**

| Category | Directive | Remarks |
|---|---|---|
| Pixel clock period | PIX_CLK {value} | Pixel clock period in ns |
| Number of video frames | NUM_FRAMES {value} | Number of video frames to be transmitted |
| Number of lines per frame | NUM_LINES {value} | Number of active lines per frame |
| Horizontal Front Porch | HFRONT {value} | Number of blanking cycles before HSYNC signal is asserted |
| Number of cycles HSYNC signal asserted | HPULSE {value} | Number of cycles for which HSYNC signal is asserted |
| Horizontal Back Porch | HBACK {value} | Number of blanking cycles after HSYNC signal is de-asserted |
| Vertical Front Porch | VFRONT {value} | Number of blanking lines before VSYNC signal is asserted |
| Number of lines VSYNC signal asserted | VPULSE {value} | Number of lines for which VSYNC signal is asserted |
| Vertical Back Porch | VBACK {value} | Number of blanking lines after VSYNC signal is de-asserted |

## 2.3. Top-Level I/O

Table 2.3 shows the top level I/O of this reference design. Actual I/O depends on the customer's configurations. All necessary I/O ports are automatically declared by compiler directives.

**Table 2.3. Parallel to MIPI Top Level I/O**

| Port Name | Direction | Description |
|---|---|---|
| **Clocks and Resets** | | |
| pix_clk_i | I | Input pixel/reference clock. Period of pixel clock is defined in simulation_directives.v |
| reset_n_i | I | Asynchronous active low system reset |
| **DSI Input Interface** | | |
| vsync_i[1] | I | Input vertical sync for parallel interface |
| hsync_i[1] | I | Input horizontal sync for parallel interface |
| de_i[1] | I | Input data enable for parallel interface |
| **CSI-2 Input Interface** | | |
| fv_i[2] | I | Input frame valid for parallel interface |
| lv_i[2] | I | Input line valid sync for parallel interface |
| dvalid_i[2] | I | Input data enable for parallel interface |
| **Input Data** | | |
| pixdata_i | I | Input pixel data. Data Bus width depends on the data type selected and Number of pixels per clock.<br>RGB888 : 24-bit bus width * Number of Pixel per clock<br>RGB666[1] : 18-bit bus width * Number of Pixel per clock<br>RAW12[2] : 12-bit bus width * Number of Pixel per clock<br>RAW10[2] : 10-bit bus width * Number of Pixel per clock<br>RAW8[2] : 8-bit bus width * Number of Pixel per clock |
| **Debug Interface** | | |
| pll_lock_o[3] | O | D-PHY PLL lock signal |
| **TX Output Interface** | | |
| d_p_io[NUM_TX_LANE -1:0][4] | I/O | Positive differential TX D-PHY data lanes |
| d_n_io[NUM_TX_LANE -1:0][4] | I/O | Negative differential TX D-PHY data lanes |
| clk_p_io | I/O | Positive differential TX D-PHY clock lane |
| clk_n_io | I/O | Negative differential TX D-PHY clock lane |

**Notes**:

1. Available only if data interface is DSI.
2. Available only if data interface is CSI-2.
3. Turned-on if Enable miscellaneous status signals attribute is selected.
4. NUM_TX_LANE = Number of TX D-PHY Lanes : 1, 2, 4 (available on user interface).

# 3. Design and Module Description

The top-level design (parallel2mipi_NX.v) consists of the following modules:

- p2b
- tx_dphy
- int_pll

The top-level design has internal and external PLL support. Which may be used if PLL_EXTERNAL is defined according to TX D-PHY configuration.

Figure 3.1 shows the timing diagram for the D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface.

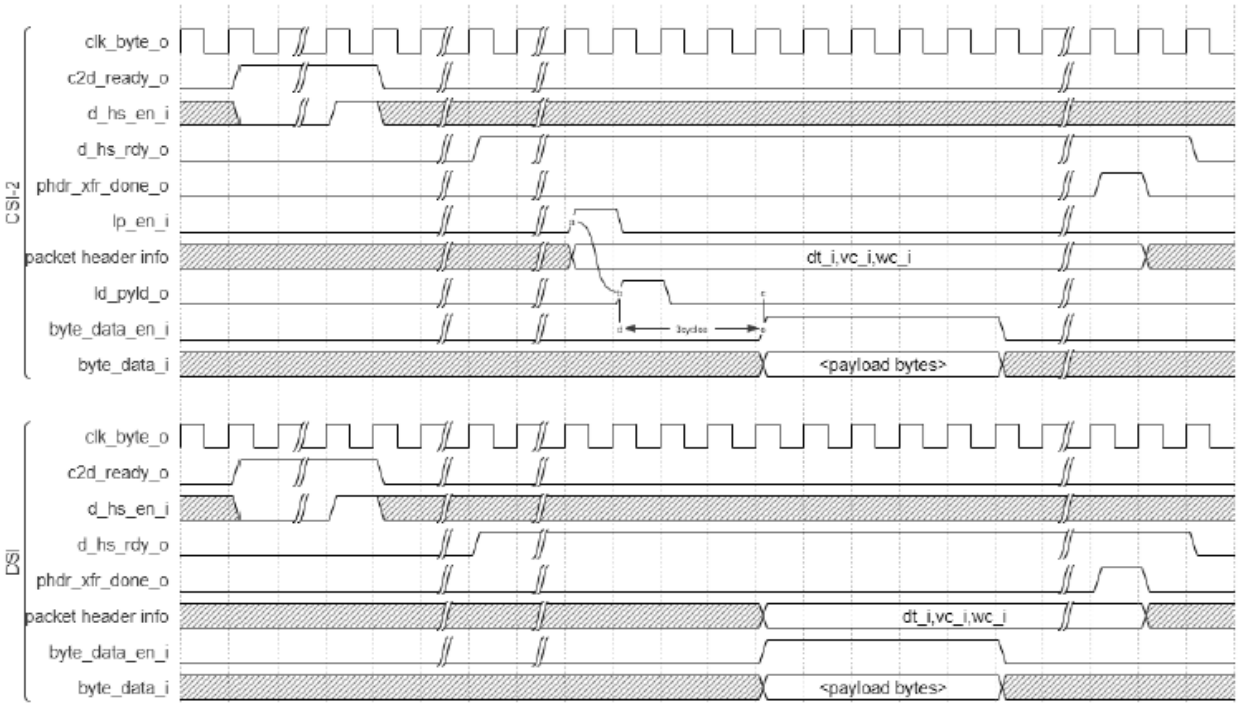


**Figure 3.1. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface**

When the protocol type selected is CSI-2, there is no internal buffer to save the incoming payload data before the creation of the header packet. Because of this, the D-PHY TX IP requires 3 cycles from the assertion of the ld_pyld_o to the arrival of the valid payload data. The ld_pyld_o asserts the next cycle after the detection of the lp_en_i. Hence little glue logic is added in the top-level design to take care of this timing requirement for the required signals for the D-PHY TX IP as shown in Figure 3.1.

## 3.1. p2b

This module must be created to convert Pixel data into Byte data output according to configurations, such as TX Interface, Data Type, number of TX Lanes, and others. Figure 3.2 shows an example of IP interface settings in Lattice Radiant for the Pixel to Byte Submodule IP. Refer to Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094) for details.

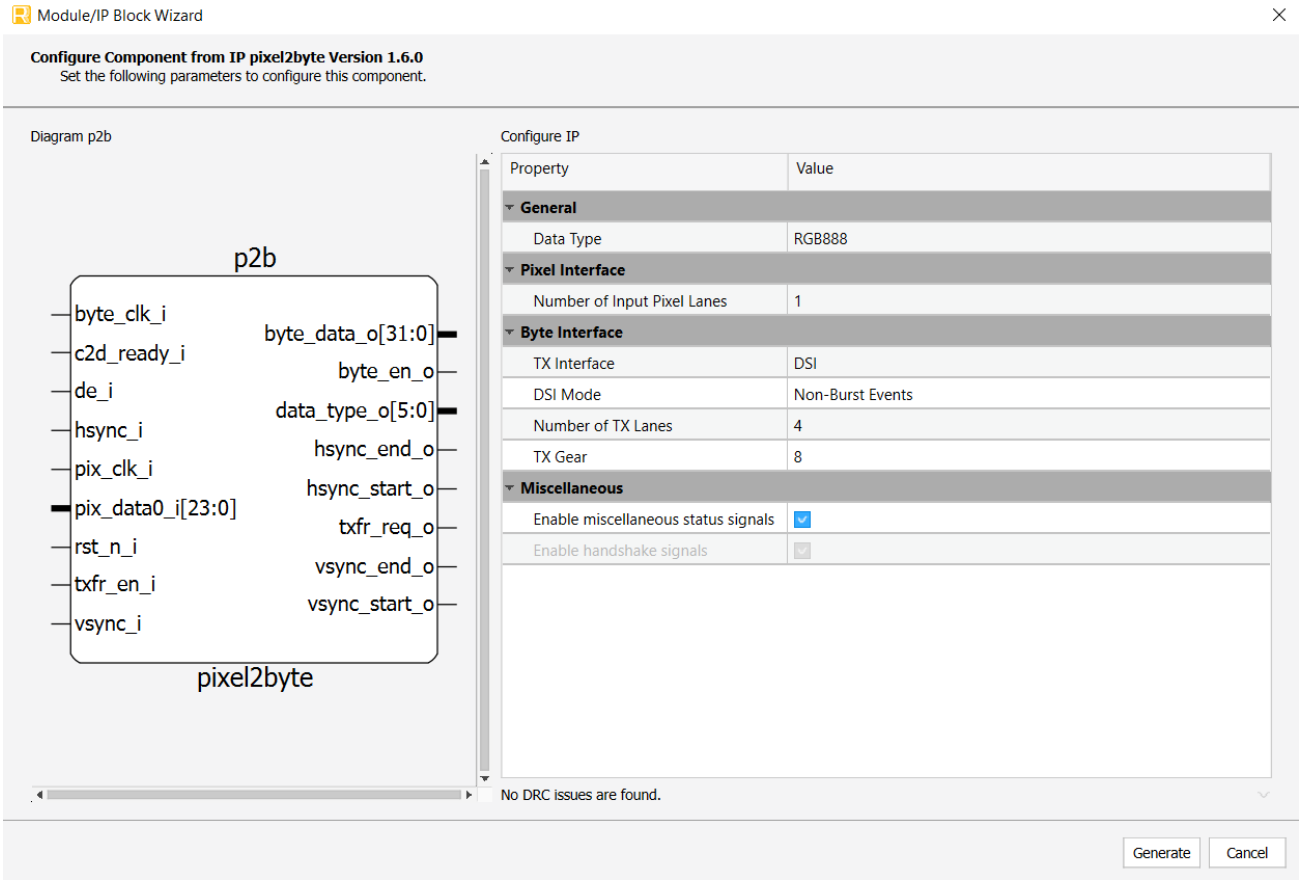


**Figure 3.2. p2b IP Creation in the Lattice Radiant Software**

The following shows the guidelines and parameter settings required for this reference design:

- TX Interface – Select DSI or CSI-2. Set the same type as TX D-PHY IP.
- Data Type – Select RGB888 or RGB666 for DSI and RGB888, RAW8, RAW10, or RAW12 for CSI-2. Others are not supported in this reference design.
- Number of TX Lanes – Select 1, 2, or 4. Set the same value as TX D-PHY IP.
- Number of Input Pixel Lanes – Select 1, 2, 4, 6, 8, and 10 for input Pixel per clock. Number of Input Pixel Per Clock 6, 8, and 10 are only supported for CSI-2, RAW10, and RAW12.
- TX Gear – Select 8 or 16 (set according to the configuration).
- Enable miscellaneous status signals – Select checkbox to enable (checked).

The Pixel-to-Byte Converter IP converts the standard pixel data format to the D-PHY CSI-2/DSI standard based byte data stream. The .ipx file included in the project (p2b/p2b.ipx) can be used to reconfigure the IP as per the user configuration requirements. If users are creating this IP from scratch, it is recommended to set the design name to *p2b* so that users do not need to modify the instance name of this IP in the top-level design as well as in the simulation setup file. Otherwise, users need to modify the names accordingly.

## 3.2. tx_dphy

You must create this module according to the channel conditions, such as number of lanes, bandwidth, and others. Figure 3.3 shows an example IP interface setting in Lattice Radiant for the CSI-2/DSI D-PHY Transmitter Submodule IP. Refer to CSI-2/DSI D-PHY Tx IP Core User Guide (FPGA-IPUG-02080) for details.

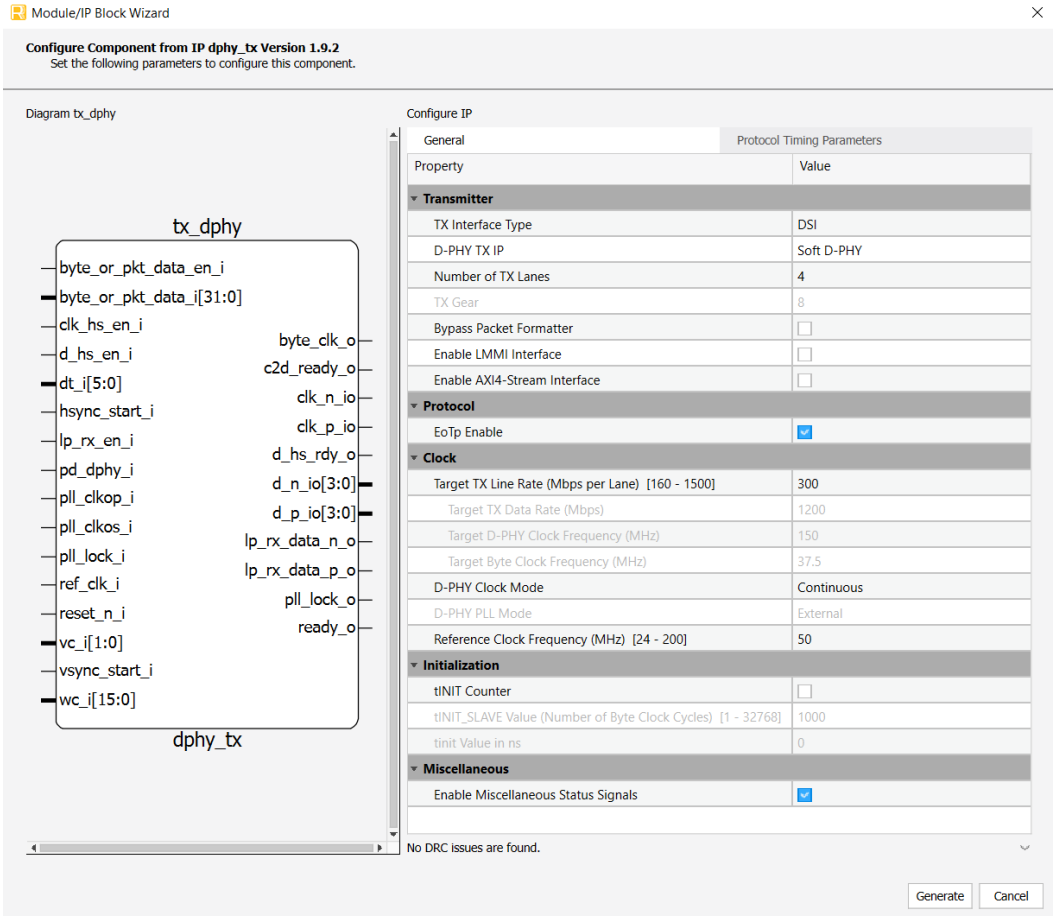


**Figure 3.3. tx_dphy IP Creation in the Lattice Radiant Software**

The following shows the guidelines and parameter settings required for this reference design:

- TX Interface Type – Select DSI or CSI-2 (set according to the required configuration).
- D-PHY TX IP – Select Soft D-PHY or Hard D-PHY (set according to the required configuration).
- Number of TX Lanes – Select 1, 2, or 4 (set according to the required configuration).
- TX Gear – Select 8 or 16 (set according to configuration). When the D-PHY TX IP is Soft D-PHY selected, then TX Gear is 8. TX Gear 8 is also automatically selected by Lattice Radiant when the lane bandwidth is less than 1500 Mbps, which means TX byte clock could be ~187.5 MHz.
- Interleaved Input Data – Select disabled (unchecked).
- CIL Bypass – Select checkbox to enable (checked).
- Bypass Packet Formatter – Select disabled (unchecked).
- Enable Frame Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2.
- Frame Number MAX Value Increment in Packet Formatter [1 - 255] – Numerical value between 1 to 255, only for CSI-2.
- Enable Line Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2.
- EoTp Enable – Select checkbox to enable (checked) EoTp insertion, only for DSI. This option is not mandatory.
- Enable LMMI Interface – Select disabled (unchecked).

- Enable AXI4-Stream Interface – Select disabled (unchecked).
- TX Line Rate per Lane (Mbps) [160 – 1500 (Soft D-PHY, 2500 (Hard D-PHY)] – Set according to the required configuration.
- D-PHY Clock Mode – Set according to the required configuration.
- D-PHY PLL Mode – Select Internal for Hard D-PHY IP (due to limitation of external PLL frequency) or Select External for Soft D-PHY IP.
- Reference Clock Frequency (MHz) [24 – 200] – Set the same value as pixel clock frequency.
- tINIT Counter – For Soft DPHY, select disabled (unchecked). For Hard DPHY, select enabled (checked). The value can be set to 100 bytes clock cycle.
- Enable Miscellaneous Status Signals – Select checkbox to enable (checked).
- Protocol Timing Parameters tab – Default values are recommended (Change timing values if required).

This module takes the byte data and outputs DSI/CSI-2 data after serialization in DSI/CSI-2 High Speed mode. The .ipx file included in the project (tx_dphy/tx_dphy.ipx) can be used to reconfigure the IP as per the user configuration requirements. If users are creating this IP from scratch, it is recommended to set the design name to *tx_dphy* so that users do not need to modify the instance name of this IP in the top-level design as well as simulation setup file. Otherwise, users need to modify the names accordingly.

## 3.3. int_pll

This module generates the required clkop for TX D-PHY module when Soft D-PHY IP is used. Figure 3.4 and Figure 3.5 show an example IP interface setting in Lattice Radiant for the PLL Submodule IP. Refer to PLL Module User Guide (FPGA-IPUG-02063) for details.

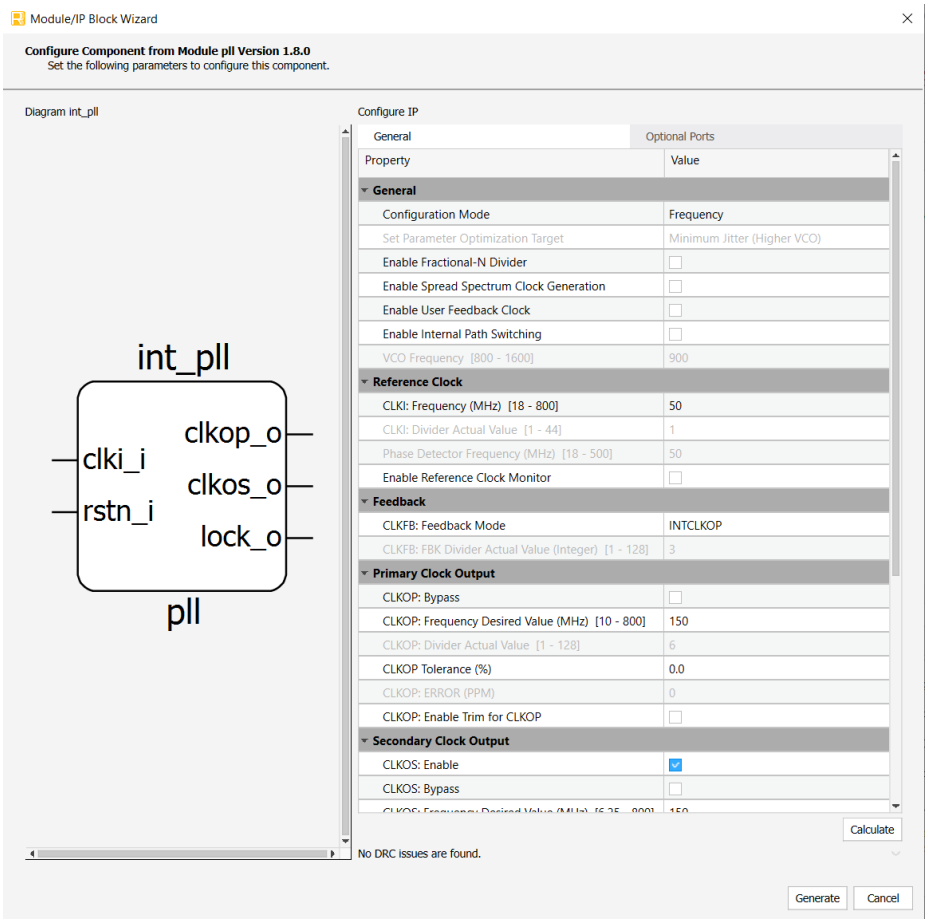


**Figure 3.4. int_pll IP Creation in the Lattice Radiant Software (1/2)**

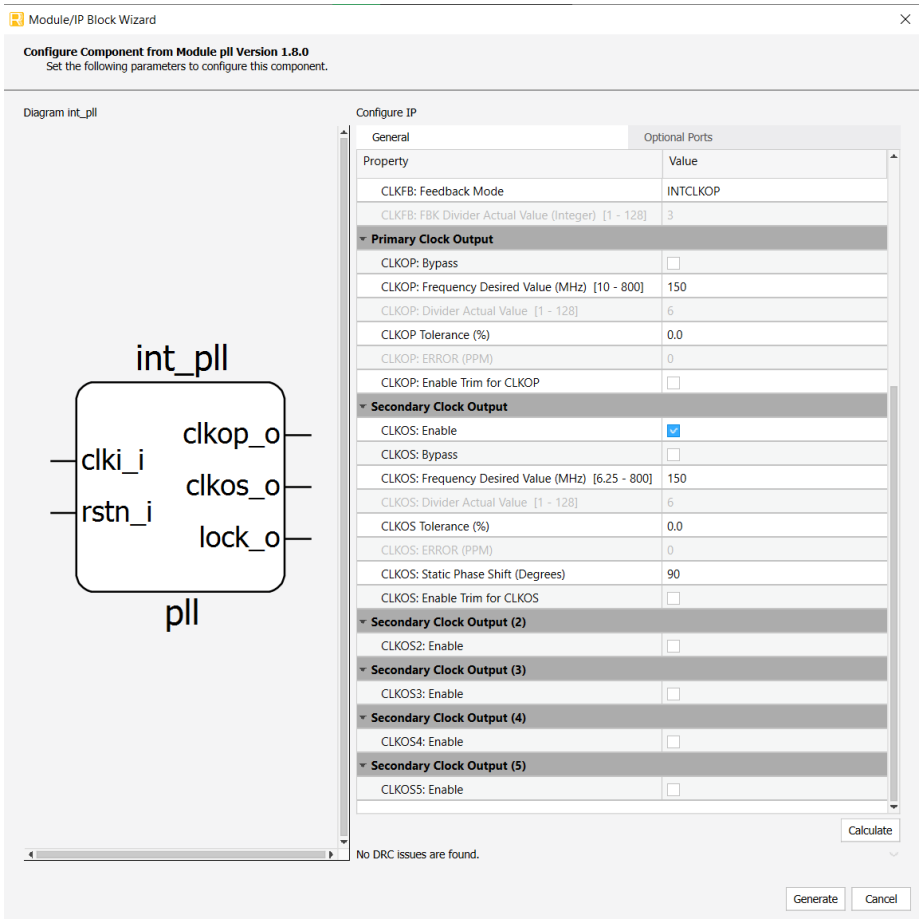


**Figure 3.5. int_pll IP Creation in the Lattice Radiant Software (2/2)**

You need to modify the reference clock frequency and the clkop frequency as per the required configuration. For Soft D-PHY TX IP, clkop frequency is half of the TX Line Rate per Lane. While for the Hard D-PHY TX IP, clkop frequency is the same as the TX Line Rate per Lane. The frequency for clkos needs to be the same as clkop, but 90-degrees phase shifted from clkop. As the Hard D-PHY TX IP has internal PLL support, only Soft D-PHY TX IP requires the external PLL to be used. The .ipx file included in the project (int_pll/int_pll.ipx) can be used to reconfigure the IP per your configuration requirements. If you create this IP from scratch, it is recommended to set the design name to int_pll so that you do not need to modify the instance names of these IPs in the top-level design file. Otherwise, you need to modify the name accordingly.

# 4. Design and File Modifications

This reference design is based on version 1.6.0 of the Pixel2Byte IP and version 1.9.2 of the TX D-PHY IP. Some modifications are required depending on user configuration in addition to two directive files (synthesis_directives.v and simulation_directives.v).

# 5. Design Simulation

To simulate the design, perform the following steps:

1. Unzip the reference design zip file.
2. Open the reference design project file (parallel2mipi_NX.rdf) with the Lattice Radiant Software.
3. You need to modify simulation_directives.v according to your configuration. Refer to the Simulation Directives section for details.
4. Click **Tools > Simulation Wizard**.
5. To create a new spf file, define **Project name** and **Project location**. Click **Next**.

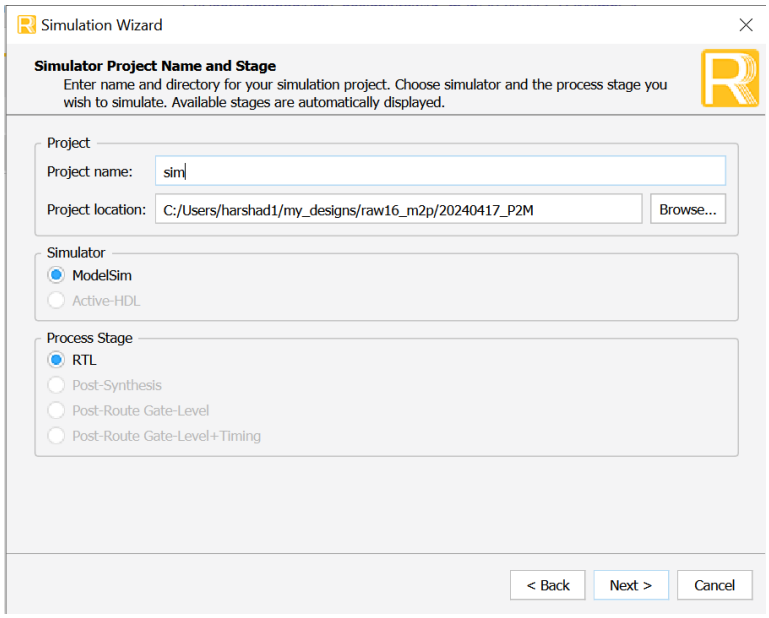


**Figure 5.1. Simulation Wizard: Create Simulation Project**

6. Set the simulation Top module as *parallel2mipi_NX_tb* and click **Next**.

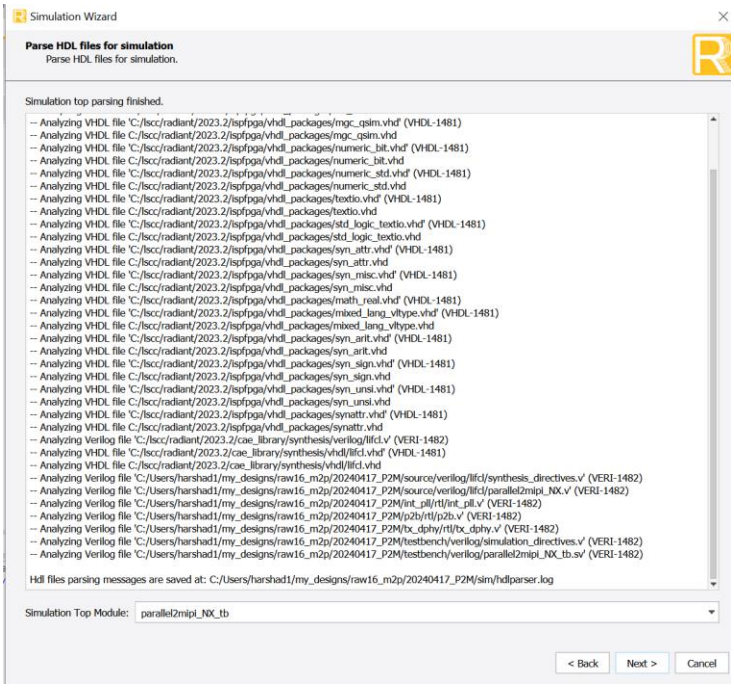


**Figure 5.2. Simulation Wizard: Select Simulation Top Module**

7. Select the configuration as shown in the following diagram and click **Finish**.

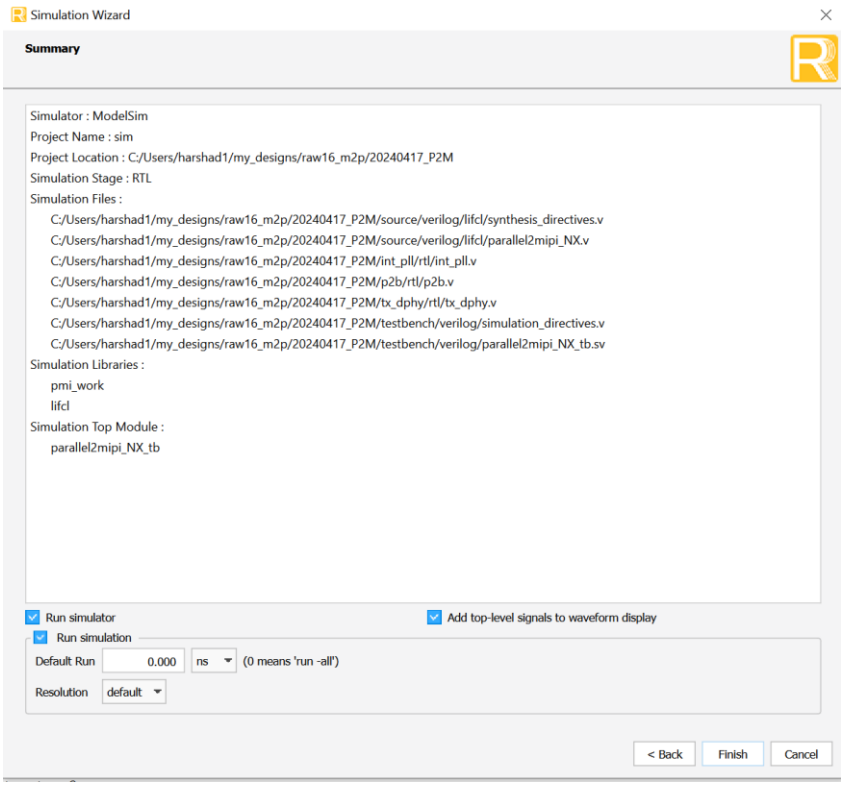


**Figure 5.3. Simulation Wizard: Summary Page**

The test-bench parallel2mipi_tb.v instantiates the top level design module, generates the stimulus video data and does the data comparison between the expected data and output data from the RD, including Frame Number, EoT Packet

check, CRC check, EoTp (Long Packet and Short Packet), ECC, and timing parameters of TX D-PHY. It shows the following statements while running the simulation.

```
#                    0       ================================
#                    0       D-PHY Type     = DSI
#                    0       Data Type      = RGB888
#                    0       No of TX LANE = 4
#                    0       No of PIX/CLK = 1
#                    0       TX Gear        = 8
#                    0       Clock Mode     = HS_ONLY
#                    0       D-PHY_IP       = LATTICE
#                    0       ================================
#                    0       TEST START
#                    0       Num of Frames          : 3
#                    0       Num of Lines per Frame : 3
#                    0       ================================
#                  525       test_hsync_front_porch : 480
#                  525       test_hsync_width       : 288
#                  525       test_hsync_back_porch  : 672
#                  525       test_h_width           : 1920
#                  525       test_v_height          : 3
#                  525       test_vsync_front_porch : 1
#                  525       test_vsync_width       : 3
#                  525       test_vsync_back_porch  : 36
#                  525       test_number_of_bytes   : 5760
#
#               1008359       FRAME #1 START
#               1060322       LINE #1 Transmitted
#               1088318       LINE #2 Transmitted
#               1116313       LINE #3 Transmitted
#               1148337       FRAME #1 END
#
#
#               1232324       FRAME #2 START
#               2264129       LINE #1 Transmitted
#               2292125       LINE #2 Transmitted
#               2320120       LINE #3 Transmitted
#               2352144       FRAME #2 END
#
#
#               2436131       FRAME #3 START
#               3467937       LINE #1 Transmitted
#               3495932       LINE #2 Transmitted
#               3523928       LINE #3 Transmitted
#               3555952       FRAME #3 END
```

When the simulation is finished, the following statements are displayed

```
#               3640032       ------------------------------------------
#               3640032       ##### DATA COMPIRING IS STARTED #####
#               3640032       ------------------------------------------
#               3640032       ***PASS : EOT PACKET CHECK***
#               3640032       ***PASS : SYNC CHECK
#               3640032       ***PASS : ECC
#               3640032       ***PASS : FRAME NO
#               3640032       ***PASS : EoTp PACKET CHECK AFTER LP***
#               3640032       ***PASS : EoTp PACKET CHECK AFTER SP***
#               3640032       ***PASS : TIMING PARAMETERS***
#               3640032       ***PASS : CRC***
#               3640032       Test fail count : 0
#
```

```
#               3640032      ------------------------------------------------------
#               3640032      ----------------- SIMULATION PASSED -------------------
#               3640032      ------------------------------------------------------
```

The test-bench generates other debug files during simulation like, *input_data.log*, *output_data.log* and *dphy_checker_timing.log* for debugging purpose. The *input_data.log* file stores the data transmitted by the test-bench. The *output_data.log* file stores the data received to the test-bench. The testbench compares both of these files. The *dphy_checker_timing.log* file stores all the timing parameters (such as LP-11, TLPX, HS-prepare, HS-0, and HS-Trail) and gives error if any timing parameter fails. The same file also saves timing of Header Packet received and Header Packet values like DT, VC, WC, and ECC.

Figure 5.5 shows the simulation waveform of the full view of three lines and three frames for the DSI: RGB888 interface. Figure 5.7 shows the simulation waveform of the full view of three lines and three frames for the DSI: RGB666 interface.

Calculation for DSI – RGB888:
1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Continuous Mode

| | |
|---|---|
| Total Horizontal Samples = **2200**<br>Total Vertical Lines = **1125** | Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format. |
| Pixel Clock Frequency<br>PCF = 2200 x 1125 x 60 = **148.5 MHz** | Input this frequency at reference clock in your int_pll & tx_dphy. |
| Bandwidth (Total Data Rate)<br>B = 148.5 MHz x 24-bit = **3.564 Gbps** | RGB888 uses 24 bits. |
| Line Rate (Data Rate per Lane)<br>LR = 3.564 Gbps/4-lane = **891 Mbps** | Input this tx line rate at tx_dphy. Maximum TX bandwidth is 2.5 Gbps/lane using D-PHY Hard IP & 1.5 Gbps/lane using D-PHY Soft IP. |
| MIPI Bit Clock Frequency<br>MBCF = 891/2 = **445.5 MHz** | Input this frequency at primary clock output in your int_pll. |

For DSI Simulation, Eopt enable (tx_dphy) is needed to be enabled.

**Figure 5.4. Calculation for DSI: RGB888**

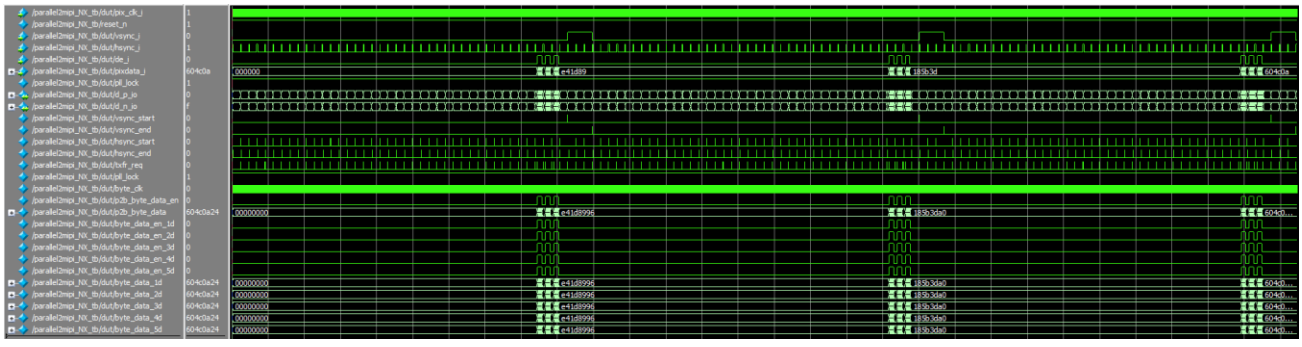

**Figure 5.5. Simulation Waveform for DSI: RGB888**

Calculation for DSI – RGB666:
1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Continuous Mode

| | |
|---|---|
| Total Horizontal Samples = **2200**<br>Total Vertical Lines = **1125** | Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format. |
| Pixel Clock Frequency<br>PCF = 2200 x 1125 x 60 = **148.5 MHz** | Input this frequency at reference clock in your int_pll & tx_dphy. |
| Bandwidth (Total Data Rate)<br>B = 148.5 MHz x 18-bit = **2.673 Gbps** | RGB666 uses 18 bits. |
| Line Rate (Data Rate per Lane)<br>LR = 2.673 Gbps/4-lane = **668.25 Mbps** | Input this tx line rate at tx_dphy. Maximum TX bandwidth is 2.5 Gbps/lane using D-PHY Hard IP & 1.5 Gbps/lane using D-PHY Soft IP. |
| MIPI Bit Clock Frequency<br>MBCF = 668.25/2 = **334.125 MHz** | Input this frequency at primary clock output in your int_pll. |

For DSI Simulation, Eopt enable (tx_dphy) is needed to be enabled.

**Figure 5.6. Calculation for DSI: RGB666**

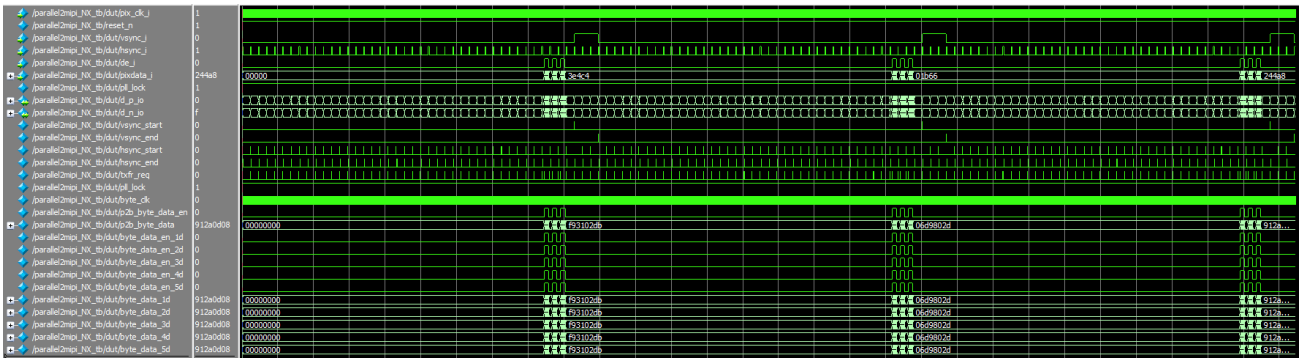

**Figure 5.7. Simulation Waveform for DSI: RGB666**

Figure 5.9 shows the simulation waveform of the full view of three lines and three frames for the CSI-2: RAW10 interface. Figure 5.11 shows the simulation waveform of the full view of three lines and three frames for the CSI-2: RAW12 interface. The waveform shows all the top level I/O and few other signals.

## Calculation for CSI – 2: RAW10
## 1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Continuous Mode

| | |
|---|---|
| Total Horizontal Samples = **2200**<br>Total Vertical Lines = **1125** | Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format. |
| Pixel Clock Frequency<br>PCF = 2200 x 1125 x 60 = **148.5 MHz** | Input this frequency at reference clock in your int_pll & tx_dphy. |
| Bandwidth (Total Data Rate)<br>B = 148.5 MHz x 10-bit = **1.485 Gbps** | RAW10 uses 10 bits. |
| Line Rate (Data Rate per Lane)<br>LR = 1.485 Gbps/4-lane = **371.25 Mbps** | Input this tx line rate at tx_dphy. Maximum TX bandwidth is 2.5 Gbps/lane using D-PHY Hard IP & 1.5 Gbps/lane using D-PHY Soft IP. |
| MIPI Bit Clock Frequency<br>MBCF = 371.25/2 = **185.625 MHz** | Input this frequency at primary clock output in your int_pll. |

For CSI-2 Simulation, configure the following parameters in tx_dphy.

| | |
|---|---|
| Enable Frame Number Increment in Packet | Enabled |
| Frame Number MAX Value Increment in Packet Formatter | 255 |
| Enable Line Number Increment in Packet Formatter | Enabled |

**Figure 5.8. Calculation for CSI-2: RAW10**

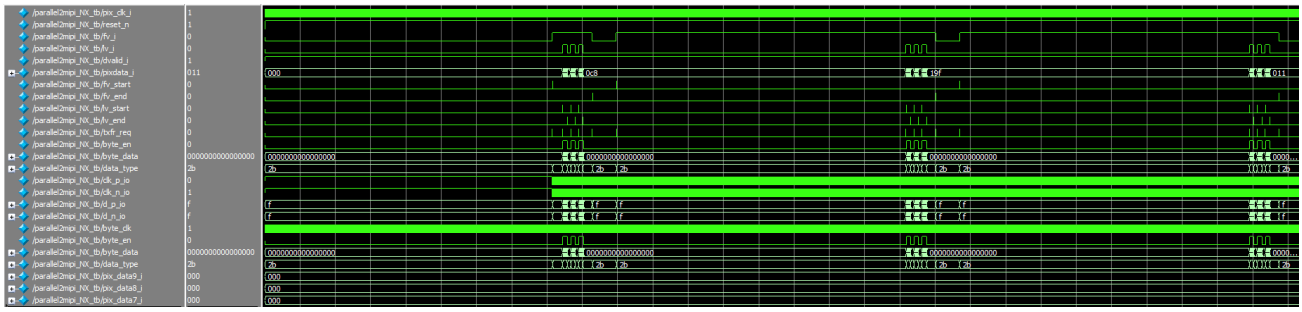

**Figure 5.9. Simulation Waveform for CSI-2: RAW10**

### Calculation for CSI – 2: RAW12
### 1920x1080p@60Hz, 4-lane, 8 Gears, 1 Pixel Lane, Continuous Mode

| | |
|---|---|
| Total Horizontal Samples = **2200**<br>Total Vertical Lines = **1125** | Refer to MIPI D-PHY Bandwidth Matrix and Implementation Table 2.1. Common Video Format. |
| Pixel Clock Frequency<br>PCF = 2200 x 1125 x 60 = **148.5 MHz** | Input this frequency at reference clock in your int_pll & tx_dphy. |
| Bandwidth (Total Data Rate)<br>B = 148.5 MHz x 12-bit = **1.782 Gbps** | RAW12 uses 12 bits. |
| Line Rate (Data Rate per Lane)<br>LR = 1.782 Gbps/4-lane = **445.5 Mbps** | Input this tx line rate at tx_dphy. Maximum TX bandwidth is 2.5 Gbps/lane using D-PHY Hard IP & 1.5 Gbps/lane using D-PHY Soft IP. |
| MIPI Bit Clock Frequency<br>MBCF = 445.5/2 = **222.750 MHz** | Input this frequency at primary clock output in your int_pll. |

For CSI-2 Simulation, configure the following parameters in tx_dphy.

| | |
|---|---|
| Enable Frame Number Increment in Packet | Enabled |
| Frame Number MAX Value Increment in Packet Formatter | 255 |
| Enable Line Number Increment in Packet Formatter | Enabled |

**Figure 5.10. Calculation for CSI-2: RAW12**

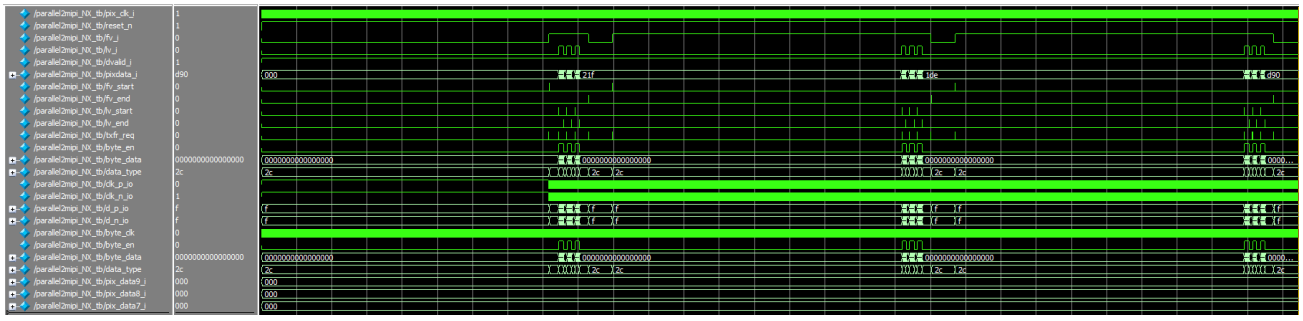

**Figure 5.11. Simulation Waveform for CSI-2: RAW12**

The simulation waveform can be accessed by opening the vsim.wlf file in the Modelsim from the simulation directory. More signals of a module can be added to the waveform as required.

# 6. Known Limitations

The following are the limitations of this reference design:

- Only following data types are supported for MIPI DSI interface: RGB888, RGB666
- Only following data types are supported for MIPI CSI-2 interface: RGB888, RAW8, RAW10, and RAW12

# 7. Design Package and Project Setup

The Parallel to MIPI with CrossLink-NX Reference Design is available on www.latticesemi.com. Figure 7.1 shows the directory structure. The design is targeted for LIFCL-40-7BG400I. synthesis_directives.v and simulation_directives.v are set to configure the design with following configuration:

- RX : DSI, RGB888 parallel data with 1 pixel/clock
- TX : 4-lanes, Gear 8 with Soft D-PHY in continuous clock mode

Users can modify the directives for their own configuration.

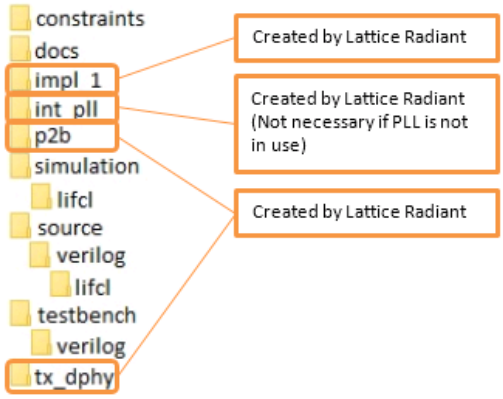


**Figure 7.1. Directory Structure**

Figure 7.2 shows the design files used in the Lattice Radiant project. Including PLL, Lattice Radiant creates three .ipx files. By specifying parallel2mipi_NX as a top-level design, all unnecessary files are ignored. Constraint file (parallel2mipi_NX.pdc) is also included in the project for reference. Users can modify it according to their own configuration.

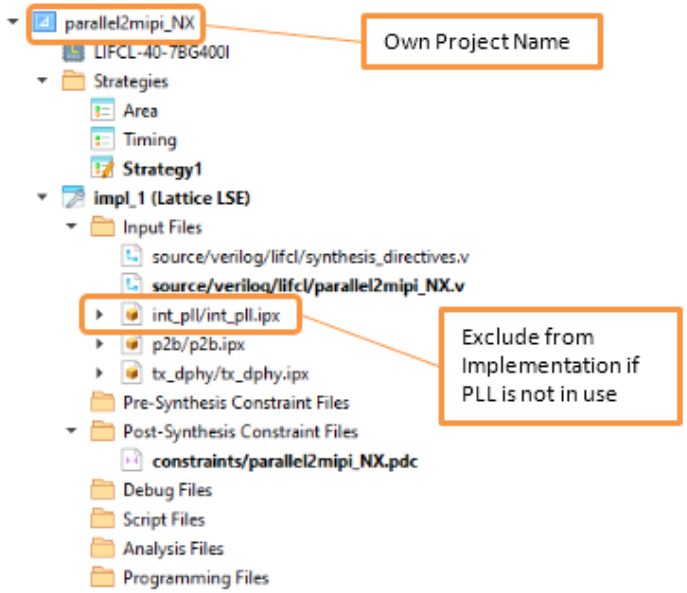


**Figure 7.2. Project Files**

# 8. Resource Utilization

Resource utilization depends on the configuration used. Table 8.1 shows resource utilization examples under certain configurations targeting LIFCL-40. This is just a reference and actual usage varies.

**Table 8.1. Resource Utilization Examples**

| Configuration | LUT % | FF % | EBR | I/O |
|---|---|---|---|---|
| 4-lane, Gear 16, Hard D-PHY, DSI, RGB888, 4 Pixels/clock | 19 | 4 | 6 | 102 |
| 1-lane, Gear 8, Soft D-PHY, DSI, RGB888, 1 Pixels/clock | 4 | 2 | 1 | 34 |
| 4-lane, Gear 16, Hard D-PHY, CSI-2, RAW12, 10 Pixels/clock | 5 | 3 | 8 | 126 |
| 1-lane, Gear 8, Hard D-PHY, CSI-2, RAW8, 1 Pixels/clock | 2 | 1 | 1 | 13 |

# References

- MIPI Alliance web page for D-PHY Specifications Version 1.2, Display Serial Interface 2 (DSI) Specifications Version 1.2, Camera Serial Interface 2 (CSI-2) Specifications Version 1.2, and Camera Serial Interface 2 (CSI-2) Specifications Version 2.0
- Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094)
- CSI-2/DSI D-PHY Tx IP Core User Guide (FPGA-IPUG-02080)
- PLL Module User Guide (FPGA-IPUG-02063)
- CrossLink-NX web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

# Revision History

**Revision 1.2, May 2024**

| Section | Change Summary |
|---|---|
| All | Renamed the document from *Parallel to MIPI with CrossLink-NX* to *Parallel to MIPI with CrossLink-NX Devices*. |
| Design and Module Description | • Updated Figure 3.2. p2b IP Creation in the Lattice Radiant Software.<br>• Updated Figure 3.3. tx_dphy IP Creation in the Lattice Radiant Software.<br>• Removed figure: *tx_dphy IP Creation in Lattice Radiant (2/2)*.<br>• Updated the parameter settings for *tINIT Counter* in the tx_dphy section.<br>• Updated Figure 3.4. int_pll IP Creation in the Lattice Radiant Software (1/2).<br>• Added Figure 3.5. int_pll IP Creation in the Lattice Radiant Software (2/2).<br>• Updated the description on clkos frequency in the int_pll section. |
| Design and File Modifications | Updated the IP versions in the Design and File Modifications section. |
| Design Simulation | Updated the steps to simulate design in the Design Simulation section. |
| References | Updated references. |

**Revision 1.1, June 2023**

| Section | Change Summary |
|---|---|
| Supported Device and IP | • Updated Compatible IP of LIFCL-40 to 'Pixel-to-Byte Converter IP version 1.4.0'.<br>• Updated Compatible IP of LIFCL-17 to 'D-PHY Transmitter IP version 1.7.2'.<br>• Updated Lattice Radiant software version to '2022.1'. |
| Design and Module Description | • Updated Figure 3.2. p2b IP Creation in Lattice Radiant to show the p2b version 1.1.0.<br>• Updated Figure 3.3. tx_dphy IP Creation in Lattice Radiant (1/2) and Figure 3.4. tx_dphy IP Creation in Lattice Radiant (2/2) to show the tx_dphy version 1.1.3.<br>• Updated Figure 3.5. int_pll IP Creation in Lattice Radiant to show the int_pll version 1.2.0. |
| Design Simulation | • Updated Figure 5.1. Script Modification #1, Figure 5.2. Script Modification #2, Figure 5.4. Simulation Waveform for DSI: RGB888, Figure 5.6. Simulation Waveform for DSI: RGB666, Figure 5.8. Simulation Waveform for CSI-2: RAW10, and Figure 5.10. Simulation Waveform for CSI-2: RAW12.<br>• Added Figure 5.3. Calculation for DSI: RGB888, Figure 5.5. Calculation for DSI: RGB666, Figure 5.7. Calculation for CSI-2: RAW10, and Figure 5.9. Calculation for CSI-2: RAW12. |
| Technical Support Assistance | Added reference link to the Lattice Answer Database. |

**Revision 1.0, February 2021**

| Section | Change Summary |
|---|---|
| All | Initial release. |


www.latticesemi.com