



# Parallel to MIPI with CrossLink-NX Devices

## Reference Design

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## Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
APB	Advanced Peripheral Bus
AXI	Advanced Extensible Interface
CDC	Clock-Domain Crossing
CIL	Control and Interface Logic
CMOS	Complementary Metal-Oxide Semiconductor
CRC	Cyclic Redundancy Check
CSI-2	Camera Serial Interface 2
DDR	Double Data Rate
DPI	Display Pixel Interface
DSI	Display Serial Interface
DUT	Device Under Test
ECC	Error Correction Code
EoTp	End-of-Transmission Packet
HDL	Hardware Description Language
HS	High Speed
IP	Intellectual Property
LMMI	Lattice Memory-Mapped Interface
LP	Low Power
LSB	Least Significant Bit
LUT	Look Up Table
LVC MOS	Low-Voltage CMOS
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
MSB	Most Significant Bit
PDC	Physical Design Constraints
PLL	Phase Locked Loop
P2B	Pixel2Byte
RTL	Register Transfer Level
RX	Receiver
TX	Transmitter

# 1. Introduction

The Mobile Industry Processor Interface (MIPI®) D-PHY was developed primarily to support camera and display interconnections in mobile devices, and it has become the industry’s primary high-speed PHY solution for these applications in smartphones. It is typically used in conjunction with MIPI Camera Serial Interface-2 (CSI-2) and MIPI Display Serial Interface (DSI) protocol specifications. It meets the demanding requirements of low power, low noise generation, and high noise immunity that mobile phone designs demand.

MIPI D-PHY is a practical PHY for typical camera and display applications. It is designed to replace traditional parallel bus based on low-voltage complementary metal-oxide semiconductor (LVCMOS) or low-voltage differential signaling (LVDS). However, many processors and displays/cameras still use RGB, CMOS, or MIPI Display Pixel Interface (DPI) as interface.

The Parallel to MIPI reference design allows the quick interface for a processor with an RGB interface to a display with a MIPI DSI interface or a camera with a CMOS interface to a processor with CSI-2 interface. The Lattice Semiconductor Parallel to MIPI D-PHY Interface reference design provides this conversion for Lattice Semiconductor CrossLink™-NX devices. This is useful for wearable, tablet, human machine interfacing, medical equipment, and many other applications.

## 1.1. Quick Facts

Download the reference design files from the [Parallel to MIPI CSI-2 / DSI Display Interface Bridge Reference Design](#) web page.

**Table 1.1. Summary of the Reference Design**

<b>General</b>	Target Devices	CrossLink-NX
	Source code format	Verilog, System Verilog
<b>Simulation</b>	Functional simulation	Performed
	Timing simulation	Not Performed
	Testbench	Available
	Testbench format	Verilog
<b>Software Requirements</b>	Software tool and version	Lattice Radiant™ software version 2025.1
	IP version (if applicable)	Pixel-to-Byte Converter IP v1.9.1 CSI-2/DSI D-PHY Transmitter IP v2.3.0

## 1.2. Features

The key features of the Parallel to MIPI reference design are:

- Compliant with MIPI D-PHY v1.2, MIPI DSI v1.2, and MIPI CSI-2 v1.2 Specifications
- Supports MIPI DSI and MIPI CSI-2 interfacing up to 6 Gbps for Soft D-PHY, up to 10 Gbps for Hard D-PHY (internal PLL mode), and 3.2 Gbps for Hard D-PHY (external PLL mode).
- Supports 1, 2, or 4 MIPI D-PHY data lanes
- Supports non-burst mode with sync events for transmission of DSI packets only
- Supports low-power (LP) mode during vertical and horizontal blanking
- Supports common MIPI DSI compatible video formats (RGB888, RGB666)
- Supports common MIPI CSI-2 compatible video formats (RGB888, RAW8, RAW10, RAW12, RAW16)

## 1.3. Naming Conventions

### 1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL. This includes radix indications and logical operators.

### 1.3.2. Data Ordering and Data Types

The highest bit within a data bus is the most significant bit. 8-bit parallel data is serialized to 1-bit data stream on each MIPI D-PHY data lane where bit 0 is the first transmitted bit.

Table 1.2 lists pixel data order coming from core module.

**Table 1.2. Pixel Data Order**

Data Type	Format
RGB	{Red[MSB:0], Green[MSB:0], Blue[MSB:0]}
RAW	RAW[MSB:0]

### 1.3.3. Signal Names

Signal names that end with:

- *\_n* are active low signals
- *\_i* are input signals  
Some signals are declared as bidirectional (I/O) but are only used as input. Hence, *\_i* identifier is used.
- *\_o* are output signals  
Some signals are declared as bidirectional (I/O) but are only used as output. Hence, *\_o* identifier is used.
- *\_io* are bidirectional signals

## 2. Directory Structure and Files

The Parallel to MIPI with CrossLink-NX reference design is available on the [Parallel to MIPI CSI-2 / DSI Display Interface Bridge Reference Design](#) web page. Figure 2.1 shows the directory structure. The design is targeted for LIFCL-40-7BG400I. The *synthesis\_directives.v* and *simulation\_directives.v* files are set to configure the design with following configurations:

- RX: DSI, RGB888 parallel data with 1 pixel/clock
- TX: 4-lanes, Gear 8 with Soft D-PHY in continuous clock mode

You can modify the directives for your own configuration.

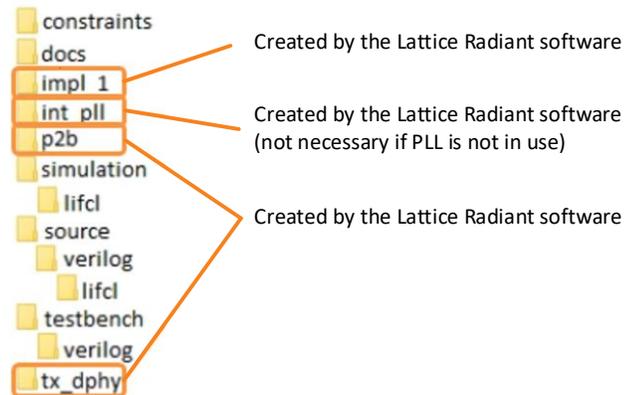


Figure 2.1. Directory Structure

### 3. Functional Description

Figure 3.1 shows the top block level diagram of the Parallel to MIPI reference design.

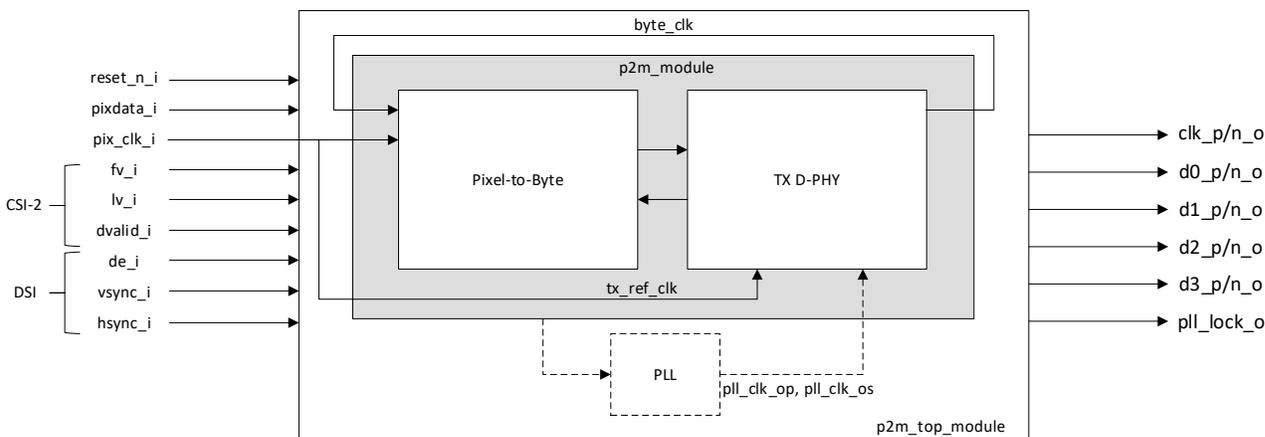


Figure 3.1. Parallel to MIPI Reference Design Block Diagram

The Parallel to MIPI D-PHY reference design converts a standard parallel video interface into either DSI or CSI-2 byte packets. The input interface for the design consists of a pixel bus (RGB888, RGB666), vertical and horizontal sync flags, a data enable and a clock for DSI and pixel bus (RGB888, RAW8, RAW10, RAW12, and RAW16), frame and line valid flags and a clock for CSI-2.

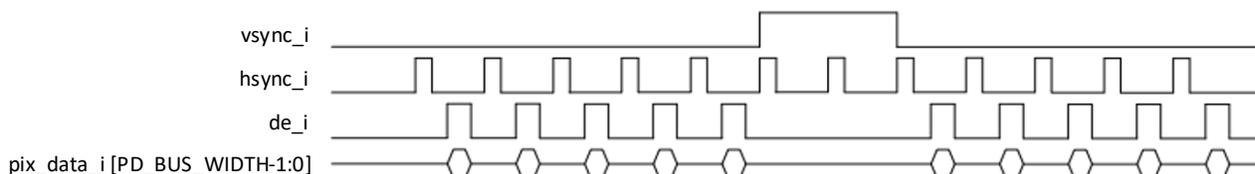


Figure 3.2. Display Parallel Input Bus Waveform

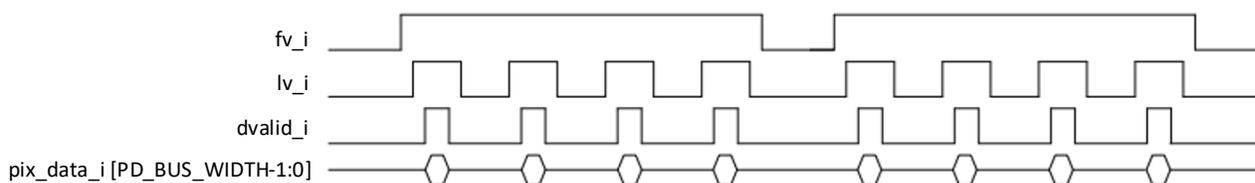


Figure 3.3. Camera Sensor Parallel Input Bus Waveform

This parallel bus in Figure 3.2 and Figure 3.3 is converted to the appropriate DSI or CSI-2 output format. The DSI/CSI-2 output serializes HS (high speed) data and controls LP (low power) data and transfers the data through the MIPI D-PHY IP. The MIPI D-PHY IP also has a maximum of 5 lanes per channel, which consists of one clock lane and up to 4 data lanes. The maximum D-PHY data rate per lane is 1.5 Gbps by Soft D-PHY IP and 2.5 Gbps by Hard D-PHY IP.

#### 3.1. Design Components

As shown in Figure 3.1, the block level diagram of the Parallel to MIPI reference design mainly consists of the following blocks:

- PLL IP
- Pixel-to-Byte IP

- TX D-PHY IP

### 3.1.1. Pixel-to-Byte (p2b)

The Pixel-to-Byte IP converts pixel data into bytes according to IP configurations such as Pixel Data Type (RGB888, RGB666, RAW8, RAW10, RAW12, and RAW16), TX Interface, Number of TX Lanes, and other parameters. Figure 3.4 shows an example IP configuration in Lattice Radiant for this module. The configurations are set by default on the packaged reference design. Refer to the [Pixel-to-Byte Converter IP User Guide \(FPGA-IPUG-02094\)](#) for details on the IP.

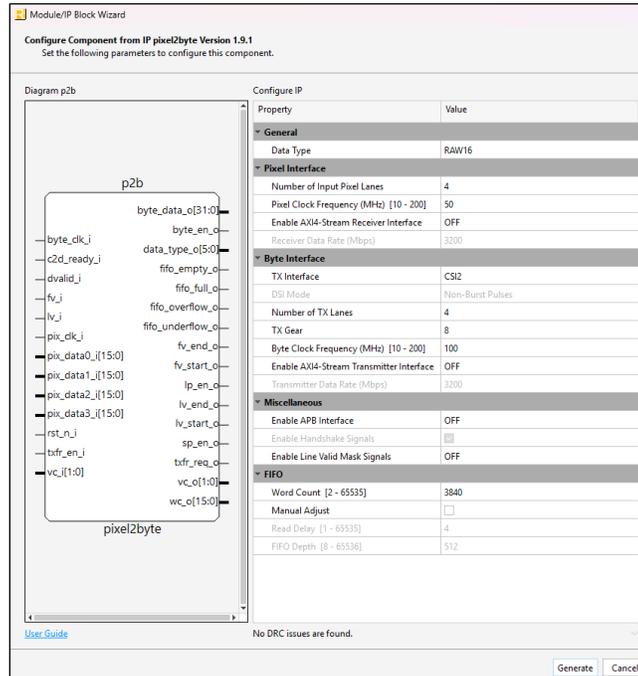


Figure 3.4. p2b IP Creation in the Lattice Radiant Software

Table 3.1 shows the guidelines and parameter settings required for this reference design.

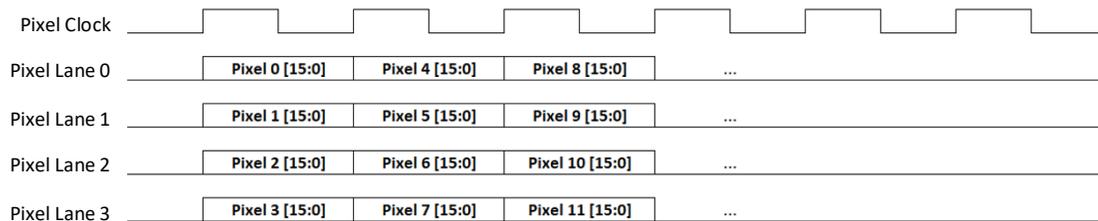
Table 3.1. Pixel-to-Byte IP Parameter Settings for the Reference Design

IP Parameter	Description
TX Interface	Select DSI or CSI depending on application. This interface must be set to the same as the TX Interface Type defined for the TX D-PHY IP.
Data Type	This setting is based on the defined TX interface of the IP. For DSI, select RGB888 or RGB666 only. For CSI, select RAW8, RAW10, RAW12, and RAW16 only. Other data type is not supported in this reference design.
Number of Pixel Lanes	Indicates the number of lanes available for the pixel data. Distributes each pixel data (depending on Data Type) into these lanes. For instance in Figure 3.4, the Number of Pixel Lanes is set to 4 with Data Type sets to RAW16, the pixel data is distributed as shown in Figure 3.5. The pixel lanes that can be set for the reference design are 1, 2, 3, 4, 6, 8, and 10. In which, 6, 8, and 10 pixel lanes are supported only for RAW10 and RAW12 (which is also supported by the IP).
Number of TX Lanes	Defines the number of lanes the TX D-PHY used. The TX lanes defines the total number of bits of the data output of the P2B IP. Number of byte_data_o = Number of TX Lanes × TX Gear
TX Gear	Defines the gearing ratio. Select 8 (if TX D-PHY used is Soft or Hard D-PHY) or 16 (if TX D-PHY used is Hard D-PHY). Number of byte_data_o = Number of TX Lanes × TX Gear

IP Parameter	Description
Pixel Clock Frequency	The pixel clock frequency is directly related to the byte clock frequency. To set the compatible byte clock frequency for the defined pixel clock frequency of the IP, the transmitter data rate (byte domain) must be greater than or equal the receiver data rate (pixel domain). The ratio between the two frequencies is called N-ratio, where the ratio must be $\geq 1$ . $N - ratio = \frac{Transmitter\ Data\ Rate}{Receiver\ Data\ Rate} = \frac{(Byte\ Clock\ Frequency) \times (Tx\ Gear) \times (Number\ of\ TX\ Lanes)}{(Pixel\ Clock\ Frequency) \times (Bits\ per\ Pixel) \times (Number\ of\ Pixel\ Lanes)}$
Byte Clock Frequency	
Word Count	Defines the number of expected generated bytes of your horizontal resolution. For instance, a 1920x1080p display has 1920 active pixels on a horizontal line. For RAW16, the Word Count can be calculated as 1920 pixels $\times$ (16 bits per pixel / 8 bits per byte) = 3840 bytes.
DSI Mode	Defines the packet sequence of data transmission for DSI interface. You must use only Non-Burst Mode with Sync Events.

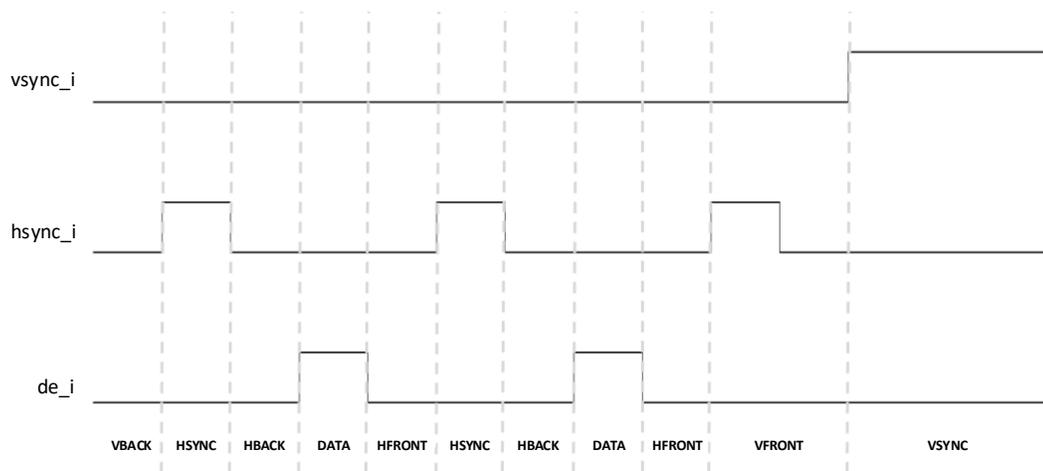
For the following IP parameters not defined in the table, set the parameters to default values:

- Enable APB Interface (OFF)
- Enable Line Valid Mask Signals (OFF)
- Enable AXI4-Stream Receiver Interface (OFF)
- FIFO Manual Adjust (Unchecked)



**Figure 3.5. Pixel Data Distribution on Pixel Lanes for 4 Pixel Lanes, RAW16**

The Pixel-to-Byte IP is mainly driven through vsync\_i, hsync\_i, and de\_i for DSI interface and fv\_i, lv\_i, and dvalid\_i for CSI-2 interface. Each input signals assertion is spaced with defined blanking periods (horizontal and vertical blanking period). The distribution of these blanking periods is shown in Figure 3.6 and Figure 3.7. To control the values of these blanking periods, refer to the Simulation Directive Results section.



**Figure 3.6. Pixel-to-Byte IP Input Signals Behavior for DSI Interface**

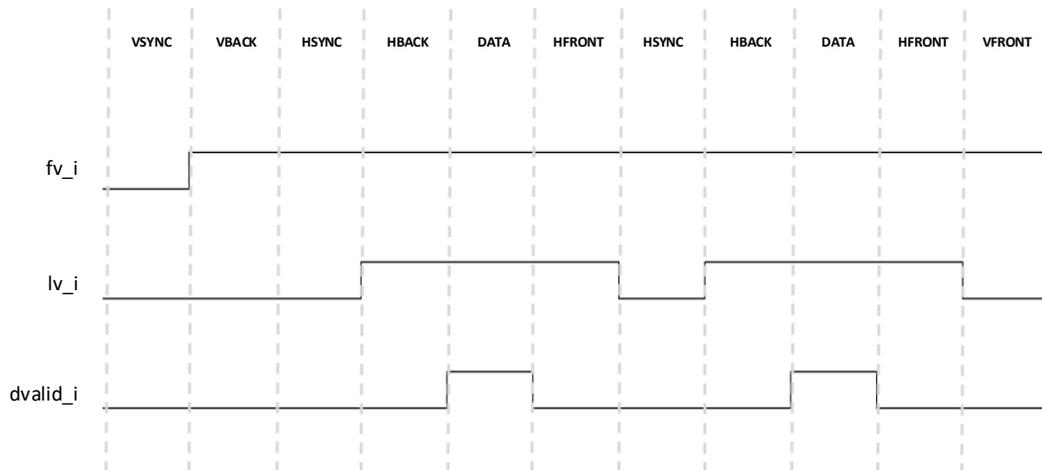


Figure 3.7. Pixel-to-Byte IP Input Signals Behavior for CSI-2 Interface

### 3.1.2. TX D-PHY (tx\_dphy)

TX D-PHY serializes bytes of data from the Pixel-to-Byte IP to the PHY based on IP configurations such as D-PHY implementation, TX Interface, Number of TX Lanes, and other parameters. Figure 3.8 shows an example of IP configuration in the Lattice Radiant software for this module. The configuration is set by default on the packaged reference design. Refer to the [CSI-2/DSI D-PHY Tx IP User Guide \(FPGA-IPUG-02080\)](#) for details on the IP.

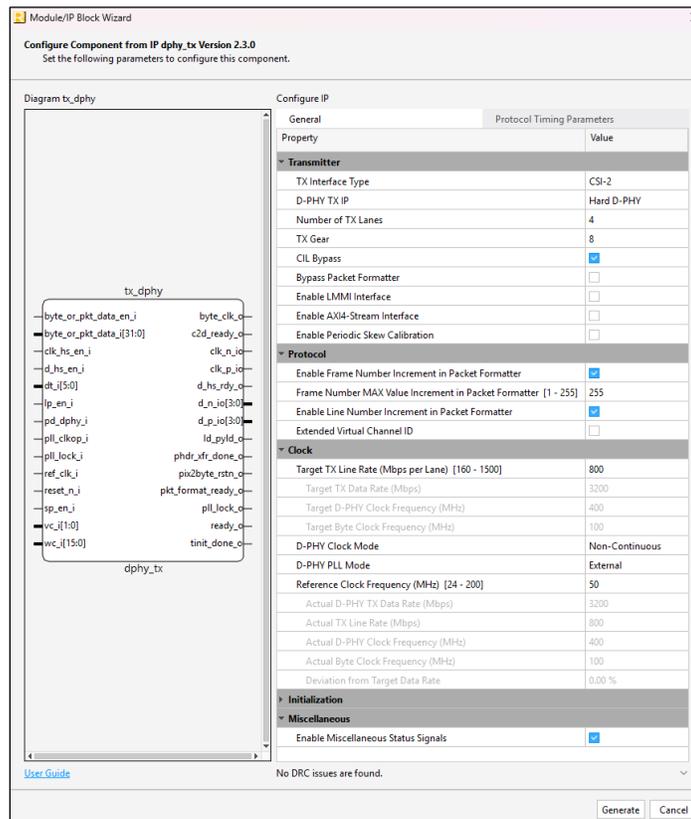


Figure 3.8. TX D-PHY IP Creation in the Lattice Radiant Software

Table 3.2 shows the guidelines and parameter settings required for this reference design.

**Table 3.2. TX D-PHY IP Parameter Settings for the Reference Design**

IP Parameter	Description
TX Interface	Select DSI or CSI depending on application. This interface must be set to the same as the TX Interface Type defined for the Pixel-to-Byte IP.
D-PHY TX IP	Select Hard D-PHY (hard block) or Soft D-PHY (soft logic).
Number of TX Lanes	Defines the number of lanes the TX D-PHY used. This IP setting must be set to the same TX Lane defined in the Pixel-to-Byte IP. Select 1, 2, or 4 TX lanes. Number of byte_data_o = Number of TX Lanes × TX Gear
TX Gear	Defines the gearing ratio. This IP setting must be set to the same TX Gear defined in the Pixel-to-Byte IP. Select 8 (if TX D-PHY used is Soft or Hard D-PHY) or 16 (if TX D-PHY used is Hard D-PHY). Number of byte_data_o = Number of TX Lanes × TX Gear
CIL Bypass	Defines whether the IP uses a Soft logic implementation (Checked) of the Control and interface logic of the D-PHY or uses the Hard CIL (Unchecked) integrated in the Hard D-PHY. Soft D-PHY always use Soft Logic CIL while Hard D-PHY can use Hard or Soft Logic CIL. For this reference design, set to Disabled (Checked) – Soft Logic CIL.
Enable Frame Number Increment in Packet Formatter	Enables or disables frame number on the TX D-PHY IP for CSI-2. For this reference design, set to Enabled (Checked), as the design simulation environment checks the frame number.
Frame Number MAX Value increment in Packet Formatter	Indicates the maximum value of the frame counter on the IP for CSI-2. This value depends on the number of frames you set from simulation directives. For this reference design, set the maximum value to 255.
Enable Line Number Increment in Packet Formatter	Enables or disables line number on the TX D-PHY IP for CSI-2. For this reference design, set to Enabled (Checked), as the design simulation environment checks the line number.
EoTp Enable	Enables or disables End of Transmit Packet (EoTp) at the end of packet transmission for DSI. For this reference design, set to Enabled (Checked), as the design simulation environment checks the EoTp.
Enable Edge Clock Synchronizer and Divider	Enables the edge clock synchronizer and divider internal from the IP to generate D-PHY clock for Soft D-PHY. For this reference design, set to Enabled (Checked). The design and simulation environment does not incorporate a separate module to drive double data rate (DDR) elements exposed when setting is disabled.
Target TX Line Rate (Mbps per Lane)	Specifies the supported bit rate for each lane. For this reference design, set any line rate from a minimum of 160 Mbps to a maximum of 1500 Mbps (for TX Gear = 8) and 2500 Mbps (for TX Gear = 16).
D-PHY Clock Mode	Defines the clock mode of the PHY layer. A continuous clock always has the clock lane running in high-speed mode, while a non-continuous clock sets the clock at low power mode in between HS transactions. For this reference design, select Continuous or Non-Continuous Clock mode.
D-PHY PLL Mode	Indicates whether the IP uses the internal PLL in the Hard D-PHY block or an external PLL. Hard D-PHY can use internal or external PLL while Soft D-PHY can only use external PLL. For This reference design, select External or Internal PLL mode.
Reference Clock Frequency (MHz)	Defines the clock frequency for the reference clock input of the Hard D-PHY and fabric-based component interfacing within the IP. For Hard D-PHY, it is recommended to set the ideal reference clock to generate the same D-PHY data rate as defined from the IP. Refer to the Actual D-PHY TX Data Rate parameter which is automatically calculated to identify the compatible reference clock. For this reference design, the reference clock used is the same as the Pixel Clock Frequency. The reference clock input of the IP and the pixel clock input share the same clock port as described in Figure 3.1. Use the same frequency for reference clock as the pixel clock frequency.
Enable Miscellaneous Status Signals	Enables additional output signals for debugging purposes. For this reference design, set to Enabled (Checked), as some signals (such as pll_lock_o) are used in the design.

IP Parameter	Description
Protocol Timing Parameter	Defines the number of byte clock cycles (CIL Bypass = Checked) for each D-PHY timing parameter. For this reference design, use the default value and change the values if required. Refer to the <a href="#">Debug Methods</a> section for example.

For the following IP parameters not defined in the table, set the parameters to default values:

- Bypass Packet Formatter (Unchecked)
- Enable LMMI Interface (Unchecked)
- Enable AXI4-Stream Interface (Unchecked)
- Enable Periodic Skew Calibration (Unchecked)
- Enable TINIT Counter (Unchecked)

### 3.1.3. Phase Locked Loop (int\_pll)

The reference design can be configured to use an external PLL if the TX D-PHY is set to the external PLL mode.

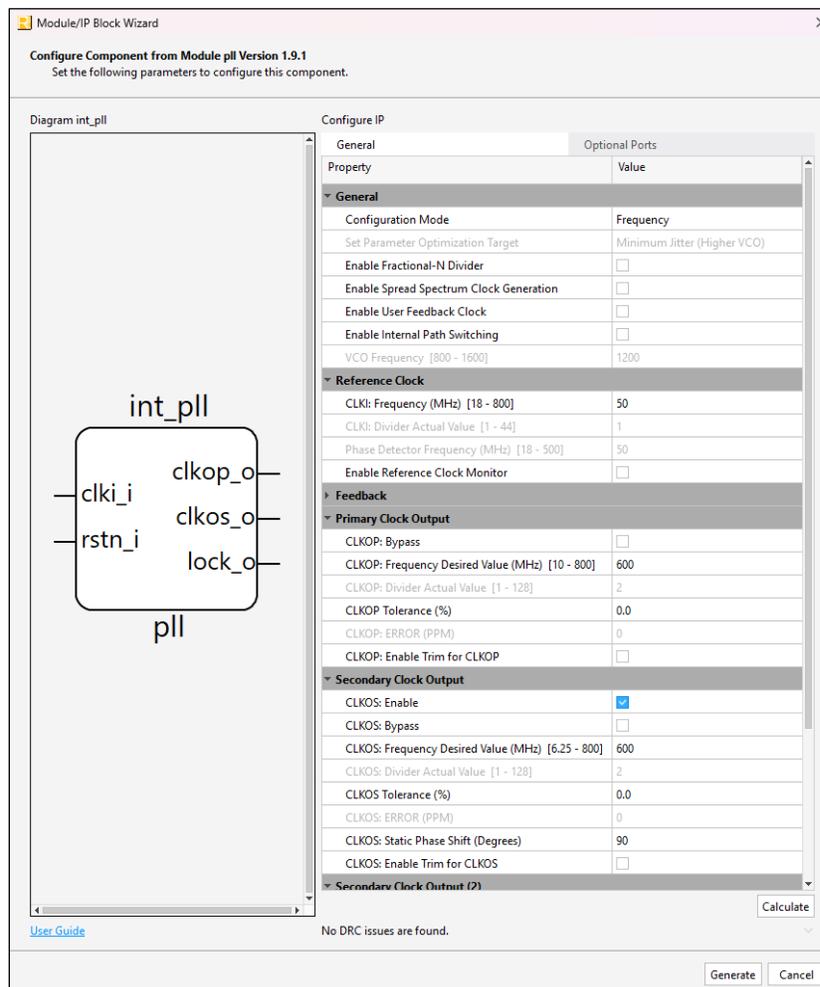


Figure 3.9. PLL IP Creation in the Lattice Radiant Software

Table 3.3 shows the guidelines and parameter settings required for this reference design.

**Table 3.3. PLL IP Parameter Settings for the Reference Design**

IP Parameter	Description
CLKI Frequency	The reference design uses pixel clock as the input clock of the PLL. Set the CLKI frequency to the same frequency as the pixel clock.
CLKOP Frequency	Defines the primary clock output frequency. For this reference design, set the clock frequency to the same as the D-PHY clock frequency, which is set from the TX D-PHY IP for Soft D-PHY. This value is half the value of line rate. For instance, a 900 Mbps line rate for the D-PHY has a 450 MHz D-PHY clock. Hence, CLKOP frequency must be set to 450 MHz. This value is twice the D-PHY clock frequency for Hard D-PHY.
CLKOS Enable	Enables the CLKOS output port from the IP. Set to Enabled when Soft D-PHY is used for TX D-PHY.
CLKOS Frequency	Defines the secondary clock output frequency if enabled.
CLKOS Static Phase Shift	For this reference design, set the clock frequency to the same as the D-PHY clock frequency, which is set from the TX D-PHY IP but shifted at 90 degrees phase shift. This value is half the value of line rate. For instance, a 900 Mbps line rate for the D-PHY has a 450 MHz D-PHY clock. Hence, CLKOS frequency must be set to 450 MHz.

### 3.2. IP Handshaking

The Pixel-to-Byte IP and TX D-PHY IP are interfaced as shown in Figure 3.10 and Figure 3.12. For this reference design, set the TX D-PHY to Soft CIL (CIL Bypass = Checked), as the direct handshaking connection is currently supported only in this configuration. For details on the handshake signals timing diagram, refer to the [Pixel-to-Byte Converter IP User Guide \(FPGA-IPUG-02094\)](#).

- CSI-2: The main signals to interface the IPs are described in Figure 3.10. The dotted line represents the connection that depends on IP configuration.
  - The `lp_en_o` and `lp_en_i` signals have a register in between. The register is required for data types RAW8, RAW10 (1, 2, 4 thexel lanes), RAW12 (1, 2, 4 pixel lanes), and RGB888 because `lp_en_i` and `byte_or_pkt_data_en_i` require a 3 byte clock cycle distance between the signals. The Pixel-to-Byte IP version 1.7 to 1.9.1 incorporates a 4 byte clock cycle between `lp_en_o` and `byte_en_o`, hence `lp_en_o` needs to be registered to provide 1 byte clock delay and meet the 3 byte clock cycle requirement. Figure 3.11 describes the input requirement of TX D-PHY when interfacing with Pixel-to-Byte for long packets.
  - The `clk_hs_en_i` signal is connected and available only for Non-Continuous Clock mode IP configuration.
- DSI: The main signals to interface the IPs are described in Figure 3.12. The dotted line represents the connection that depends on IP configuration.
  - The `clk_hs_en_i` signal is connected and available only for Non-Continuous Clock mode IP configuration.

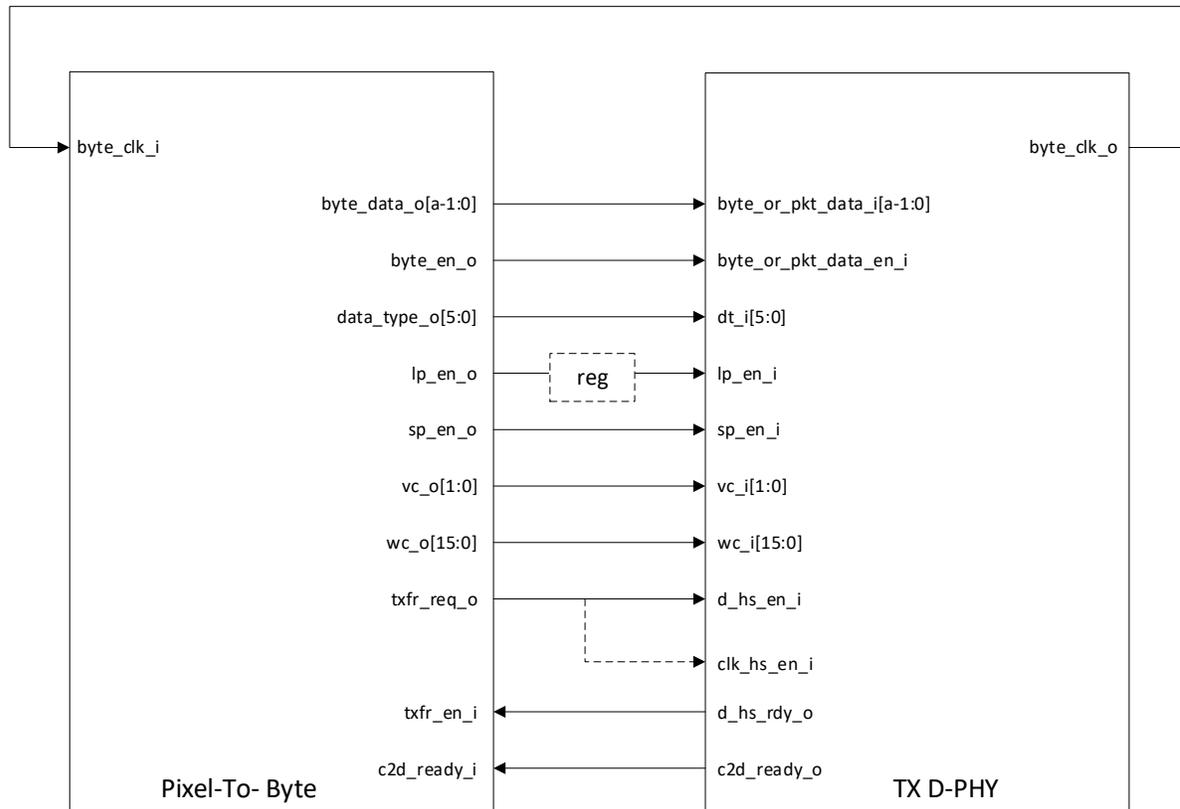


Figure 3.10. Pixel-to-Byte IP and TX D-PHY IP Handshaking for CSI-2

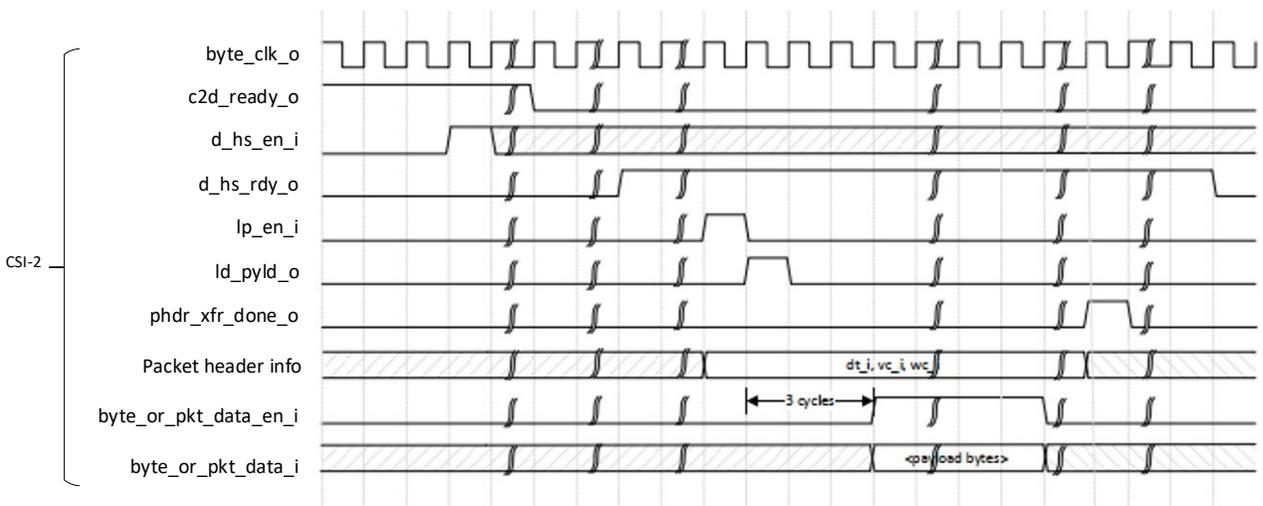


Figure 3.11. TX D-PHY IP Input Side Timing Diagram for CSI-2 Long Packet

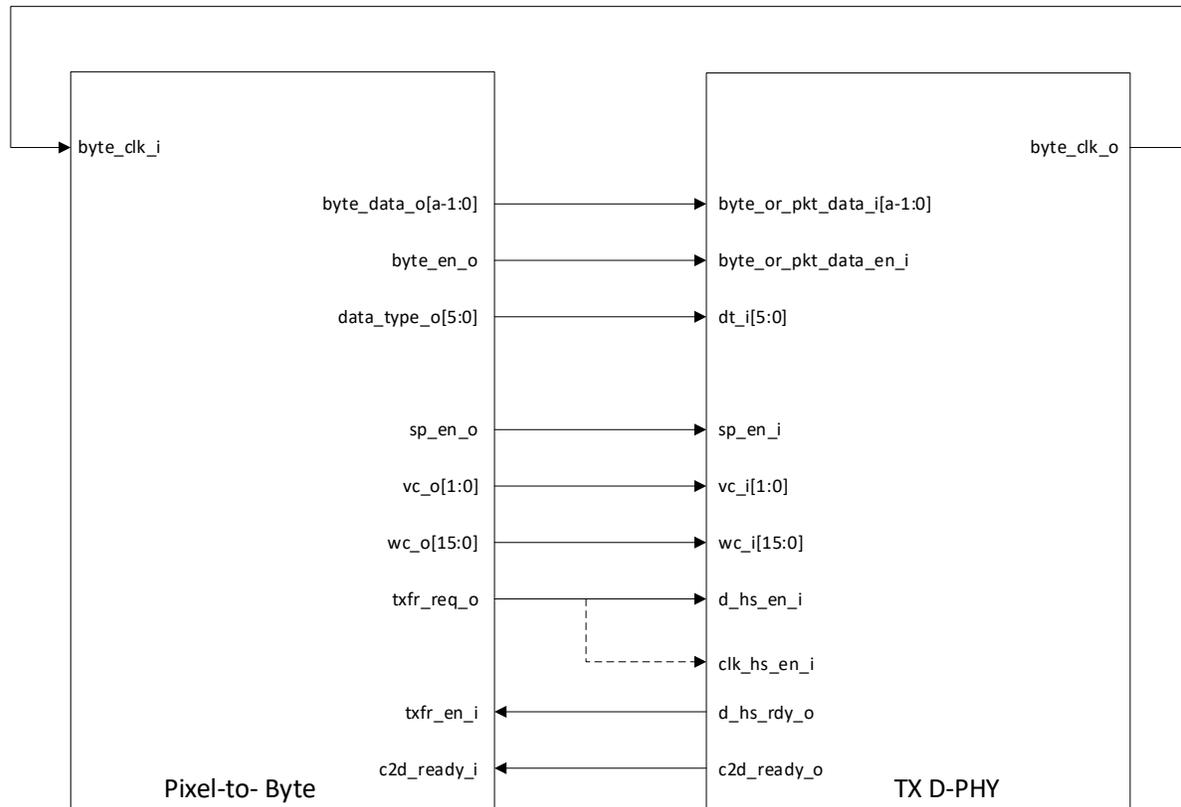


Figure 3.12. Pixel-to-Byte IP and TX D-PHY IP Handshaking for DSI

### 3.3. Clocking Scheme

The five main clocks in the reference design shown in Figure 3.1 are described as follows:

- Pixel clock (pix\_clk\_i) – This clock is generated externally from the reference design. All signals (except reset\_n\_i) towards the input side of the Pixel-to-Byte IP are synchronized to the pixel clock.
- Reference clock (tx\_ref\_clk) – This clock is the reference clock of the TX D-PHY IP and is driven by the same pixel clock.
- PLL input clocks – PLL clock input signals are available when TX D-PHY uses external PLL mode. The following are the two main clocks:
  - pll\_clk\_op – This is driven by the primary clock output of the PLL. This input clock signal on TX D-PHY is used as an input bit-rate clock of the Hard D-PHY or used as edge clock of the Soft D-PHY implementation.
  - pll\_clk\_os – This is driven by the secondary clock output of the PLL and is shifted by 90°. This signal is used to clock the DDR primitives as clock serializer internal to the IP. This is available only for Soft D-PHY.
- Byte clock (byte\_clk) – The byte clock is driven by the byte clock output of the TX D-PHY. This clock is used to clock the byte domain signals (output signals) of the Pixel-to-Byte IP.

### 3.4. Reset Scheme

The reference design is controlled by asynchronous reset signal reset\_n\_i and is asserted at the beginning of the simulation. The reset\_n\_i is also used to control the power down (pdphy\_i) of the TX D-PHY in which the reset\_n\_i signal is gated with PLL lock signals from D-PHY (pll\_lock\_o) or external PLL clock signal.

## 4. Reference Design Parameter Description

There are two directive files for this reference design:

- *synthesis\_directives.v* – used for design compilation by Lattice Radiant software and for simulation.
- *simulation\_directives.v* – used for simulation.

You can modify these directives according to your own configuration. The settings in these files must match Pixel-to-Byte IP and TX D-PHY IP settings created by the Lattice Radiant software.

### 4.1. Synthesis Directives

Table 4.1 shows the synthesis directives that affect this reference design. These are used for both synthesis and simulation. Some parameter selections are restricted by other parameter settings as shown in Table 4.1 and Table 4.2.

**Table 4.1. Synthesis Directives**

Category	Directive	Remarks
D-PHY Type	TX_DSI	Only one of these directives must be defined. Used for DSI or CSI-2 transmission.
	TX_CSI2	
Video Data Type	RGB888	Only one of these directives must be defined. Type of video data to convert from pixel format to byte format for Pixel-to-Byte converter.
	RGB666	
	RAW8	
	RAW10	
	RAW12	
	RAW16	
Number of TX Lane	NUM_TX_LANE_1	Only one of these directives must be selected.
	NUM_TX_LANE_2	
	NUM_TX_LANE_4	
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_1	Only one of these directives must be defined. Number of pixels per pixel clock used for the input to the Pixel-to-Byte converter.
	NUM_PIX_LANE_2	
	NUM_PIX_LANE_4	
	NUM_PIX_LANE_6	
	NUM_PIX_LANE_8	
	NUM_PIX_LANE_10	
TX D-PHY Clock Gear	TX_GEAR_8	TX D-PHY clock gear. Only one of these directives must be defined.
	TX_GEAR_16	
Number of Active Pixels	NUM_PIXELS {value}	<p>Number of active pixels per line. This setting must be aligned with the word count set on the Pixel-to-Byte IP. The relationship is described as follows:</p> $\text{Word Count} = (\text{NUM\_PIXELS}) \times [(\text{BITS PER PIXEL}) / 8]$ <p>Where BITS PER PIXEL depends on the selected data type: RAW16 (16 bits per pixel), RAW12(12 bits per pixel), RAW10 (10 bits per pixel), RAW8 (8 bits per pixel), RGB888 (24 bits per pixel), RGB666 (18 bits per pixel).</p> <p>Example: 3840 word count for RAW16 = (NUM_PIXELS) × [(16 bits per pixel) / 8] and NUM_PIXELS = 1920 active pixels.</p>
Clock Mode <sup>1</sup>	CLK_MODE_HS_ONLY	TX D-PHY clock mode. Only one of these two directives must be defined. This is aligned with clock mode set in TX D-PHY.
	CLK_MODE_HS_LP	
PLL Mode	PLL_INTERNAL	Internal PLL or external PLL to be used for TX D-PHY. Only one of these directives must be used. For DPHY_SOFT/ Soft D-PHY, set to PLL_EXTERNAL as Soft D-PHY does not have internal PLL. For DPHY_HARD / Hard D-PHY, set to PLL_INTERNAL or PLL_EXTERNAL.
	PLL_EXTERNAL	

Category	Directive	Remarks
D-PHY IP	DPHY_HARD	Hard and Soft configuration of D-PHY TX IP. Only one of these directives must be used.
	DPHY_SOFT	

**Note:**

1. HS\_LP mode means non-continuous clock mode and HS\_ONLY means continuous clock mode for TX D-PHY.

## 4.2. Simulation Directives

Table 4.2 shows the simulation directives for this reference design. These signals affect how data is presented in simulation, as described in the [Simulating the Reference Design](#) section.

**Table 4.2. Simulation Directives**

Category	Directive	Remarks
Pixel clock period	PIX_CLK {value}	Pixel clock period in ns. This is the period of the clock that drives the pixel clock port (pix_clk_i) which is source of Pixel-to-Byte, pixel clock port, TX D-PHY reference clock (tx_ref_clk), and external PLL reference clock (when PLL_EXTERNAL is used).
Number of video frames	NUM_FRAMES {value}	Number of video frames to be transmitted.
Number of lines per frame	NUM_LINES {value}	Number of active lines per frame.
Horizontal Front Porch	HFRONT {value}	Number of blanking cycles before HSYNC signal is asserted based on pixel clock.
Number of cycles HSYNC signal asserted	HPULSE {value}	Number of cycles for which HSYNC signal is asserted based on pixel clock.
Horizontal Back Porch	HBACK {value}	Number of blanking cycles after HSYNC signal is de-asserted based on pixel clock.
Vertical Front Porch	VFRONT {value}	Number of blanking lines before VSYNC signal is asserted based on pixel clock.
Number of lines VSYNC signal asserted	VPULSE {value}	Number of lines for which VSYNC signal is asserted based on pixel clock.

## 5. Signal Description

Table 5.1 shows the top level I/O of this reference design. Actual I/O depends on the your configurations. All necessary I/O ports are automatically declared by compiler directives.

**Table 5.1. Parallel to MIPI Top-Level I/O**

Port Name	Direction	Description
<b>Clocks and Resets</b>		
pix_clk_i	I	Input pixel/reference clock. Period of pixel clock is defined in the <i>simulation_directives.v</i> file.
reset_n_i	I	Asynchronous active low system reset.
<b>DSI Input Interface</b>		
vsync_i <sup>1</sup>	I	Input vertical sync for parallel interface.
hsync_i <sup>1</sup>	I	Input horizontal sync for parallel interface.
de_i <sup>1</sup>	I	Input data enable for parallel interface.
<b>CSI-2 Input Interface</b>		
fv_i <sup>2</sup>	I	Input frame valid for parallel interface.
lv_i <sup>2</sup>	I	Input line valid sync for parallel interface.
dvalid_i <sup>2</sup>	I	Input data enable for parallel interface.
<b>Input Data</b>		
pixdata_i <sup>5</sup>	I	Input pixel data. Data bus width depends on the data type selected and the number of pixels per clock. RGB888: 24-bit bus width × Number of pixel per clock RGB666 <sup>1</sup> : 18-bit bus width × Number of pixel per clock RAW12 <sup>2</sup> : 12-bit bus width × Number of pixel per clock RAW10 <sup>2</sup> : 10-bit bus width × Number of pixel per clock RAW8 <sup>2</sup> : 8-bit bus width × Number of pixel per clock RAW16 <sup>2</sup> : 16-bit bus width × Number of pixel per clock
<b>Debug Interface</b>		
pll_lock_o <sup>3</sup>	O	D-PHY PLL lock signal.
<b>TX Output Interface</b>		
d_p_io[NUM_TX_LANE -1:0] <sup>4</sup>	I/O	Positive differential TX D-PHY data lanes.
d_n_io[NUM_TX_LANE -1:0] <sup>4</sup>	I/O	Negative differential TX D-PHY data lanes.
clk_p_io	I/O	Positive differential TX D-PHY clock lane.
clk_n_io	I/O	Negative differential TX D-PHY clock lane.

**Notes:**

1. Available only if data interface is DSI.
2. Available only if data interface is CSI-2.
3. Turned-on if the *Enable miscellaneous status signals* attribute is selected.
4. NUM\_TX\_LANE = Number of TX D-PHY Lanes: 1, 2, 4 (available on user interface).
5. Number of pixel per clock is equivalent to number of pixel lanes.

## 6. Simulating the Reference Design

To simulate the design, perform the following steps:

1. Unzip the reference design .zip file.
2. Open the reference design project file (*parallel2mipi\_NX.rdf*) using the Lattice Radiant software.
3. Modify the *simulation\_directives.v* file according to your configuration. Refer to the [Simulation Directives](#) section for details.
4. Click **Tools > Simulation Wizard**.
5. To create a new .spf file, define **Project name** and **Project location**. Click **Next**.

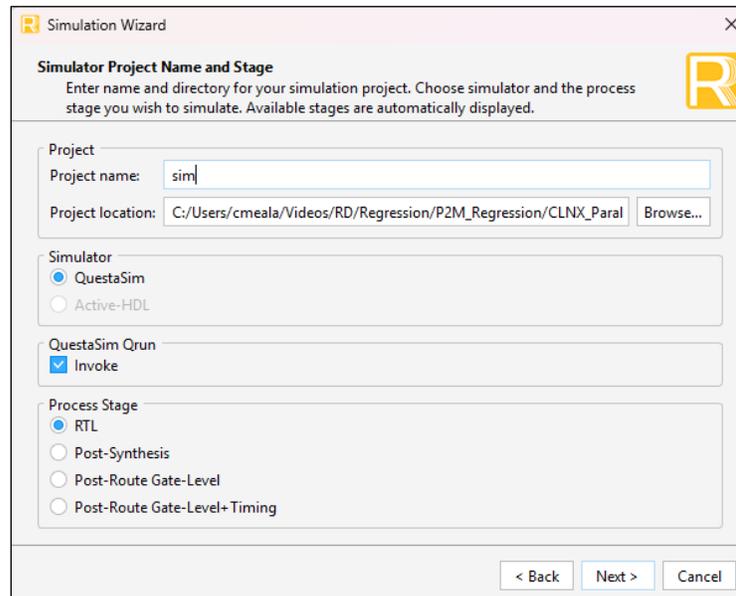


Figure 6.1. Simulation Wizard: Creating Simulation Project

6. Set the simulation top module as *parallel2mipi\_NX\_tb* and click **Next**.

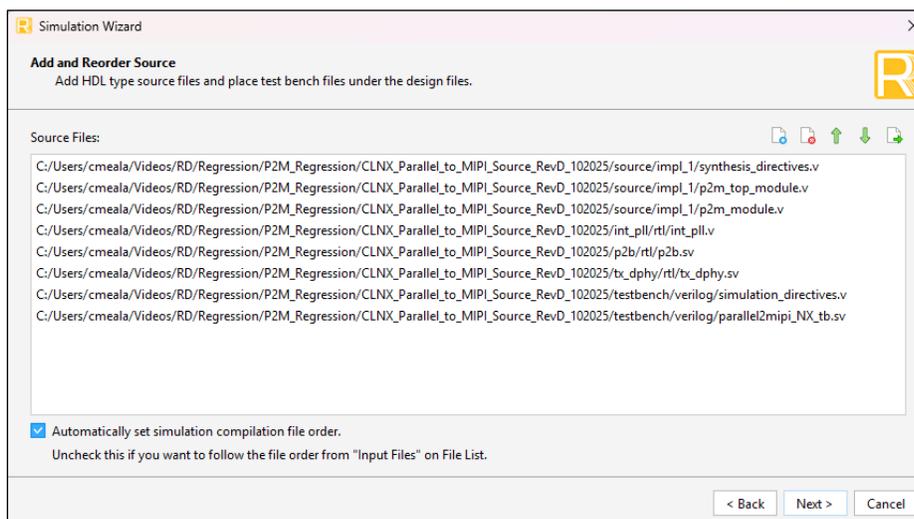


Figure 6.2. Simulation Wizard: Selecting Simulation Top Module

7. Select the configuration as shown in the following figure and click **Finish**.

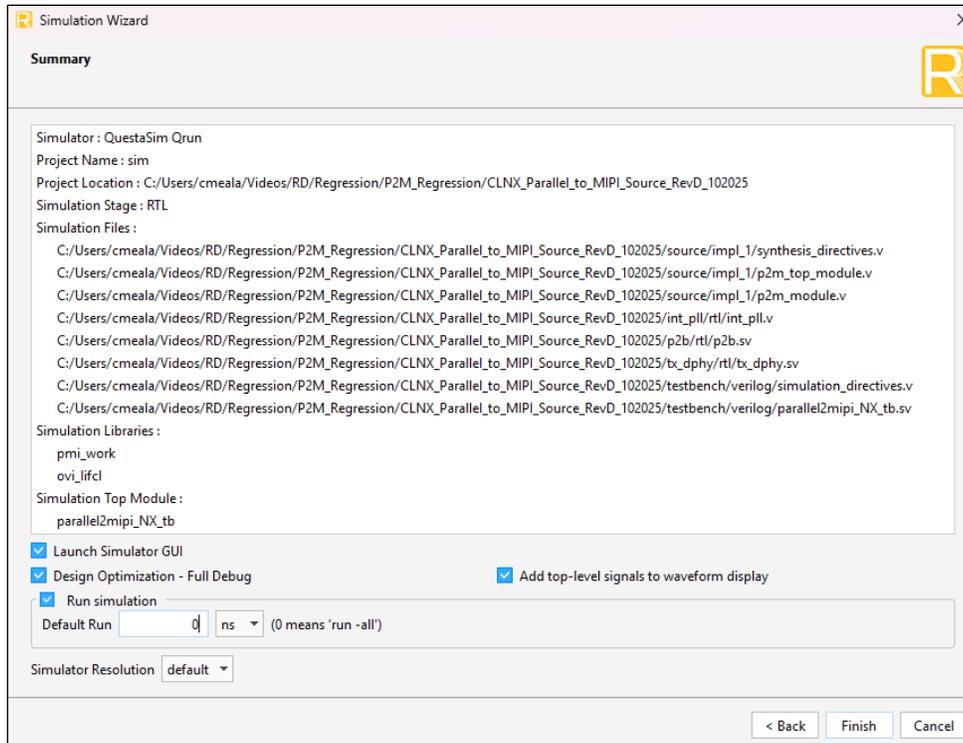


Figure 6.3. Simulation Wizard: Summary Page

8. The QuestaSim for Lattice software opens and runs the simulation.

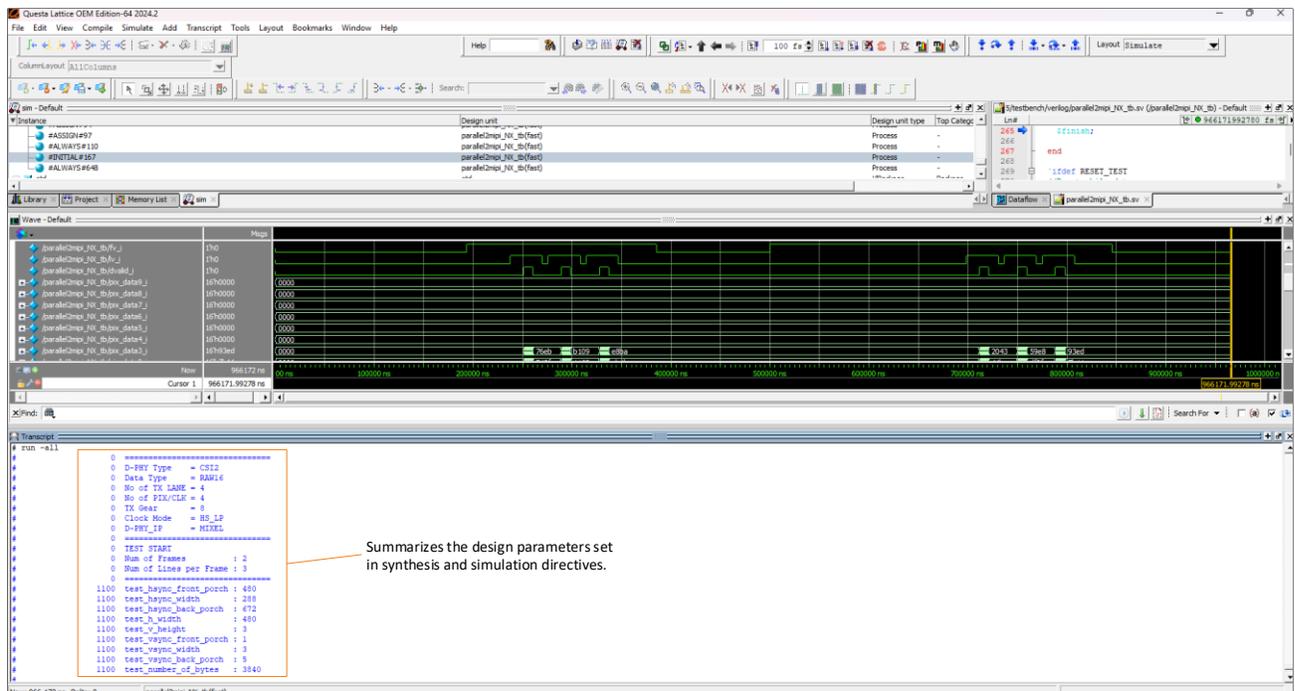


Figure 6.4. Simulation Results (1/2)

```

# 193090 FRAME #1 START
# 260280 LINE #1 Transmitted
# 298680 LINE #2 Transmitted
# 337080 LINE #3 Transmitted
# 385090 FRAME #1 END
#
#
# 500290 FRAME #2 START
# 721080 LINE #1 Transmitted
# 759480 LINE #2 Transmitted
# 797880 LINE #3 Transmitted
# 845890 FRAME #2 END
#
# 961071 Video generation stopped
#
# 961072 TEST DONE for CSI2 :: DATA TYPE is RAW16
# 961172 -----
# 961172 ##### DATA COMPILING IS STARTED #####
# 961172 -----
# 961172 ***PASS : EOT PACKET CHECK***
# 961172 ***PASS : SYNC CHECK
# 961172 ***PASS : ECC
# 961172 ***PASS : FRAME NO
# 961172 ***PASS : TIMING PARAMETERS***
# 961172 ***PASS : CRC***
# 961172 Test fail count : 0
#
# -----
# 961172 ----- SIMULATION PASSED -----
# 961172 -----
# 961172 TEST END
#
# ** Note: $finish : C:/Users/cmeala/Videos/RD/Regression/P2M_Regression/CLNX_Parallel_to_MIPI_Source_RevD_102025/testbench/verilog/parallel2mipi_NX_tb.v(265)
# Time: 966172 ns Iteration: 0 Instance: /parallel2mipi_NX_tb

```

Indicates video generation frame-by-frame and line-by-line.

Indicates that the simulation has passed the multiple d-PHY checks. The simulation fails when there is at least one failure in the D-PHY checks.

Figure 6.5. Simulation Results (2/2)

## 6.1. Simulation Environment

The simulation environment is composed of the top testbench *parallel2mipi\_NX\_tb.v* which instantiates the device under test (DUT) (p2m module), video generator *vid\_timing\_gen\_driver.sv*, and D-PHY checker *dphy\_checker.v*.

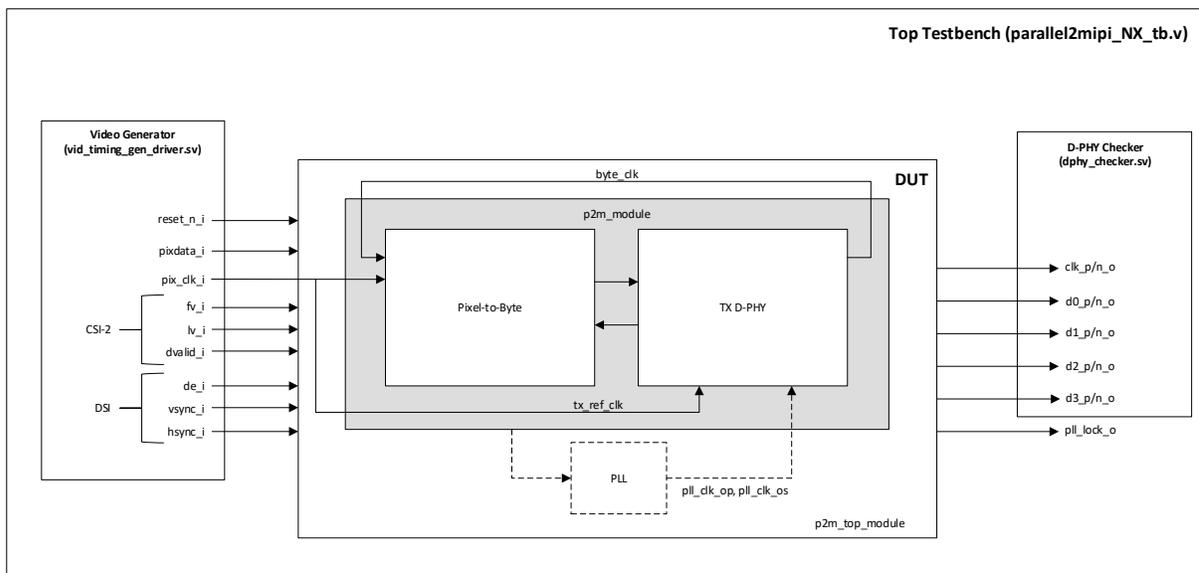


Figure 6.6. Simulation Modules

- *vid\_timing\_gen\_driver.sv* – This module is used to generate signals on the input side of the p2m module. The module drives the signals based on the D-PHY type set in the synthesis directives. For instance, if TX\_CSI2 is set, this module drives fv\_i, lv\_i, and dvalid\_i, and the general input signals for p2b, such as pixdata\_i. The output file of this module is the *input\_data.log* file where the file stores the data transmitted by this module. This file is generated when you run the simulation.
- *dphy\_checker.v* – This module is used to check any clock and data stream in MIPI data and MIPI clock lanes. This module checks the frame number, EoT packet check, cyclic redundancy check (CRC) check, EoTp (long packet and short packet), Error Correction Code (ECC), packet header, data transmission, packet footer, and checks whether

the transmitter meets the required timing parameters (LP-00, LP-01, HS-0, and so on). There are two output files for this module:

- The *output\_data.log* file stores the data received to the testbench.
- The *dphy\_checker\_timing.log* file stores all the timing parameters (such as LP-11, TLPX, HS-prepare, HS-0, and HS-Trail) and shows error if any timing parameter fails. This file also saves timing of header packet received and header packet values like DT, VC, WC, and ECC.

These files are generated when you run the simulation.

```

1 TIMING VALUES OF DATA LINES
2 START
3 ALL TIMING VALUES IN ns
4 Wait for new packet
5
6 TIME(start for packet) 3542
7 LP-11 = 190029
8 TLPX = 60
9 HS-prepare = 50
10 HS-0 = 229
11 UI = 1
12 Header Rx (time) = 193927
13 DT (in hex) = 0
14 VC (in hex) = 0
15 WC (in hex) = 1
16 ECC (in hex) = 1a
17 HS-Trail = 124
18 TIME(end for packet) 194051
19
20 Packet received
21
22 Wait for new packet
23
24 TIME(start for packet) 194053
25 LP-11 = 43678
26 TLPX = 60
27 HS-prepare = 50
28 HS-0 = 229
29 UI = 1
30 Header Rx (time) = 238087
31 DT (in hex) = 2
32 VC (in hex) = 0
33 WC (in hex) = 1
34 ECC (in hex) = 11
35 HS-Trail = 124
36 TIME(end for packet) 238211
37
38 Packet received
39

```

Figure 6.7. D-PHY Checker File Content

- *parallel2mipi\_NX\_tb.v* – This module is the top testbench of the design. This module integrates the other modules and the DUT (p2m\_top\_module). The top testbench checks the data captured in the *input\_data.log* file and compares with the *output\_data.log* file. This module checks if the data from one file to another is matching and whether the files are written with data. The top testbench also provides early warnings based on the Pixel-to-Byte output. For example, this module checks for the correctness of Frame Valid Start, Line Valid Start, Line Valid End, and Data Type.

## 6.2. Simulation Directive Results

The simulation directives affect the video generation module of the simulation environment. The simulation of this reference design uses the following settings:

- NUM\_PIXELS 1920

- PIX\_CLK 20
- HFRONT `NUM\_PIXELS\*0.25
- HPULSE `NUM\_PIXELS\*0.15
- HBACK `NUM\_PIXELS\*0.35
- VFRONT 1
- VPULSE 3
- VBACK 5

### 6.2.1. CSI-2

The figure below shows each line is composed of horizontal blanking (HSYNC, HBLANK, HFRONT) and valid data.

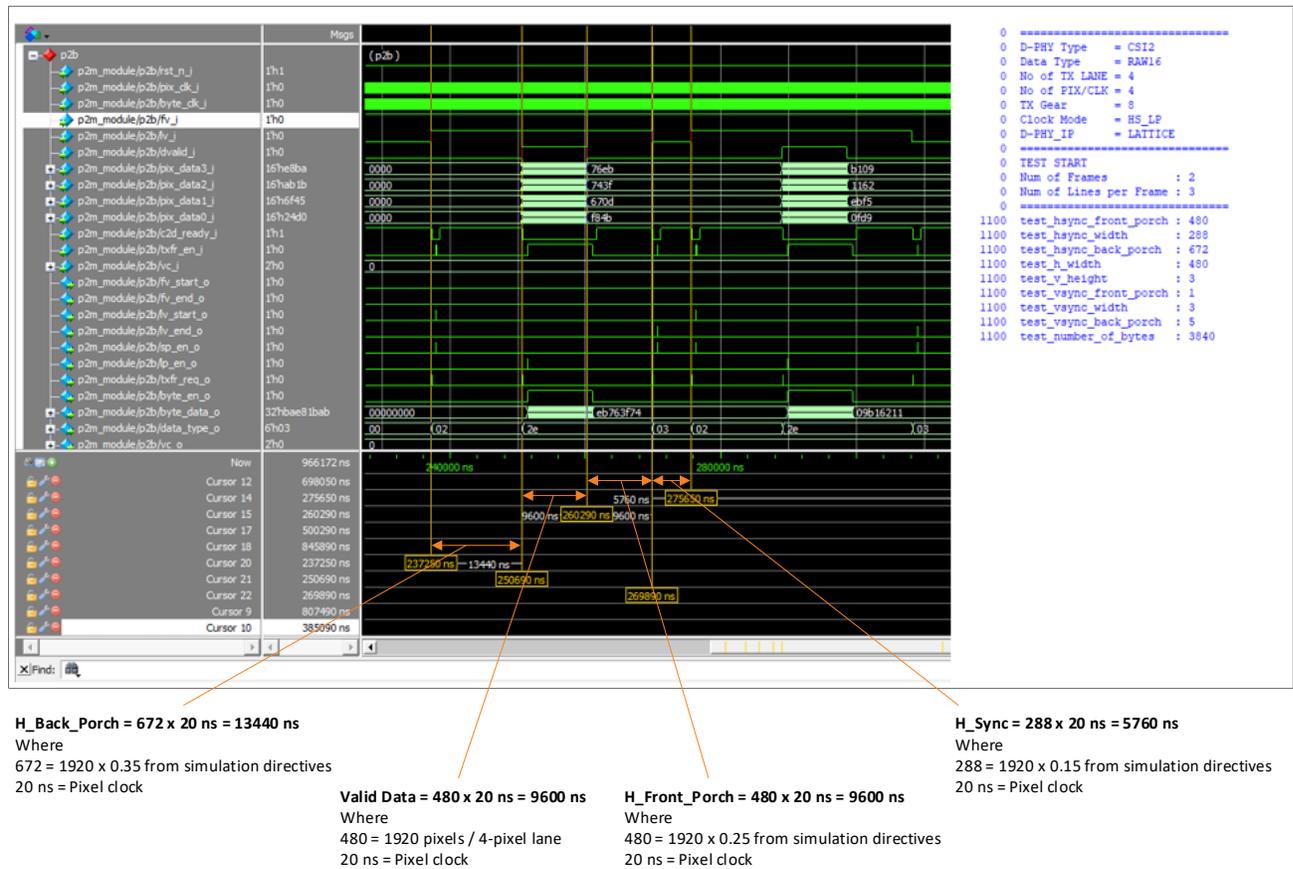
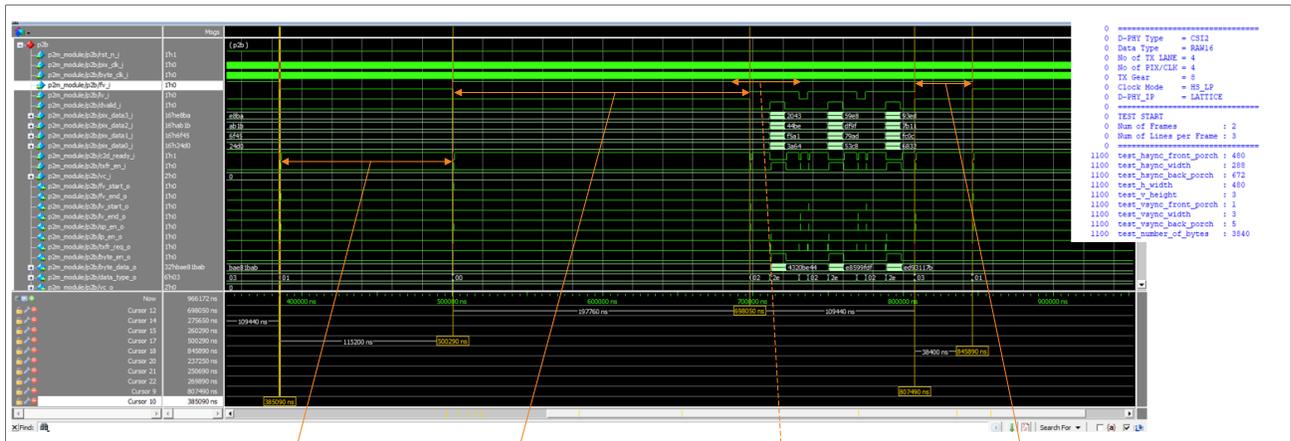


Figure 6.8. CSI-2 Horizontal Blanking Behavior with Simulation Directives

The figure below shows each frame is composed of vertical blanking (VSYNC, VBLANK, VFRONT) and lines.



**V\_Sync = 3 x 38400 ns = 115200 ns**  
Where  
3 = Set from simulation directives  
38400 ns = Total delay per line

**V\_Back\_Porch = 5 x 38400 ns = 192000 ns**  
Where  
5 = Set from simulation directives  
38400 ns = Total delay per line  
**Note:** Delay from simulation is 197760,  
192000 = 197760 - 5760, where 5760 is Hsync.

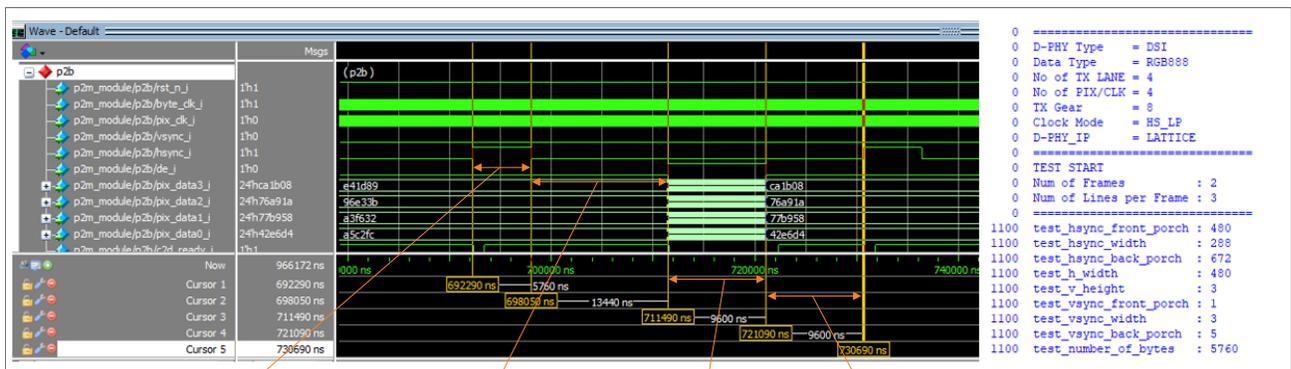
Each line is equal to H-Blanking Period + Valid Data  
13440 + 9600 + 9600 + 5760 = 38400 ns per line  
The vertical blanking period is distributed according to total line delay.

**V\_Front\_Porch = 1 x 38400 ns = 38400 ns**  
Where  
1 = Set from simulation directives  
38400 ns = Total delay per line

Figure 6.9. CSI-2 Vertical Blanking Behavior with Simulation Directives

### 6.2.2. DSI

The figure below shows each line is composed of horizontal blanking (HSYNC, HBLANK, HFRONT) and valid data.



**H\_Sync = 288 x 20 ns = 5760 ns**  
Where  
288 = 1920 x 0.15 from simulation directives  
20 ns = Pixel clock

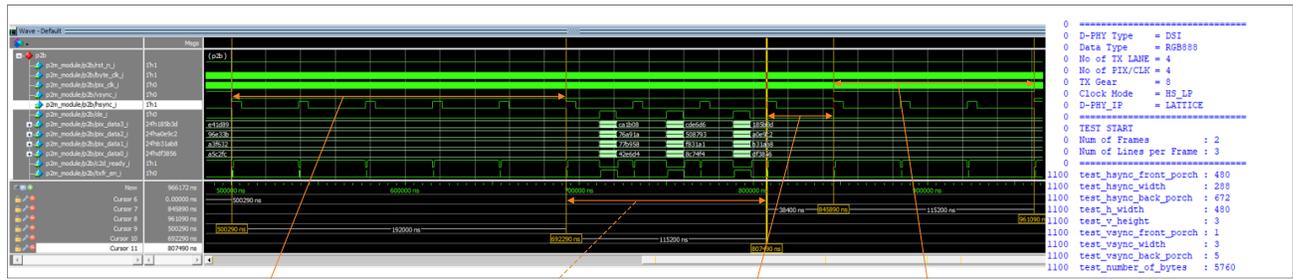
**H\_Back\_Porch = 672 x 20 ns = 13440 ns**  
Where  
672 = 1920 x 0.35 from simulation directives  
20 ns = Pixel clock

**Valid Data = 480 x 20 ns = 9600 ns**  
Where  
480 = 1920 pixels / 4-pixel lane  
20 ns = Pixel clock

**H\_Front\_Porch = 480 x 20 ns = 9600 ns**  
Where  
480 = 1920 x 0.25 from simulation directives  
20 ns = Pixel clock

Figure 6.10. DSI Horizontal Blanking Behavior with Simulation Directives

The figure below shows each frame is composed of vertical blanking (VSYNC, VBLANK, VFRONT) and lines.



**V\_Back\_Porch = 5 x 38400 ns = 192000 ns**  
Where  
5 = Set from simulation directives  
38400 ns = Total delay per line  
**Note:** Delay from simulation is 197760 ns,  
192000 = 197760 - 5760, where 5760 is Hsync.

Each line is equal to H-Blanking Period + Valid Data  
13440 + 9600 + 9600 + 5760 = 38400 ns per line  
Total for all lines = 115200 ns  
The vertical blanking period is distributed  
according to total line delay.

**V\_Front\_Porch = 1 x 38400 ns = 38400 ns**  
Where  
1 = Set from simulation directives  
38400 ns = Total delay per line

**V\_Sync = 3 x 38400 ns = 115200 ns**  
Where  
3 = Set from simulation directives  
38400 ns = Total delay per line

**Figure 6.11. DSI Vertical Blanking Behavior with Simulation Directives**

## 7. Customizing the Reference Design

This section provides examples of customizing the reference design based on common video formats, and shows the calculations and IP settings for these calculations. For other non-calculation IP parameters, for example, CIL Bypass setting for TX D-PHY, refer to the [Pixel-to-Byte \(p2b\)](#) section.

### 7.1. Example 1: CSI-2 – RAW10

Parameter settings:

- 1920x1080p at 60 Hz
- CSI-2 – RAW10
- 4-lane
- 8 gears
- Continuous clock mode
- 1 pixel lane
- Hard D-PHY (internal PLL mode)

**Table 7.1. Reference Design Parameter Calculation**

Parameter	Description
Total Horizontal and Vertical Resolution <sup>1</sup>	Total Horizontal (active pixel in a line + horizontal blanking) = 2200 Total Vertical (active lines + vertical blanking) = 1125
Pixel Clock Frequency	Pixel Clock Frequency = Total Horizontal × Total Vertical × Frame Rate = 2200 × 1125 × 60 = 148.5 MHz
Total Bandwidth	Total Bandwidth = Pixel Clock Frequency × Bits Per Pixel = 1.485 Gbps where RAW10 has 10 bits per pixel
Line Rate	Line Rate = BW/Number of TX Lanes = 371.25 Mbps
Byte Clock Frequency	Byte Clock Frequency = Line Rate/8 = 46.4025 MHz Or Using the calculation described in <a href="#">Table 3.1</a> , Byte Clock Frequency = (Pixel Clock Frequency × Number of Pixel Lanes × Bits Per Pixel)/(TX Gear × Number of TX Lanes) = (148.5 × 1 × 10)/(8 × 4) = 46.4025 MHz
Word Count	Word Count = 1920 × (10/8) = 2400 bytes
Reference Clock	Reference Clock = Pixel Clock Frequency = 148.5 MHz

**Note:**

1. For details on the common video format, refer to the [MIPI D-PHY Bandwidth Matrix and Implementation User Guide \(FPGA-TN-02090\)](#).

The following figures show the IP settings.

Property	Value
<b>General</b>	
Data Type	RAW10
<b>Pixel Interface</b>	
Number of Input Pixel Lanes	1
Pixel Clock Frequency (MHz) [10 - 200]	148.5
Enable AXI4-Stream Receiver Interface	OFF
Receiver Data Rate (Mbps)	1485
<b>Byte Interface</b>	
TX Interface	CSI2
DSI Mode	Non-Burst Pulses
Number of TX Lanes	4
TX Gear	8
Byte Clock Frequency (MHz) [10 - 200]	46.40625
Enable AXI4-Stream Transmitter Interface	OFF
Transmitter Data Rate (Mbps)	1485
<b>Miscellaneous</b>	
Enable APB Interface	OFF
Enable Handshake Signals	<input checked="" type="checkbox"/>
Enable Line Valid Mask Signals	OFF
<b>FIFO</b>	
Word Count [5 - 65535]	2400
Manual Adjust	<input type="checkbox"/>
Read Delay [1 - 65535]	4
FIFO Depth [8 - 65536]	512

Figure 7.1. Pixel-to-Byte IP Configuration

Property	Value
<b>General</b>	
<b>Transmitter</b>	
TX Interface Type	CSI-2
D-PHY TX IP	Hard D-PHY
Number of TX Lanes	4
TX Gear	8
CIL Bypass	<input checked="" type="checkbox"/>
Bypass Packet Formatter	<input type="checkbox"/>
Enable LMMI Interface	<input type="checkbox"/>
Enable AXI4-Stream Interface	<input type="checkbox"/>
Enable Periodic Skew Calibration	<input type="checkbox"/>
<b>Protocol</b>	
Enable Frame Number Increment in Packet Formatter	<input checked="" type="checkbox"/>
Frame Number MAX Value Increment in Packet Formatter [1 - 255]	255
Enable Line Number Increment in Packet Formatter	<input checked="" type="checkbox"/>
Extended Virtual Channel ID	<input type="checkbox"/>
<b>Clock</b>	
Target TX Line Rate (Mbps per Lane) [160 - 1500]	371.25
Target TX Data Rate (Mbps)	1485
Target D-PHY Clock Frequency (MHz)	185.625
Target Byte Clock Frequency (MHz)	46.40625
D-PHY Clock Mode	Continuous
Enable Manual Control of D-PHY Clock	<input type="checkbox"/>
D-PHY PLL Mode	Internal
Reference Clock Frequency (MHz) [24 - 200]	148.5
Actual D-PHY TX Data Rate (Mbps)	1485
Actual TX Line Rate (Mbps)	371.25
Actual D-PHY Clock Frequency (MHz)	185.625
Actual Byte Clock Frequency (MHz)	46.40625
Deviation from Target Data Rate	0.00 %
<b>Initialization</b>	
<b>Miscellaneous</b>	
Enable Miscellaneous Status Signals	<input checked="" type="checkbox"/>

Figure 7.2. TX D-PHY IP Configuration

The following tables show the settings for the synthesis and simulation directives.

**Table 7.2. Synthesis Directives Settings**

Category	Directive
D-PHY Type	TX_CS12
Video Data Type	RAW10
Number of TX Lane	NUM_TX_LANE_4
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_1
TX D-PHY Clock Gear	TX_GEAR_8
Number of Pixels	1920
Clock Mode	CLK_MODE_HS_ONLY
PLL Mode	PLL_INTERNAL
D-PHY IP	DPHY_HARD

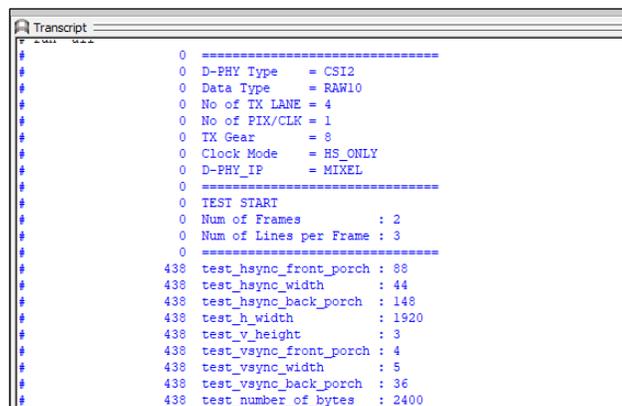
**Table 7.3. Simulation Directives Settings**

Category	Directive
Pixel clock period	6.734
Number of video frames	2
Number of lines per frame	3
Horizontal Front Porch	88
Number of cycles HSYNC signal asserted	44
Horizontal Back Porch	148
Vertical Front Porch	4
Number of lines VSYNC signal asserted	5
Vertical Back Porch	36

**Note:**

1. The blanking period of full HD 1920x1080p at 60 Hz is distributed as 280 pixels for horizontal blanking (88 – Hfront, 44 – HSync, 148 – Hback) and 45 lines for vertical blanking (4 – Vfront, 5 – VSync, 36 – Vback).

The following figures show the simulation results.



```

#
#
# 0 =====
# 0 D-PHY Type = CS12
# 0 Data Type = RAW10
# 0 No of TX LANE = 4
# 0 No of PIX/CLK = 1
# 0 TX Gear = 8
# 0 Clock Mode = HS_ONLY
# 0 D-PHY_IP = MIXEL
# 0 =====
# 0 TEST START
# 0 Num of Frames : 2
# 0 Num of Lines per Frame : 3
# 0 =====
# 438 test_hsync_front_porch : 88
# 438 test_hsync_width : 44
# 438 test_hsync_back_porch : 148
# 438 test_h_width : 1920
# 438 test_v_height : 3
# 438 test_vsync_front_porch : 4
# 438 test_vsync_width : 5
# 438 test_vsync_back_porch : 36
# 438 test_number_of_bytes : 2400
#

```

**Figure 7.3. Simulation Results**

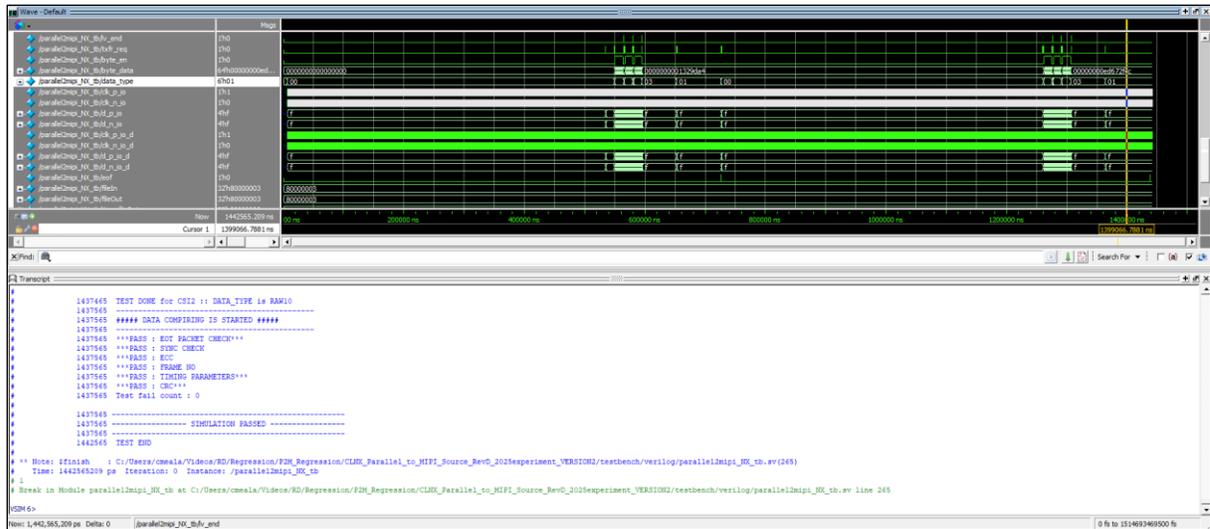


Figure 7.4. Simulation Waveforms

## 7.2. Example 2: CSI-2 – RAW16

Parameter settings:

- 1920x1080p at 60 Hz
- CSI-2 – RAW16
- 4-lane
- 8 gears
- Non-continuous clock mode
- 4 pixel lane
- Hard D-PHY (external PLL mode)

Table 7.4. Reference Design Parameter Calculation

Parameter	Description
Total Horizontal and Vertical Resolution <sup>1</sup>	Total Horizontal (active pixel in a line + horizontal blanking) = 2200 Total Vertical (active lines + vertical blanking) = 1125
Pixel Clock Frequency	At 1 pixel lane, Pixel Clock Frequency = Total Horizontal × Total Vertical × Frame Rate = 2200 × 1125 × 60 = 148.5 MHz At 4 pixel lanes, Pixel Clock Frequency = 148.5 MHz/4 = 37.125 MHz
Total Bandwidth	Total Bandwidth = Pixel Clock Frequency × Bits Per Pixel = 2376 Mbps where RAW16 has 16 bits per pixel
Line Rate	Line Rate = BW/Number of TX Lanes = 594 Mbps
Byte Clock Frequency	Byte Clock Frequency = Line Rate/8 = 74.25 MHz Or Using the calculation described in Table 3.1, Byte Clock Frequency = (Pixel Clock Frequency × Number of Pixel Lanes × Bits Per Pixel)/(TX Gear × Number of TX Lanes) = (37.125 × 4 × 16)/(8 × 4) = 74.25 MHz
Word Count	Word Count = 1920 × (16/8) = 3840 bytes
Reference Clock	Reference Clock = Pixel Clock Frequency at 4 pixel lanes = 37.125 MHz
External PLL Primary Clock Output	The line rate identified is 594 Mbps. The primary clock output must be set to 594 MHz. The secondary clock output is not used for external PLL with Hard D-PHY.
External PLL Reference Clock	This is the same as the Pixel Clock Frequency, 37.125 MHz.

Note:

1. For details on the common video format, refer to the [MIPI D-PHY Bandwidth Matrix and Implementation User Guide \(FPGA-TN-02090\)](#).

The following figures show the IP settings.

Property	Value
<b>General</b>	
Configuration Mode	Frequency
Set Parameter Optimization Target	Minimum Jitter (Higher VCO)
Enable Fractional-N Divider	<input type="checkbox"/>
Enable Spread Spectrum Clock Generation	<input type="checkbox"/>
Enable User Feedback Clock	<input type="checkbox"/>
Enable Internal Path Switching	<input type="checkbox"/>
VCO Frequency [800 - 1600]	1188
<b>Reference Clock</b>	
CLKI: Frequency (MHz) [18 - 800]	37.125
CLKI: Divider Actual Value [1 - 44]	1
Phase Detector Frequency (MHz) [18 - 500]	37.125
Enable Reference Clock Monitor	<input type="checkbox"/>
<b>Feedback</b>	
CLKFB: Feedback Mode	INTCLKOP
CLKFB: FBK Divider Actual Value (Integer) [1 - 128]	16
<b>Primary Clock Output</b>	
CLKOP: Bypass	<input type="checkbox"/>
CLKOP: Frequency Desired Value (MHz) [10 - 800]	594
CLKOP: Divider Actual Value [1 - 128]	2
CLKOP Tolerance (%)	0.0
CLKOP: ERROR (PPM)	0
CLKOP: Enable Trim for CLKOP	<input type="checkbox"/>
<b>Secondary Clock Output</b>	
Secondary Clock Output (2)	
Secondary Clock Output (3)	
Secondary Clock Output (4)	
Secondary Clock Output (5)	

Figure 7.5. PLL IP Configuration

Property	Value
<b>General</b>	
Data Type	RAW16
<b>Pixel Interface</b>	
Number of Input Pixel Lanes	4
Pixel Clock Frequency (MHz) [10 - 200]	37.125
Enable AXI4-Stream Receiver Interface	OFF
Receiver Data Rate (Mbps)	2376
<b>Byte Interface</b>	
TX Interface	CSI2
DSI Mode	Non-Burst Pulses
Number of TX Lanes	4
TX Gear	8
Byte Clock Frequency (MHz) [10 - 200]	74.25
Enable AXI4-Stream Transmitter Interface	OFF
Transmitter Data Rate (Mbps)	2376
<b>Miscellaneous</b>	
Enable APB Interface	OFF
Enable Handshake Signals	<input type="checkbox"/>
Enable Line Valid Mask Signals	OFF
<b>FIFO</b>	
Word Count [2 - 65535]	3840
Manual Adjust	<input type="checkbox"/>
Read Delay [1 - 65535]	4
FIFO Depth [8 - 65536]	512

Figure 7.6. Pixel-to-Byte IP Configuration

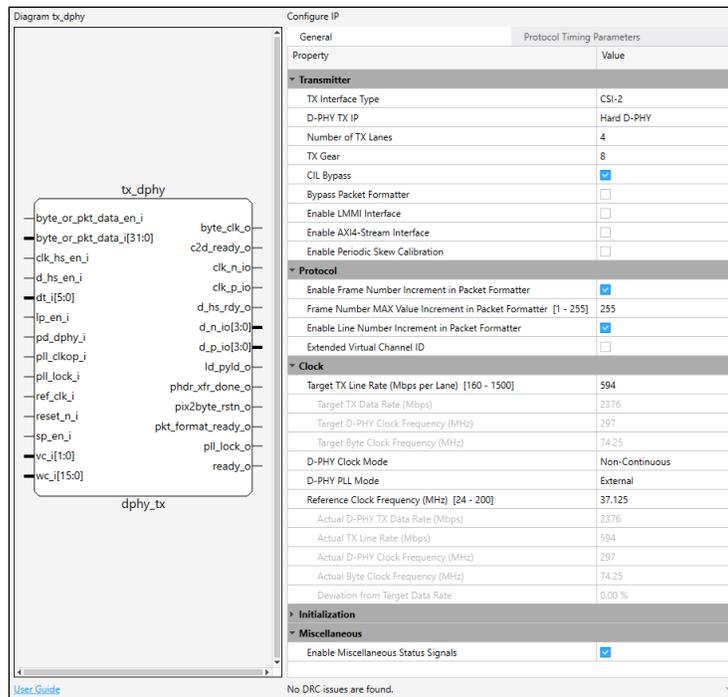


Figure 7.7. TX D-PHY IP Configuration

The following tables show the settings for the synthesis and simulation directives.

Table 7.5. Synthesis Directives Settings

Category	Directive
D-PHY Type	TX_CSI2
Video Data Type	RAW16
Number of TX Lane	NUM_TX_LANE_4
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_4
TX D-PHY Clock Gear	TX_GEAR_8
Number of Pixels	1920
Clock Mode	CLK_MODE_HS_LP
PLL Mode	PLL_EXTERNAL
D-PHY IP	DPHY_HARD

Table 7.6. Simulation Directives Settings

Category	Directive
Pixel clock period	26.936
Number of video frames	2
Number of lines per frame	3
Horizontal Front Porch	88
Number of cycles HSYNC signal asserted	44
Horizontal Back Porch	148
Vertical Front Porch	4
Number of lines VSYNC signal asserted	5
Vertical Back Porch	36

**Note:**

- The blanking period of full HD 1920x1080p at 60 Hz is distributed as 280 pixels for horizontal blanking (88 – Hfront, 44 – Hsync, 148 – Hback) and 45 lines for vertical blanking (4 – Vfront, 5 – Vsync, 36 – Vback).

The following figures show the simulation results.

```

Transcript
#
# =====
# 0 D-PHY Type = CSI2
# 0 Data Type = RAW16
# 0 No of TX LANE = 4
# 0 No of PIX/CLK = 4
# 0 TX Gear = 8
# 0 Clock Mode = HS_LP
# 0 D-PHY_IP = MIXEL
# 0 =====
# 0 TEST START
# 0 Num of Frames : 2
# 0 Num of Lines per Frame : 3
# 0 =====
# 1455 test_hsync_front_porch : 88
# 1455 test_hsync_width : 44
# 1455 test_hsync_back_porch : 148
# 1455 test_h_width : 480
# 1455 test_v_height : 3
# 1455 test_vsync_front_porch : 4
# 1455 test_vsync_width : 5
# 1455 test_vsync_back_porch : 36
# 1455 test_number_of_bytes : 3840
#
    
```

Figure 7.8. Simulation Results

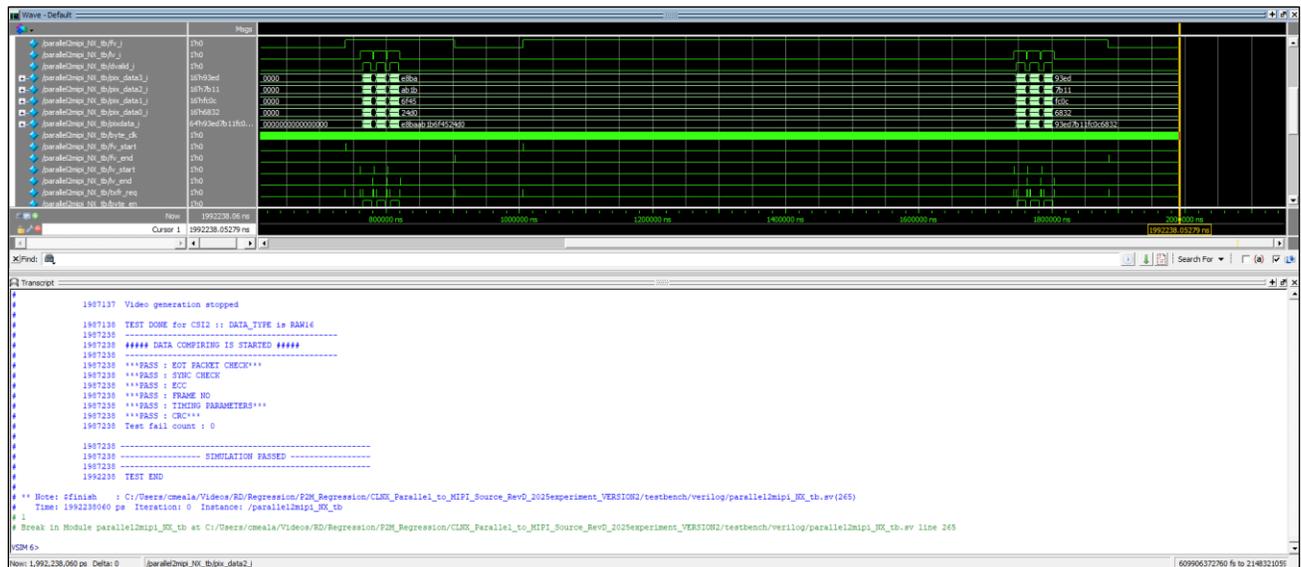


Figure 7.9. Simulation Waveforms

### 7.3. Example 3: DSI – RGB888

Parameter settings:

- 1920x1080p at 60 Hz
- DSI – RGB888
- 4-lane
- 16 gears
- Continuous clock mode
- 4 pixel lanes
- Hard D-PHY (internal PLL mode)

Table 7.7. Reference Design Parameter Calculation

Parameter	Description
Total Horizontal and Vertical Resolution <sup>1</sup>	Total Horizontal (active pixel in a line + horizontal blanking) = 2200 Total Vertical (active lines + vertical blanking) = 1125

Parameter	Description
Pixel Clock Frequency	At 1 pixel lane, Pixel Clock Frequency = Total Horizontal × Total Vertical × Frame Rate = 2200 × 1125 × 60 = 148.5 MHz At 4 pixel lanes, Pixel Clock Frequency = 148.5 MHz/4 = 37.125 MHz
Total Bandwidth	Total Bandwidth = Pixel Clock Frequency × Bits Per Pixel = 3564 Mbps where RGB888 has 24 bits per pixel
Line Rate	Line Rate = BW/Number of TX Lanes = 891 Mbps
Byte Clock Frequency	Byte Clock Frequency = Line Rate/16 = 55.69 MHz Or Using the calculation described in <a href="#">Table 3.1</a> , Byte Clock Frequency = (Pixel Clock Frequency × Number of Pixel Lanes × Bits Per Pixel)/(TX Gear × Number of TX Lanes) = (37.125 × 4 × 24)/(16 × 4) = 55.69 MHz
Word Count	Word Count = 1920 × (24/8) = 5760 bytes
Reference Clock	Reference Clock = Pixel Clock Frequency at 4 pixel lanes = 37.125 MHz

**Note:**

- For details on the common video format, refer to the [MIPI D-PHY Bandwidth Matrix and Implementation User Guide \(FPGA-TN-02090\)](#).

The following figures show the IP settings.

The screenshot displays the configuration interface for the 'p2b' IP block. On the left, a block diagram shows the 'p2b' block with inputs like 'byte\_clk\_i', 'c2d\_ready\_i', 'de\_i', 'hsync\_i', 'pix\_clk\_i', 'pix\_data0\_i[23:0]', 'pix\_data1\_i[23:0]', 'pix\_data2\_i[23:0]', 'pix\_data3\_i[23:0]', 'rst\_n\_i', 'txfr\_en\_i', 'vc\_i[1:0]', and 'vsync\_i'. It also shows outputs like 'byte\_data\_o[63:0]', 'byte\_en\_o', 'data\_type\_o[5:0]', 'fifo\_empty\_o', 'fifo\_full\_o', 'fifo\_overflow\_o', 'fifo\_underflow\_o', 'hsync\_end\_o', 'hsync\_start\_o', 'lp\_en\_o', 'sp\_en\_o', 'txfr\_req\_o', 'vc\_o[1:0]', 'vsync\_end\_o', 'vsync\_start\_o', and 'wc\_o[15:0]'. The right pane, titled 'Configure IP', lists properties and their values:

Property	Value
<b>General</b>	
Data Type	RGB888
<b>Pixel Interface</b>	
Number of Input Pixel Lanes	4
Pixel Clock Frequency (MHz) [10 - 200]	37.125
Enable AXI4-Stream Receiver Interface	OFF
Receiver Data Rate (Mbps)	3564
<b>Byte Interface</b>	
TX Interface	DSI
DSI Mode	Non-Burst Events
Number of TX Lanes	4
TX Gear	16
Byte Clock Frequency (MHz) [10 - 200]	55.69
Enable AXI4-Stream Transmitter Interface	OFF
Transmitter Data Rate (Mbps)	3564.16
<b>Miscellaneous</b>	
Enable APB Interface	OFF
Enable Handshake Signals	<input checked="" type="checkbox"/>
Enable Line Valid Mask Signals	OFF
<b>FIFO</b>	
Word Count [3 - 65535]	5760
Manual Adjust	<input type="checkbox"/>
Read Delay [1 - 65535]	4
FIFO Depth [8 - 65536]	512

At the bottom of the configuration pane, it states 'No DRC issues are found.'

**Figure 7.10. Pixel-to-Byte IP Configuration**

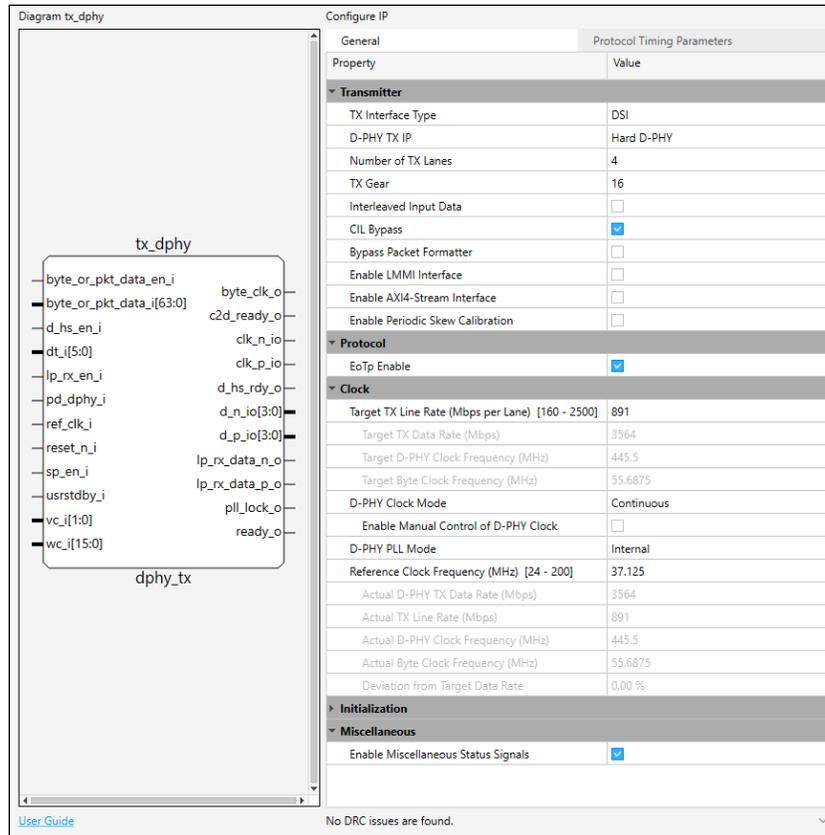


Figure 7.11. TX D-PHY IP Configuration

The following tables show the settings for the synthesis and simulation directives.

Table 7.8. Synthesis Directives Settings

Category	Directive
D-PHY Type	TX_DSI
Video Data Type	RGB888
Number of TX Lane	NUM_TX_LANE_4
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_4
TX D-PHY Clock Gear	TX_GEAR_16
Number of Pixels	1920
Clock Mode	CLK_MODE_HS_ONLY
PLL Mode	PLL_INTERNAL
D-PHY IP	DPHY_HARD

Table 7.9. Simulation Directives Settings

Category	Directive
Pixel clock period	26.936
Number of video frames	2
Number of lines per frame	3
Horizontal Front Porch	88
Number of cycles HSYNC signal asserted	44
Horizontal Back Porch	148
Vertical Front Porch	4



- 4 pixel lanes
- Soft D-PHY (external PLL mode)

**Table 7.10. Reference Design Parameter Calculation**

Parameter	Description
Total Horizontal and Vertical Resolution <sup>1</sup>	Total Horizontal (active pixel in a line + horizontal blanking) = 2200 Total Vertical (active lines + vertical blanking) = 1125
Pixel Clock Frequency	At 1 pixel lane, Pixel Clock Frequency = Total Horizontal × Total Vertical × Frame Rate = 2200 × 1125 × 60 = 148.5 MHz At 4 pixel lanes, Pixel Clock Frequency = 148.5 MHz/4 = 37.125 MHz
Total Bandwidth	Total Bandwidth = Pixel Clock Frequency × Bits Per Pixel = 2673 Mbps where RGB666 has 18 bits per pixel
Line Rate	Line Rate = BW/Number of TX Lanes = 668.25 Mbps
Byte Clock Frequency	Byte Clock Frequency = Line Rate/8 = 83.53125 MHz Or Using the calculation described in <a href="#">Table 3.1</a> , Byte Clock Frequency = (Pixel Clock Frequency × Number of Pixel Lanes × Bits Per Pixel)/(TX Gear × Number of TX Lanes) = (37.125 × 4 × 18)/(8 × 4) = 83.53125 MHz
Word Count	Word Count = 1920 × (18/8) = 4320 bytes
Reference Clock	Reference Clock = Pixel Clock Frequency at 4 pixel lanes = 37.125 MHz
External PLL Primary Clock Output	The byte clock frequency is set to 594 Mbps. The primary clock and secondary clock outputs must be set to Byte Clock Frequency × 4 = 334.125 MHz.
External PLL Reference Clock	This is the same as the Pixel Clock Frequency, 37.125 MHz.

**Note:**

1. For details on the common video format, refer to the [MIPI D-PHY Bandwidth Matrix and Implementation User Guide \(FPGA-TN-02090\)](#).

The following figures show the IP settings.

Property	Value
<b>General</b>	
Configuration Mode	Frequency
Set Parameter Optimization Target	Minimum Jitter (Higher VCO)
Enable Fractional-N Divider	<input type="checkbox"/>
Enable Spread Spectrum Clock Generation	<input type="checkbox"/>
Enable User Feedback Clock	<input type="checkbox"/>
Enable Internal Path Switching	<input type="checkbox"/>
VCO Frequency [800 - 1600]	1002.375
<b>Reference Clock</b>	
CLKI: Frequency (MHz) [18 - 800]	37.125
CLKI: Divider Actual Value [1 - 44]	1
Phase Detector Frequency (MHz) [18 - 500]	37.125
Enable Reference Clock Monitor	<input type="checkbox"/>
<b>Feedback</b>	
<b>Primary Clock Output</b>	
CLKOP: Bypass	<input type="checkbox"/>
CLKOP: Frequency Desired Value (MHz) [10 - 800]	334.125
CLKOP: Divider Actual Value [1 - 128]	3
CLKOP Tolerance (%)	0.0
CLKOP: ERROR (PPM)	0
CLKOP: Enable Trim for CLKOP	<input type="checkbox"/>
<b>Secondary Clock Output</b>	
CLKOS: Enable	<input checked="" type="checkbox"/>
CLKOS: Bypass	<input type="checkbox"/>
CLKOS: Frequency Desired Value (MHz) [6.25 - 800]	334.125
CLKOS: Divider Actual Value [1 - 128]	3
CLKOS Tolerance (%)	0.0
CLKOS: ERROR (PPM)	0
CLKOS: Static Phase Shift (Degrees)	90
CLKOS: Enable Trim for CLKOS	<input type="checkbox"/>
<b>Secondary Clock Output (2)</b>	

No DRC issues are found.

Figure 7.14. PLL IP Configuration

Property	Value
<b>General</b>	
Data Type	RGB666
<b>Pixel Interface</b>	
Number of Input Pixel Lanes	4
Pixel Clock Frequency (MHz) [10 - 200]	37.125
Enable AXI4-Stream Receiver Interface	OFF
Receiver Data Rate (Mbps)	2673
<b>Byte Interface</b>	
TX Interface	DSI
DSI Mode	Non-Burst Events
Number of TX Lanes	4
TX Gear	8
Byte Clock Frequency (MHz) [10 - 200]	83.53125
Enable AXI4-Stream Transmitter Interface	OFF
Transmitter Data Rate (Mbps)	2673
<b>Miscellaneous</b>	
Enable APB Interface	OFF
Enable Handshake Signals	<input type="checkbox"/>
Enable Line Valid Mask Signals	OFF
<b>FIFO</b>	
Word Count [9 - 65535]	4320
Manual Adjust	<input type="checkbox"/>
Read Delay [1 - 65535]	4
FIFO Depth [8 - 65536]	512

No DRC issues are found.

Figure 7.15. Pixel-to-Byte IP Configuration

The screenshot shows the configuration interface for the TX D-PHY IP. On the left, a block diagram of the 'tx\_dphy' block is visible, showing its various input and output pins. On the right, the 'Configure IP' window is open, showing the configuration parameters for the IP. The 'General' tab is selected, and the 'Protocol Timing Parameters' section is expanded. The configuration parameters are as follows:

Property	Value
<b>Transmitter</b>	
TX Interface Type	DSI
D-PHY TX IP	Soft D-PHY
Number of TX Lanes	4
TX Gear	8
Bypass Packet Formatter	<input type="checkbox"/>
Enable LMMI Interface	<input type="checkbox"/>
Enable AXI4-Stream Interface	<input type="checkbox"/>
<b>Protocol</b>	
EoTp Enable	<input checked="" type="checkbox"/>
<b>Clock</b>	
Target TX Line Rate (Mbps per Lane) [160 - 1500]	668.25
Target TX Data Rate (Mbps)	2673
Target D-PHY Clock Frequency (MHz)	334.125
Target Byte Clock Frequency (MHz)	83.53125
D-PHY Clock Mode	Non-Continuous
D-PHY PLL Mode	External
Enable Edge Clock Synchronizer and Divider	<input checked="" type="checkbox"/>
Reference Clock Frequency (MHz) [24 - 200]	37.125
<b>Initialization</b>	
Enable tINIT Counter	<input type="checkbox"/>
tINIT Counter Value (Number of Byte Clock Cycles) [1 - 32768]	1000
tINIT Counter Value in ns	0
<b>Miscellaneous</b>	
Enable Miscellaneous Status Signals	<input checked="" type="checkbox"/>

Figure 7.16. TX D-PHY IP Configuration

The following tables show the settings for the synthesis and simulation directives.

Table 7.11. Synthesis Directives Settings

Category	Directive
D-PHY Type	TX_DSI
Video Data Type	RGB666
Number of TX Lane	NUM_TX_LANE_4
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_4
TX D-PHY Clock Gear	TX_GEAR_8
Number of Pixels	1920
Clock Mode	CLK_MODE_HS_LP
PLL Mode	PLL_EXTERNAL
D-PHY IP	DPHY_SOFT

Table 7.12. Synthesis Directives Settings

Category	Directive
Pixel clock period	26.936
Number of video frames	2
Number of lines per frame	3
Horizontal Front Porch	88
Number of cycles HSYNC signal asserted	44
Horizontal Back Porch	148
Vertical Front Porch	4

Category	Directive
Number of lines VSYNC signal asserted	5
Vertical Back Porch	36

**Note:**

- The blanking period of full HD 1920x1080p at 60 Hz is distributed as 280 pixels for horizontal blanking (88 – Hfront, 44 – HSync, 148 – Hback) and 45 lines for vertical blanking (4 – Vfront, 5 – VSync, 36 – Vback).

The following figures show the simulation results.

```

Transcript
# =====
# 0 D-PHY Type = DSI
# 0 Data Type = RGB666
# 0 No of TX LANE = 4
# 0 No of PIX/CLK = 4
# 0 TX Gear = 8
# 0 Clock Mode = HS_LP
# 0 D-PHY_IP = LATTICE
# =====
# 0 TEST START
# 0 Num of Frames : 2
# 0 Num of Lines per Frame : 3
# =====
# 1455 test_hsync_front_porch : 88
# 1455 test_hsync_width : 44
# 1455 test_hsync_back_porch : 148
# 1455 test_h_width : 480
# 1455 test_v_height : 3
# 1455 test_vsync_front_porch : 4
# 1455 test_vsync_width : 5
# 1455 test_vsync_back_porch : 36
# 1455 test_number_of_bytes : 4320
    
```

Figure 7.17. Simulation Results

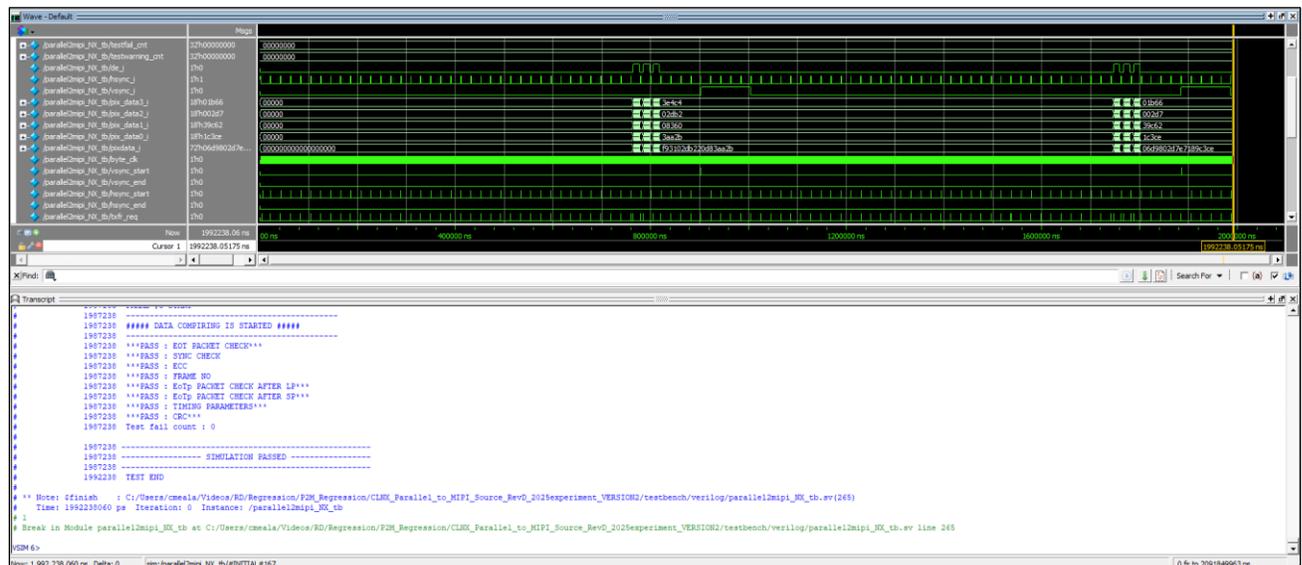


Figure 7.18. Simulation Waveforms

## 8. Resource Utilization

Resource utilization depends on the configuration used. [Table 8.1](#) shows resource utilization examples under certain configurations targeting the LIFCL-40- CABGA400 devices. This is a reference and actual usage varies.

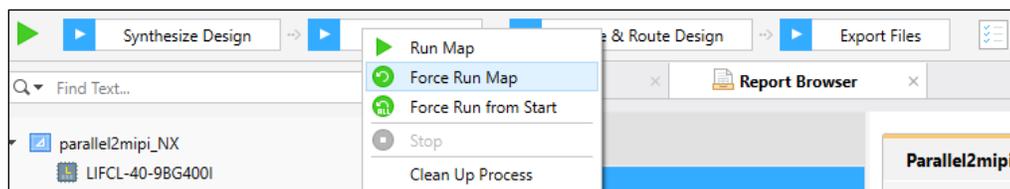
**Table 8.1. Resource Utilization Examples**

Configuration	LUTs	Register	Block RAM
4-lane, Gear 16, Hard D-PHY, DSI, RGB888, 4 pixels/clock	3% (947 out of 32256)	3% (1011 out of 32811)	12% (10 out of 84)
4-lane, Gear 8, Soft D-PHY, DSI, RGB888, 4 Ppixels/clock	3% (834 out of 32256)	2% (765 out of 32811)	10% (8 out of 84)
4-lane, Gear 16, Hard D-PHY, CSI-2, RAW12, 10 pixels/clock	4% (1364 out of 32256)	3% (1044 out of 32811)	17% (14 out of 84)
4-lane, Gear 8, Soft D-PHY, CSI-2, RAW8, 4 pixels/clock	2% (649 out of 32256)	2% (659 out of 32811)	5% (4 out of 84)

To identify the resource utilization for your desired configuration, follow these steps:

1. Customize the reference design based on desired settings. For details on the customization, refer to the [Customizing the Reference Design](#) and [Pixel-to-Byte \(p2b\)](#) sections.
2. Run the design flow until Map Design is complete.
 

**Note:** To verify the IP parameters, you can simulate the design to identify the incorrect IP settings if the simulation fails.



**Figure 8.1. Running MAP Design**

3. The Map Design is complete as shown in the figure below.



**Figure 8.2. Map Design Complete**

4. To check the design summary, go to **View > Reports > Report Browser > Map Reports > Map** or **Map Resource Usage**.

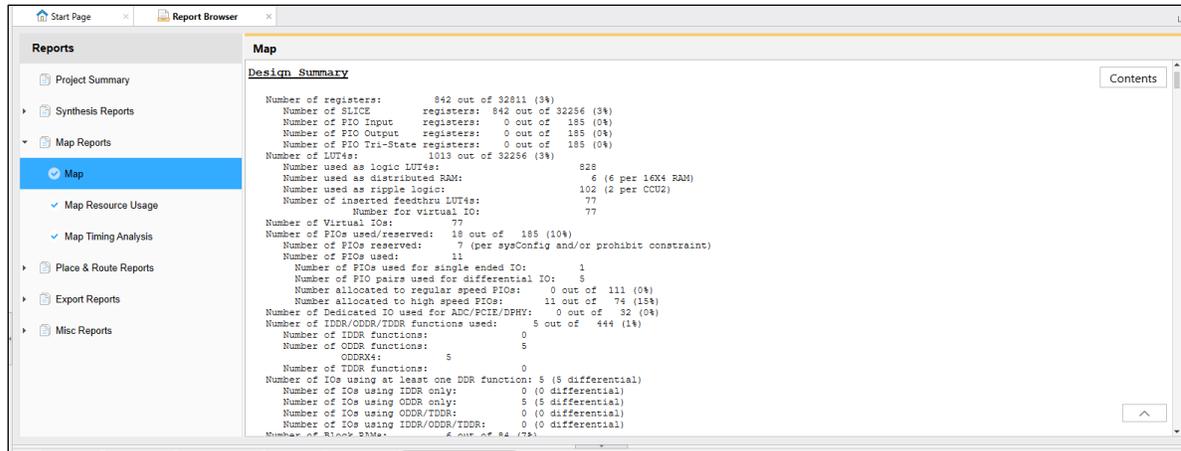


Figure 8.3. Map Report

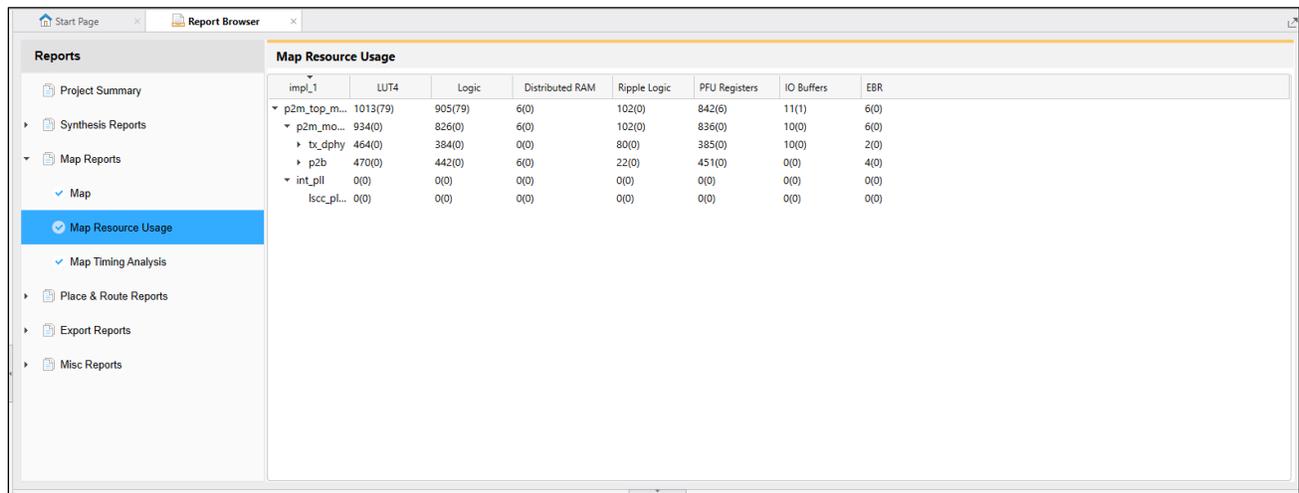


Figure 8.4. Map Resource Usage

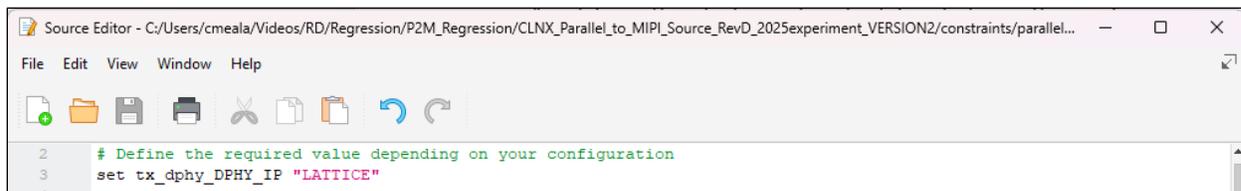
## 9. Reference Design Timing Constraints

As described in the [IP Handshaking](#) section, there are 6 clocks in the design where the logic and modules are synchronized to in the design. Each clock is constrained as described in the table below.

**Table 9.1. Clock Constraints**

Clock	Clock Constraint (.pdc)	Description
pix_clk_i tx_ref_clk External PLL input	set pix_clock_period 26.936 create_clock -name {pix_clk_i} -period \$pix_clock_period [get_ports pix_clk_i]	These three clocks are driven by the same clock port, hence the clocks are all covered in the same create_clock constraint. Refer to the <a href="#">IP Handshaking</a> section for details. This constraint is defined in the .pdc file of the reference design. Depending on your configuration, you must define the clock period for this timing constraint correctly. In this example, the clock period defined is 26.936.
byte_clk	No defined constraint in the .pdc file	This constraint is <u>auto-generated</u> and is inserted directly in the design post synthesis .udb file. You may check the auto-generated constraint in the post synthesis timing constraint editor.
pll_clkop, pll_clkos	No defined constraint in the .pdc file	This constraint is <u>auto-generated</u> and is inserted directly in the design post synthesis .udb file. You may check the auto-generated constraint in the post synthesis timing constraint editor.

Timing exceptions are defined in the design to generate a clean design in timing. False paths are defined to remove asynchronous paths and maximum delays defined on clock-domain crossing (CDC) synchronizers. The timing constraints are defined in the .pdc file while other constraints are automatically added in pre-synthesis for each IP. For timing exceptions defined in the .pdc file, define the D-PHY IP using "LATTICE" for Soft D-PHY and "MIXEL" for Hard D-PHY, and define byte clock period using byte\_clock\_period.

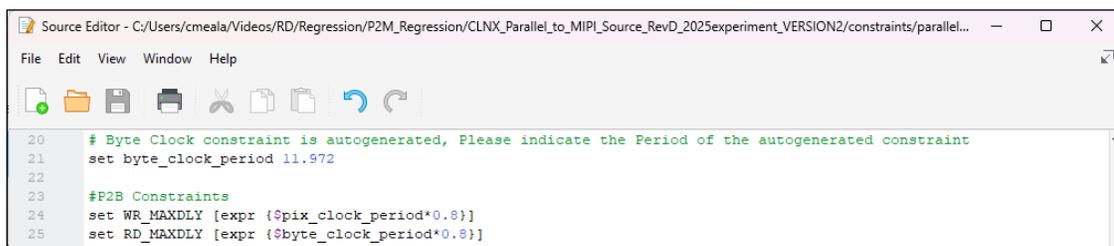


```

2  # Define the required value depending on your configuration
3  set tx_dphy_DPHY_IP "LATTICE"

```

**Figure 9.1. Defining the D-PHY IP in the PDC Constraint File Macros**



```

20  # Byte Clock constraint is autogenerated, Please indicate the Period of the autogenerated constraint
21  set byte_clock_period 11.972
22
23  #P2B Constraints
24  set WR_MAXDLY [expr {$pix_clock_period*0.8}]
25  set RD_MAXDLY [expr {$byte_clock_period*0.8}]

```

**Figure 9.2. Defining the Byte Clock Period in the PDC Constraint File Macros**

## 10. Debugging

This section lists the possible issues and suggested troubleshooting steps that you can follow.

### 10.1. Debug Methods

#### 10.1.1. Simulation Error: PLL won't work

You may encounter this error when you use internal PLL and Hard D-PHY on the reference design. The reference clock of the internal PLL in the Hard D-PHY can only accept clock frequencies in integer numbers between 24 to 200 MHz.

```

Transcript
# 2209 test_vsync_back_porch : 36
# 2209 test_number_of_bytes : 4320
# ERROR : PLL won't work!
# ERROR : error_clkref_range
# ERROR : clkref_period 41670 - clkref_min_period = 5000 - clkref_max_period = 41667
# ERROR : error_clkref_N_range
# ERROR : clkref_N_period 41670 - clkref_N_min_period = 20000 - clkref_N_max_period = 41667
# ERROR : error_clkref_N_M_range
# ERROR : clkref_N_M_period 1158 - clkref_N_M_min_period = 400 - clkref_N_M_max_period = 800
    
```

Figure 10.1. Simulation Error: PLL won't work

For instance, for clock period of 41.66666666 ns, you may encounter PLL error as 41.67 ns is equivalent to ~23.998 MHz. To avoid the PLL error, round off the clock period to 24 MHz.

```

simulation_directives.v
13 */
14
15
16 `define PIX_CLK 41.67
    
```

Figure 10.2. Defining Clock Period

Define the clock period in nanosecond (ns) for PIX\_CLK in the simulation directives when converting the clock period.

#### 10.1.2. Invalid End of Transaction Packet (EoTp)

When utilizing DSI mode in the reference design, you need to enable EoTp in the TX D-PHY IP. Check **EoTp Enable** to enable this feature. Without EoTp enabled, the IP does not insert the EoTp on the PHY transaction on the data lanes. EoTp is equivalent to {ECC[7:0] = x01, Payload Data [15:0] = x0F0F, Virtual Channel = DI [7:6] = 0b00, Data Type = DI [5:0] = 0b001000} as defined in the DSI specification and is aligned with the IP. EoTp is propagated as least significant bit (LSB) first hence seen as 10f0f008 in the simulation.

```

Transcript
# *38410_FRAME #1 START
# *399318 FAIL : EoTp (SP) :: Expected 10f0f08 and Received ffff00ff
# 799318 EoTp bit 0 is invalid
# 799318 EoTp bit 1 is invalid
# 799318 EoTp bit 2 is invalid
# 799318 EoTp bit 4 is invalid
# 799318 EoTp bit 5 is invalid
# 799318 EoTp bit 6 is invalid
# 799318 EoTp bit 7 is invalid
# 799318 EoTp bit 8 is invalid
# 799318 EoTp bit 9 is invalid
# 799318 EoTp bit 10 is invalid
# 799318 EoTp bit 11 is invalid
# 799318 EoTp bit 20 is invalid
# 799318 EoTp bit 21 is invalid
# 799318 EoTp bit 22 is invalid
Now: 814,315,684 ps Delta: 4 (p2m_top_module(fast))
    
```

Figure 10.3. Invalid EoTp in Simulation

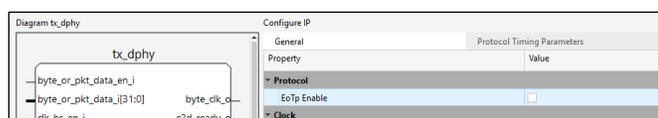


Figure 10.4. Enabling EoTp in TX D-PHY IP

### 10.1.3. D-PHY Timing Parameters Do Not Meet Specification

The D-PHY checker monitors the data lane and clock lane transitions in terms of meeting the D-PHY timing parameters. For example, LPX and HS-Prepare. If the checker detects the transition does not meet the minimum and maximum requirements of each timing parameter, the checker flags that the timing parameter has failed checking.

```

Transcript
#
1987238 -----
1987238 ***FAIL COUNT IN DPHY_CHECKER = 43
1987238 ***PASS : EOT PACKET CHECK***
1987238 ***PASS : SYNC CHECK
1987238 ***PASS : ECC
1987238 ***PASS : FRAME NO
1987238 ***PASS : EOTp PACKET CHECK AFTER LP***
1987238 ***PASS : EOTp PACKET CHECK AFTER SP***
1987238 ***FAIL : TIMING PARAMETERS***
1987238 ***PASS : CRC***
#
1987238 ERROR: Test fail count : 43
#
1987238 -----
1987238 !!!!!!!!!!!!!!! SIMULATION FAILED !!!!!!!!!!!!!!!
1987238 -----
1992238 TEST END
    
```

Figure 10.5. Timing Parameter Failed Checking

To identify the timing parameter that has failed to meet the D-PHY timing parameters, open the *dphy\_checker\_timing.log* generated by the simulation environment. The file is in your current simulation folder. To check for the simulation folder, type *pwd* in the console.

```

Transcript
# 1
# Break in Module parallel2mipi_NX_tb at C:/Users/cmeala/Videos/RD/Regression/P2M_Regression/CLNX_Parallel_to_MIPI_Source_RevD_2025experiment_VERSION2
VSIM 6> pwd
# C:/Users/cmeala/Videos/RD/Regression/P2M_Regression/CLNX_Parallel_to_MIPI_Source_RevD_2025experiment_VERSION2/DPHYTimingParameterError
VSIM 7> ]
Now: 1,992,238,060 ps Delta: 0 sim:/parallel2mipi_NX_tb/#INITIAL#167
    
```

Figure 10.6. Checking for the Simulation Folder

As observed from the log file, HS-Prepare is below the minimum value. To fix the D-PHY, modify the *t\_HS-Prepare* in IP protocol timing parameters. Note that the protocol timing parameters values are based on byte clock period. For instance, for *t\_HS-Prepare* = 5, the protocol timing parameter value is equivalent to  $5 \times 11.97156753$  ns (byte clock period in the figure below) = 59.85. If *t\_HS-Prepare* is set to 4, the protocol timing parameters value is 47.886 ns, which is below the anticipated value in the simulation environment.

```

dphy_checker_timing.log
52 ECC (in hex) = 22
53 HS-Trail = 125
54 ***ERROR*** HS_prepare is 47 but must be minimum 48
55 TIME(end for packet) 63896
56 ☹ _____ ☹
57 Packet received
    
```

Figure 10.7. Example Byte Clock Period

Configure Component from IP dphy\_tx Version 2.3.0  
Set the following parameters to configure this component.

Diagram tx\_dphy

Configure IP

General		Protocol Timing Parameters	
Property		Value	
<b>TX Global Operation Timing Parameters</b>			
Customize TX Timing Parameter Values <input checked="" type="checkbox"/>			
t_LPX [1 - 255]		5	
t_HS-PREPARE [1 - 255]		5	
t_HS_ZERO during skew calibration [1 - 255]		10	
t_HS_ZERO [1 - 255]		10	
t_HS_TRAIL [1 - 255]		11	
t_HS_EXIT [1 - 255]		9	
t_CLK-PREPARE [1 - 255]		4	
t_CLK-ZERO [1 - 255]		22	
t_CLK-PRE [1 - 255]		2	
t_CLK-POST [2 - 255]		12	
t_CLK-TRAIL [2 - 255]		7	
t_CLK-EXIT [1 - 255]		9	
t_SKEWCAL-INIT 2*15UI to 100us [1 - 4097]		4097	
t_SKEWCAL-PERIOD 2*10UI to 10us [1 - 129]		129	

No DRC issues are found.

Figure 10.8. TX D-PHY IP Protocol Timing Parameters

### 10.1.4. Actual and Expected Byte Counts Not Equal

This issue is mainly encountered when word count for the Pixel-to-Byte IP is set to significantly greater than the expected value. For instance, you may define the word count based on the total horizontal pixels instead of total horizontal active pixels. For example, total horizontal pixels for 1920x1080p is 2200 (word count for RAW16 = 4400), while the total horizontal active pixel is 1920 (word count for RAW16 = 3840). The actual and expected byte count numbers are actual number of bytes in the *input\_data.log* and *output\_data.log* respectively.

```

500272 TEST DONE for CSI2 :: DATA_TYPE is RAW16
500372 -----
500372 *** E R R O R: Actual and Expected byte counts are not equal***
500372 **** I N F O : Actual byte Count is 13200
500372 **** I N F O : Expected byte Count is 11520
500372 -----
500372 ***FAIL COUNT IN DPHY_CHECKER = 3
500372 ***PASS : EOT PACKET CHECK***
500372 ***PASS : SYNC CHECK
500372 ***PASS : ECC
500372 ***PASS : FRAME NO
500372 ***PASS : TIMING PARAMETERS***
500372 ***FAIL : CRC***
500372 ERROR: Test fail count : 4

500372 -----
500372 !!!!!!!!!!!!!!!!!!!!! SIMULATION FAILED !!!!!!!!!!!!!!!!!!!!!
500372 -----
    
```

Figure 10.9. Actual and Expected Byte Counts Not Equal

## 11. Known Limitations

The limitations of this reference design are as follows:

- Only the following data types are supported for MIPI DSI interface: RGB888, RGB666.
- Only the following data types are supported for MIPI CSI-2 interface: RGB888, RAW8, RAW10, RAW12 and RAW16.
- The reference design is mainly validated with Soft CIL and Packet Formatter for both Hard D-PHY and Soft D-PHY.
- The reference design is only tested on register transfer level (RTL) simulation. The design is not hardware validated.
- You may encounter a sync error when reaching line rates above 1500 Mbps. This is an expected error as the current simulation environment does not accommodate the delay generated by skewing on the sync. However, the reference design can capture the right data output, and does not affect the overall output of the reference design.

## References

- [MIPI Alliance](#) web page for D-PHY Specifications Version 1.2, Display Serial Interface 2 (DSI) Specifications Version 1.2, Camera Serial Interface 2 (CSI-2) Specifications Version 1.2, and Camera Serial Interface 2 (CSI-2) Specifications Version 2.0
- [Pixel-to-Byte Converter IP User Guide \(FPGA-IPUG-02094\)](#)
- [CSI-2/DSI D-PHY Tx IP User Guide \(FPGA-IPUG-02080\)](#)
- [PLL Module User Guide \(FPGA-IPUG-02063\)](#)
- [MIPI D-PHY Bandwidth Matrix and Implementation User Guide \(FPGA-TN-02090\)](#)
- [CrossLink-NX](#) web page
- [Parallel to MIPI CSI-2 / DSI Display Interface Bridge Reference Design](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

For frequently asked questions, refer to the Lattice Answer Database at [www.latticesemi.com/Support/AnswerDatabase](http://www.latticesemi.com/Support/AnswerDatabase).

## Revision History

### Revision 1.3, January 2026

Section	Change Summary
All	Performed minor formatting and editorial edits.
Abbreviations in This Document	Updated list of abbreviations.
Introduction	<ul style="list-style-type: none"> <li>• Reworked the <i>Supported Device and IP</i> section and renamed to subsection <a href="#">1.1 Quick Facts</a>.</li> <li>• Reworked subsection 1.1 <i>Features List</i> and renamed to subsection <a href="#">1.2 Features</a>.</li> <li>• Renamed subsection 1.4 <i>Conventions</i> to subsection <a href="#">1.3 Naming Conventions</a>.</li> </ul>
Directory Structure and Files	Reworked section 7 <i>Design Package and Project Setup</i> and renamed to section <a href="#">2 Directory Structure and Files</a> .
Functional Description	<ul style="list-style-type: none"> <li>• Reworked subsection 1.2 <i>Block Diagram</i> and subsection 1.3 <i>Functional Description</i>, and renamed to section <a href="#">3 Functional Description</a>.</li> <li>• Reworked section 3 <i>Design and Module Description</i> and renamed to subsection <a href="#">3.1 Design Components</a>.</li> <li>• Added the following subsections: <ul style="list-style-type: none"> <li>• <a href="#">3.2 IP Handshaking</a></li> <li>• <a href="#">3.3 Clocking Scheme</a></li> <li>• <a href="#">3.4 Reset Scheme</a></li> </ul> </li> </ul>
Reference Design Parameter Description	<ul style="list-style-type: none"> <li>• Reworked section 2 <i>Parameters and Port List</i> and renamed to section <a href="#">4 Reference Design Parameter Description</a>.</li> <li>• Reworked subsection 2.1 <i>Synthesis Directives</i> and moved to subsection <a href="#">4.1 Synthesis Directives</a>.</li> <li>• Reworked subsection 2.2 <i>Simulation Directives</i> and moved to subsection <a href="#">4.2 Simulation Directives</a>.</li> </ul>
Signal Description	Reworked subsection 2.3 <i>Top-Level I/O</i> and renamed to section <a href="#">5 Signal Description</a> .
Simulating the Reference Design	Reworked section 5 <i>Design Simulation</i> and renamed to section <a href="#">6 Simulating the Reference Design</a> .
Customizing the Reference Design	Reworked section 4 <i>Design and File Modifications</i> and renamed to section <a href="#">7 Customizing the Reference Design</a> .
Resource Utilization	Reworked section 8 <i>Resource Utilization</i> and moved to section <a href="#">8 Resource Utilization</a> .
Reference Design Timing Constraints	Added this section
Debugging	Added this section.
Known Limitations	Reworked section 6. <i>Known Limitations</i> and moved to section <a href="#">11 Known Limitations</a> .
References	Updated references.

### Revision 1.2, May 2024

Section	Change Summary
All	Renamed the document from <i>Parallel to MIPI with CrossLink-NX</i> to <i>Parallel to MIPI with CrossLink-NX Devices</i> .
Design and Module Description	<ul style="list-style-type: none"> <li>• Updated Figure 3.2. p2b IP Creation in the Lattice Radiant Software.</li> <li>• Updated Figure 3.3. tx_dphy IP Creation in the Lattice Radiant Software.</li> <li>• Removed figure: tx_dphy IP Creation in Lattice Radiant (2/2).</li> <li>• Updated the parameter settings for tINIT Counter in the tx_dphy section.</li> <li>• Updated Figure 3.4. int_pll IP Creation in the Lattice Radiant Software (1/2).</li> <li>• Added Figure 3.5. int_pll IP Creation in the Lattice Radiant Software (2/2).</li> <li>• Updated the description on clkos frequency in the int_pll section.</li> </ul>
Design and File Modifications	Updated the IP versions in the Design and File Modifications section.
Design Simulation	Updated the steps to simulate design in the Design Simulation section.
References	Updated references.

### Revision 1.1, June 2023

Section	Change Summary
Supported Device and IP	<ul style="list-style-type: none"> <li>Updated Compatible IP of LIFCL-40 to 'Pixel-to-Byte Converter IP version 1.4.0'.</li> <li>Updated Compatible IP of LIFCL-17 to 'D-PHY Transmitter IP version 1.7.2'.</li> <li>Updated Lattice Radiant software version to '2022.1'.</li> </ul>
Design and Module Description	<ul style="list-style-type: none"> <li>Updated Figure 3.2. p2b IP Creation in Lattice Radiant to show the p2b version 1.1.0.</li> <li>Updated Figure 3.3. tx_dphy IP Creation in Lattice Radiant (1/2) and Figure 3.4. tx_dphy IP Creation in Lattice Radiant (2/2) to show the tx_dphy version 1.1.3.</li> <li>Updated Figure 3.5. int_pll IP Creation in Lattice Radiant to show the int_pll version 1.2.0.</li> </ul>
Design Simulation	<ul style="list-style-type: none"> <li>Updated Figure 5.1. Script Modification #1, Figure 5.2. Script Modification #2, Figure 5.4. Simulation Waveform for DSI: RGB888, Figure 5.6. Simulation Waveform for DSI: RGB666, Figure 5.8. Simulation Waveform for CSI-2: RAW10, and Figure 5.10. Simulation Waveform for CSI-2: RAW12.</li> <li>Added Figure 5.3. Calculation for DSI: RGB888, Figure 5.5. Calculation for DSI: RGB666, Figure 5.7. Calculation for CSI-2: RAW10, and Figure 5.9. Calculation for CSI-2: RAW12.</li> </ul>
Technical Support Assistance	Added reference link to the Lattice Answer Database.

### Revision 1.0, February 2021

Section	Change Summary
All	Initial release.



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