MachXO3D Slew Rate Control Demo

User Guide

FPGA-UG-02067-1.1

January 2020

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1. Introduction

In electronics, slew rate is defined as the change of voltage or current, or any other electrical quantity, per unit of time.

Electronic circuits may specify minimum or maximum limits on the slew rates for their inputs or outputs, with these limits only valid under some set of given conditions, for example, output loading.

The Lattice Semiconductor MachXO3D™ devices feature single-ended output buffer for each device I/O pin with programmable output slew rate control that can be configured for either low noise, SLEWRATE=SLOW, or high speed, SLEWRATE=FAST, performance. Each I/O pin has an individual slew rate control. This slew rate control affects both rising edge and falling edge. The rise and fall ramp rates for each I/O standard can be found in the device IBIS file for a given I/O configuration. This demo shows how to enable slew rate control features through Lattice Diamond® software.

1.1. Demo Overview

This demo project outputs clocks in the same frequency but with different slew rate settings to two test points for comparison.

This demo covers the following operations:

- Configuring different slew rates in the design
- Programming the board with the design
- Validating the slew rate with hardware test

1.2. MachXO3D Development Board and Resources

Figure 1.1 shows the top side of the MachXO3D Development Board and resources used for this demo.

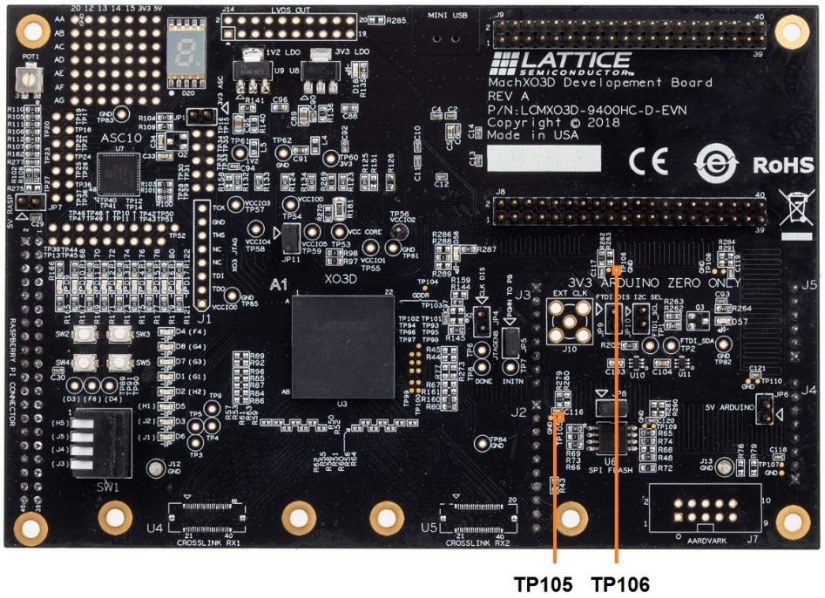

Figure 1.1. MachXO3D Development Board

- **TP105:** Test point for Ball Site M22 to output clock
- **TP106:** Test point for Ball Site B21 to output clock

1.3. Slew Rate Control Demo Circuits on the Board

MachXO3D Development Board reserves circuits to simulate the customer application board with different board sizes or routing trace lengths, with 4-, 8-, or 16-inch configuration, as shown in Figure 1.2. For example, to simulate 16-inch length, you need to populate R280 or R281, and depopulate R279 or R290, then test waveform on TP109. In this demo, the default 4-inch setting is used to show the slew rate control feature. TP105 and TP106 are used.

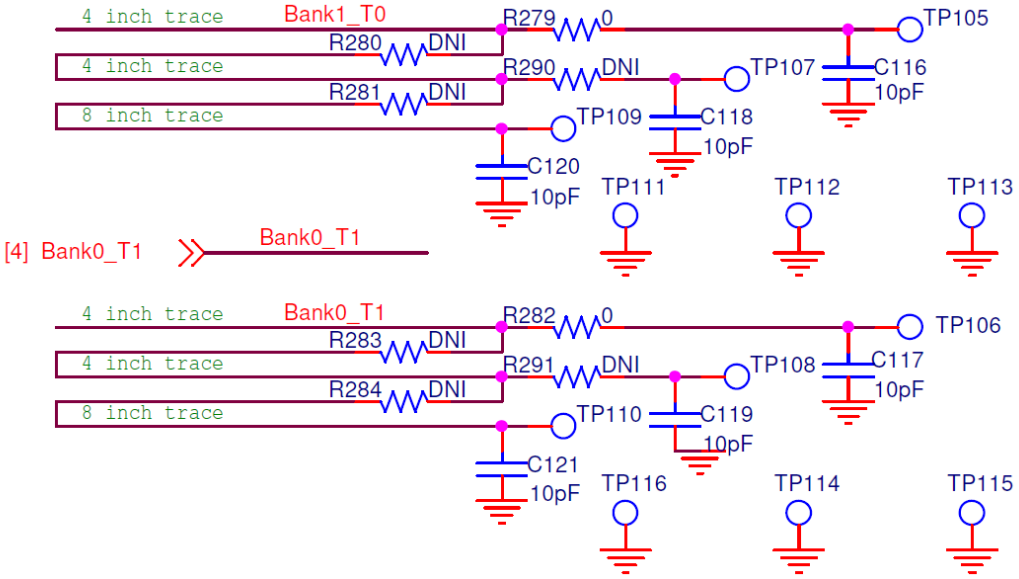

Figure 1.2. Slew Rate Control Demo Circuits

2. Demo Package

2.1. Hardware Requirements

To run the demo, the following hardware are required:

- PC running Windows 7 Operating System
- MachXO3D Development Kit including Mini-USB cable
- Oscilloscope, >200 MHz bandwidth preferred, with at least two probe channels

2.2. Software Requirements

To run the demo, the following software are required:

- MachXO3D Slew Rate Control Demo package
- Lattice Diamond 3.11 or later

Note: The software programs are available at www.latticesemi.com/en/Products/DesignSoftwareAndIP.

3. Demo Package Directory Structure

Figure 3.1 shows the demo package directory structure.

Figure 3.1. Demo Package Directory Structure

4. Running the Slew Rate Control Demo

4.1. Opening the Slew Rate Control Demo Design

To open the slew rate control demo design:

1. Open Lattice Diamond software.
2. Select **File > Open > Project…**. Browse to find and open **slew_rate.ldf** from the downloaded demo package folder. The Slew Rate Control Demo design is opened as shown in Figure 4.1.

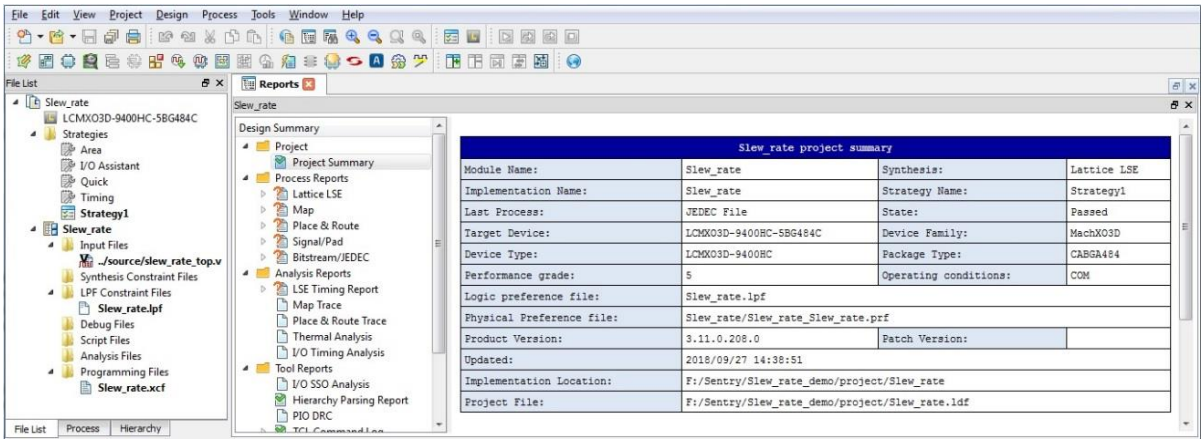

Figure 4.1. Open the Slew Rate Control Demo Project

3. Double-click **slew_rate_top.v** under **File List**. **slew_rate_top.v** is opened as shown in Figure 4.2. Check the default output clock frequency setting for **OSCJ_inst.NOM_FREQ** is **33.25** MHz for the MachXO3D internal Oscillator **OSCJ**.

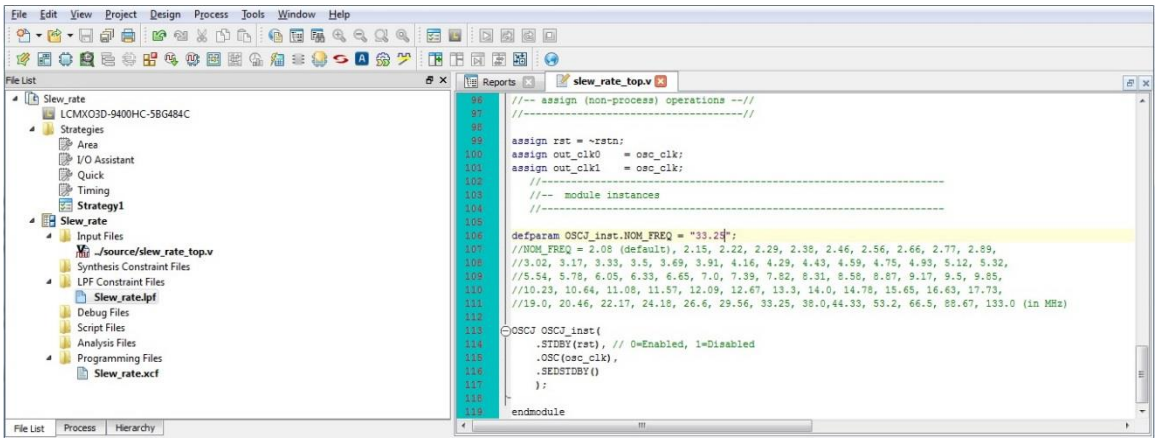

Figure 4.2. Open the Slew Rate Control Demo Project

4. From the Process tab, as shown in Figure 4.3, double-click **Export Files**, or right-click **Export Files** and choose **Rerun All** ( ) to re-run all the previous processes to generate the JEDEC file.

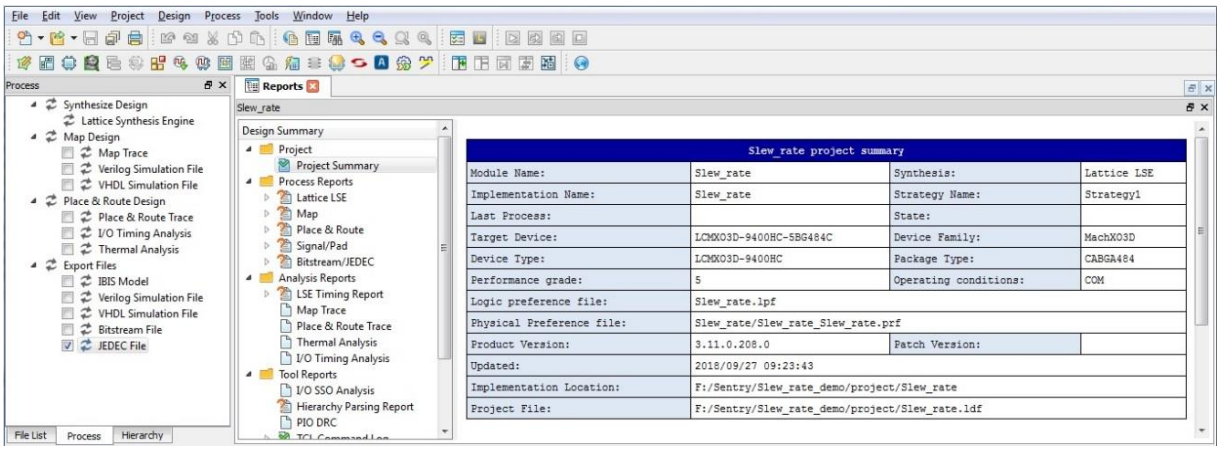

Figure 4.3. Process of Slew Rate Control Demo Project

5. Select **Tools > Spreadsheet View** from the Diamond main interface. Open the **Spreadsheet View** to review the Port Assignments for slew rate control demo project, as shown in Figure 4.4. By default, the SLEWRATE setting for the output pin is SLOW.

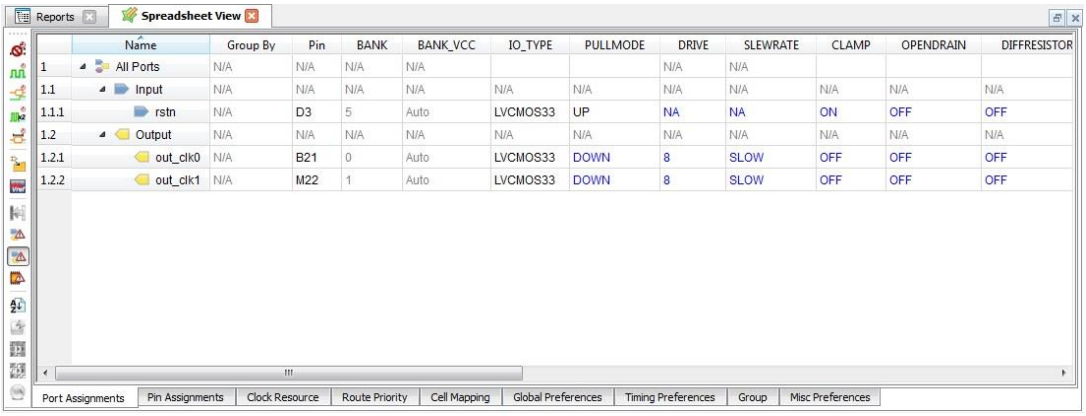

Figure 4.4. Spreadsheet View of Slew Rate Control Demo Project

4.2. Programming Default Image to MachXO3D Devices

To program the default image to MachXO3D devices:

1. Connect the PC to the MachXO3D Development Board using the Mini-USB cable. The board is powered ON.
2. In the Diamond main interface, from the **File List** tab (Figure 4.1), double-click **Slew_rate.xcf**. This XCF file for programming CFG0 is opened in the embedded **Programmer**, as shown in Figure 4.5.

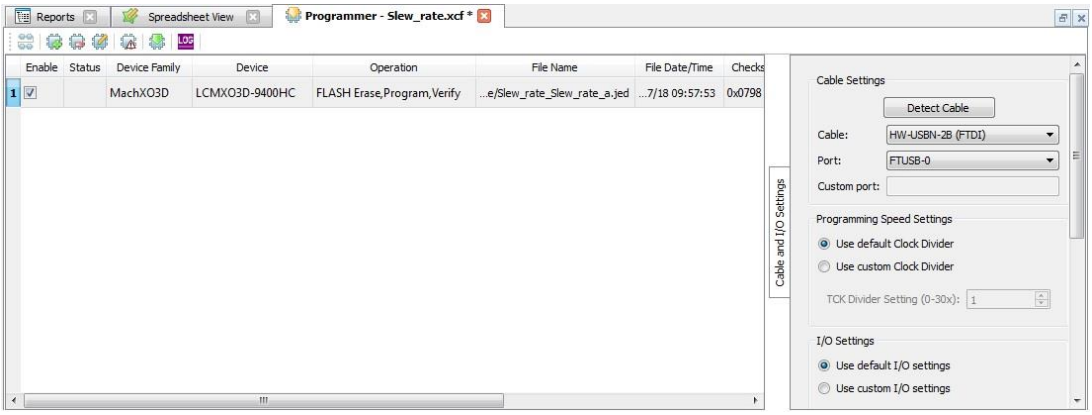

Figure 4.5. Embedded Programmer in the Demo Project

3. Select to highlight the only file information row (Figure 4.5). You can now see file information clearly. Double-click **Slew_rate_Slew_rate_a.jed** from the **File Name** column (Figure 4.5). The **Device Properties** dialog box is opened as shown in Figure 4.6.

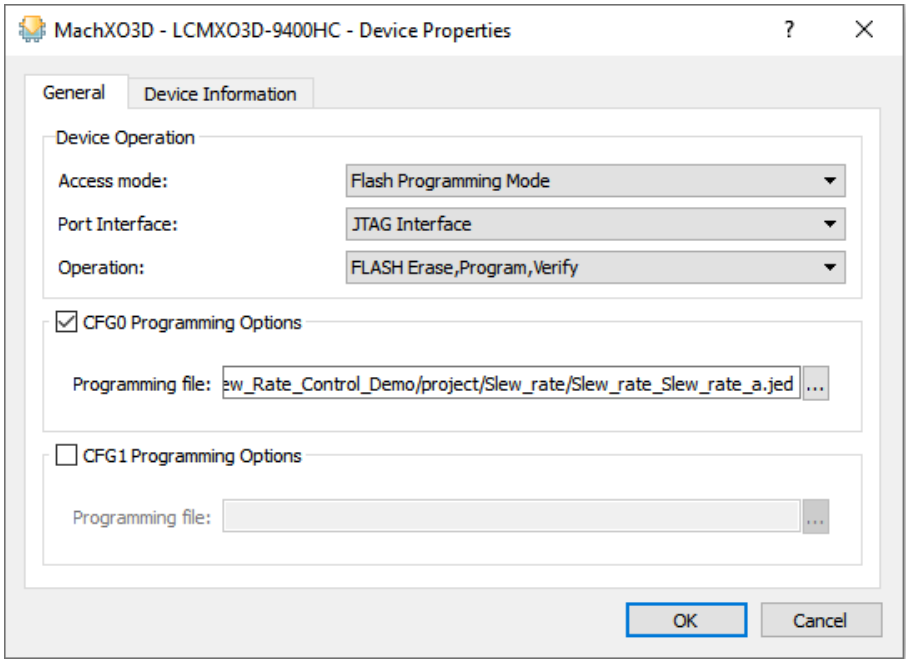

Figure 4.6. Set Device Properties for Programing CFG0

4. Note that at this phase you may not be able to operate the *.jed file because of the different demo package installation directory. To make the *.jed file work, in **CFG0 Programming Options** (Figure 4.6), click the **…** button to re-appoint to **Slew_rate_Slew_rate_a.jed**.
5. Click **OK** (Figure 4.6), and return to embedded Programmer **Slew_rate.xcf** interface as shown in Figure 4.5.
6. Click the **Program** button ( ) from the toolbar (Figure 4.5) to download bitstream to CFG0 with embedded Programmer.
7. After the programming is successfully completed, you can use oscilloscope to probe **TP105** and **TP106**. There are duplicated clock waveforms, as shown in Figure 4.7.

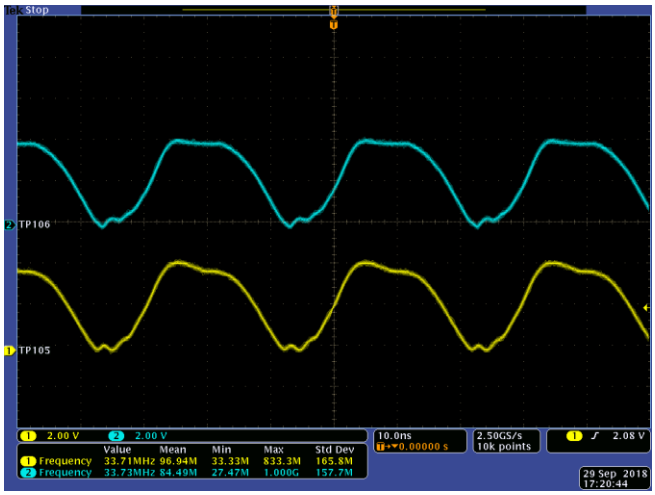

Figure 4.7. Output Clocks with Slow Slew Rate (Frequency Setting is 33.25 MHz)

4.3. Changing the Slew Rate Settings for a Single Output

To change the slew rate for a single output:

1. In the **Spreadsheet View**, change slew rate setting to **FAST** for **out_clk1**, as shown in Figure 4.8. **out_clk1** from pin **M22** connects to **TP105**.

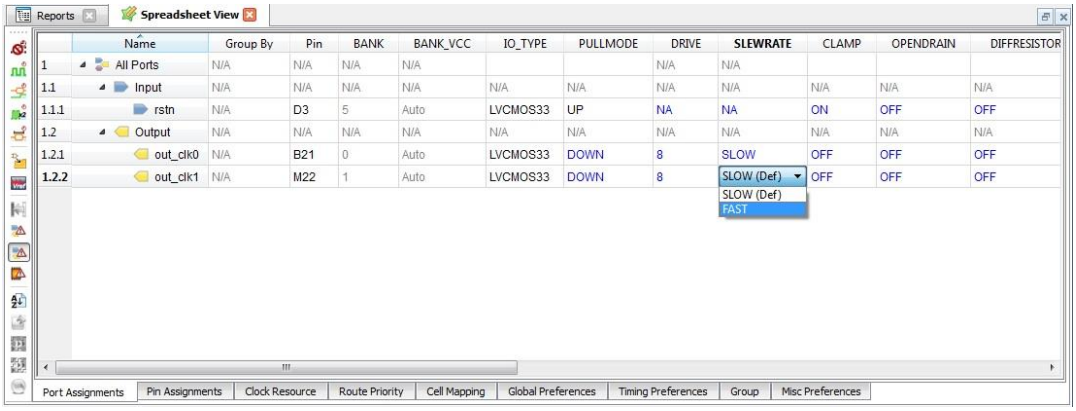

Figure 4.8. Change Slew Rate Setting in the Spreadsheet View

2. Save all the design changes by choosing **File > Save All**, or click the **Save All** button ( ) in the Diamond main interface.
3. In the **Process** view of the Diamond main interface, as shown in Figure 4.9, double-click **Export Files**, or right-click **Export Files** and choose **Rerun All** ( ) to re-run all the previous processes to generate JEDEC files for the new design.

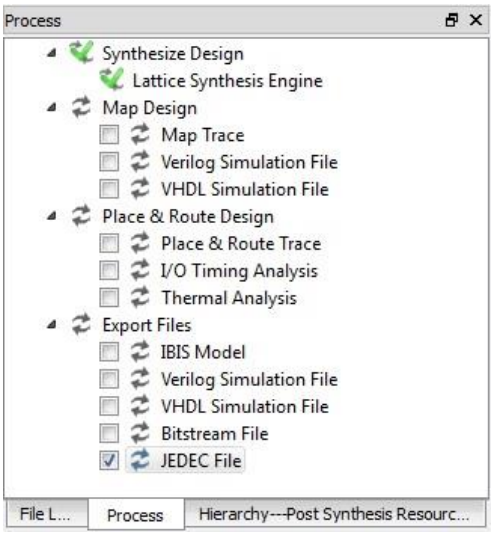

Figure 4.9. Process View of the Diamond Main Interface

4. In the embedded Programmer interface of **Slew_rate.xcf** (Figure 4.5), click the **Program** button ( ) to download new generated bitstream file to CFG0.
5. After the programming is successfully completed, you can use oscilloscope to probe **TP105** and **TP106** again. Different clock waveforms are shown as Figure 4.10. With the same frequency, **TP105** outputs clock signal with faster ramp speed on both rising edge and falling edge.

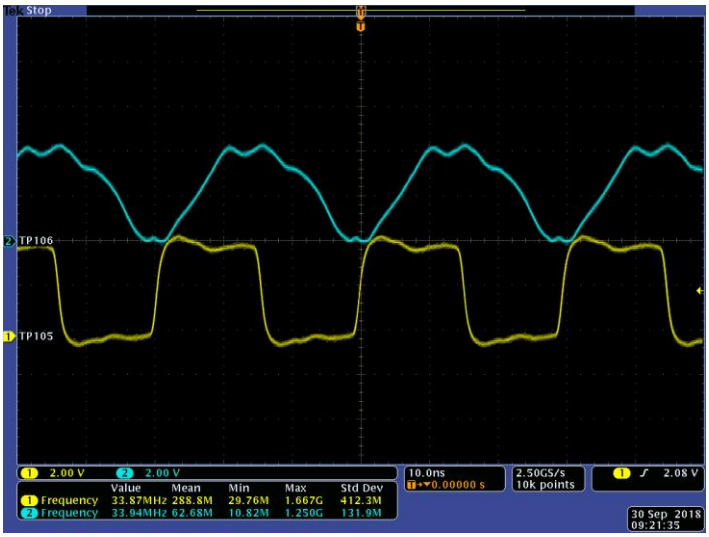

Figure 4.10. Output clocks with Different Slew Rate (Frequency Setting is 33.25 MHz)

4.4. Changing Clock Speed to Show the Difference of Slew Rate Impact

To change Clock Speed and show the difference of Slew Rate impact:

1. In the Diamond main interface, edit **slew_rate_top.v** by changing the output frequency to 133 MHz. To do this, set **defparam OSCJ_inst.NOM_FREQ = "133.0"** (Figure 4.2).
2. Save all the design changes by choosing **File > Save All** or click the **Save All** button ( ) in the Diamond main interface.
3. In **Process** view of the Diamond main interface, as shown in Figure 4.9, double-click **Export Files**, or right-click **Export Files** and choose **Rerun All** ( ) to re-run all the previous processes to generate JEDEC files for the new design.
4. In the embedded Programmer interface of **Slew_rate.xcf** (Figure 4.5), click the **Program** button ( ) to download new generated bitstream file to CFG0.
5. After the programming is successfully completed, you can use oscilloscope to probe **TP105** and **TP106** again. Different clock waveforms are shown as Figure 4.11. With high output clock frequency, **TP105** shows good clock waveform with FAST Slew Rate. **TP106**, however, is not good with SLOW Slew Rate setting.

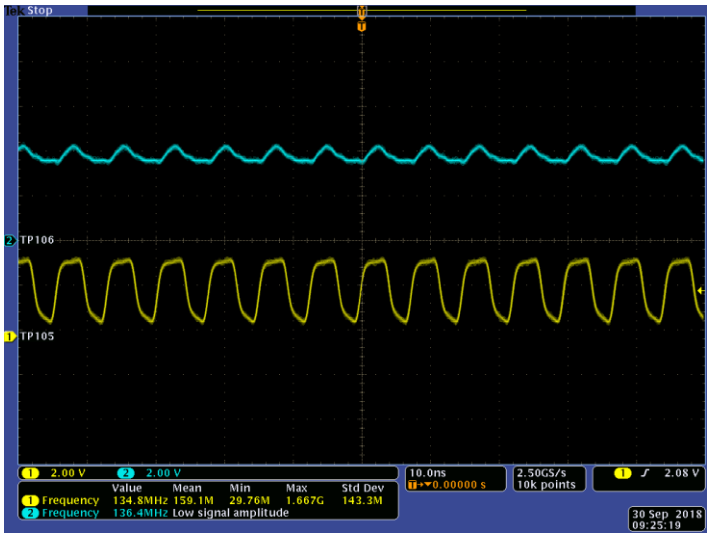

Figure 4.11. Output Clocks with Different Slew Rate (Frequency Setting is 133.0 MHz)

References

A variety of documents for the MachXO3D family are available on the Lattice web site.

- MachXO3D Family Data Sheet (FPGA-DS-02026)
- MachXO3D Development Board User Guide (FPGA-EB-02020)
- MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069)

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Revision 1.1, January 2020

Section	Change Summary
Programming Default Image to MachXO3D Devices	Changed all “internal Flash-A” to CFG0.
Changing the Slew Rate Settings for a Single Output	Changed all “internal Flash-A” to CFG0.
Changing Clock Speed to Show the Difference of Slew Rate Impact	Changed all “internal Flash-A” to CFG0.

Revision 1.0, November 2018

Section	Change Summary
All	Initial release.

www.latticesemi.com