Certus-NX Innovates General-Purpose FPGAs

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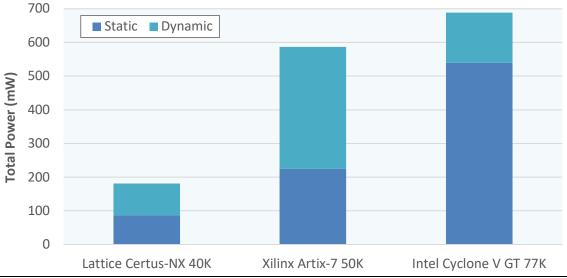
Certus-NX Innovates General-Purpose FPGAs

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Certus-NX is the second product in Lattice's Nexus family, bringing the benefits of FD-SOI to a broader range of applications. These general-purpose FPGAs offer low power, small packages, and flexible I/O along with PCIe Gen2, Gigabit Ethernet, and advanced encryption. They are well suited for many applications including smart home, IoT, consumer networking, and motor control. Lattice sponsored this white paper, but the opinions and analysis are those of the author.

Introduction

Certus-NX brings the benefits of Lattice's Nexus FPGA technology to new markets, targeting applications that need PCI Express and Ethernet connectivity. The new product comes in two models, one with 17,000 logic cells and the other with 39,000. The larger Certus-NX-40 offers a PCIe Gen2 interface that can connect to host processors, wireless or wired communications chips, and many other devices. Both models support Gigabit Ethernet using hard circuitry to improve performance and power efficiency. The new products also offer much smaller packages than competitors do while doubling their I/O density.

The Nexus platform is unique in employing FD-SOI manufacturing. This technology takes a different approach from standard CMOS that greatly reduces power. This capability enables Certus-NX to use 3-4x less power than similar FPGAs from Intel and Xilinx, as Figure 1 shows. Faster configuration times allow systems to boot faster. Another hard block offloads both authentication and encryption to improve security functions.
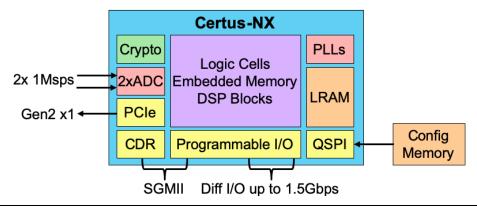

Figure 1. Lattice Certus-NX products. Compared with similar FPGAs from Intel and Xilinx, Certus-NX reduces power by 70–75%. Power is estimated for the PCIe Gen2 interface, worst process, Tj=85ºC, 125MHz. (Source: vendor power calculators)

Certus-NX targets many control and compute applications across the network, from automated industrial equipment operating at the edge, to 5G communications infrastructure, and cloud datacenters. The FPGA can handle a variety of communications protocols, and its security features are well suited for Internet-connected devices. The product can offload neural networks (AI), in many cases while performing communications tasks. Certus-NX can also connect to analog motors and sensors.

Product Overview

The Certus-NX FPGAs provide a flexible set of I/Os along with enough gates to implement a wide variety of protocols. With up to 39,000 logic cells, many designs will have enough logic left over to implement a neural network or other acceleration function using the embedded DSP cores. A hard crypto block accelerates elliptic curve (ECDSA) algorithm for boot-code authentication and AES for bulk encryption. To assist with Ethernet designs, the chips include hard logic for clock and data recovery (CDR) that supports Ethernet data rates up to 1Gbps; combining this block with enough LUTs to implement the Ethernet protocol, the chip can implement an SGMII connection to an external PHY chip.

For higher-speed communication, the Certus-NX-40 model includes hard logic for a PCIe Gen2 controller, as Figure 2 shows. This interface operates a single lane at up to 5Gbps. Both models include two analog-to-digital converters (ADCs), each 12-bit successive-approximation (SAR) models that operates at up to 1 million samples per second (Msps). For other protocols, the chip's programmable I/O can implement single and differential interfaces at up to 1.5Gbps, including LVDS, subLVDS, and DRAM up to DDR3-1066; for these interfaces, the controller must be implemented using LUTs. The logic fabric includes the LUTs, embedded memory, and 18x18-bit multipliers for DSP functions. A "large RAM" sits outside the fabric, providing a block of up to 2.5Mbits for additional storage.

Figure 2. Certus-NX block diagram. The new FPGA includes hard logic for AES and elliptic-curve cryptography, clock and data recovery (CDR) for Gigabit Ethernet (SGMII), a PCIe Gen2 controller, and an analog-to-digital converter (ADC).

FD-SOI technology enables back body bias, which Lattice uses to reduce leakage current by 75% relative to standard CMOS. Operating at 1.0V reduces active power. The technology also improves reliability. FPGAs store their configuration in SRAM, so a random

soft error can cause a failure (SEU). Relative to CMOS, FD-SOI eliminates more than 99% of soft SRAM errors, practically eliminating SEUs.

The Certus-NX products are available in a variety of packages as small as 6x6mm. The design's lower power requirement reduces the number of power and ground connections, leaving more room for I/O. The smallest package includes up to 82 I/O connections, whereas the largest (14mm) package enables 192 I/O connections. Lattice has also reduced boot time by shortening the time required to load the FPGA configuration into SRAM; using a quad-SPI connection to external flash memory, the Certus-NX-40 is ready to run in just 14ms. In fact, the I/O connection initialize in just 3ms.

Product Comparison

For applications that require PCIe, the Certus-NX-40 competes against products such as Intel's Cyclone V and the Xilinx Artix-7 family. Both are 28nm CMOS FPGAs with hard PCIe interfaces. For both, we have chosen models with about 50,000 logic cells, as the next smaller models have about 33,000, considerably less than the Certus-NX product. As Table 1 shows, these models have slightly more total memory, corresponding to their larger gate count. The competitors also offer more DSP blocks.

	Lattice Certus-NX-40	Intel Cyclone V 5CGXC4	Xilinx Artix-7 XC7A50T
Logic Cells	39,000 LCs	50,000 LEs	52,160 LCs
Total RAM	2.5Mbits	2.8Mbits	3.3Mbits
DSP (18x18 Mult)	56 multipliers	140 multipliers	120 multipliers
Hard Crypto Blocks	AES, ECDSA	AES	AES
PCI Express	Gen2 x1	Gen1 x2	Gen2 x1
Other Hard I/O	SGMII, ADC	DDR3	SGMII, ADC
Max I/O Count*	82–192	129–336	106–250
Diff I/O Speed	1,500Mbps	840Mbps	1,250Mbps
IC Process	28nm FD-SOI	28nm CMOS	28nm CMOS
Min Package Size	6mm x 6mm	11mm x 11mm	10mm x 10mm
Soft-Error Rate (FIT)	19 failures	Not reported	3,102 failures‡
Configuration Time	14ms	139ms‡	173ms‡
Estimated Power†	181mW	688mW	539mW

Table 1. FPGAs for PCIe designs. Certus-NX provides better encryption and Ethernet support along with faster I/O speeds. *Range for different package sizes; †PCIe Gen2 interface, worst process, Tj=85ºC, 125MHz. (Source: vendors except †Lattice)

Certus-NX shines in several other areas. It offers the best encryption support, offering user-mode AES acceleration as well as both authentication (ECDSA) and encryption of the FPGA-configuration bitstream. Intel and Xilinx lack authentication and support AES only for configuration. The Cyclone FPGA also lacks PCIe Gen2 support, although its two Gen1 lanes can provide the same total bandwidth, and it lacks a hard CDR block for Ethernet designs. Certus-NX offers the fastest I/O speeds, and its package is a third the size of the others, saving board area.

For applications that don't need a PCIe interface, the Certus FPGAs compete against products such as the Cyclone V E family and the Spartan-7 family. Table 2 compares the smaller Certus-NX-17 against similar-capacity FPGAs in these families. Although the Lattice product has slightly fewer logic cells, it has considerably more memory, both embedded in the fabric and in a large block outside the fabric, enabling it to buffer more data or store larger neural networks. As in the previous comparison, Certus-NX excels in encryption support, I/O speed. Its tiny 6mm package requires less than a quarter of the board area of the others and offers about twice the I/O density. Certus-NX is the only FPGA in this group with hard Ethernet logic.

	Lattice Certus-NX-17	Intel Cyclone V 5CEA2	Xilinx Spartan-7 XC7S25
Logic Cells	17,000 LCs	25,000 LEs	23,360 LCs
Total RAM	3.0Mbits	1.9Mbits	1.9Mbits
DSP (18x18 Mult)	24 multipliers	50 multipliers	80 multipliers
Hard Crypto Blocks	AES, ECDSA	AES	AES
Other Hard I/O	SGMII, ADC	DDR3	ADC
Max I/O Pins	78 I/O	223 GPIO	150 I/O
Max I/O Density	2.2 per mm²	1.3 per mm²	0.9 per mm²
Diff I/O Speed	1,500Mbps	840Mbps	1,250Mbps
IC Process	28nm FD-SOI	28nm CMOS	28nm CMOS
Min Package Size	6mm x 6mm	13mm x 13mm	13mm x 13mm

Table 2. FPGAs for edge devices. Certus-NX offers a much smaller package, 100x better resistance to soft errors, and 10x shorter configuration time. (Source: vendors except †Lattice)

Both Certus-NX products draw on their unique FD-SOI technology to achieve huge advantages in power and failure rate. As Figure 1 shows, in a basic implementation the Certus-NX chip uses 3–4x less power than the Intel and Xilinx products. The Lattice chip has only 19 failures in time (FIT), 160x better than the competition. The device also configures 10x faster than the competitors when booting from quad-SPI memory, as is common. None of the competitors offers instant-on for the I/O pins, which respond in just 3ms on Certus-NX. Lattice also offers its SensAI package to enable customers to develop neural networks using Caffe or TensorFlow tools; we expect the company to make these capabilities available on the Certus-NX devices. SensAI also includes RTL overlays that programs the FPGAs for neural-network inferencing using integer or binary calculations.

Conclusion

Many of the Certus-NX's advantages can directly improve end products. Its tiny 6mm package enables smaller board designs or frees up space to add new system features. Competing FPGAs require 10mm to 13mm packages, even for relatively small gate counts. Despite the small package, Certus-NX provides better I/O density, giving board designers plenty of flexibility. The chip's unique FD-SOI technology also burns much less power than standard CMOS, easing the power budget as well as area.

For communications and other application, Certus-NX provides hard logic for both PCIe Gen2 and Gigabit Ethernet, simplifying the implementation of these popular standards.

Its flexible I/O pins operate at up to 1.5Gbps, handling faster communication than competing FPGAs. To improve security for Internet-connected devices, the FPGA has a cryptography block that accelerates both AES for bulk encryption and elliptic curve (ECDSA) for authentication. This block can also help implement secure boot by validating the external configuration memory. No other FPGA with less than 100,000 logic cells includes an ECDSA block. Certus-NX also initializes 10x faster than competing devices, reducing the time end users must wait for their device to start.

The new FPGA features an A/D converter that can handle analog sensors in an IoT design. Combined with programmable outputs in PWM mode, the ADC works well for motor control. Alternatively, Certus-NX can serve as an accelerator, implementing a neural network using Lattice's SensAI platform or a customer-specific algorithm in the logic cells. In these types of designs, the FPGA can connect directly to the host processor through the fast PCIe link while using few pins. FD-SOI's near-immunity to soft errors makes Certus-NX an ideal choice for aerospace applications. For DSP-intensive workloads, however, the Lattice design offers fewer multipliers.

Certus-NX is the second product in Lattice's Nexus family, bringing the benefits of FD-SOI to a broader range of applications. These general-purpose FPGAs offer low power, small packages, and flexible I/O along with PCIe Gen2, Gigabit Ethernet, and advanced encryption. They are well suited for many edge applications including smart home, IoT, and consumer networking. They can also handle motor-control and other analog applications or provide power-efficient accelerator for AI and other specialized algorithms. Lattice's focus on this market segment delivers unique and innovative capabilities that set Certus-NX apart from the competition.

Linley Gwennap is principal analyst at The Linley Group and editor-in-chief of Microprocessor Report. *The Linley Group offers the most-comprehensive analysis of microprocessors and SoC design. We analyze not only the business strategy but also the internal technology. Our in-depth articles cover topics including embedded processors, mobile processors, server processors, AI accelerators, IoT processors, processor-IP cores, and Ethernet chips. For more information, see our website at* www.linleygroup.com.