I²C to WISHBONE Configuration Interface Bridge Usage Guide

Reference Design

FPGA-RD-02190-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
LUT	Lookup-Table
I²C	Inter-Integrated Circuit
WB	WISHBONE Bus
SDA	Serial Data
SCL	Serial Clock
NVM	Non-Volatile Memory (NVCM for MachXO3L, Flash memory for others)
SDM	Self-Download Mode
GPIO	General Purpose Input/Output
EFB	Embedded Function Block

1. Introduction

I²C to WISHBONE Configuration Interface Bridge Reference Design provides an I²C slave interface with bridging logic to convert the I²C traffic into WISHBONE bus format. Hence, it allows the external I²C master to access Lattice FPGA configuration logic through the internal fabric WISHBONE interface, which exists on MachXO2™, MachXO3™, and MachXO3D™ device families. This Reference Design can serve as a replacement for the Primary I²C sysConfig™ interface, and provide flexibility for the I²C interface from any available GPIO.

Two main concerns are paramount for the I²C to WISHBONE Configuration Interface Bridge:

- Provide an efficient way to access the configuration NVM in Transparent Mode.
- Flexiable I/O pin assignment, independent from sysConfig pins.
- Reducing the number of physical pins used by the interface, relative to JTAG or SPI sysConfig options.

This design is implemented in Verilog. Lattice design tools are language agnostic, so the Verilog design can be seamlessly added to a VHDL design if needed. Lattice Diamond® Software Place and Route tool integrated with Synplify Pro® synthesis tool is used for design implementation. The design can be targeted to all MachXO2, MachXO3, and MachXO3D family devices.

1.1. Quick Facts

Table 1.1 presents a summary of the I²C to WISHBONE Configuration Interface Bridge Reference Design Core.

Table 1.1. Quick Facts

Reference Design Requirements	Supported FPGA Family	MachXO2, MachXO3, MachXO3D
	Minimal Device Needed	MachXO2-256
Device Requirements	Targeted Device	Any device in MachXO2, MachXO3, and MachXO3D families
	Supported User Interfaces	WISHBONE Bus Interface
Design Tool Support	Lattice Implementation	Lattice Diamond Software 3.11 or higher
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro for Lattice
	Simulation	For the list of supported simulators, see the Lattice Diamond Software 11.0 User Guide.

1.2. Conventions

1.2.1. Definition of Terms

This document uses the following terms to describe common functions:

- Configuration – Configuration refers to a change in the state of the MachXO3D SRAM memory cells.
- Transparent Mode – Transparent mode is used to update the Configuration Flash and the User Flash Memory while leaving the MachXO3D devices in user mode.
- User Mode – The MachXO3D device is in user mode when configuration is complete and the FPGA is performing the logic functions it is programmed to perform.

1.2.2. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.3. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

2. Features

The I²C to WISHBONE Configuration Interface Bridge behave as a slave on the I²C bus. It passes the I²C data packet onto the built-in WISHBONE bus inside the MachXO2, MachXO3, or MachXO3D device, which is a system configuration logic interface. Therefore, you can establish NVM programming in the user functional mode.

The I²C to WISHBONE Configuration Interface Bridge presents the following features and requirements:

- Two wire I²C interface up to 1 MHz
- 7-bit addressing is supported
- Parameterized I²C slave address with 7'h40 as default
- The WISHBONE clock must be at least 16x of the I²C bus clock.
- Provides digital glitch filter on SCL for two WISHBONE clock periods, which is 50 ns for 40 MHz WISHBONE clock.

3. Signal Description

Table 3.1 lists and describes the input and output signals for I²C to WISHBONE Configuration Interface Bridge.

Table 3.1. Ports Description

Signal	Direction	Description
System Control Interface		
bridge_enable	Input	Enable signal for this reference design
I²C Interface		
SCL_in	Input	I²C clock input to Slave from Master
SDA_in	Input	I²C data input to Slave from Master
SDA_oe	Output	Open Drain Output Enable for I²C data output
WISHBONE Interface		
wb_rst_i	Input	WISHBONE Reset Resets the WISHBONE interface and sets registers to their default values. Also, reset the internals of the reference design block.
wb_clk_i	Input	WISHBONE Clock Clock for the WISHBONE interface and the rest of the reference design, include the Slave I²C interface
wb_we_o	Output	WISHBONE Write Enable
wb_adr_o[7:0]	Output	WISHBONE Address
wb_dat_o[7:0]	Output	WISHBONE Output Data
wb_dat_i[7:0]	Input	WISHBONE Input Data
wb_str_o	Output	WISHBONE Strobe
wb_cyc_o	Output	WISHBONE Cycle (= Strobe)
wb_rd_data_reg[7:0]	Output	WISHBONE read data register out

4. Functional Overview

The I²C to WISHBONE Configuration Interface Bridge supports standard I²C communication transactions on the two-wire interface, SDA bidirectional data line and SCL input. The data packets between the I²C slave interface inside the Reference Design and the external I²C master goes through the bridging logic and feed into the WISHBONE configuration Interface to invoke the device configuration logic to access the on chip Non-volatile Memory. The bridging logic handles the WISHBONE addressing for the WISHBONE Configuration Interface.

The I²C to WISHBONE Configuration Interface Bridge functional diagram is shown in Figure 4.1.

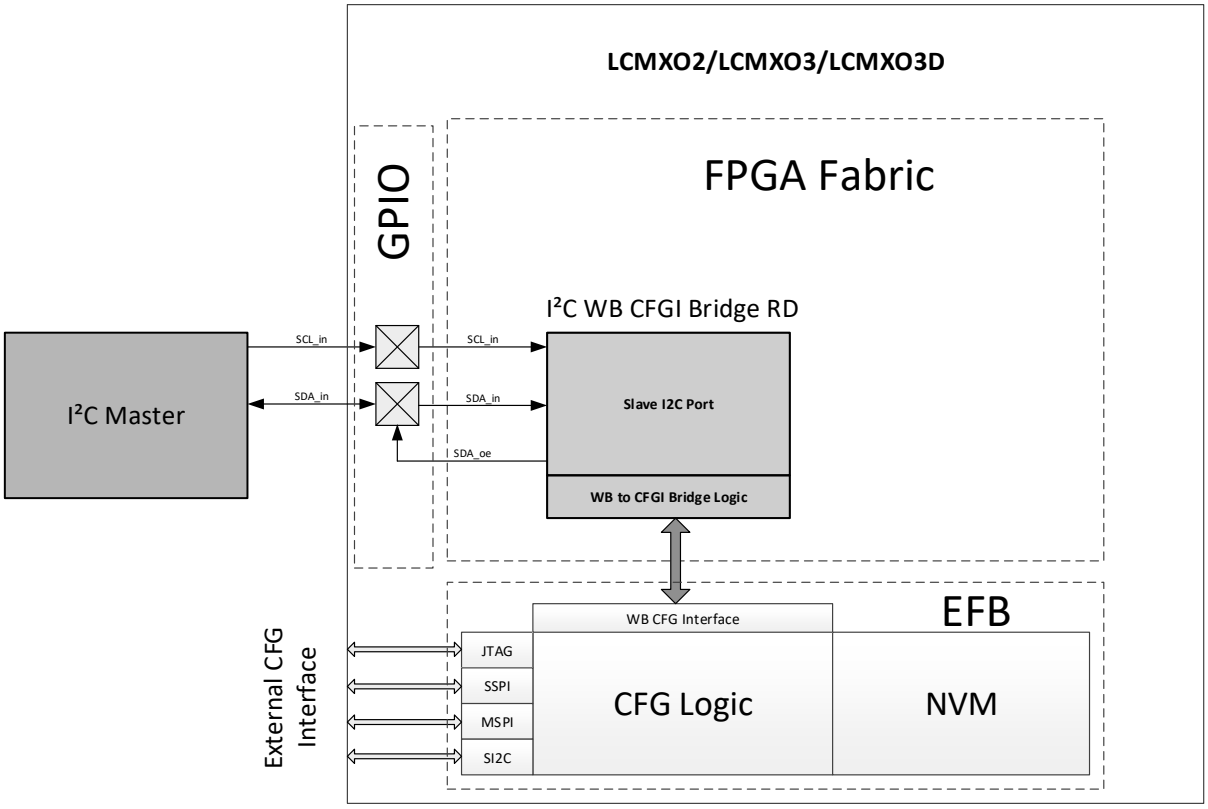

Figure 4.1. I²C to WISHBONE Configuration Interface Bridge Functional Diagram

The I²C to WISHBONE Configuration Interface Bridge pin diagram is shown in Figure 4.2.

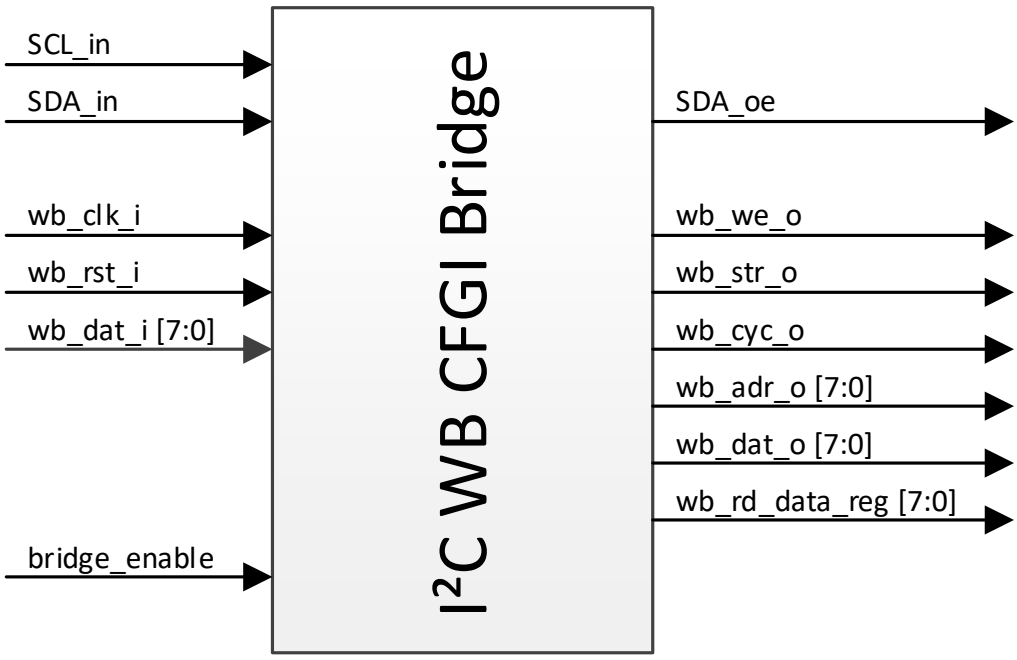

Figure 4.2. I²C to WISHBONE Configuration Interface Bridge Pin Diagram

5. Attributes Summary

Table 5.1 provides the list of user-selectable and compile time configurable parameters for the I²C to WISHBONE Configuration Interface Bridge. The parameter settings are specified using I²C to WISHBONE Configuration Interface Bridge Configuration user interface in Lattice Diamond software.

Table 5.1. Parameter Table

Attribute	Selectable Values	Default	Dependency on Other Attributes	Description
General				
I²C Bus Characteristics				
I2C_ADDR	7'h08 – 7'h77	7'h40	None	Slave Address for the Slave I²C port of the reference design

6. Design Instantiation, Simulation, and Validation

This section provides information on how to instantiate the I²C to WISHBONE Configuration Interface Bridge, including using the Lattice Diamond Software to generate the EFB, and how to run simulation and synthesis. For more details on the Lattice Diamond Software, refer to the Lattice Diamond Software 3.11 User Guide.

6.1. EFB Generation

The I²C to WISHBONE Configuration Interface Bridge Reference Design can access the Configuration Flash, User Flash Memory, and the Feature Row from an internal WISHBONE bus. To use the WISHBONE bus, the Embedded Function Block must be inserted into your design. This allows for flexible utilization of the EFB, for example if your design makes use of other features of the EFB such as UFM.

If no other features are required, the EFB can be generated as shown below. In either case, insert the generated EFB instantiation into your design and hook up the WISHBONE bus to the Bridge Reference Design.

To configure the EFB hard IP functions and generate the EFB module using IPExpress:

1. From the Lattice Diamond top menu, select **Tools > IPExpress**.
2. With a device targeted for the Diamond project, the IPExpress window opens and the EFB module can be found under **Modules > Architecture Modules**.

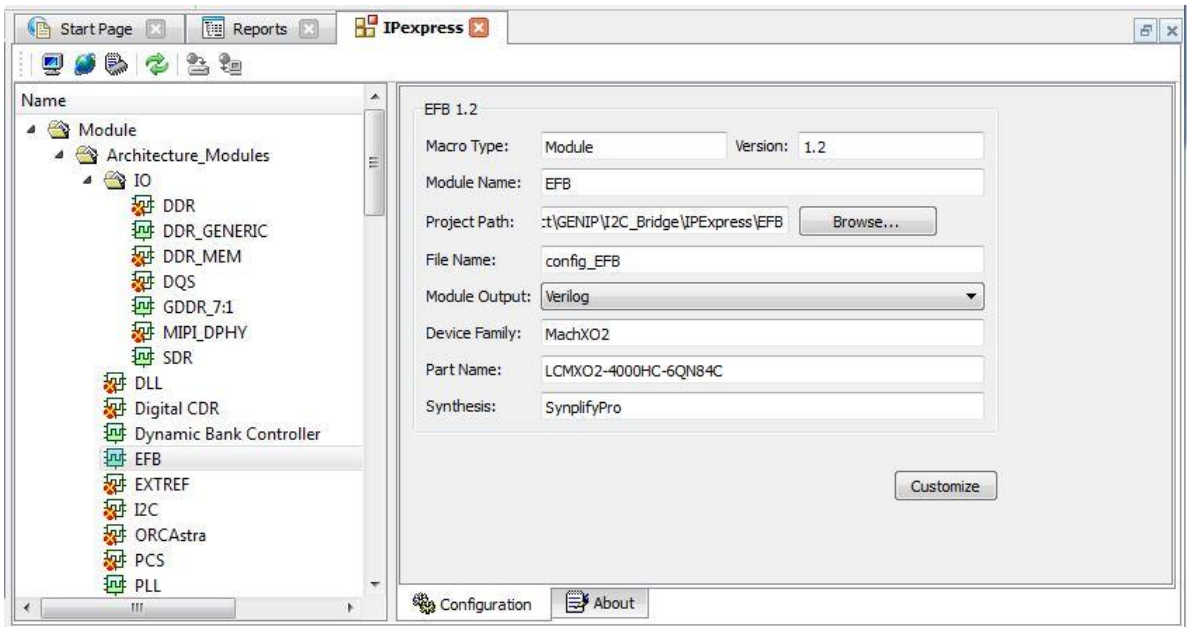

Figure 6.1. EFB Module in IPExpress

3. Fill in the **Project Path**, **File Name**, and **Design Entry** fields, and click **Customize**.
4. The EFB configuration dialog appears. The left side of the EFB window dis-plays a graphical representation of the I/O associated with each IP function. The I/O pins appear and disappear as each IP is enabled or disabled. Check the tab for **WISHBONE**, and enter the **WISHBONE Clock Frequency**. An example EFB with all features enabled is shown in Figure 6.2.
5. Click the **Generate** button.

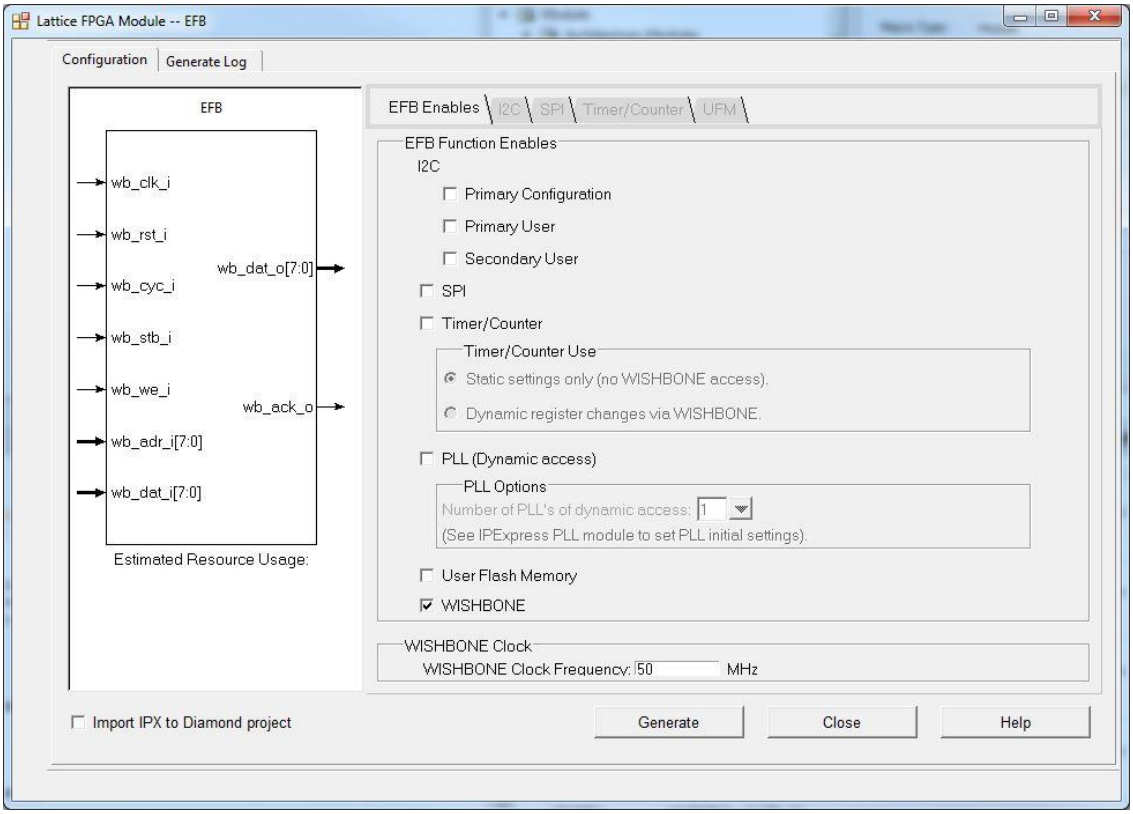

Figure 6.2. Generating an EFB Module wit IPExpress

The EFB module is generated and ready to be instantiated in your design.

6.2. Reference Design Module Declaration and Instantiation

The I²C to WISHBONE Configuration Interface Bridge can be instantiated into the RTL design, as shown in the example below.

Module Declaration

```
module #(I2C_ADDR) I2C2WB_birdge (bridge_enable, SCL_in, SDA_in, SDA_oe, wb_clk_i,
wb_rst_i, wb_we_o, wb_adr_o,
                                                                    wb_dat_o,
wb_dat_i, wb_str_o, wb_cyc_o, wb_rd_data_reg);
parameter I2C_ADDR  = 7'h40;
input bridge_enable;
input SCL_in;
input SDA_in;
output SDA_oe;
input wb_clk_i;
input wb_rst_i;
output wb_we_o;
output [7:0] wb_adr_o;
output [7:0] wb_dat_o;
input [7:0] wb_dat_i;
output wb_str_o;
output wb_cyc_o;
output [7:0] wb_rd_data_reg;
endmodule
```

Instantiation

```
parameter I2C_ADDR = 7'h40;    // Define I2C slave address for the Reference
Design, value between 7'h08 – 7'h77;
wire              wb_clk_i  ;
wire              wb_rst_i  ;
wire              wb_we_i  ;
wire    [7:0]   wb_adr_i ;
wire    [7:0]   wb_dat_i ;
wire    [7:0]   wb_dat_o ;
wire              wb_str_i ;
wire              wb_cyc_i ;
wire              wb_ack_o ;

// I2C to WISHBONE Configuration Bridge
I2C2WB_birdge #(I2C_ADDR) I2CWB_bridge_inst (
        .bridge_enable    (bridge_enable   ),
        .SCL_in    (SCL_in   ),
        .SDA_in    (SDA_in   ),
        .SDA_oe    (SDA_oe   ),
        .wb_clk_i  (wb_clk_i),
        .wb_rst_i  (wb_rst_i),
        .wb_we_o   (wb_we_i ),
        .wb_adr_o  (wb_adr_i),
        .wb_dat_o  (wb_dat_i),
        .wb_dat_i  (wb_dat_o),
        .wb_str_o  (wb_str_i),
        .wb_cyc_o  (wb_cyc_i),
        .wb_rd_data_reg (wb_rd_data_reg));

// MachXO EFB
config_EFB EFB_inst (
       .wb_clk_i(wb_clk_i ),
       .wb_rst_i(wb_rst_i ),
       .wb_we_i  (wb_we_i  ),
       .wb_adr_i(wb_adr_i ),
       .wb_dat_i(wb_dat_i ),
       .wb_dat_o(wb_dat_o ),
       .wb_stb_i(wb_str_i ),
       .wb_cyc_i(wb_cyc_i ),
       .wb_ack_o(wb_ack_o ));
```

6.3. WISHBONE Configuration Commands

The WISHBONE Configuration commands consist of one byte mandatory OPCODE, three bytes mandatory OPERANDs (except for ISC_NOOP command, which is OPCODE only), and optional data bytes and dummy bytes, which are defined on a per command basis as shown in Table 6.1.

Table 6.1. WISHBONE Configuration Command Format

OPCODE (1 Byte)	OPERAND1 (1 Byte)	OPERAND2 (1 Byte)	OPERAND3 (1 Byte)	DATA (X Bytes)
Mandatory	Mandatory	Mandatory	Mandatory	Optional

The supported WISHBONE Configuration Commands for MachXO2, MachXO3, and MachXO3D product families are shown in Table 6.2.

Table 6.2. WISHBONE Configuration Command Table

Command Name [SVF Synonym]	Command	Operands	Write Data	Read Data	Notes
Read Device ID [IDCODE_PUB]	0xE0	00 00 00	N/A	YY YY YY YY	YY characters represent the device-specific ID code
Enable Configuration Interface (Transparent Mode) [ISC_ENABLE_X]	0x74	08 00 00 [1]	N/A	N/A	Enable the Configuration Logic for device programming in transparent mode. [1]
Read Busy Flag [LSC_CHECK_BUSY]	0xF0	00 00 00	N/A	YY	Bit 1 0 7 Busy Ready
Read Status Register [LSC_READ_STATUS]	0x3C	00 00 00	N/A	YY YY YY YY	Bit 1 0 12 Busy Ready 13 Fail OK
Erase [ISC_ERASE]	0x0E	0Y 00 00	N/A	N/A	Y = Memory space to erase Y is a bitwise OR Bit 1=Enable Bit 1=Enable 16 Erase SRAM 17 Erase Feature Row 18 Erase Configuration Flash 19 Erase UFM
Erase UFM [LSC_ERASE_TAG]	0xCB	00 00 00	N/A	N/A	Erase the UFM sector only.
Reset Configuration Flash Address [LSC_INIT_ADDRESS]	0x46	00 00 00	N/A	N/A	Set Page Address pointer to the beginning of the Configuration Flash sector
Set Address [LSC_WRITE_ADDRESS]	0xB4	00 00 00	M0 00 PP PP	N/A	Set the Page Address pointer to the Flash page specified by the least significant 14 bits of the PP PP field. The 'M' field defines the Flash memory space to access. Field 0x0 0x4 M Configuration Flash UFM
Program Page [LSC_PROG_INCR_NV]	0x70	00 00 01	YY * 16	N/A	Program one Flash page. Can be used to program the Configuration Flash, or UFM.
Reset UFM Address	0x47	00 00 00	N/A	N/A	Set the Page Address Pointer to the

Command Name [SVF Synonym]	Command	Operands	Write Data	Read Data	Notes
[LSC_INIT_ADDR_UFM]					beginning of the UFM sector
Program UFM Page [LSC_PROG_TAG]	0xC9	00 00 01	YY * 16	N/A	Program one UFM page
Program USERCODE [ISC_PROGRAM_USERCODE]	0xC2	00 00 00	YY * 4	N/A	Program the USERCODE.
Read USERCODE [USERCODE]	0xC0	00 00 00	N/A	YY * 4	Retrieves the 32-bit USERCODE value
Write Feature Row [LSC_PROG_FEATURE]	0xE4	00 00 00	YY * 8	N/A	Program the Feature Row bits
Read Feature Row [LSC_READ_FEATURE]	0xE7	00 00 00	N/A	YY * 8	Retrieves the Feature Row bits
Write FEABITS [LSC_PROG_FEABITS]	0xF8	00 00 00	YY * 2	N/A	Program the FEABITS
Read FEABITS [LSC_READ_FEABITS]	0xFB	00 00 00	N/A	YY * 2	Retrieves the FEABITS
Read Flash [LSC_READ_INCR_NV]	0x73	M0 PP PP	N/A	YY * N² * PPPP	Retrieves PPPP count pages. Only the least significant 14 bits of PP PP are used. The 'M' field must be set based on the con-figuration port being used to read the Flash memory. 0x0 I²C 0x1 JTAG/SSPI/WB
Program DONE [ISC_PROGRAM_DONE]	0x5E	00 00 00	N/A	N/A	Program the DONE status bit enabling SDM
Program OTP Fuses [LSC_PROG_OTP]	0xF9	00 00 00	UCFSUCFS	N/A	Makes the selected memory space One Time Programmable. Matching bits must be set in unison to activate the OTP feature. Bit 1 0 0, 4 SRAM OTP SRAM Writable 1, 5 Feature OTP Feature Writable 2, 6 CF OTP CF Writable 3, 7 UFM OTP UFM Writable
Disable Configuration Interface [ISC_DISABLE]	0x26	00 00	N/A	N/A	Exit Transparent programming mode.
Bypass [ISC_NOOP]	0xFF	N/A	N/A	N/A	No Operation
Refresh [LSC_REFRESH]	0x79	00 00	N/A	N/A	Force the MachXO2 to reconfigure. Trans-mitting a REFRESH command reconfigures the MachXO2 in the same fashion as asserting

Command Name [SVF Synonym]	Command	Operands	Write Data	Read Data	Notes
					PROGRAMN.
Program SECURITY [ISC_PROGRAM_SECURITY]	0xCE	00 00 00	N/A	N/A	Program the Security bit (Secures CFG Flash sector).[3]
Program SECURITY PLUS [ISC_PROGRAM_SECPLUS]	0xCF	00 00 00	N/A	N/A	Program the Security Plus bit (Secures CFG and UFM Sectors).[3]
Read TraceID code [UIDCODE_PUB]	0x19	00 00 00	N/A	YY * 8	Read 64-bit TraceID.

Notes:

1. Transmit the command opcode and first two operand bytes when using the I²C port. The final operand byte must not be transmitted.
2. The N is determined by the DSR size of the device, which N = Total DSR Bits / 8.
3. SECURITY and SECURITY PLUS commands are mutually exclusive.

For details on the Non-Volatile Memory Programming Flow, refer to:

- MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155)
- MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055)
- MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069)

6.4. I²C Transmission Format

The typical WISHBONE Configuration write operation through the I²C to WISHBONE Configuration Interface Bridge is shown in Figure 6.3.

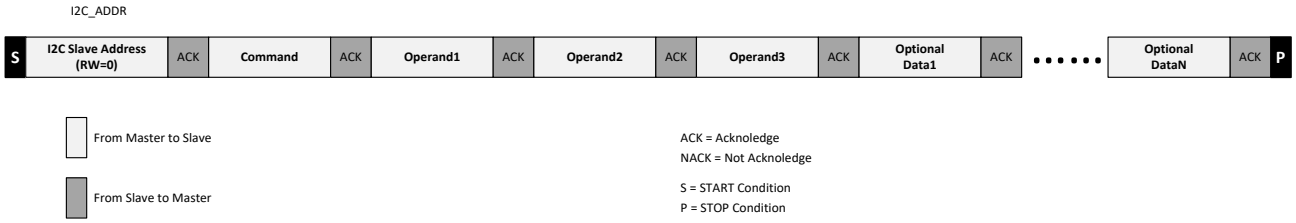

Figure 6.3. I²C Transmission Format for Write

The typical WISHBONE Configuration read operation through the I²C to WISHBONE Configuration Interface Bridge is shown in Figure 6.4.

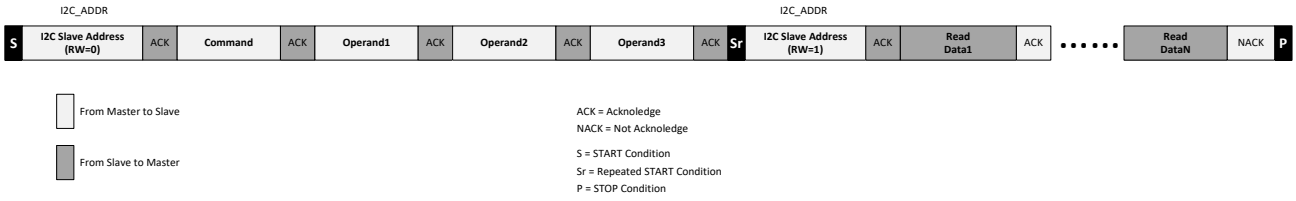

Figure 6.4. I²C Transmission Format for Reading

6.5. Design Simulation

The simulation environment and test bench *tb_I2C_bridge.v* instantiates the *I2C2WB_bridge_sysconfig.v*, which contains the I²C to WISHBONE Configuration Interface Bridge module, FPGA device EFB module, and an I²C Master driver (i2c_master.v).

To simulate the design:

1. Invoke the entire simulation setup by opening the project file *Project/I2C_Bridge_sim.ldf* from Lattice Diamond. The I²C to WISHBONE Configuration Interface Bridge inputs are driven with a generated pattern from the I²C Master driver.

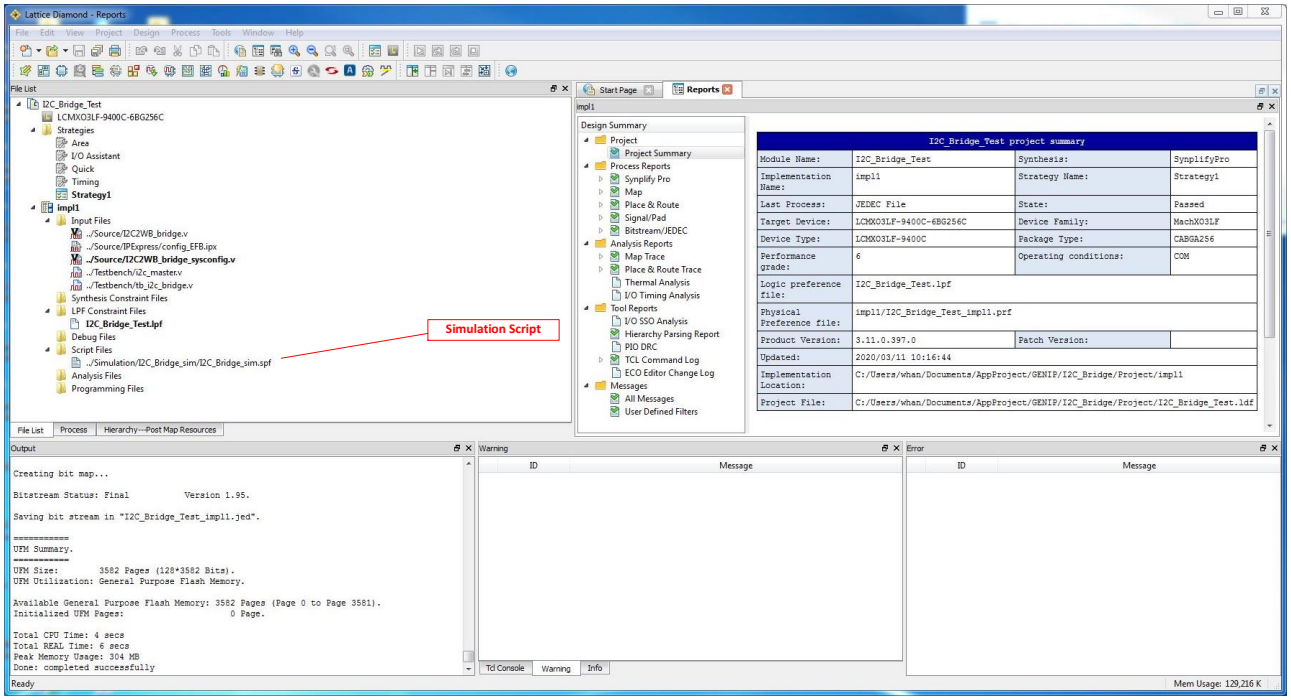

Figure 6.5. Simulation Project in Lattice Diamond

2. Access the simulation environment by double clicking on the *I2C_Bridge_sim.spf* script file in Lattice Diamond from the file list.
3. Click **OK**. The Aldec ActiveHDL opens.
4. Compile the project and initialize the simulation.
5. Add signals to the waveform viewer to view and run the simulation.

The testbench shows the following statements while running:

```
run @3ms
# KERNEL: Configuration complete. EFB now in user mode.                820
# KERNEL:                50000: Starting I2C Slave Simulation
# KERNEL:
# KERNEL:                50000: Initializing Test Bench
# KERNEL:
# KERNEL:                51500: Sending ISC_Enable_X Command 0x74
# KERNEL:               135627: I2C Master Command = 74
# KERNEL:               180627: I2C Master Operand/Data = 08
# KERNEL:               225627: I2C Master Operand/Data = 00
# KERNEL:               270627: I2C Master Operand/Data = 00
# KERNEL:
# KERNEL:               289250: Sending Read Device ID Command 0xE0
```

```
# KERNEL:                373127: I2C Master Command = e0
# KERNEL:                418127: I2C Master Operand/Data = 00
# KERNEL:                463127: I2C Master Operand/Data = 00
# KERNEL:                508127: I2C Master Operand/Data = 00
# KERNEL:                605002: Data Read = 01
# KERNEL:                650002: Data Read = 2b
# KERNEL:                695002: Data Read = 20
# KERNEL:                740002: Data Read = 43
# KERNEL:
# KERNEL:                761750: Sending ISC_Disable Command 0x26
# KERNEL:                845627: I2C Master Command = 26
# KERNEL:                890627: I2C Master Operand/Data = 00
# KERNEL:                935627: I2C Master Operand/Data = 00
# KERNEL:                980627: I2C Master Operand/Data = 00
# KERNEL:
# KERNEL:                994250: Sending Bypass/NOP Command 0xFF
# KERNEL:               1078127: I2C Master Command = ff
# KERNEL:               1123127: I2C Master Operand/Data = ff
# KERNEL:               1168127: I2C Master Operand/Data = ff
# KERNEL:               1213127: I2C Master Operand/Data = ff
# KERNEL:
# KERNEL:               1226750: I2C Simulation Complete
# KERNEL:
# RUNTIME: Info: RUNTIME_0068 i2c_master.v (167): $finish called.
# KERNEL: Time: 1326750 ns,  Iteration: 0,  Instance: /tb_i2c_bridge/MST,  Process:
@INITIAL#98_2@.
# KERNEL: stopped at time: 1326750 ns
```

An example of the simulation waveform for transmitting the transparent flash access enable command is shown in Figure 6.6. In addition, an example of the simulation for reading the device ID is shown in Figure 6.7.

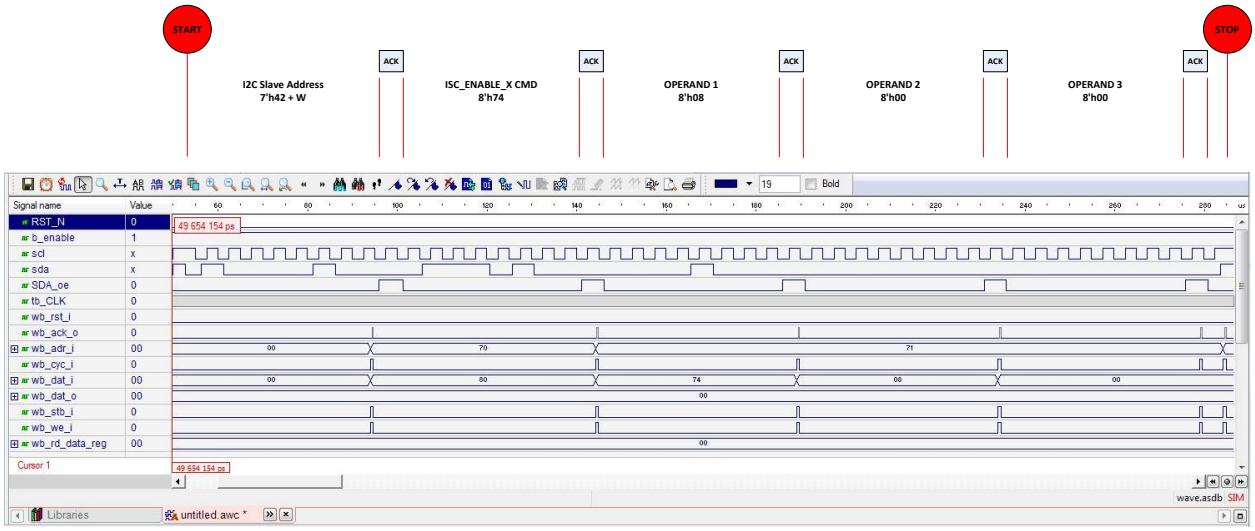

Figure 6.6. Simulation Waveform for Transparent Flash Access Enable

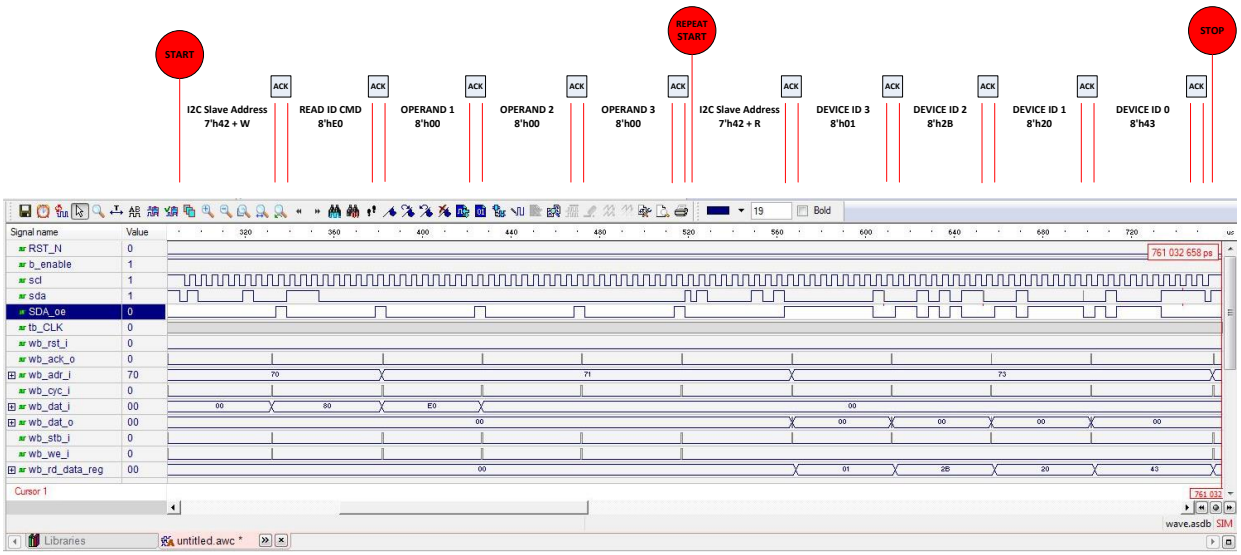

Figure 6.7. Simulation Waveform for Transparent Flash Access Enable

Appendix A. Resource Utilization

Resource utilization information for a sample Slave configuration using Lattice Diamond Software is shown in Table A.1. For more information on Lattice Diamond Software, visit the Lattice web site at www.latticesemi.com/Products/DesignSoftwareAndIP.

Table A.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization	Fmax (MHz)	I/O	Architecture Resources
MachXO2	Verilog-LSE	-6	106 LUTs	40	2	EFB
	Verilog-Syn	-6	95 LUTs	40	2	EFB
MachXO3FL	Verilog-LSE	-6	106 LUTs	40	2	EFB
	Verilog-Syn	-6	95 LUTs	40	2	EFB
MachXO3D	Verilog-LSE	-6	106 LUTs	40	2	EFB
	Verilog-Syn	-6	95 LUTs	40	2	EFB

References

For complete information on Lattice Diamond Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Diamond Software 3.11 User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, March 2020

Section	Change Summary
All	Initial release

www.latticesemi.com