MachXO3D-Dev-Brd

Rev - A

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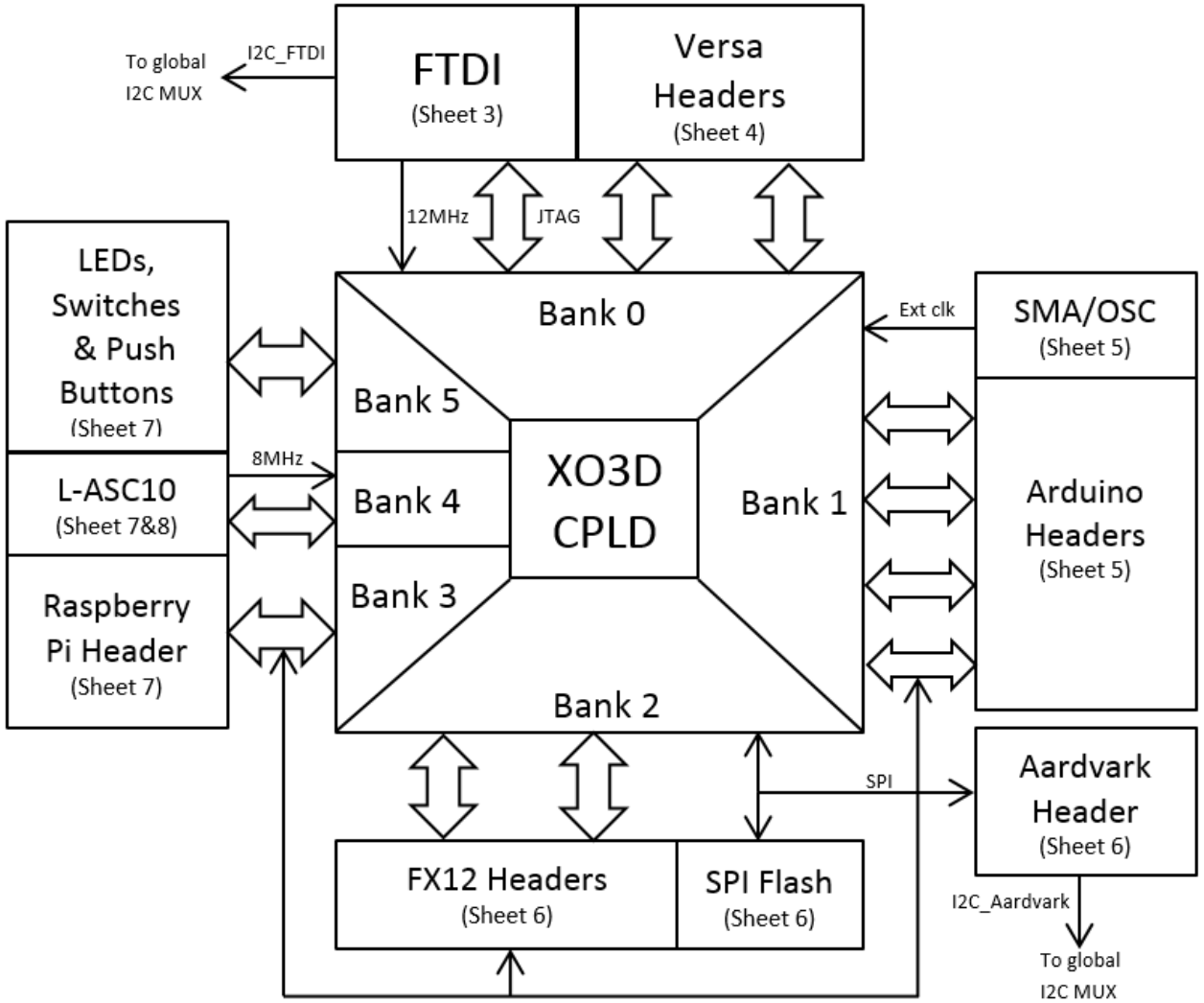
Title: Title page		
Size: A	Project: MachXO3D-Dev-Brd	Schematic Rev: 1.0
		Board Rev: A
Date: Wednesday, April 11, 2018	Sheet 1 of 10	



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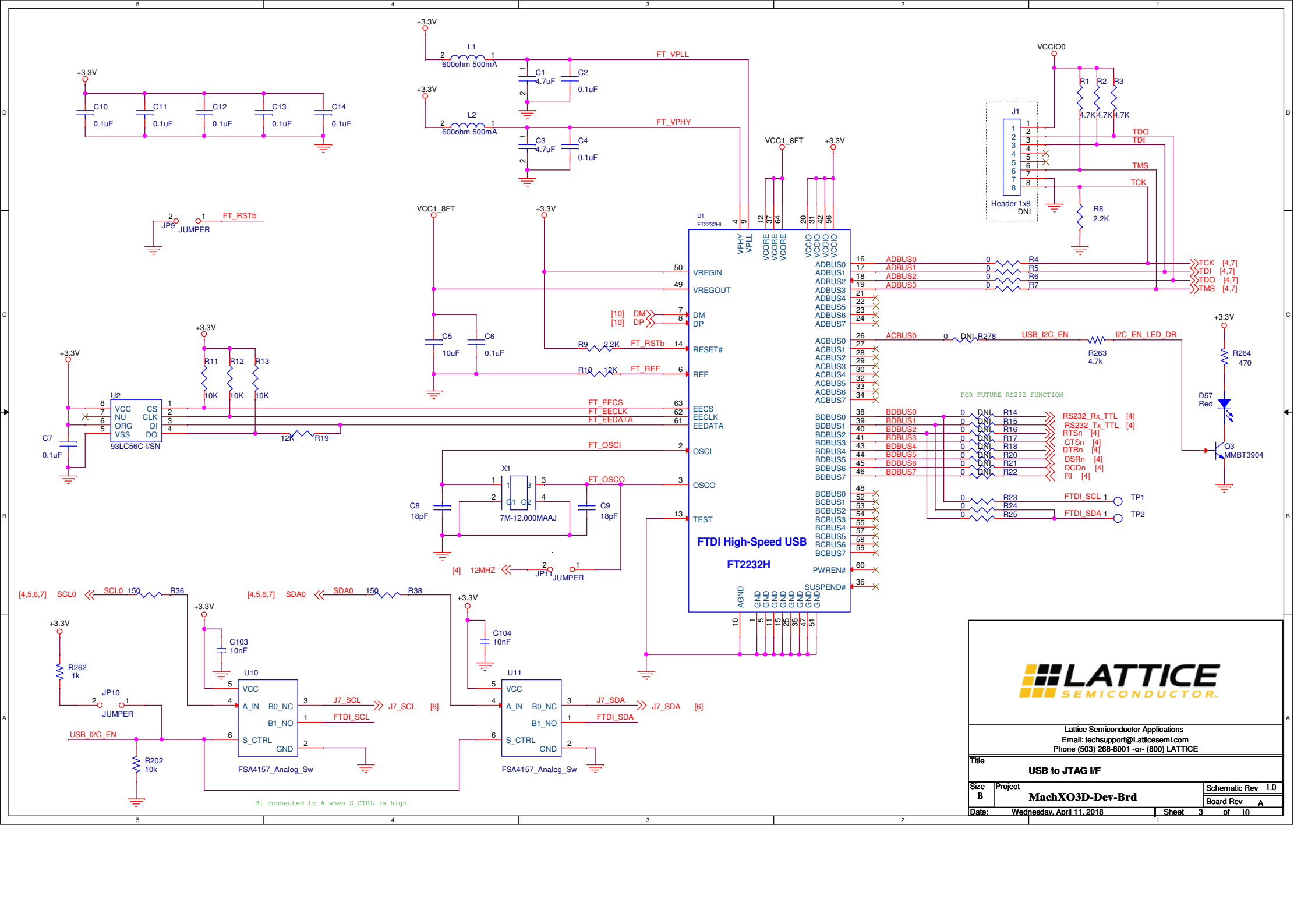
Title: **Block diagram**		
Size: B	Project: **MachXO3D-Dev-Brd**	Schematic Rev 1.0 Board Rev A
Date: Wednesday, April 11, 2018	Sheet 2 of 10	


FTDI High-Speed USB
FT2232H
FT2232HL
93LC56C-I/SN
7M-12.000MAAJ
FSA4157_Analog_Sw
FSA4157_Analog_Sw
B1 connected to A when S_CTRL is high
FOR FUTURE RS232 FUNCTION
Header 1x8
DNI
JUMPER
JUMPER
JUMPER
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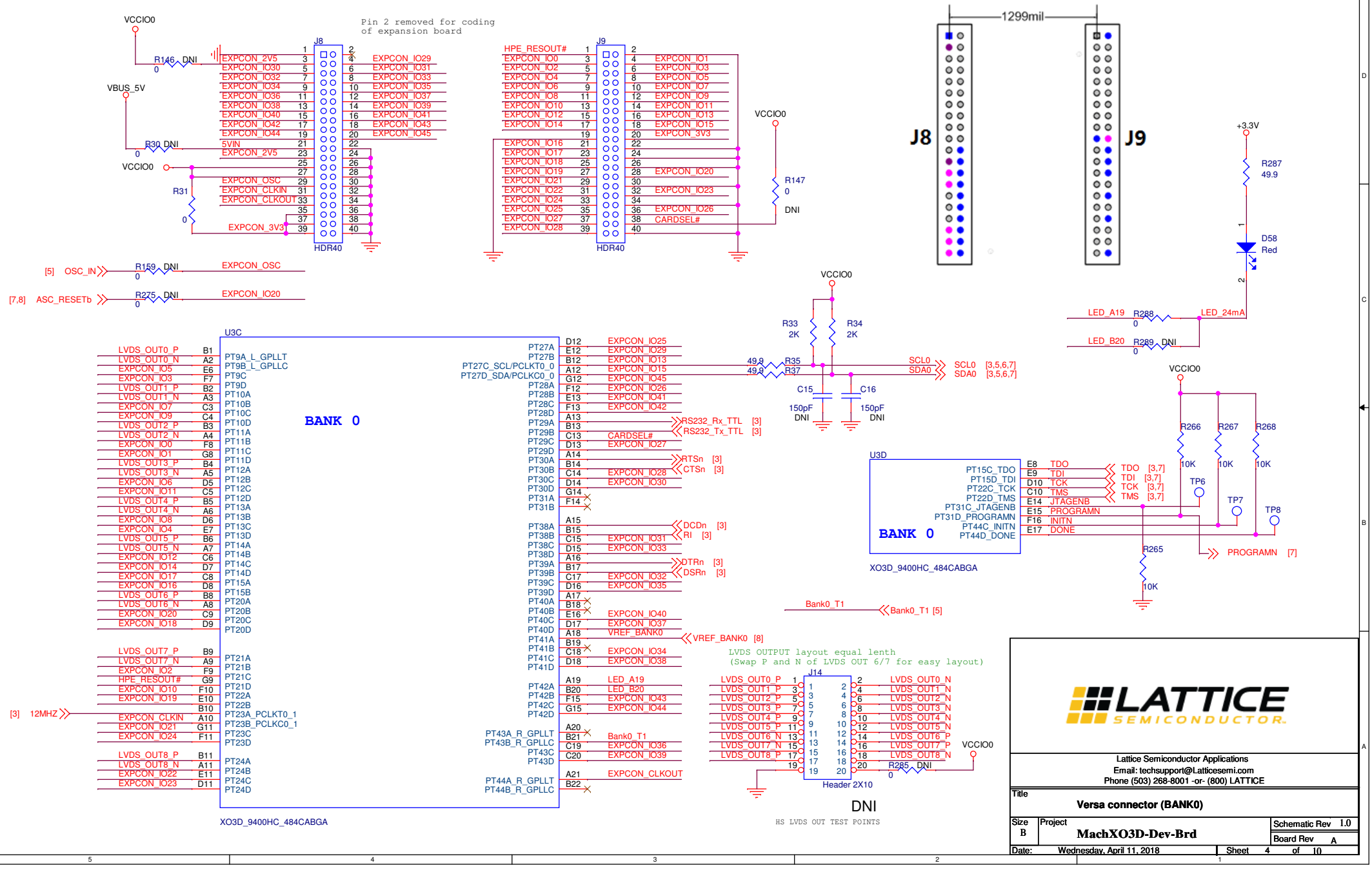
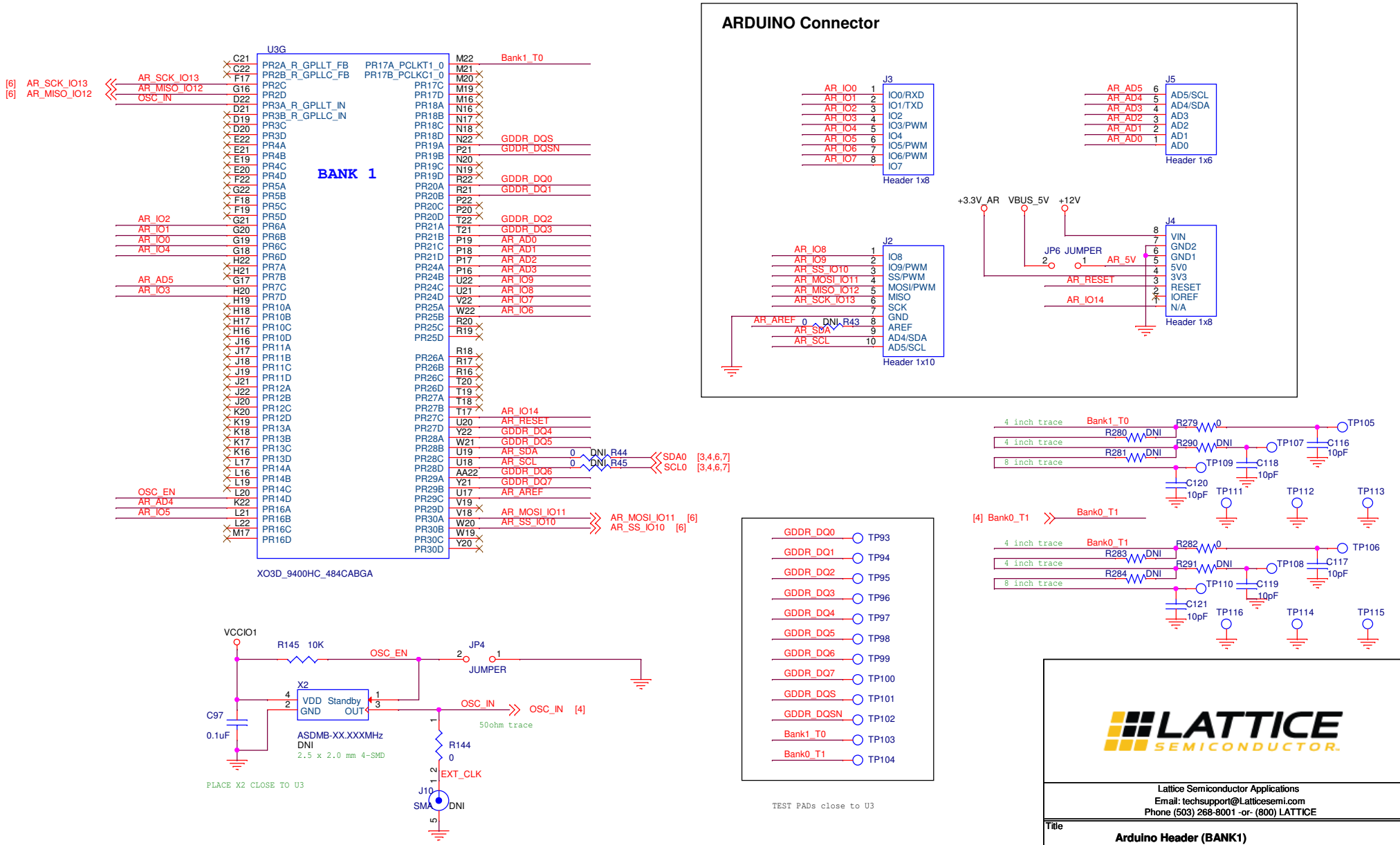
Title
USB to JTAG I/F
Size
B
Project
MachXO3D-Dev-Brd
Schematic Rev 1.0
Board Rev A
Date: Wednesday, April 11, 2018
Sheet 3 of 10

VERSA Connectors




U3G
BANK 1
XO3D_9400HC_484CABGA
ARDUINO Connector
J3
Header 1x8
J5
Header 1x6
J2
Header 1x10
J4
Header 1x8
JP6 JUMPER
DNI R43
DNI R44
DNI R45
JP4
JUMPER
X2
ASDMB-XX.XXXMHz
DNI
2.5 x 2.0 mm 4-SMD
R144
EXT_CLK
J10
SMA
DNI
PLACE X2 CLOSE TO U3
TEST PADs close to U3
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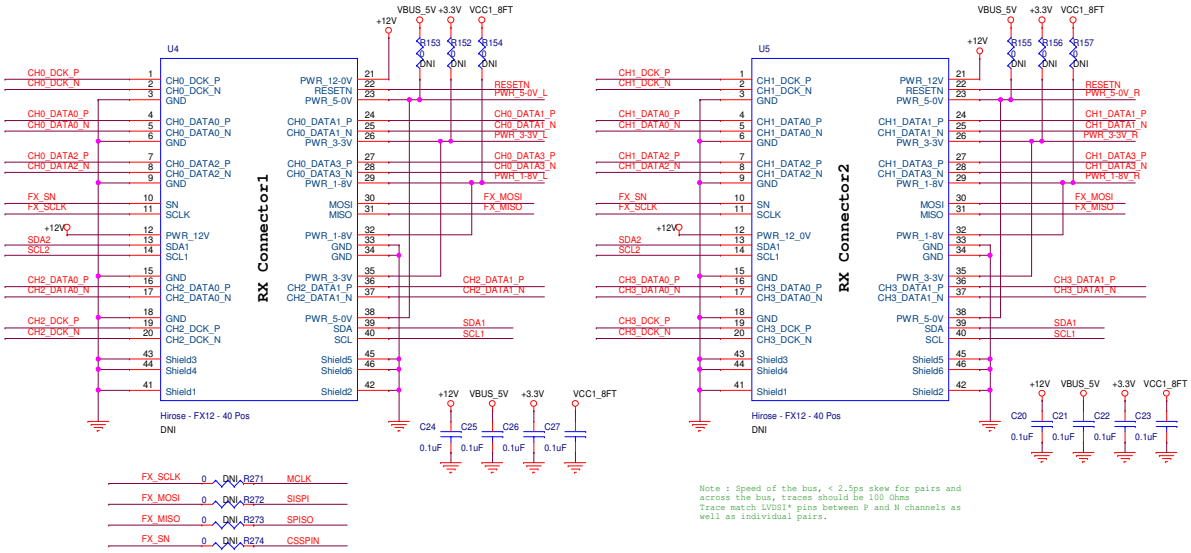
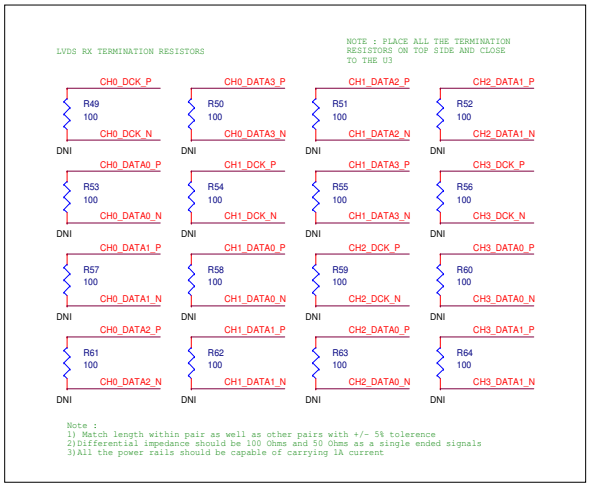
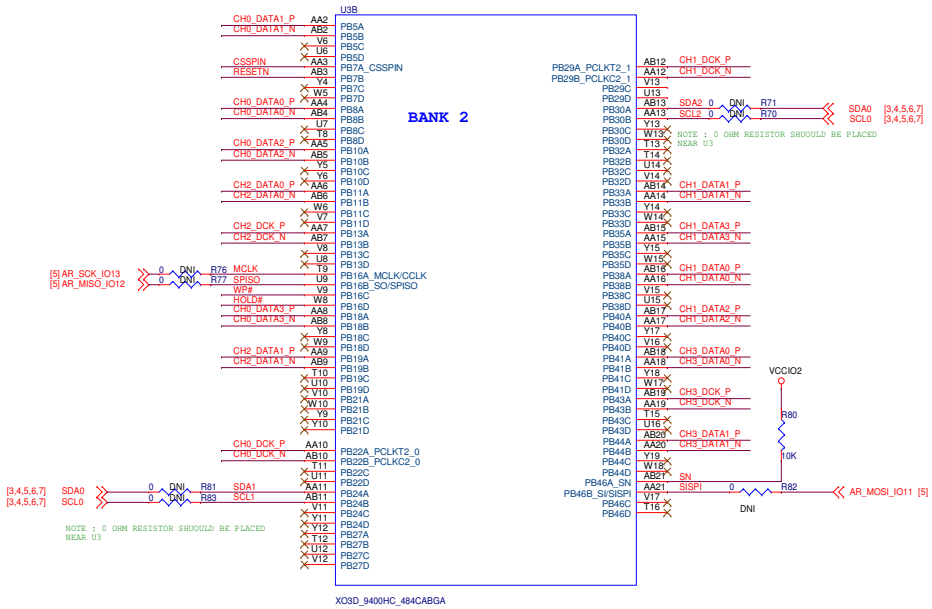
Title
Arduino Header (BANK1)
Size B
Project
MachXO3D-Dev-Brd
Schematic Rev 1.0
Board Rev A
Date: Wednesday, April 11, 2018
Sheet 5 of 10

CrossLink Headers

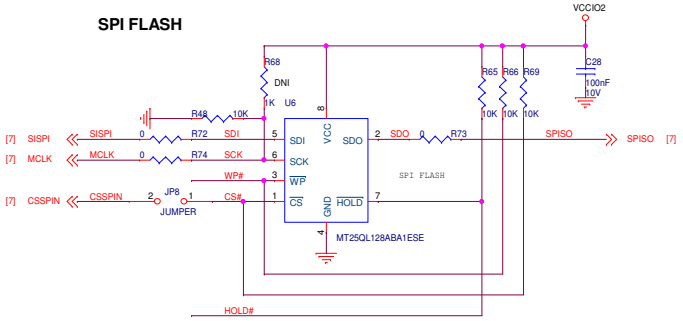


Note : Speed of the bus, < 2.5ps skew for pairs and across the bus, traces should be 100 Ohms
Trace match LVDSI* pins between P and N channels as well as individual pairs.

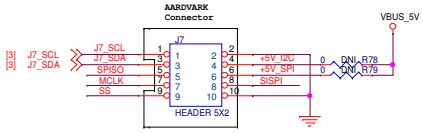


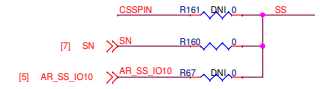


SPI FLASH



AARDVARK





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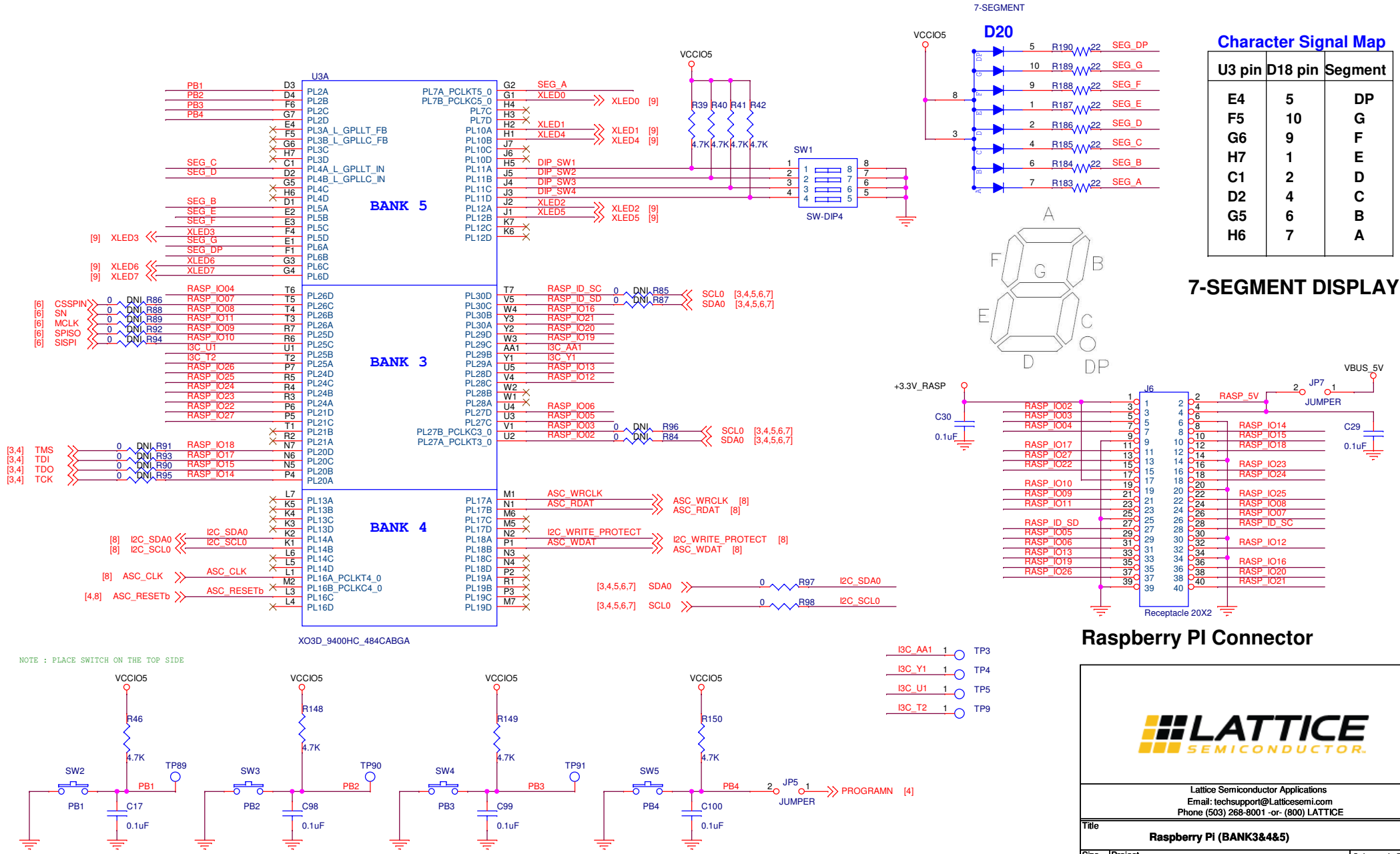
Title	CrossLink Header (BANK2)
Size C	Project: MachXO3D-Dev-Brd
Schematic Rev	1.0
Board Rev	A
Date: Wednesday, April 11, 2018	Sheet 6 of 10



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Title	Raspberry PI (BANK3&4&5)
Size B	Project: MachXO3D-Dev-Brd
Schematic Rev	1.0
Board Rev	A
Date:	Wednesday, April 11, 2018
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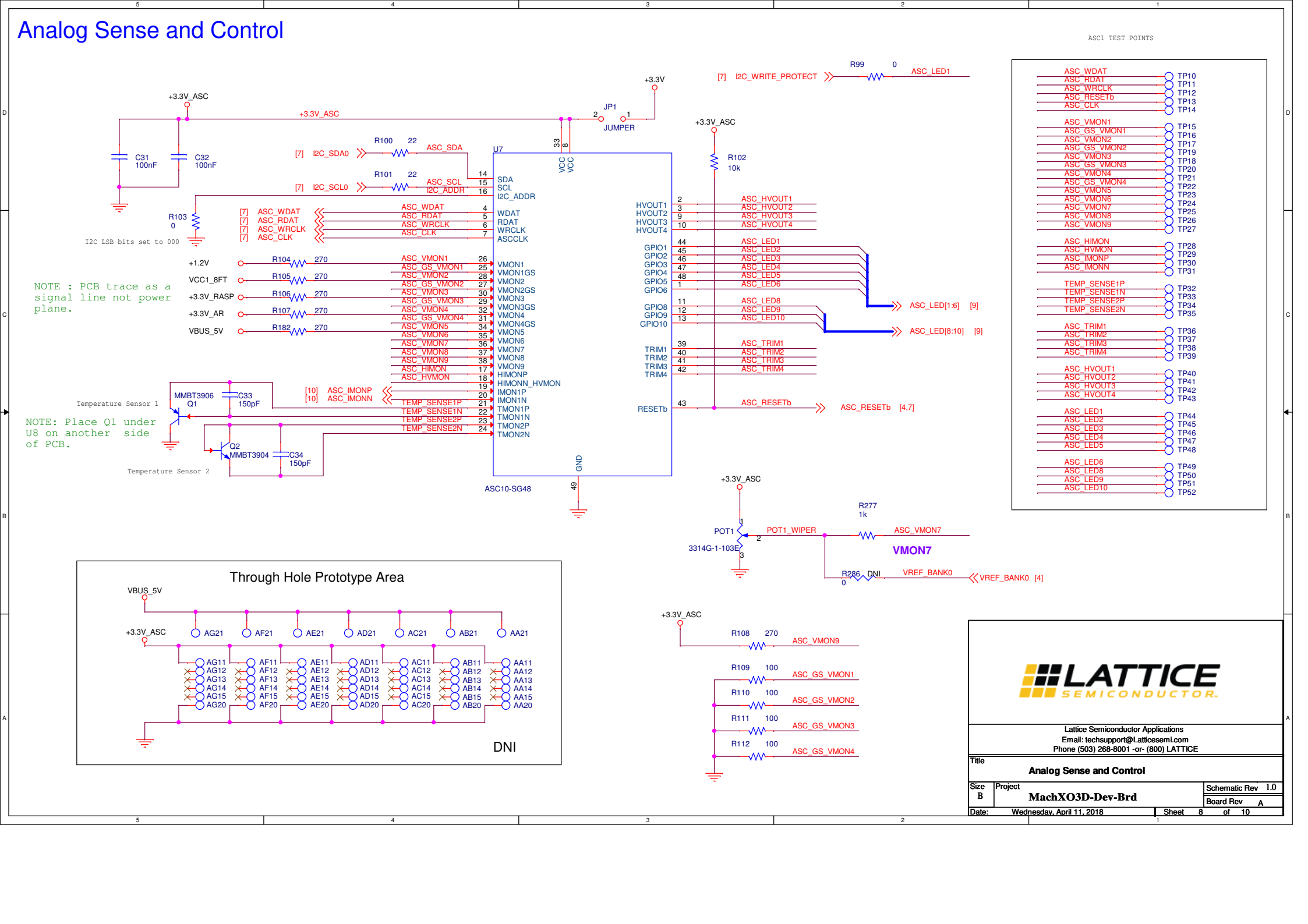
Analog Sense and Control



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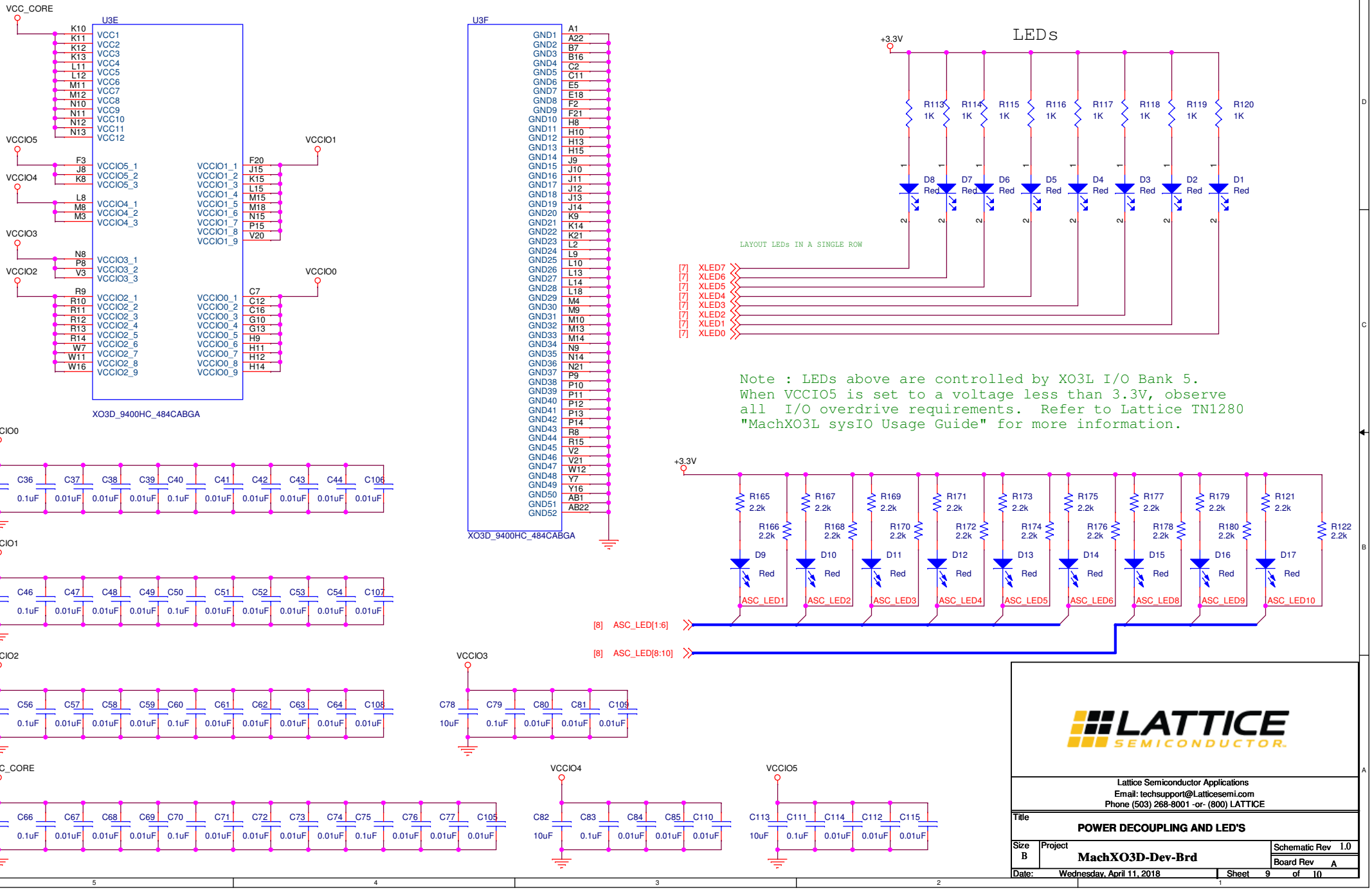
Title	Analog Sense and Control	
Size B	Project MachXO3D-Dev-Brd	Schematic Rev 1.0
		Board Rev A
Date: Wednesday, April 11, 2018		Sheet 8 of 10


VCC_CORE
U3E
VCCIO5
VCCIO4
VCCIO3
VCCIO2
VCCIO1
VCCIO0
XO3D_9400HC_484CABGA
U3F
XO3D_9400HC_484CABGA
LEDs
+3.3V
LAYOUT LEDs IN A SINGLE ROW
[7] XLED7
[7] XLED6
[7] XLED5
[7] XLED4
[7] XLED3
[7] XLED2
[7] XLED1
[7] XLED0
Note : LEDs above are controlled by XO3L I/O Bank 5.
When VCCIO5 is set to a voltage less than 3.3V, observe
all I/O overdrive requirements. Refer to Lattice TN1280
"MachXO3L sysIO Usage Guide" for more information.
[8] ASC_LED[1:6]
[8] ASC_LED[8:10]
VCC_CORE
VCCIO4
VCCIO5
LATTICE SEMICONDUCTOR
Lattice Semiconductor Applications
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Phone (503) 268-8001 -or- (800) LATTICE
Title
POWER DECOUPLING AND LED'S
Size B
Project
MachXO3D-Dev-Brd
Schematic Rev 1.0
Board Rev A
Date: Wednesday, April 11, 2018
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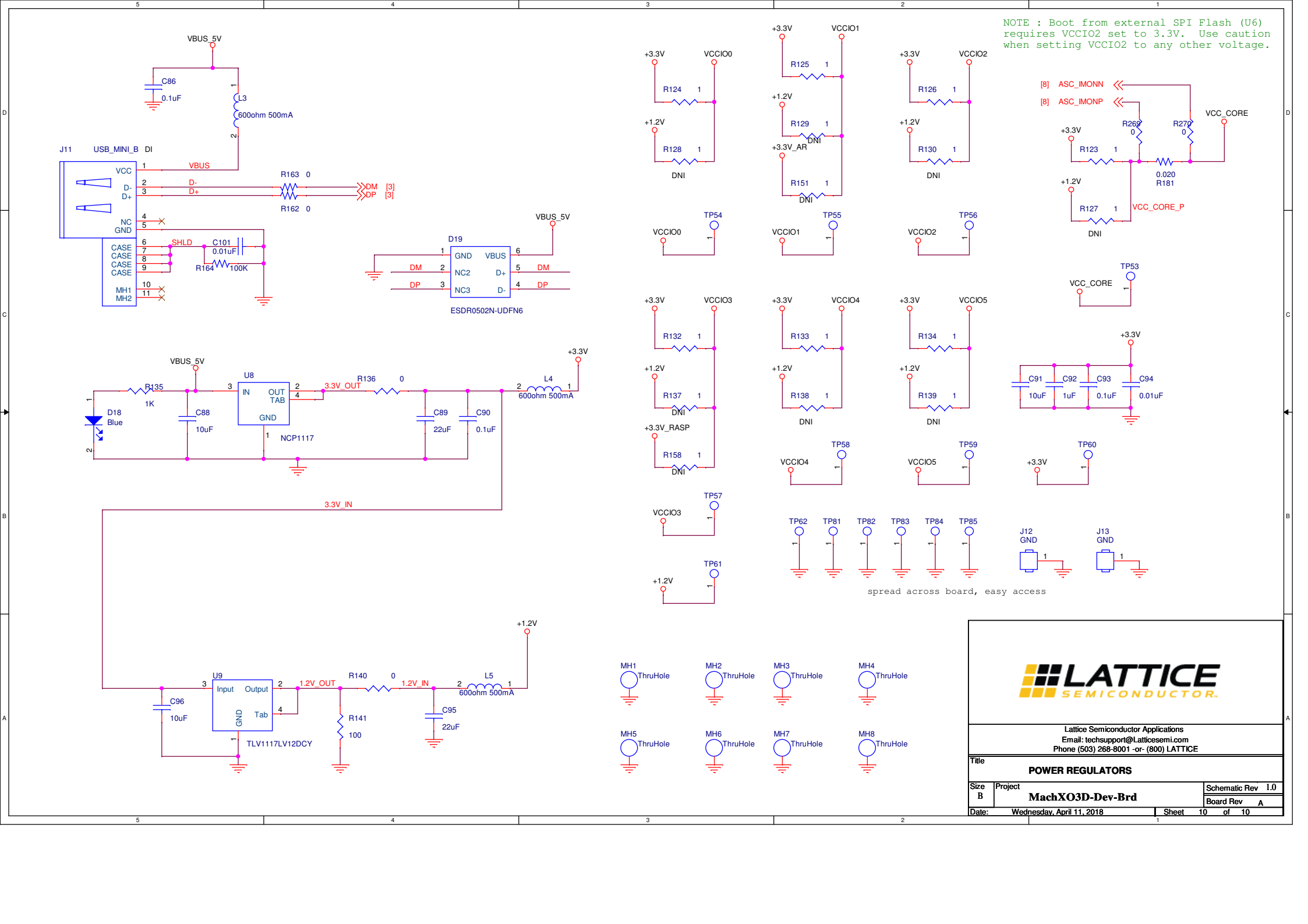
NOTE : Boot from external SPI Flash (U6) requires VCCIO2 set to 3.3V. Use caution when setting VCCIO2 to any other voltage.
VBUS_5V
C86
0.1uF
L3
600ohm 500mA
J11
USB_MINI_B
DI
VCC
D-
D+
NC
GND
CASE
MH1
MH2
VBUS
R163 0
R162 0
DM [3]
DP [3]
SHLD
C101
0.01uF
R164
100K
D19
ESDR0502N-UDFN6
GND
VBUS
NC2
NC3
U8
IN
OUT
TAB
R135
1K
D18
Blue
C88
10uF
NCP1117
3.3V_OUT
R136 0
C89
22uF
C90
0.1uF
L4
600ohm 500mA
3.3V_IN
U9
Input
Output
Tab
GND
TLV1117LV12DCY
1.2V_OUT
R140 0
1.2V_IN
L5
600ohm 500mA
C96
10uF
R141
100
C95
22uF
VCCIO0
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
R124
R125
R126
R128
R129
R130
R151
R123
R127
R181
R262 0
R270 0
0.020
DNI
+3.3V
+1.2V
+3.3V_AR
VCC_CORE
VCC_CORE_P
[8] ASC_IMONN
[8] ASC_IMONP
R132
R133
R134
R137
R138
R139
R158
+3.3V_RASP
C91
C92
C93
C94
10uF
1uF
0.1uF
0.01uF
TP53
TP54
TP55
TP56
TP57
TP58
TP59
TP60
TP61
TP62
TP81
TP82
TP83
TP84
TP85
J12
J13
GND
spread across board, easy access
MH1
MH2
MH3
MH4
MH5
MH6
MH7
MH8
ThruHole
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Title
POWER REGULATORS
Size B
Project
MachXO3D-Dev-Brd
Schematic Rev 1.0
Board Rev A
Date: Wednesday, April 11, 2018
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