Lattice Nexus Platform: Redefining the Low Power, Small Form Factor FPGA

A Lattice Semiconductor White Paper.

April 2020

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TABLE OF CONTENTS

Emerging applications ranging from AI for IoT, embedded vision, hardware security, 5G communications, and industrial/automotive automation are redefining hardware requirements for developers designing products that operate at the network Edge. In order to support these applications, Edge devices need hardware options that offer:

- Low power consumption
- High performance
- High reliability
- Small form factor

To provide customers with a hardware platform with these characteristics, a few years ago Lattice R&D engineers began searching for new areas of innovation in the FPGA development process. The research culminated with Lattice's decision to become the first low power FPGA supplier to support the use of 28 nm Fully Depleted Silicon-on-Insulator (FD-SOI) process technology. Developed by Samsung, the process is similar to the bulk CMOS process technology used to manufacture the vast majority of semiconductors sold today, yet enables previously unseen reductions in device size and power consumption, while greatly improving performance and reliability.

In addition to supporting a new manufacturing platform, Lattice leveraged its years of expertise as the industry's leading developer of low power, small form factor FPGAs to implement innovations at every level of system design (from complete system solutions, to the FPGA fabric architecture, and down to the individual circuit) that reduce power consumption and FPGA form factor even further, yet still increase system performance. This combination of a new manufacturing process with additional innovations resulted in the launch of the Lattice Nexus™ FPGA development platform.

Lattice Nexus Sets News Standard for Low Power FPGAs

The FD-SOI process offered Lattice engineers the opportunity to develop new circuit designs that exploit the inherent advantages of the process. One such advantage is FD-SOI's support for a programmable body bias; a bulk resistor that sits on the body of transistor and allows the developer to control the strength of the transistor during operation. The Lattice R&D team invented a programmable body bias that allows developers to operate in either a high-performance mode or a low-power mode depending on the specific power and thermal management needs of their design. Developers control the mode of operation through a simple software switch. By programming the body bias to favor either high performance or low power, developers can refine the FPGA's power/performance to best meet their application's power consumption and thermal management needs. This not only conserves power in battery-powered Edge devices, but can also help reduce high electricity costs associated with industrial and datacenter operations. Lattice estimates that FPGAs manufactured on the Nexus platform will offer power consumption up to 75 percent lower than competing FPGAs of a similar class.

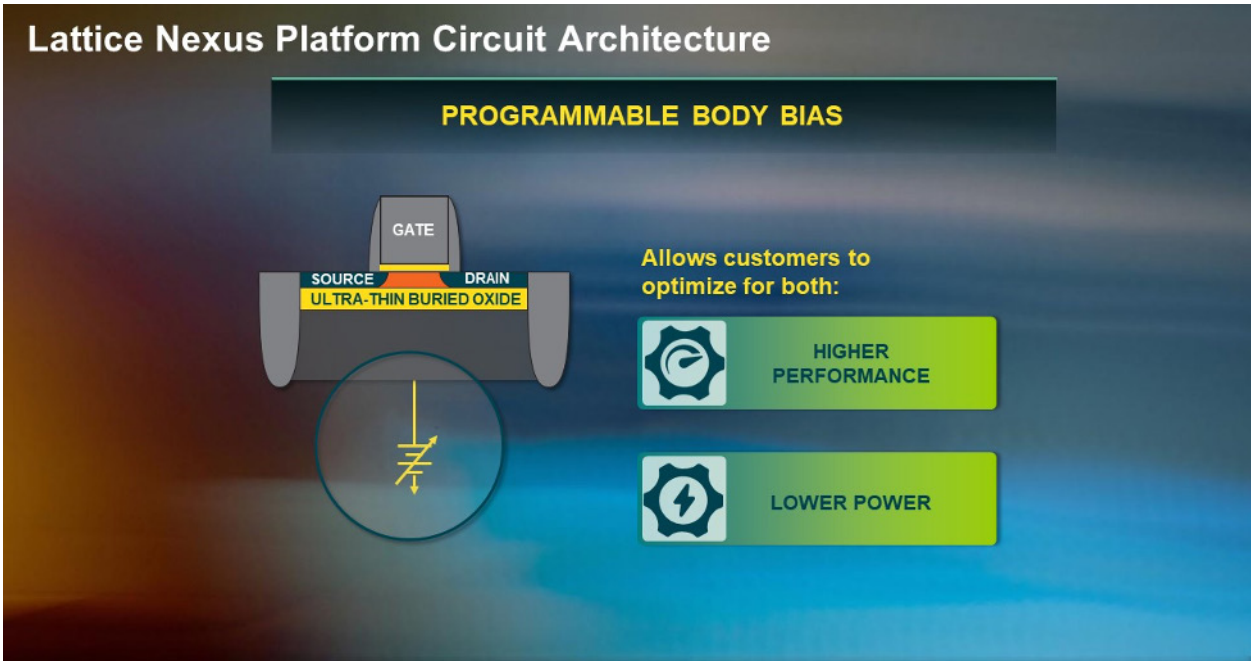

Figure 1: A programmable body bias gives developers working with Lattice Nexus FPGAs the ability to tightly control circuit current leakage and fine tune the device for either low power or high performance.

Accelerating AI Processing Performance with Lattice Nexus

To support emerging technologies at the network Edge like AI, device developers need to make their systems smarter. They are trying to achieve this by integrating more intelligence into their system to allow Edge devices to perform some real-time data processing and analysis at the Edge. The challenge for AI designers is that AI inferencing algorithms are very compute intensive and require large blocks of memory to store values locally for computation. Historically when AI solution developers required high levels of DSP to implement an algorithm, they went off-chip to find it; either to another processor in the system or to the cloud. The need to perform AI calculations off-chip can cause issues with data latency, not to mention that sending customer data to the cloud raises concerns around data privacy and security.

With the Nexus FPGA platform, Lattice is addressing the latency problem by integrating larger blocks of RAM and optimizing DSP blocks so they can store data and perform computations locally. As a consequence, developers can implement AI inferencing algorithms at the Edge as Nexus FPGAs deliver twice the performance of earlier Lattice FPGAs (while consuming only half the power). Potential applications for local Edge AI inferencing range from autonomous industrial robots and ADAS systems to security cameras and smart doorbells.

Lattice Nexus FPGAs Deliver High Reliability

Normal semiconductor device performance can be negatively impacted by high energy particles (typically cosmic rays or alpha particles) striking the device's transistors; a phenomenon known as a soft error. Recovering from such errors could require the FPGA to reset itself; not an option for mission-critical applications that can't tolerate even a few milliseconds of system down time. To combat this, devices developed in a bulk CMOS semiconductor manufacturing processes often include features to help

mitigate soft errors, typically on-chip soft error correction (SEC) and error code correction (ECC) blocks. Lattice Nexus FPGAs not only support SEC and ECC, but also benefit from a thin oxide layer (part of the FD-SOI manufacturing technology) that protects every transistor in the FPGA from the effects of particle strikes to the substrate. As a result, FPGAs developed on the Lattice Nexus platform deliver a 100x improvement in soft error rates in comparison to competing FPGAs of a similar class. Such a significant improvement in reliability is compelling for any application, but particularly in mission-critical automotive or industrial applications where device failure could lead to significant injury or property damage.

Enabling Small Form Factors

The Lattice Nexus platform also addresses the need for ever-shrinking form factors in Edge devices. As other FPGA vendors design their products for data analysis applications in datacenters, their products feature larger architectures that scale poorly to the number of logic cells typical in a small FPGA. Lattice drew on its expertise developing small, low power FPGAs to create a compact FPGA architecture that enables devices with a physical footprint up to ten times smaller than competing FPGAs of similar logic density.

Lattice Nexus Platform Provides Full System Solutions

In addition to innovating the Nexus platform's transistor architecture, Lattice also took a look at higher levels of abstraction in the design process to see ways it could help customers quickly and easily implement Nexus FPGAs in their application designs. Lattice has created or sourced and verified easy-to-use, intuitive design software and pre-engineered soft IP blocks, evaluation boards, kits, and complete reference designs to enable applications common to Lattice's target markets (communications, computing, industrial, automotive and consumer), including sensor aggregation, sensor bridging, and image processing.

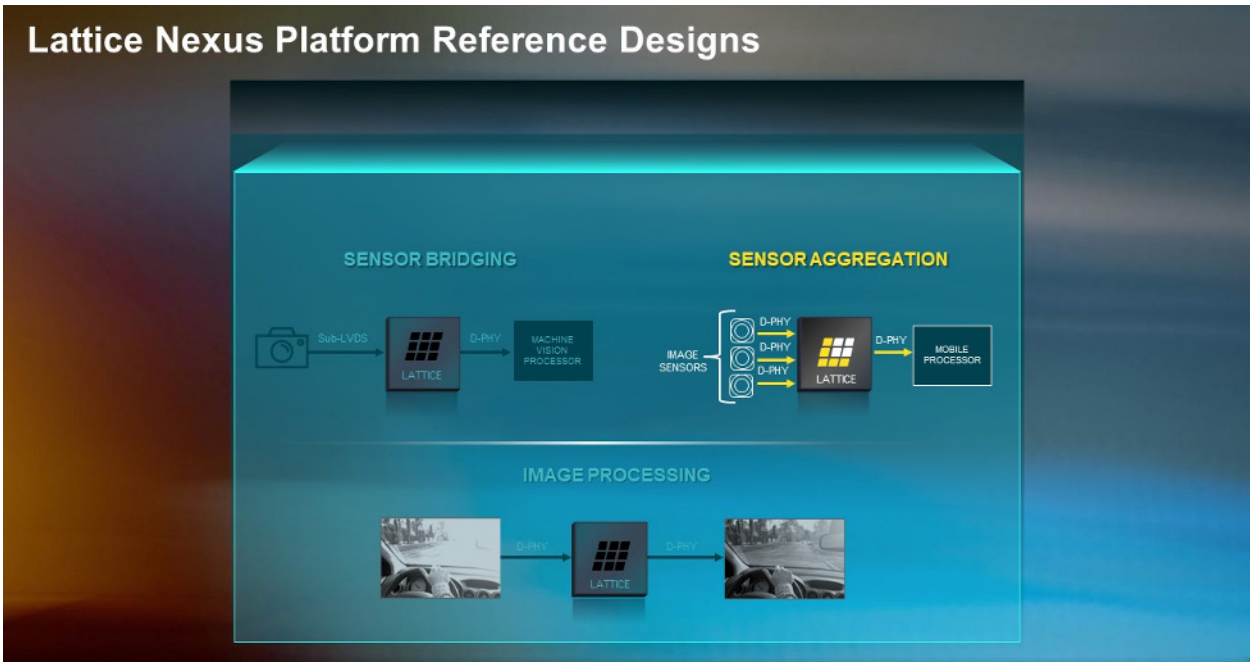

Figure 2: For the embedded vision market, Lattice offers complete reference designs that let developers quickly and easily add support for popular applications to new or existing product designs.

Let's take a closer look at the sensor aggregation demo (highlighted in Figure 2) to see just how these demos help customers get products to market quickly. Targeted for use in embedded vision systems, the demo takes video data streams from up to four sources, combines them into a single stream, and then forwards that stream over a fast MIPI D-PHY to a display or processor for additional processing. Potential applications for the demo include ADAS systems where developers need to collect data from multiple cameras and/or radar sensors, aggregate the data and then forward it to a processor to make safety decisions in real time. By eliminating the need to connect multiple sensors to the car's AP, developers can lower system cost and overall size by reducing the number of traces on the system's PCB and conserving valuable AP I/O ports.

On the software front, Lattice Nexus FPGAs come with design software and a robust library of pre-engineered IP picked by Lattice to enable the various applications the Nexus platform was created to support.

Introducing the first Lattice Nexus FPGA: CrossLink-NX

CrossLink-NX™, the first of a four planned new product families to be developed using Lattice Nexus, illustrates the tremendous opportunity this new platform offers. Based on Lattice's popular CrossLink family of FPGAs for video signal bridging, splitting and aggregation, the new CrossLink-NX FPGA family supports all of the same video signal applications as the original CrossLink device. Thanks to being developed on the Lattice Nexus development platform, the CrossLink-NX FPGA family's higher memory-to-logic ratio, optimized DSPs, larger logic capacity and faster I/Os can process video data using AI algorithms while running twice as fast as Lattice's previous FPGAs. Moreover, in industrial and automotive applications, the CrossLink-NX improves reliability with up to a 100X reduction in soft error rates in a form factor up to 10X smaller than it previous generation. Finally, to further accelerate time-to-market, Lattice offers the Radiant Design Software, proven IP blocks, and application reference designs based on CrossLink-NX FPGAs.

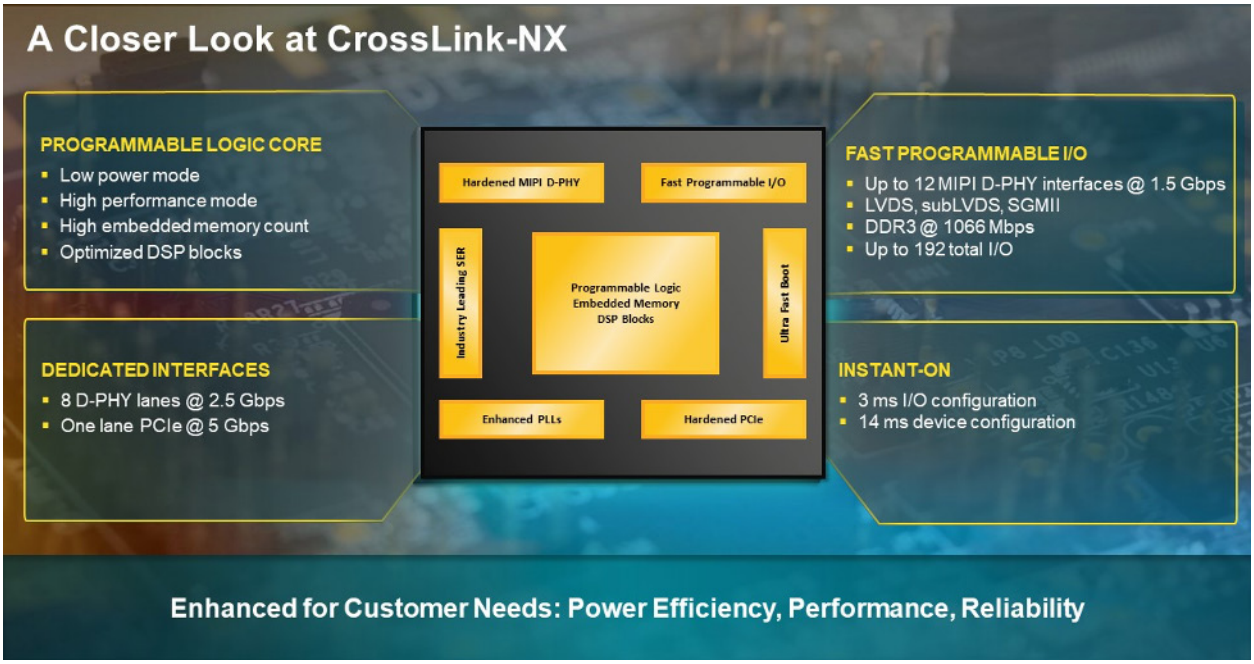

Figure 3: Developed for use in AI and embedded vision applications, the CrossLink-NX FPGA family is the first from Lattice developed on the Lattice Nexus platform.

Conclusion

Today's rapidly evolving market for Edge devices demands higher performance and reliability while consuming minimal power in a compact footprint. Lattice has a long history of helping developers bring to market smart, low power Edge devices for a range of applications. With the launch of the Lattice Nexus platform, Lattice Semiconductor can rapidly develop new FPGAs, so developers can accelerate their own product development and meet new market needs. The Lattice Nexus platform has redefined what developers should expect from small, low power FPGAs.

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