# Certus-NX Hardware Checklist

## Technical Note

FPGA-TN-02151-1.9

September 2025

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# Abbreviations in This Document

A list of abbreviations used in this document.

| Abbreviation | Definition |
|---|---|
| ADC | Analog to Digital Converter |
| BGA | Ball Grid Array |
| CML | Current-Mode Logic |
| ECDSA | Elliptic Curve Digital Signature Algorithm |
| FPGA | Field Programmable Gate Array |
| GPLL | General-Purpose Phase Locked Loop |
| HPIO | High-Performance Input/Output |
| I/O | Input/Output |
| IBIS | I/O Buffer Information Specification |
| JTAG | Joint Test Action Group |
| LUT | Look Up Table |
| LVCMOS | Low-Voltage Complementary Metal Oxide Semiconductor |
| LVDS | Low-Voltage Differential Signaling |
| MIPI | Mobile Industry Processor Interface |
| PCB | Printed Circuit Board |
| PLL | Phase-Locked Loop |
| POR | Power-On-Reset |
| RST | Reset |
| SERDES | Serializer/Deserializer |
| SI | Signal Integrity |
| SLVS | Scalable Low Voltage Signaling |
| SRAM | Static Random Access Memory |
| SSPI | Serial SPI |
| USB | Universal Serial Bus |
| WLCSP | Wafer Level Chip Scale Package |
| WRIO | Wide-Range Input/Output |

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# 1. Introduction

When designing complex hardware using the Lattice Certus™-NX device, you must pay close attention to critical hardware configuration requirements. This technical note outlines these critical hardware implementation items specific to the Certus-NX device. It does not provide detailed step-by-step instructions but offers a high-level checklist to support the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that you are familiar with the Certus-NX device features as described in Certus-NX Family Data Sheet (FPGA-DS-02078). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to Certus-NX Family Data Sheet (FPGA-DS-02078) for details. The critical hardware areas covered in this technical note are:

- Power supplies, as they relate to the Certus-NX power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

**Important:** Refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- Certus-NX High-Speed I/O Interface (FPGA-TN-02216)
- Thermal Management (FPGA-TN-02044)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SERDES Jitter (TN1084)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- Certus-NX-related pinout information can be found on the Lattice Certus-NX web page.
- ADC User Guide for Nexus Platform (FPGA-TN-02129)

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# 2. Power Supplies

At power up, LFD2NX-15/25/35/65 devices monitor the $V_{CC}$, $V_{CCAUXA}$, $V_{CCIO1}$, and $V_{CCIO2}$ power supplies to determine when the Certus-NX should de-assert its internal Power-On Reset state and enter the Power Good condition, initiating device initialization and configuration. LFD2NX-9/17/28/40 devices monitor the $V_{CC}$, $V_{CCAUXA}$, $V_{CCIO0}$, and $V_{CCIO1}$ power supplies. These supplies must rise monotonically. Although the device does not monitor other supplies during power-up, they must reach valid and stable level before the device configuration completes.

Several other supplies are used in conjunction with onboard SERDES Blocks and ADCs on Certus-NX devices.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

**Table 2.1. Power Supplies**

| Supply | Voltage (Nominal Value) | Description |
|---|---|---|
| $V_{CC}$ | 1.0 V | FPGA core power supply.<br>Required for Power Good condition. |
| $V_{CCECLK}$ | 1.0 V | FPGA core clock power supply. |
| $V_{CCAUX}$ | 1.8 V | Auxiliary power supply voltage for WRIO I/O Banks.<br>Used for generating stable drive current for the I/O. |
| $V_{CCAUXHx}$ | 1.8 V | Auxiliary power supply pin for HPIO I/O Banks.<br>Used for generating stable drive current for the I/O and stable current for the differential input comparators. |
| $V_{CCAUXA}$ | 1.8 V | Auxiliary supply voltage for core logic.<br>Required for Power Good condition. |
| $V_{CCIO[11, 9:0]}$<br>LFD2NX-15/25/35/65 | Wide-Range Banks (WRIO):<br>Banks 0, 1, 2, 3, 4, 7, 8, 9, 11:<br>1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V<br><br>High-Performance Banks (HPIO):<br>Banks 5, 6:<br>1.0 V, 1.2 V, 1.35 V (DDR3L Only), 1.5 V, 1.8 V | Bank I/O Driver Supply Voltage.<br>Each bank has its own VCCIO supply.<br><br>VCCIO1 and VCCIO2 have pins used for device configuration and are required for Power Good condition. |
| $V_{CCIO[7\ 0]}$<br>LFD2NX-9/17/28/40 | Wide-Range Banks (WRIO):<br>Banks 0, 1, 2, 6, 7:<br>1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V<br><br>High-Performance Banks (HPIO):<br>Banks 3, 4, 5:<br>1.0 V, 1.2 V, 1.35 V (DDR3L Only), 1.5 V, 1.8 V | Bank I/O driver supply voltage.<br>Each bank has its own VCCIO supply.<br><br>VCCIO0 and VCCIO1 have pins used for device configuration and are required for Power Good condition. |
| $V_{CCADC18}$ | 1.8 V | ADC block power supply.<br>Should be isolated from excessive noise. |
| ADC_REFP[1:0] | 1.0 V to 1.8 V Typical | ADC external reference.<br>Should be isolated from excessive noise and have high accuracy (< 0.1%). |
| $V_{CCSD0}$ | 1.0 V | SERDES block core power supply voltage.<br>Should be isolated from excessive noise. |
| $V_{CCPLLSD0}$ | 1.8 V | SERDES block PLL power supply voltage.<br>Should be isolated from excessive noise. |
| $V_{CCAUXSD}$ | 1.8 V | SERDES block auxiliary power supply voltage.<br>Should be isolated from excessive noise. |

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## 2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

## 2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage
- Expected voltage drops due to power filtering the ferrite bead's ESR × expected current draw
- Expected voltage drops due to current measuring resistor's ESR × expected current draw

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is particularly sensitive to noise, as every 10 mV represents 1% of the rail voltage. For SERDES power rails, it is recommended to target a maximum 1% peak noise. For PLLs, they target less than 0.5% peak noise to minimize jitter.

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# 3. Power Supply Filtering

Providing a quiet, filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB-related crosstalk with sensitive blocks are related to FPGA outputs found in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

It is critical to have very low-noise, highly filtered supplies for the SERDES and ADCs. These supplies are also paired with dedicated ground pins.

## 3.1. Recommended Power Filtering Groups and Components

**Table 3.1. Recommended Power Filtering Groups and Components**

| Power Input | Recommended Filter | Notes |
|---|---|---|
| $V_{CC}$, $V_{CCECLK}$ | 10 µF x 2 + 100 nF per pin | Core and clock logic.<br>Tie $V_{CC}$ and $V_{CCECLK}$ pins together.<br>1.0 V |
| $V_{CCAUX}$, $V_{CCAUXHx}$ | 120 Ω FB + 10 µF x 2 + 100 nF per pin | Auxiliary power supply pins.<br>Tie $V_{CCAUX}$ and $V_{CCAUXHx}$ pins together.<br>1.8 V |
| $V_{CCAUXA}$ | 120 FB + 10 µF + 100 nF per pin | Auxiliary power supply pin for internal sensitive analog circuitry.<br>1.8 V |
| $V_{CCIO[11, 9:0]}$ | 10 µF + 100 nF per pin for each $V_{CCIOx}$ | Bank I/O.<br>Unused banks can use a single 1.0 µF.<br>For banks with lots of outputs or large capacitive loading replace the 10 µF with a 22 µF (or use two 10 µF).<br><br>LFD2NX-15/25/35/65<br>Banks 0, 1, 2, 3, 4, 7, 8, 9, 11: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V<br>Banks 5, 6: 1.0 V, 1.2 V, 1.35 V (DDR3L Only), 1.5 V, 1.8 V<br><br>LFD2NX-9/17/28/40<br>Banks 0, 1, 2, 6, 7: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V<br>Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V |
| $V_{CCADC18}$ | 220 Ω or 120 Ω FB + 10 µF + 100 nF per pin | ADC Blocks.<br>Powering $V_{CCADC18}$ allows reading of internal temperature and voltage rails.<br><br>If both ADC blocks are not used, and reading internal temperature and voltage rails are not required then leave $V_{CCADC18}$ open.<br>1.8 V |

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| Power Input | Recommended Filter | Notes |
|---|---|---|
| ADC_REFP[1:0] | 220 Ω or 120 Ω FB + 1 µF + 100 nF per pin | ADC Block External Reference.<br>Must have very low noise and high accuracy (< 0.1%).<br>Voltage source/regulator should be filtered by<br>220 Ω or 120 Ω FB + 1 µF.<br>If ADC Block is not used, connect to board ground.<br>1.0 V to 1.8 V Typical |
| $V_{CCSD0}$ | 120 Ω FB + 10 µF + 100 nF per pin | SERDES Block Core.<br>If SERDES block is not used, leave it open.<br>1.0 V |
| $V_{CCPLLSD0}$ | 220 Ω FB + 47 µF + 470 nF per pin<br>IMPORTANT: Connect capacitor grounds only to FPGA pin SDx_REFRET | SERDES Block PLL.<br>If SERDER block is not used, leave it open.<br>Route bypass capacitor grounds only to SDx_REFRET.<br>1.8 V |
| $V_{CCAUXSD}$ | 120 Ω FB + 10 µF + 100 nF per pin | SERDES Block Auxiliary.<br>If SERDES block is not used, leave it open.<br>Route bypass capacitor grounds only to SDx_REFRET.<br>1.8 V |

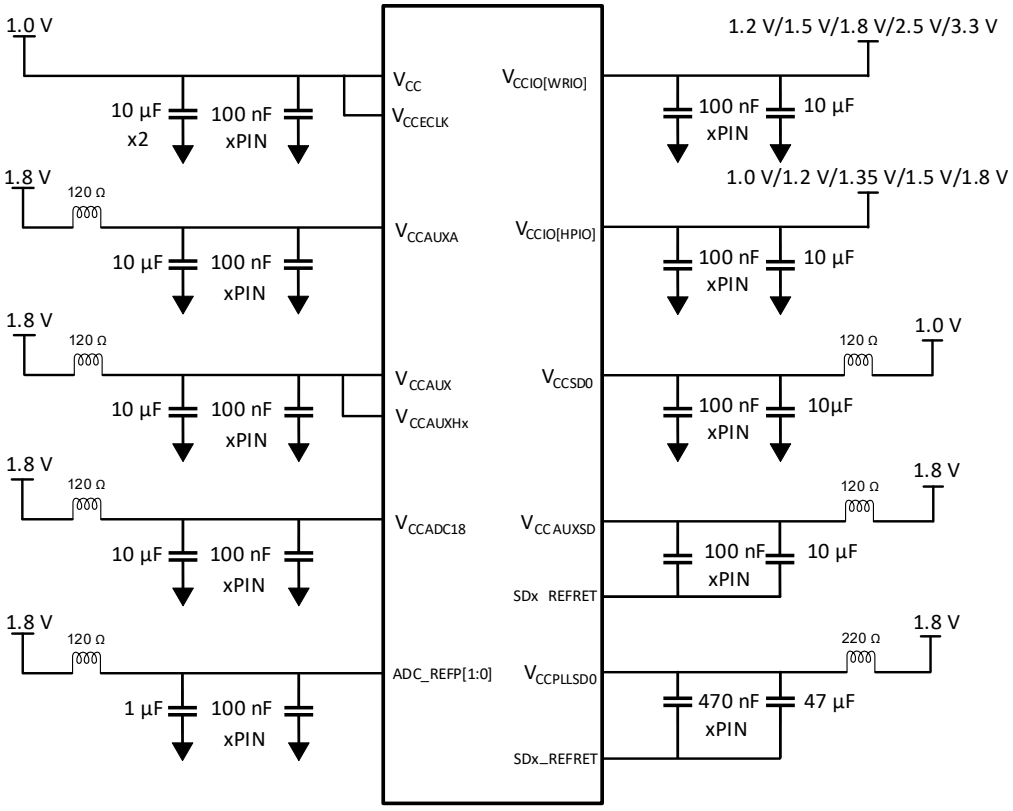


**Figure 3.1. Recommended Power Filters**

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## 3.2. Ground Pins

- All ground pins need to be connected to the board ground plane.
- $V_{SSSD0}$ and $V_{SSADC}$ pins are sensitive to noise and should be isolated from fast switching high current pathways on the ground plane. Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.
- SD0_REFRET — Input SERDES Reference Return Input. This pin should be AC coupled (bypassed) to the $V_{CCPLLSD0}$ supply.

## 3.3. Unused Bank $V_{CCIOx}$

Connect unused $V_{CCIO}$ pins to a power rail, do not leave them open.

## 3.4. Unused ADC Blocks

- Powering $V_{CCADC18}$ allows reading of internal temperature and voltage rails.
  If both ADC blocks are not used, and reading internal temperature and voltage rails are not required then leave $V_{CCADC18}$ open.
- Unused ADC Blocks should connect ADC_REFPx, ADC_DPx and ADC_DNx to board ground.
- $V_{SSADC}$ pins should be connected to the board's ground plane even if ADC blocks are unused.

## 3.5. Unused SERDES Blocks

Connect $V_{SSSD}$, Rx Differential Inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REXT, SDx_REFRET to board ground. Leave $V_{CCSD0}$, $V_{CCPLLSD0}$, $V_{CCAUX}$, and Tx Differential Pair Outputs open.

## 3.6. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-end or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator are recommended.

When specifying components, choose *good-quality* ceramic capacitors in small packages and place them as close to the clock oscillator supply pins as possible. *Good-quality* capacitors for bypassing generally meet the requirement.

## 3.7. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR x CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with an ESR between 0.025 Ω and 0.10 Ω depending on the current load.
- PLL rails draw low current, which allows ferrite beads with an ESR ≤ 0.3 Ω.
- Small package size ferrite beads have a higher ESR than large package size ferrite beads of the same impedance.
- High impedance ferrite beads have a higher ESR than low impedance ferrite beads in the same package size.

## 3.8. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the power supply pins as possible. Good quality capacitors for bypassing generally meet the requirements discussed in the following subsections.

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### 3.8.1. Dielectric

Use dielectrics such as X5R, X7R and similar dielectrics which have good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U and similarly poor capacitance-controlled dielectrics.

### 3.8.2. Voltage Rating

The capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the voltage rail (maximum). Example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

### 3.8.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size-related inductance, the following capacitor sizes are recommended:

**Table 3.2. Recommended Capacitor Sizes**

| Capacitance | Size Preferred | Size Next Best |
|---|---|---|
| 0.1 µF, 1.0 µF, 2.2 µF | 0201 | 0402 |
| 4.7 µF | 0402 | 0603 |
| 10 µF | 0402 | 0603 |
| 22 µF | 0603 | 0805 |

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# 4. Power Sequencing

There is no power-up sequence required for the Certus-NX device.

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# 5. Power Estimation

Once the Certus-NX device density, package, and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant® design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current and maximum DC and AC current for the given system environmental conditions.
- Thermal considerations are also important. The thermal design of the system environment and Certus-NX device should be able to support operating at the maximum operating junction temperature.

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# 6. Configuration Considerations

The Certus-NX device includes provisions to configure the FPGA via the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

**Table 6.1. JTAG Pin Recommendations**

| JTAG Pin | PCB Recommendation |
|---|---|
| TDI/SI | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO}$[1] |
| TMS/SCSN | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO}$[1] |
| TDO/SO | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO1}$[1] |
| TCK/SCLK | 2.2 kΩ pull-down to GND |
| JTAG_EN | 4.7 kΩ pull-down to GND (JTAG port disabled)<br>or 1.0 kΩ pull-up to $V_{CCIO}$[1] (JTAG port enabled) |

**Note:**

1. Use $V_{CCIO1}$ for LFD2NX-9/17/28/40 and use $V_{CCIO2}$ for LFD2NX-15/25/35/65.

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with the corresponding $V_{CCIO}$ and ground.

External resistors are necessary for configuration signals when they are used to handshaking with other devices. However, external pull-up resistors are not required on individual configuration pins if the signal pin is not persistent.

Recommended pull-up resistors to the appropriate bank $V_{CCIO}$ and pull-down resistors to board ground should be used on the pins listed in Table 6.2.

**Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins**

| Pin | PCB Connection |
|---|---|
| PROGRAMN | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO}$[2] |
| INITN | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO}$[2] |
| DONE | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO}$[2] |
| MCLK | 1.0 kΩ to GND (Not installed by default)<br>1.0 kΩ to $V_{CCIO}$[2] (Not installed by default) |
| MCSN | 4.7 kΩ to 10 kΩ pull-up to $V_{CCIO}$[2] |
| SCL/SDA[1] | 1.0 kΩ to 4.7 kΩ pull-up to $V_{CCIO}$[3] |

**Notes**:

1. Pull-up resistors are not required in target I3C configuration mode.
2. Use $V_{CCIO0}$ for LFD2NX-9/17/28/40 and use $V_{CCIO1}$ for LFD2NX-15/25/35/65.
3. Use $V_{CCIO1}$ for LFD2NX-9/17/28/40 and use $V_{CCIO2}$ for LFD2NX-15/25/35/65.

**Table 6.3. Configuration Pins Needed per Programming Mode[1]**

| Configuration Mode | Bank | Enablement | Clock | | Bus Size | Pins |
|---|---|---|---|---|---|---|
| | | | Pin | I/O | | |
| MSPI | 0 | (Default) | MCLK | Output | 1 | MCLK, MCSN, MOSI, MISO |
| | | | | | 2 | MCLK, MCSN, MD0, MD1 |
| | | | | | 4 | MCLK, MCSN, MD0, MD1, MD2, MD3 |
| JTAG | 1 | JTAG_EN pin[2] | TCLK | Input | 1 | TCK, TMS, TDI, TDO |
| SSPI | 1 | Activation key[2] | SCLK | Input | 1 | SCLK, SCSN, SI, SO |
| | | | | | 2 | SCLK, SCSN, SD0, SD1 |
| | | | | | 4 | SCLK, SCSN, SD0, SD1, SD2, SD3 |
| I2C/I3C | 1 | Activation key | SCL | Input | 1 | SCL, SDA |

**Notes:**

1. Leave unused Configuration ports open.
2. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

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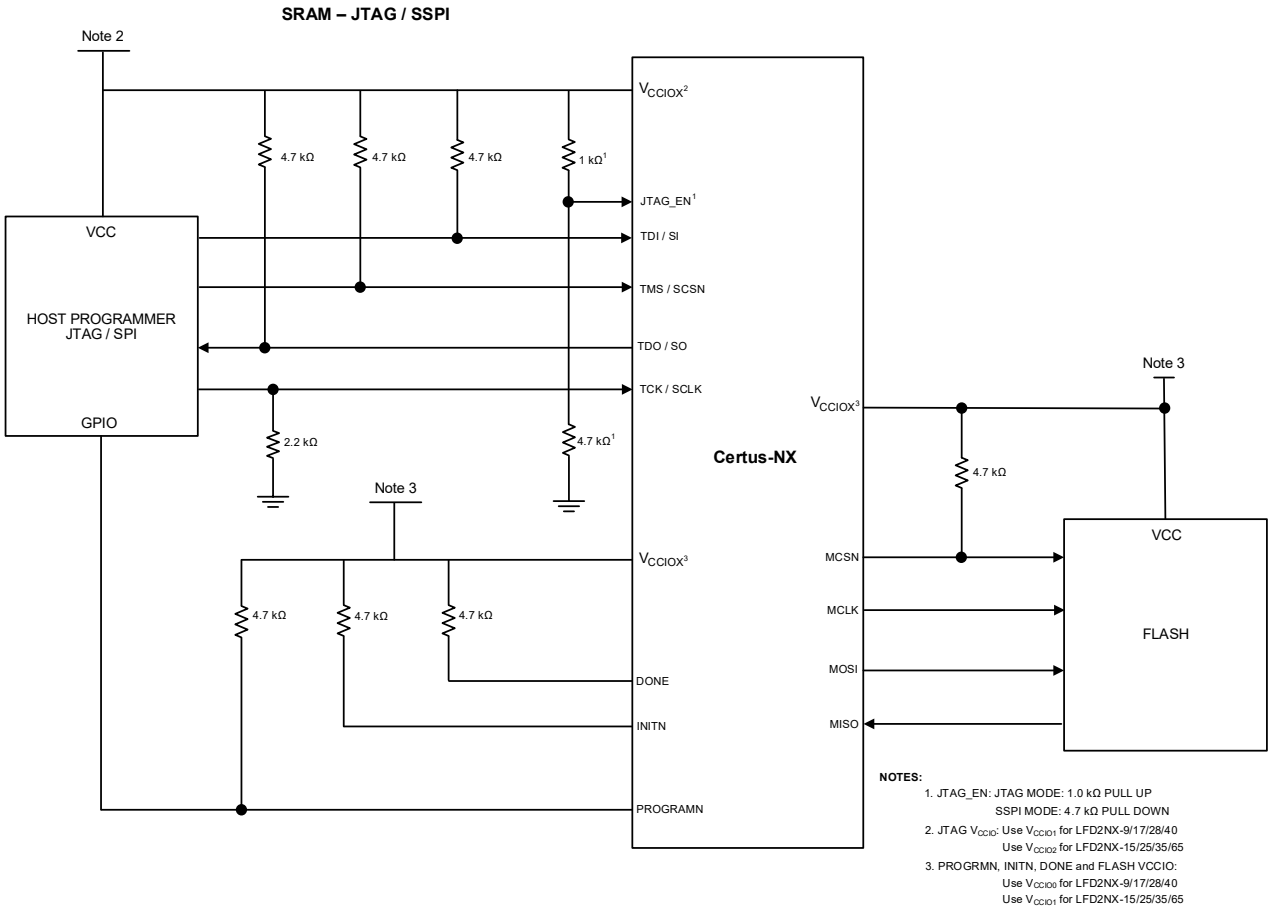


**Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI**

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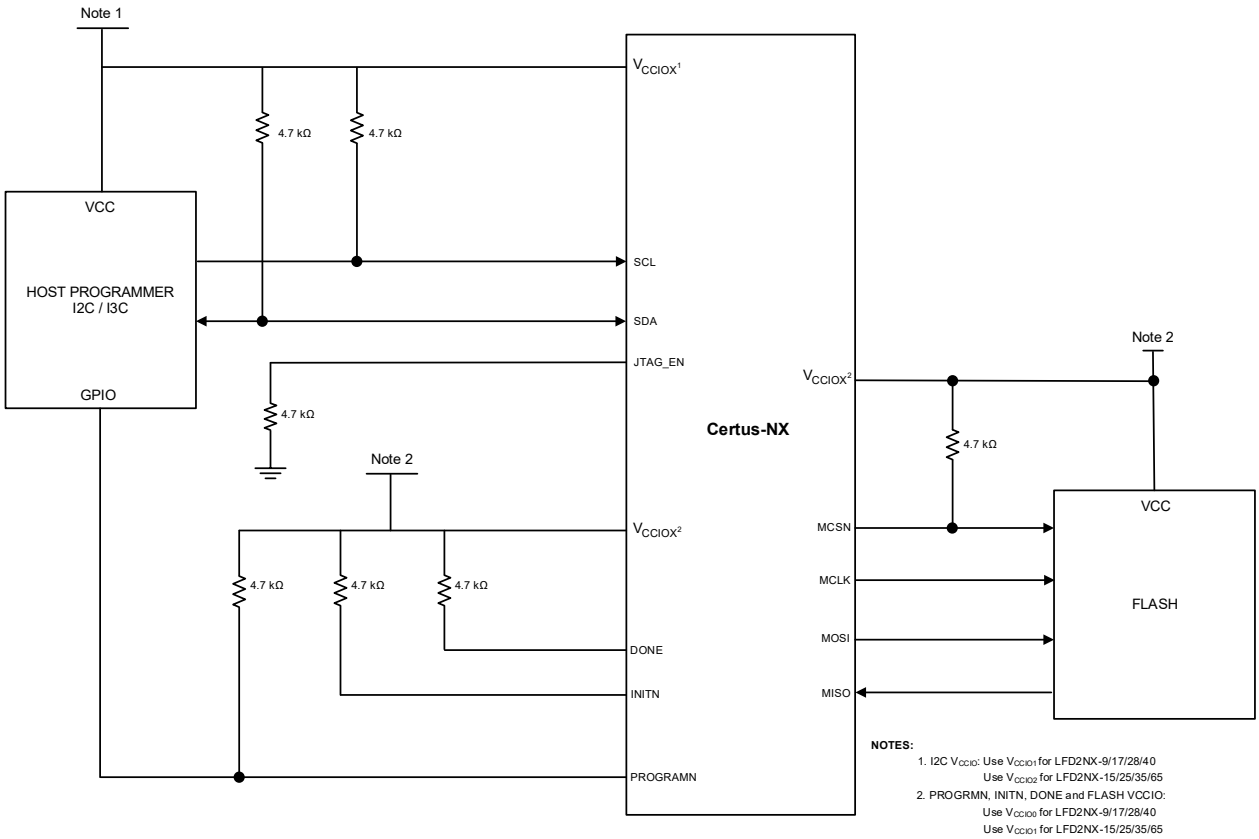


**Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C**

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# 7. External SPI Flash

The SPI Flash voltage should match the Certus-NX bank's $V_{CCIO}$ voltage.

It is recommended to use SPI Flash devices that are supported by the Lattice Radiant Programmer.

You can view the list of supported devices by searching for *SPI Flash support* in the Lattice Radiant Programmer Help menu. For SPI Flash devices that are not listed in the *SPI Flash support*, using the custom flash option may allow non-supported devices to work.

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# 8. I/O Pin Assignments

The $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ provide quiet power supplies for the SERDES blocks. For optimal jitter performance, careful pin assignment is essential to keep noisy I/O pins away from sensitive ones. A leading cause of PCB-related SERDES crosstalk is the placement of FPGA outputs in close proximity to the sensitive SERDES power supplies. These supplies require meticulous board layout to ensure immunity to switching noise generated by FPGA outputs. While guidelines are provided to help build quiet, filtered supplies, robust PCB layout practice are still necessary to prevent noise from infiltrating these analog supplies.

Although coupling has been reduced in the device packages of Certus-NX devices—resulting in minimal crosstalk—the PCB can still introduce significant noise injection from any I/O pin located adjacent to SERDES data, reference clock, power pins, or other critical I/O signals such as clocks. The Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing hardware to reduce the likelihood of crosstalk affecting the analog supplies. PCB traces that run in parallel over long distances require careful analysis. Use a PCB crosstalk simulation tool to evaluate any suspect traces and determine whether they pose a risk.

It is common practice for designers to select pinouts early in the design cycle. This requires FPGA designers to have a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/Os. Lattice Semiconductor provides detailed pinout information, available for download in .csv format from its website, which designers can use as a resource when creating pinout configurations. For example, by accessing the pinout.csv file, users can obtain pinout details for all package variants within a device family, including I/O banking, differential pairing, dual -function pins, and input/output characteristics.

## 8.1. Early I/O Release

The Certus-NX device supports an Early I/O Release feature, which enables I/O pins located in the left and right I/O banks to assume user-defined drive states early in the bitstream processing sequence. Specifically, this applies to LFD2NX-15/25/35/65 devices (Banks 2, 3, 4, 7, 8, 9) and LFD2NX-9/17/28/40 devices (Banks 1, 2, 6, 7). The feature activates after the I/O configuration data for these banks—located near the beginning of the bitstream—is processed. Once the left/right Memory Interface Block is programmed, the corresponding I/O pins are released to their predefined states. To enable this feature, set the EARLY_IO_RELEASE preferences to ON in the Lattice Radiant Device Constraint Editor.

In addition, using the Early I/O Release feature requires instantiating an output buffer register with an asynchronous set or reset function to define the desired drive behavior—logic high (1) or logic low (0), respectively—during the early release period. Unregistered outputs in Early-Release banks will remain in High-Z (high impedance) state until the full device configuration is complete. Note that certain dual-purpose sysCONFIG I/O pins cannot be used for Early I/O Release. Refer to the device pinlist .csv file to identify which pins supports this feature. Additionally, if ECDSA bitstream authentication is enabled on the Certus-NX device, the Early I/O Release feature is not supported.

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# 9. sysI/O

The Certus-NX device offers flexibility to configure each I/O according to your design requirements. Pins can be set as input, output, or tri-state. You can also configure attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH.

For PULLMODE, both pull-up and pull-down resistors can be enabled. These resistors are implemented using a constant current source, with values specified in Table 9.1.

**Table 9.1. Weak Pull-up/Pull-down Current Specifications**

| Configuration | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Pull-up | I/O Weak Pull-up Resistor Current | $0 \le V_{IN} \le 0.7 \times V_{CCIO}$ | –30 | –150 | µA |
| Pull-down | I/O Weak Pull-down Resistor Current | $V_{IL}$ (max) $\le V_{IN} \le V_{CCIO}$ | 30 | 150 | µA |

The Certus-NX device also provides special I/O like HPIO and WRIO that can be used for high-speed communication. Figure 9.1 shows the block diagram for HPIO and Figure 9.2 shows the block diagram for WRIO.

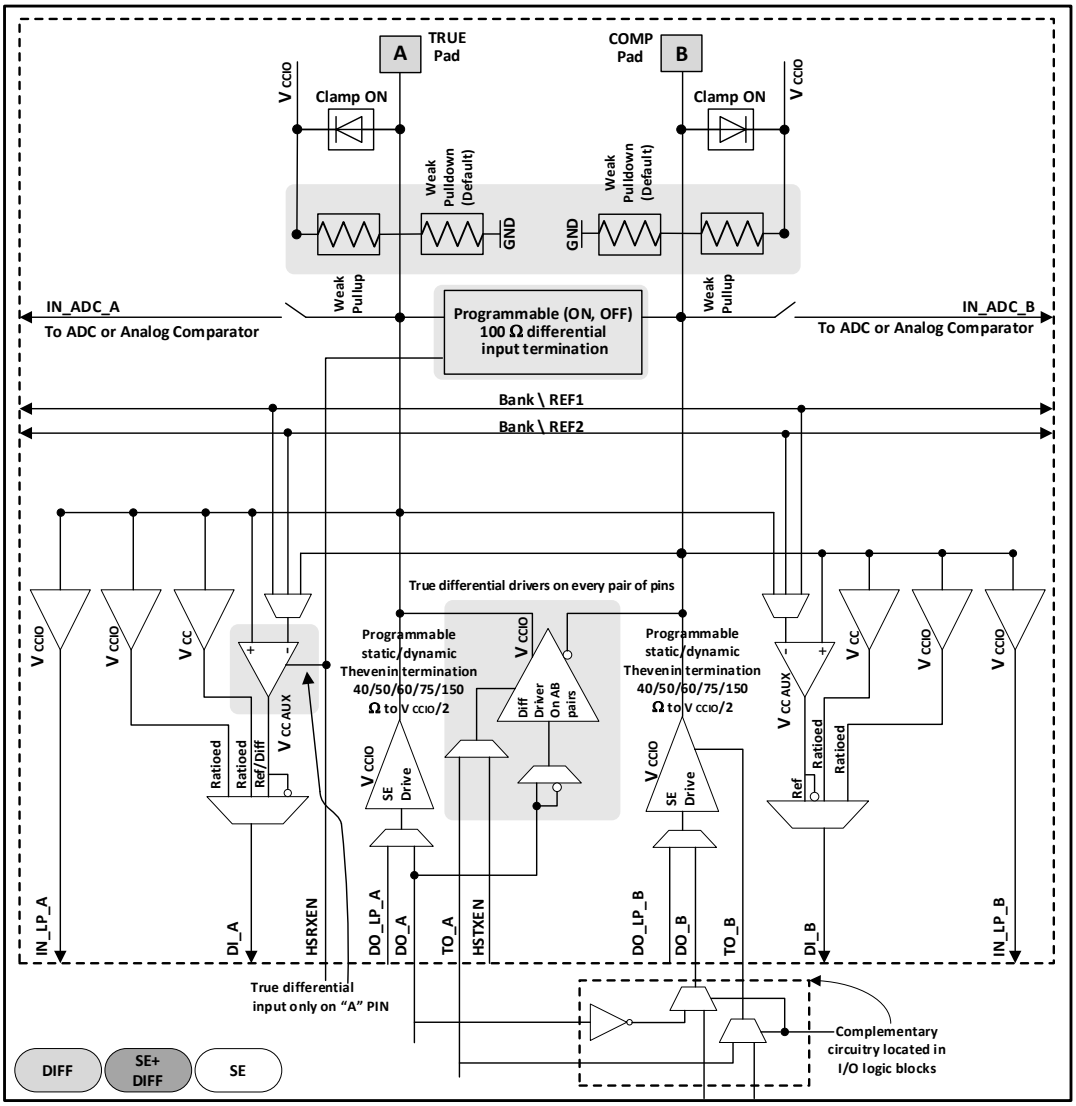


**Figure 9.1. High-Performance sysI/O Buffer Pair for Bottom Side**

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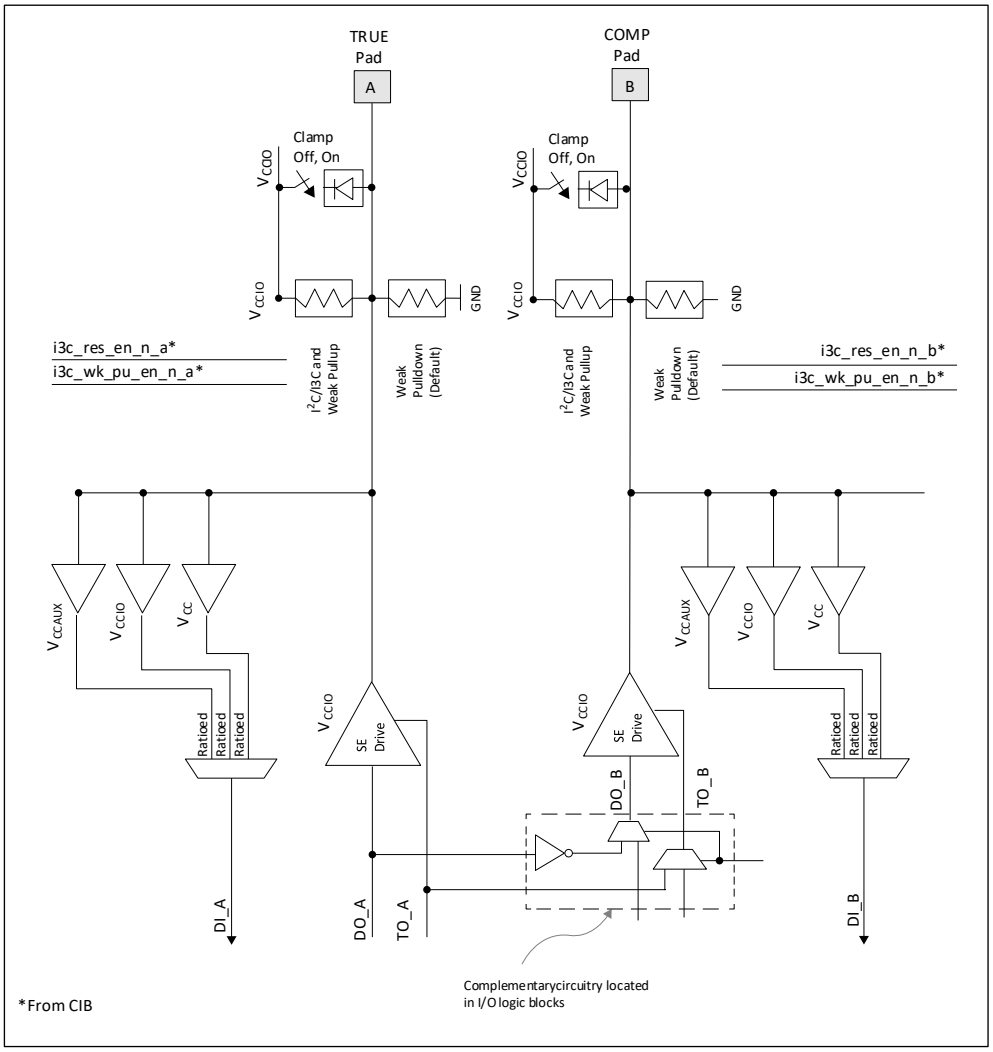


**Figure 9.2. Wide-Range sysI/O Buffer for Top and Left/Right Sides**

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# 10. Clock Inputs

The Certus-NX device provides dedicated pins in each I/O bank that can be used as clock inputs. These pins are shared and may alternately function as general-purpose I/Os. When using them for clocking purposes, it is important to minimize signal noise on these pins. For detailed guidance, refer to the Certus-NX High-Speed I/O Interface (FPGA-TN-02216).

These shared clock input pins, typically labeled as GPLL and PCLK, are listed under the *Dual Function* column of the pinlist .csv file. High-speed differential interfaces (such as MIPI) must route their differential clock pairs into inputs that support differential clocking, specifically labeled as PCLKTx_y (+true) and PCLKCx_y (–complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage does not exceed the voltage level of the target I/O bank. Proper power supply decoupling of the clock oscillator is also essential to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

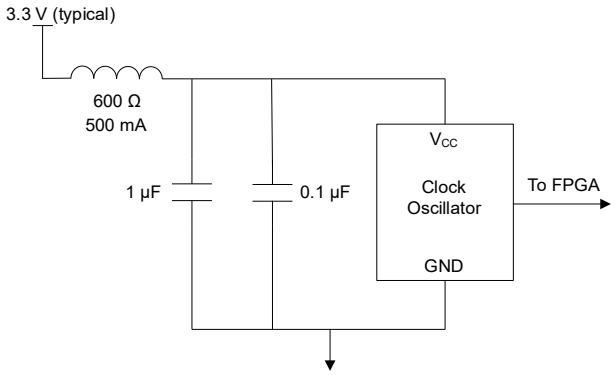


**Figure 10.1. Clock Oscillator Bypassing**

For differential clock inputs to banks with a $V_{CCIO}$ voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to ensure the clock voltage remains less than or equal to the bank's $V_{CCIO}$. An LVDS oscillator may also be used if it is AC-coupled and then DC-biased to half of the $V_{CCIO}$ voltage. An example of a dual-footprint design that supports both HCSL and LVDS oscillators is as shown in Figure 10.2.

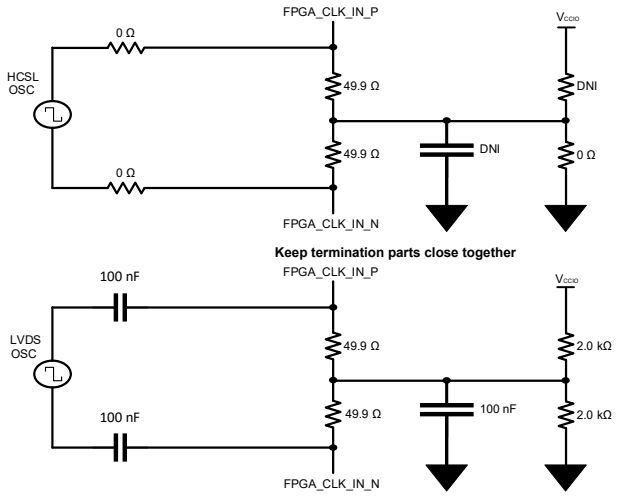


**Figure 10.2. PCB Dual Footprint Design Supporting HCSL and LVDS Oscillators**

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## 10.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enabled pin is shown in Figure 10.3.

**Note:** External board oscillators typically require 5 to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

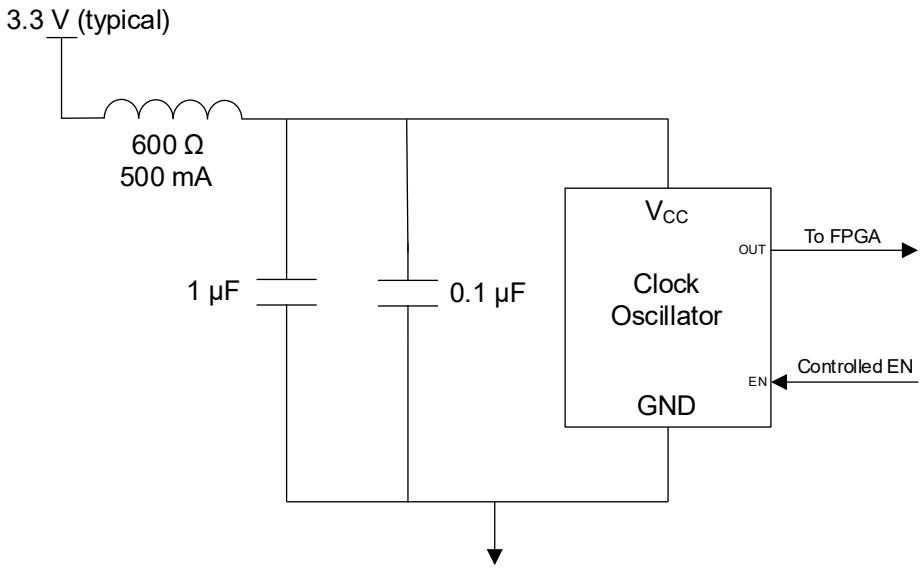


**Figure 10.3. Clock Oscillator with Controlled Enable Pin**

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# 11. Pinout Considerations

The Certus-NX device supports a wide range of high-speed interface applications. These interfaces often require rule-based pinouts that must be understood before beginning PCB design. Pinout selection should be done with a clear understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and the use of PLLs and DLLs. To minimize noise and ensure signal integrity, avoid placing noisy I/Os adjacent to sensitive analog I/Os. For detailed guidelines on these interface types, refer to the Certus-NX High-Speed I/O Interface (FPGA-TN-02216).

## 11.1. LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins located on the bottom side of the devices. The top, left, and right side I/O banks do not support the True LVDS standard but can support emulated LVDS outputs. True LVDS input pairings on the bottom banks are listed under the High-Speed column in the pinlist .csv file.

Emulated LVDS outputs are available in pairs across all banks; however, they require external termination resistors. This implementation is described in sysI/O User Guide for Nexus Platform (FPGA-TN-02067).

## 11.2. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards that require an external reference voltage. These standards are supported only on the bottom I/O banks of the device.

When assigning pins on the PCB, give high priority to the $V_{REF}$ pins. These can be identified in the Dual Function column of the pinlist .csv file, labeled as $V_{REF}$. Each I/O bank has a dedicated reference voltage ($V_{REF}$), which sets the threshold for the referenced input buffers. Individual I/Os are configurable based on the bank's supply and reference voltages.

Connect a 0.1 µF capacitor to ground near each active $V_{REF}$ pin. The $V_{REF}$ power source should have a relatively low output impedance (≤ 130 Ω).

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# 12. DPHY and SERDES Pin Considerations

High-speed signaling requires careful PCB design to maintain proper transmission line characteristics. A continuous ground reference should be preserved along high-speed routing paths. Differential pairs must be tightly length-matched, with a mismatch no greater than ±4 mils, and should have minimal discontinuities.

The DPHY clock input must use a PCLK pin to ensure direct routing to the edge clock tree.

For recommended methods and design guidance, refer to High-Speed PCB Design Considerations (FPGA-TN-02178).

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# 13. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a $V_{CC}$ plane, then a stitching capacitor should be used (ground to $V_{CC}$).

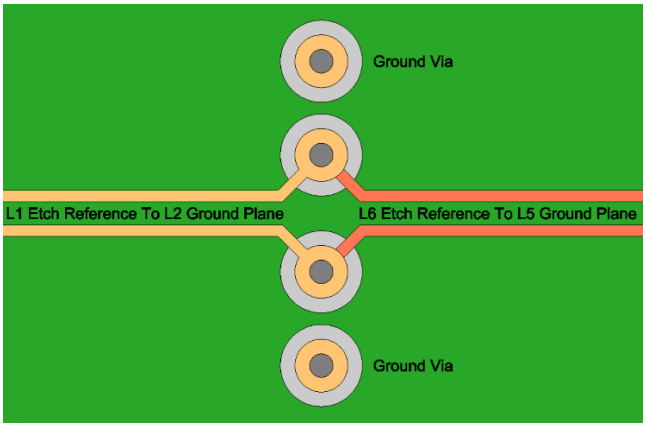


**Figure 13.1. Ground Vias Implementation**

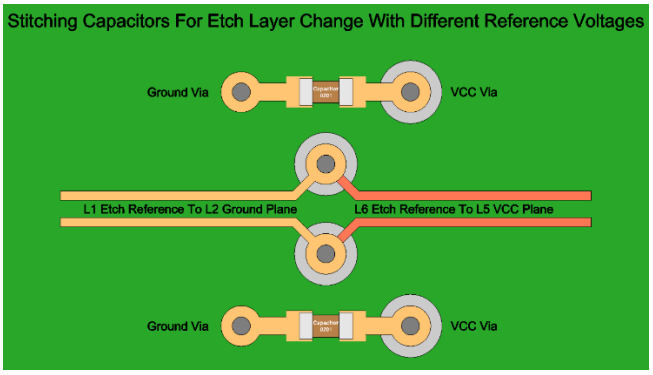


**Figure 13.2. Stitching Vias Implementation**

6. High-speed signals have a corresponding impedance requirement. Calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5 mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

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# 14. Simulation and Board Measurement of Critical Signals

To ensure design reliability and high manufacturing yield, critical signals should be simulated during the design phase and subsequently measured on the assembled PCB to verify proper functionality.

## 14.1. Critical Signals

Signals that are sensitive to Signal Integrity (SI) degradation are considered critical signal and require additional design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

## 14.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often require recurring subscription fees. These premium tools can import board design files and provide accurate simulations that include crosstalk and other signal integrity (SI) degrading effects.

Free IBIS-based tools (like Micro-cap) can offer useful basic simulations, but they require more manual effort to set up SI effects—especially when dealing with multiple signals, varying transmission line lengths, lossy lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

## 14.3. Board Measurements

Critical signals should be measured on the assembled PCB using an oscilloscope to verify proper signaling behavior and signal integrity (like eye diagrams and other SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (for example output series termination resistor value).
- Adjust the setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (for example USB, MIPI).

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# 15. Checklist

**Table 15.1. Hardware Checklist**

| No. | Item | OK | NA |
|---|---|---|---|
| **1** | **FPGA Power Supplies** | | |
| 1.1 | Core Supplies | | |
| 1.1.1 | $V_{CC}$ and $V_{CCECLK}$ tied together core at 1.0 V ±3% (allowing for 2% noise). | | |
| 1.1.2 | Use a PCB plane for $V_{CC}$ and $V_{CCECLK}$ core with proper decoupling. | | |
| 1.1.3 | $V_{CC}$ and $V_{CCECLK}$ core sized to meet power requirement calculation from software. | | |
| 1.1.4 | $V_{CCAUX}$, $V_{CCAUXHx}$, and $V_{CCAUXA}$ at 1.8 V ±3% (allowing for 2% noise). | | |
| 1.1.5 | $V_{CCAUX}$, $V_{CCAUXHx}$, and $V_{CCAUXA}$ must be quiet and isolated from other switching noises. | | |
| 1.1.6 | $V_{CCAUX}$ pins ganged together with $V_{CCAUXHx}$ pins. Solid PCB plane is recommended. | | |
| 1.1.7 | $V_{CCAUXA}$ is sensitive, these pins should be ganged together and use a separate FB + Capacitor filtering. Solid PCB plane is recommended. | | |
| 1.2 | I/O Supplies | | |
| 1.2.1 | All *Wide Range* $V_{CCIO}$ are between 1.2 V to 3.3 V<br>LFD2NX-15/25/35/65 Banks 0, 1, 2, 3, 4, 7, 8, 9, 11<br>LFD2NX-9/17/28/40 Banks 0, 1, 2, 6, 7 | | |
| 1.2.2 | All *High Performance* $V_{CCIO}$ are between 1.0 V to 1.8 V<br>LFD2NX-15/25/35/65 Banks 5, 6<br>LFD2NX-9/17/28/40 Banks 3, 4, 5 | | |
| 1.2.3 | $V_{CCIOx}$ bank voltage matches sysCONFIG peripheral devices such as system I3C, SPI Flash, and the like. | | |
| 1.3 | ADC power supplies | | |
| 1.3.1 | $V_{CCADC18}$ is 1.8 V ±5% | | |
| 1.3.2 | $V_{CCADC18}$ quiet and isolated | | |
| 1.3.3 | Use accurate voltage reference for ADC_REFP[1:0] (≤ ±0.1%). | | |
| 1.3.4 | If both ADC blocks are not used, and reading internal temperature and voltage rails are not required then leave $V_{CCADC18}$ open. | | |
| 1.3.5 | Unused ADC Blocks should connect ADC_REFPx, ADC_DPx and ADC_DNx to board ground. | | |
| 1.3.6 | $V_{SSADC}$ pin should connect to the board's ground plane even if ADC Blocks are unused. | | |
| 1.4 | SERDES Power Supplies | | |
| 1.4.1 | $V_{CCSD0}$ are at 1.0 V ±5% | | |
| 1.4.2 | $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ are 1.8 V +5% | | |
| 1.4.3 | $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ quiet and isolated from each other and other 1.8 V supplies | | |
| 1.4.4 | $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ bypass capacitor grounds go only to SDx_REFRET. | | |
| 1.4.5 | Unused SERDES<br>Connect to board ground $V_{SSSDQ}$ pins, SD_RXDP/N, SD_REXT, SD_REFRET and SD_REFCLKP/N.<br>Leave the following open: $V_{CCSD0}$, $V_{CCPLLSD0}$, SD_TXDP/N, $V_{CCAUXSD}$. | | |
| 1.5 | Grounds | | |
| 1.5.1 | All ground pins must be connected to low impedance ground plane. | | |
| **2** | **JTAG** | | |
| 2.1 | Apply a pull-up or pull-down resistor to the JTAG_EN pin, as specified in Table 6.2. | | |
| 2.2 | Ensure the JTAG_EN pin remains accessible on the PCB to allow JTAG port recovery, particularly during development. | | |
| 2.3 | Ensure JTAG port pins remain accessible on the PCB, particularly during development. | | |
| 2.4 | Pull-down on TCK as specified in Table 6.1. | | |
| 2.5 | Pull-up on TMS as specified in Table 6.1. | | |
| **3** | **Configuration** | | |
| 3.1 | Apply pull-up or pull-down resistors on persisted configuration-specific pins as specified in Table 6.1 and Table 6.2. | | |
| 3.2 | $V_{CCIO}$ bank voltages must match the sysCONFIG peripheral devices such as SPI Flash. | | |

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| No. | Item | OK | NA |
|---|---|---|---|
| **4** | **Special Pin Assignments** | | |
| 4.1 | $V_{REF}$ assignments must be applied for single-ended SSTL input signals. | | |
| 4.2 | Properly decouple the $V_{REF}$ source. | | |
| **5** | **Critical Pinout Selection** | | |
| 5.1 | The pinout is selected to align FPGA resource connections with I/O logic and clock resources, in accordance with the Certus-NX High-Speed I/O Interface (FPGA-TN-02216). | | |
| 5.2 | Shared general-purpose I/Os are used as inputs for the FPGA PLL and clock input signals. | | |
| 5.3 | Differential pair I/O polarity: I/O are named P[T/B/L/R] [Number]_[A/B].<br>In differential pair, the positive signal connects to the pin ending in **A**, and the negative signal connects to the pin ending in **B**. | | |
| 5.4 | Differential clock inputs must be assigned to PCLK pins to enable direct routing to the edge clock tree. | | |
| 5.5 | For single-ended I/Os, use only PCLKT pins as primary CLK pads. | | |
| 5.6 | Soft MIPI interfaces are supported only on HPIO banks. | | |
| **6** | **DDR3, DDR3L, and LPDDR2 Interface Requirements** | | |
| 6.1 | DQ, DM, and DQS signals should be routed as a data group with similar trace lengths and matched via counts. It is recommended to use no more than three vias between the FPGA controller and the memory device. | | |
| 6.2 | Maintain trace length matching to a maximum of ±50 mil between each DQ/DM signal and its associated DQS strobe in a DQ group. Use precise serpentine routing technique to achieve this requirement. | | |
| 6.3 | Each data group must reference a continuous ground plane within the PCB stack-up. | | |
| 6.4 | DDR trace must reference a solid, uninterrupted ground plane, with no slots or breaks, along the entire path between the FPGA and the memory device. | | |
| 6.5 | Maintain a minimum spacing of 3 W between each data group and any unrelated signals to minimize crosstalk. For all DDR traces— excluding differential CK and DQS pairs—use a minimum of 2 W spacing (W refers to the minimum trace width allowed). | | |
| 6.6 | FPGA I/O assignments within a data group may be swapped to optimize layout, except for DQS signals, which must remain fixed. | | |
| 6.7 | Differential pairs of DQS to DQS_N trace lengths should be matched at ±10 mil. | | |
| 6.8 | Placing resistor terminations (DQ) in a fly-by configuration at the FPGA is highly recommended. If stub-style terminations are used, ensure that stub lengths do not exceed 600 mil. | | |
| 6.9 | LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil. | | |
| 6.10 | Address and control signals, along with associated CK and CK_N differential clock pair, should be routed with trace length matching within ±100 mil. | | |
| 6.11 | CK to CK_N trace lengths must be matched within ±10 mil. | | |
| 6.12 | Address and control signals may reference a power plane if a ground plane is unavailable; however, a ground reference is preferred. | | |
| 6.13 | Route address and control signals on a separate layer from DQ, DQS, and DM signals to minimize crosstalk. | | |
| 6.14 | The differential termination for the CLK/CLKN pair must be placed as close as possible to the memory device. | | |
| 6.15 | Using a fly-by termination technique—placing address and control terminations after the memory component is highly recommended. If stub-style terminations are used, stub lengths must not exceed 600 mils. | | |
| **7** | **External Flash** | | |
| 7.1 | Flash voltage should match $V_{CCIO}$ voltage. | | |
| **8** | **SERDES** | | |
| 8.1 | The dedicated reference clock input from the clock source must meet both DC and AC electrical requirements. | | |
| 8.2 | External AC coupling capacitors may be required to ensure compatibility with common-mode voltage levels of connected devices. | | |
| 8.3 | Reference clock termination resistors may be required to ensure compatible signaling levels. | | |

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| No. | Item | OK | NA |
|---|---|---|---|
| 8.4 | Ensure proper routing of high-speed transmission line. | | |
| 8.5 | Continuous ground reference plane to serial channels | | |
| 8.6 | Tightly length matched differential traces, ±4 mils maximum | | |
| 8.7 | Do not route other signals on the PCB layers directly above or below high-speed SERDES without isolation. | | |
| 8.8 | Avoid routing non-SERDES signal traces above or below the $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ power plane without isolation. | | |
| **9** | **ADC** | | |
| 9.1 | When using the ADC function, route the clock through the lower-right corner PLL. | | |
| **10** | **Clock Input** | | |
| 10.1 | External clock source must be connected to PCLK or GPLL pins. | | |
| 10.2 | PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the PLL Reference Clock Locking section for more details. | | |
| **11** | **Layout Recommendations** | | |
| 11.1 | Power should be delivered through dedicated power planes to ensure reliable power distribution and thermal stability. | | |
| 11.2 | Analog circuits should be placed away from digital circuits and high-switching components. | | |
| 11.3 | High-speed signal traces should maintain a clearance of at least five times the trace width from adjacent signals. | | |
| 11.4 | When high-speed signals transitions between PCB layers, a corresponding ground via should be placed nearby if both reference planes are ground. If the reference planes differ, a stitching capacitor should be used. | | |
| 11.5 | High-speed signals have specific impedance requirements. Calculate the necessary trace width and trace gap (differential gap) based on the intended PCB stack-up. Always verify the trace dimensions with your PCB vendor. | | |
| **12** | **Simulation and Board Measurement of Critical Signals** | | |
| 12.1 | Simulations: Use IBIS model to simulate critical signals for proper signal integrity. | | |
| 12.1.1 | Simulate differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like). | | |
| 12.1.2 | Simulate clock nets (Oscillator Inputs, Output Clocks). | | |
| 12.1.3 | Simulate data nets with embedded clocks. | | |
| 12.1.4 | Simulate interrupts (Edge Triggered). | | |
| 12.1.5 | Simulate logic signals travelling long distances requiring termination. | | |
| 12.1.6 | Simulation results should be used to optimize each critical signal for best signal integrity:<br>• Define output pin drive strength<br>• Define output pin slew rate<br>• Define output pin termination design (for example output series termination resistor value)<br>• Define setting of internal pin pull-up and pull-down resistors<br>Improve PCB layout. | | |
| 12.2 | Board Measurements: Use an oscilloscope to measure critical signals on the assembled PCB to verify proper functionality and signal integrity. | | |
| 12.2.1 | Measure differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like). | | |
| 12.2.2 | Measure clock nets (Oscillator Inputs, Output Clocks). | | |
| 12.2.3 | Measure data nets with embedded clocks. | | |
| 12.2.4 | Measure interrupts (Edge Triggered). | | |
| 12.2.5 | Measure logic signals travelling long distances requiring termination. | | |

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| No. | Item | OK | NA |
|---|---|---|---|
| 12.2.6 | Measurement results should be used to optimize each critical signal for best signal integrity:<br>• Adjust output pin drive strength<br>• Adjust output pin slew rate<br>• Adjust output pin termination design (for example output series termination resistor value).<br>Adjust setting of internal pin pull-up and pull-down resistors. | | |
| 12.3 | Specification compliance testing is recommended for widely used signaling standards (like USB, MIPI). | | |

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# References

- Certus-NX web page
- Certus-NX Family Data Sheet (FPGA-DS-02078)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- Certus-NX High-Speed I/O Interface (FPGA-TN-02216)
- Thermal Management (FPGA-TN-02044)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SERDES Jitter (TN1084)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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# Revision History

**Revision 1.9, October 2025**

| Section | Change Summary |
|---|---|
| All | Minor editorial fixes. |
| Abbreviations in This Document | Updated section contents. |
| Introduction | The statement, *The device family consists of FPGA densities ranging from 9K to 40K Logic Cells,* has been removed as of revision 1.8. |
| Clock Inputs | • Added the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*.<br>• Added PLL Reference Clock Locking section. |
| Layout Recommendations | Replaced Figure 13.1 and Figure 13.2 with colored versions. |
| Checklist | • Added item 5.5, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*.<br>• Added *Clock Inputs* under *item 10*. |

**Revision 1.8, July 2025**

| Section | Change Summary |
|---|---|
| All | • Minor editorial fixes.<br>• Changed *SerDes* to *SERDES*. |
| Abbreviations in This Document | Replaced *Acronyms* with *Abbreviations*. |
| Introduction | Added *Hardware Checklists are developed after Evaluation boards and incorporate optimized designs that supersede the circuitry of Evaluation boards. Customers copying circuits from Evaluation boards should optimize their designs according to the Hardware Checklists*, after the first paragraph of this section. |
| Power Supplies | • Reworked the first paragraph of this section.<br>• Added *LFD2NX-15/25/35/65* and *LFD2NX-9/17/28/40* in this section.<br>• Updated the title of Table 2.1 from *Single-Ended I/O Standards* to *Power Supplies*.<br>• Reworked Table 2.1. Power Supplies. Deleted VCCIO[7 0] and added the following:<br>  • *VCCIO[11, 9:0] LFD2NX-15/25/35/65*<br>  • *VCCIO[7 0] LFD2NX-9/17/28/40*<br>• Replaced *0.25% peak noise* with *0.50% peak noise* in the last sentence of the Power Source section. |
| Power Supply Filtering | • Reworked this section.<br>• Updated section title from *Certus-NX SERDES and ADC Power Supplies* to *Power Supply Filtering*.<br>• Updated Table 3.1. Recommended Power Filtering Groups and Components.<br>  • Updated the notes of VCCAUX, VCCAUXHx, VCCIO[11, 9:0], VCCADC18, and ADC_REFP[1:0].<br>• Updated Figure 3.1. Recommended Power Filters. |
| Power Estimation | Updated the second bullet of this section to *Thermal considerations are also important. The thermal design of the system environment and Certus-NX device should be able to support operating at the maximum operating junction temperature*. |
| Configuration Considerations | Reworked section contents including tables and figures. |
| External Flash | Added *Certus-NX bank* in the first sentence of this section. |
| I/O Pin Assignments | • Added Early I/O Release section.<br>• Removed *Solder Reflow Guide (FPGA-TN-02041)* document from this section. |

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| Section | Change Summary |
|---|---|
| Clock Inputs | Replaced the statement *It is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's $V_{CCIO}$ for differential clock inputs to banks with $V_{CCIO}$ voltage of 1.5 V and lower* with: *For differential clock inputs to banks with a VCCIO voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to ensure the clock voltage remains less than or equal to the bank's $V_{CCIO}$.* |
| Pinout Considerations | Added the statement *Avoid placing noisy I/O adjacent to sensitive analog I/Os*. |
| HSUL and SSTL Pin Assignments | Added the statement *Connect a 0.1 µF capacitor to ground near each active VREF pin. The VREF power source should have a relatively low output impedance ($\leq$ 130 Ω).* |
| Layout Recommendations | Replaced Figure 15.1 Recommended Layout with Figure 13.1. Ground Vias Implementation and Figure 13.2. Stitching Vias Implementation. |
| Simulation and Board Measurement of Critical Signals | Added this section. |
| Checklist | Reworked checklist contents.<br>• Item 1 FPGA Power Supplies<br>• Item 3 Configuration<br>• Item 5 Critical Pinout Selection<br>• Item 10 Layout Recommendations<br>• Item 11 Simulation and Board Measurement of Critical Signals |

**Revision 1.7, July 2024**

| Section | Change Summary |
|---|---|
| Introduction | Updated *17K* to *9K* Logic Cells in the Introduction section. |

**Revision 1.6, June 2024**

| Section | Change Summary |
|---|---|
| All | • Minor editorial fixes.<br>• Changed *$I^2C$ to I2C*.<br>• Changed *Master to Controller*.<br>• Changed *Slave to Target*. |
| Inclusive Language | Added this section. |
| Certus-NX SerDes and ADC Power Supplies | • Updated the recommended filter of VCCPLLSD0 to *220 Ω FB + 47 µF + 470 nF per pin* in Table 3.1. Recommended Power Filtering Groups and Components.<br>• Added *Bypass capacitor grounds go only to SDx_REFRET* to the VCCAUXSD notes in Table 3.1. Recommended Power Filtering Groups and Components.<br>• Updated Figure 3.1. Recommended Power Filters to align with the changes of VCCPLLSD0 and VCCAUXSD in Table 3.1. Recommended Power Filtering Groups and Components. |

**Revision 1.5, April 2024**

| Section | Change Summary |
|---|---|
| All | Minor editorial fixes. |
| Certus-NX SerDes and ADC Power Supplies | Updated the Unused ADC Blocks to *Connect $V_{SSADC}$, ADC_REFPx, ADC_DPx, and ADC_DNx pins to board ground. Leave $V_{CCADC18}$ floating (not connected)*. |

**Revision 1.4, March 2024**

| Section | Change Summary |
|---|---|
| Disclaimers | Updated boilerplate. |
| Acronyms in This Document | Added *ADC*, *FPGA*, *HPIO*, *I/O*, *MIPI*, *PCB*, *WLCSP*, and *WRIO* to the list of acronyms. |

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| Section | Change Summary |
|---|---|
| Introduction | Added ADC User Guide for Nexus Platform (FPGA-TN-02129) to the list of documents for detailed recommendations. |
| Power Supplies | Updated the *Voltage* value for the *ADC_REFP[1:0]* in Table 2.1. Single-Ended I/O Standards. |
| Certus-NX SERDES and ADC Power Supplies | • Updated the *Recommended Filter* and *Notes* in Table 3.1. Recommended Power Filtering Groups and Components for the following *Power Inputs*:<br>• *ADC_REFP[1:0]*<br>• $V_{CCPLLSD0}$<br>• Replaced previous *Figure 3.1. Clock Oscillator Bypassing* with new Figure 3.1. Recommended Power Filters.<br>• Removed the following sentences from Clock Oscillator Supply Filtering section:<br>• *A typical bypassing circuit is shown below in Figure 3.1. Clock Oscillator Bypassing.*<br>• *When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the clock oscillator supply pins as practically possible.*<br>• *Good quality capacitors for bypassing generally meet the following requirements:*<br>• Moved Dielectric, Voltage Rating, and Size subsections into newly added Capacitor Selection section.<br>• Updated the heading numbers of remaining section headers after Capacitor Selection section.<br>• Updated the paragraphs of Unused SERDES Blocks section. |
| Configuration Considerations | • Updated Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins:<br>• Updated *PCB Connection* recommendations for *MCLK* pin .<br>• Added a *Note* for *SCL/SDA* pin.<br>• . Updated the *Notes* section for Table 6.3. Configuration Pins Needed per Programming Mode1.<br>• Added Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI and Figure 6.2. Typical Connections for Programming SRAM via $I^2C$/I3C.<br>• Updated the figure number of Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks. |
| External SPI Flash | Added this section and updated the heading numbers of remaining sections accordingly. |
| sysI/O | Added this section and updated the heading numbers of remaining sections accordingly. |
| Clock Inputs | • Updated the paragraphs of this section.<br>• Added Figure 10.1. Clock Oscillator Bypassing and Figure 10.2. PCB Dual Footprint Design Supporting HCSL and LVDS Oscillators. |
| Layout Recommendations | Added this section and updated the heading numbers of remaining sections accordingly. |
| Checklist | • Added checklist items *7. External Flash* and *9. ADC*.<br>• Updated checklist number for item *8. SERDES*. |
| References | Added references to:<br>• Certus-NX Family Data Sheet (FPGA-DS-02078)<br>• ADC User Guide for Nexus Platform (FPGA-TN-02129)<br>• PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)<br>• PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)<br>• Lattice Insights web page |

**Revision 1.3, July 2023**

| Section | Change Summary |
|---|---|
| Checklist | Updated Table 13.1. Hardware Checklist to change row 6 from 'LPDDR3 and DDR3 Interface Requirements' to 'DDR3, DDR3L, and LPDDR2 Interface Requirements'. |
| References | Newly added section. |

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**Revision 1.2, March 2022**

| Section | Change Summary |
|---|---|
| Power Supplies | Added the $V_{CCECLK}$ in the Supply column of Table 2.1. Single-Ended I/O Standards. |
| Certus-NX SERDES and ADC Power Supplies | In Table 3.1. Recommended Power Filtering Groups and Components, changed the Power Input $V_{CC}$ to $V_{CC}$, $V_{CCECLK}$ and updated the corresponding Recommended Filter and Notes. |

**Revision 1.1, February 2022**

| Section | Change Summary |
|---|---|
| DPHY & SERDES PIN Considerations | • Updated the title of Section 12 from SERDES PIN Considerations to DPHY & SERDES PIN Considerations.<br>• Added a line to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. |
| Checklist | Added a row in Table 13.1 to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. |

**Revision 1.0, July 2020**

| Section | Change Summary |
|---|---|
| All | Initial release. |

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