High-Speed PCB Design Considerations

Technical Notes

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
BGA	Ball Grid Array
CML	Current Mode Logic
DC Drop	Voltage Drop
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
ESL	Equivalent Series Inductance
ESR	Effective Series Resistance
GND	Ground
IC	Integrated Circuit
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board
SERDES	Serializer/Deserializer
SPICE	Simulation Program with Integrated Circuit Emphasis
TDR	Time Domain Reflectometer
Tx	Transmitter
Rx	Receiver
RTF	Reverse Treat Foil
VLP	Very low profile
HVLP	Ultra low profile
ISI	Intersymbol Interference

1. Introduction

This document will assist PCB designers in successfully implementing high-speed PCB transmission channels. An important factor in designing a distributed-load, high-performance PCB is a basic understanding of the design practices used to ensure good signal integrity.

This document uses the following sections to understand the PCB high-speed design challenges you may be facing:

- Section 1.1 lists the signal integrity theory and terminology.
- Section 2 covers general PCB high-speed design considerations: Design the right PCB stack up for the high-speed board, reduce Pad capacitance, minimize via reflection, and reduce power noise.
- Section 3 provides LPDDR4 layout guidelines and LPDDR4 interface trace routing examples.
- Section 4 provides SERDES Layout Guideline and SERDES trace routing example and simulation results.

1.1. Signal Integrity Theory and Terminology

In the communication system, data is exchanged between high-speed IO banks (output buffer to input buffer) or SERDES Interfaces (transmitter to receiver). The transmission line ensures that the output power is transmitted to the receiver at maximum power.

1.1.1. Impedance Formula of the Transmission Line

The maximum power transfer theorem published by Moritz von Jacobi states that to obtain maximum external power from a power source with internal resistance, the resistance of the load must equal the resistance of the sources. The following figure shows the simulation of the Maximum power transfer theorem. The Source resistance is 50 Ω. The load resistance is changed from 10 Ω to 100 Ω. The output power is peak at RL= RS = 50 Ω.

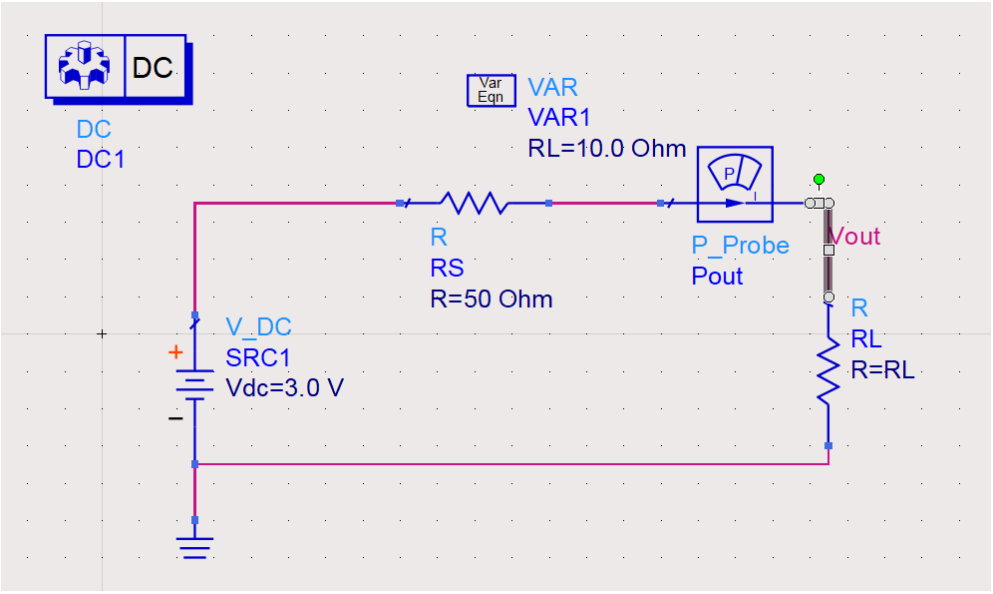


Figure 1.1. Simulation of the Maximum Power Transfer Theorem

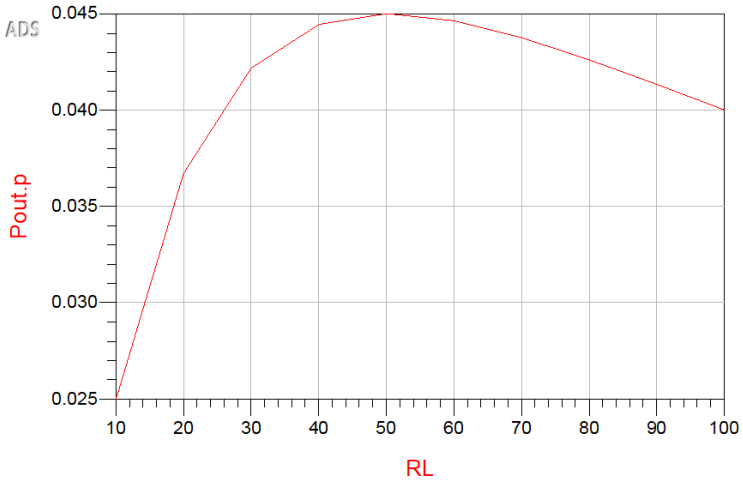


Figure 1.2. Simulation of the Maximum Power Transfer Theorem – Graph

Based on the above theory, the characteristic impedance (Z0) of the PCB transmission channel should match the output impedance for maximum output power. The telegrapher's equations are the general expression for the characteristic impedance of a transmission line:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Where:

R is the resistance per unit length.

L is the inductance per unit length

G is the conductance of the dielectric per unit length.

C is the capacitance per unit length.

j is the imaginary unit

ω is the angular frequency

1.1.2. PCB Microstrip/Stripline Trace Impedance Calculation

A PCB transmission line is a form of interconnection that connects buffer outputs to the input buffers on a printed circuit board. A PCB transmission line consists of two copper traces: a signal trace and a return path (ground plane). There are two types of PCB transmission lines: microstrip and stripline traces.

Calculating the characteristic impedance of a printed circuit board trace is a sophisticated, error-prone process that requires complex calculations and approximations. Nomographs and simplified formulas have been developed to make the design process easier; however, they are often inaccurate.

The samples below are taken from online resources.

- Wheeler's Equation is one of the impedance formulas used to calculate the approximate microstrip impedance:

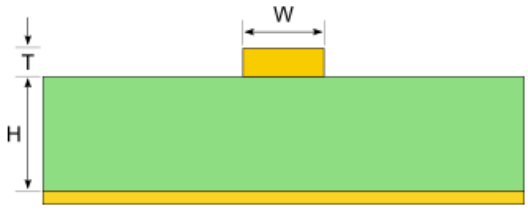


Figure 1.3. Illustration to calculate approximate microstrip impedance

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{2}\sqrt{E_r+1}} \cdot \ln\left(1 + 4 \cdot \left(\frac{h}{w_{eff}}\right) \cdot (X_1 + X_2)\right)$$

Where

$$W_{eff} = W + \left(\frac{t}{\pi}\right) \cdot ln\left\{\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left(\frac{t}{w\pi + 1.1t\pi}\right)^2}}\right\} \cdot \frac{E_r + 1}{2 \cdot E_r}$$

$$X_1 = 4\left(\frac{14E_r + 8}{11E_r}\right)\left(\frac{h}{W_{eff}}\right)$$

$$X_2 = \sqrt{16 \cdot \left(\frac{h}{W_{eff}}\right)^2 \cdot \left(\frac{14 \cdot E_r + 8}{11 \cdot E_r}\right)^2 + \left(\frac{E_r + 1}{2 \cdot E_r}\right) \cdot \pi^2}$$

Where:

W = width of the copper trace

T = Trace Thickness

H = Substrate Height

Er = Substrate Dielectric

- Formulas in IPC-2141A are one of the impedance formulas to calculate symmetric stripline impedance:

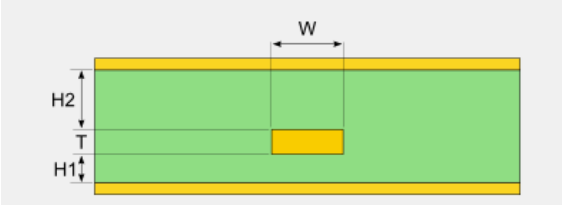


Figure 1.4. Illustration to calculate symmetric stripline impedance

For the narrow signal conductor, that is for w/b < 0.35, the appropriate formula for the characteristic impedance, $Z_{0,SS}$ is:

$$Z_{0,ss,t-2} = \frac{60}{\sqrt{\varepsilon_r}} ln\left(\frac{4b}{\pi D}\right)$$

Where:

b = 2h + t

and:

$$D = \frac{w}{2}\left\{1 + \frac{t}{\pi w}\left[1 + \ln\left(\frac{4\pi w}{t}\right)\right] + 0.551\left(\frac{t}{w}\right)^2\right\}$$

For the wide signal conductor, which is for w/b ≥ 0.35, the appropriate formula for the characteristic impedance, $Z_{0,SS}$ is:

$$Z_{0,ss,w-2} = \frac{94.15}{\left(\frac{w/b}{1-t/b} + \frac{\theta}{\pi}\right)}$$

where:

$$\theta = \left(\frac{2b}{b-1}\right) ln\left(\frac{2b-1}{b-1}\right) - \left(\frac{t}{b-1}\right) ln\left[\frac{2bt-t^2}{(b-t)^2}\right]$$

where:

W = width of the copper trace

T = Trace Thickness

H1, **H2** = Substrate Height

Er = Substrate Dielectric

The most accurate method available is using field solver programs, which solve Maxwell's equations directly over the volume of PCB under consideration using finite elements. The following is an impedance calculation example by the Hyperlynx SI/PI program.

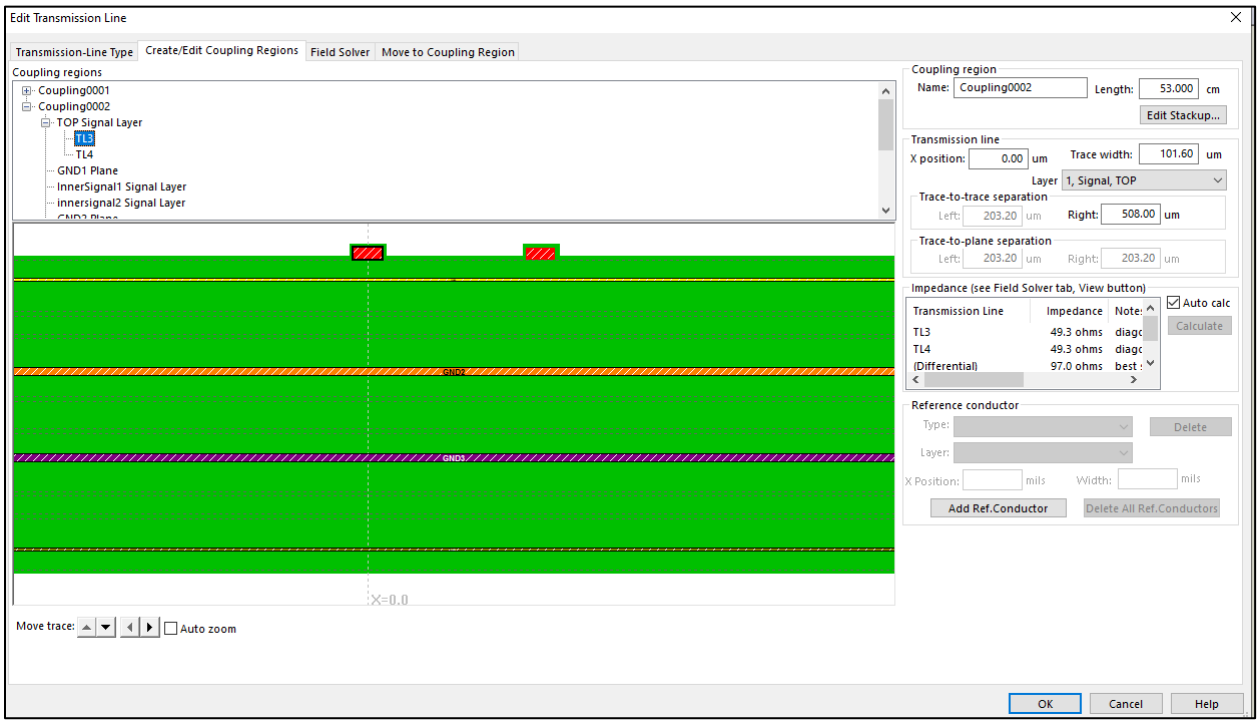


Figure 1.5. Hyperlynx Impedence Calculation Example

The typical impedance of a single-end trace is 50 Ω. The typical impedance of a differential signal interface is 100 Ω. The following table lists impedances defined in the protocol specification.

Table 1.1. Impedance Defined in the Protocol Specification

Protocol name	Differential Impedance Target (Ω)	Single End Impedance Target (Ω)	Typical Target Impedance (Ω)
PCIE Gen2 5.0GT/s	68 to 105	—	100
PCIE Gen3 8.0GT/s	70 to 100	—	85
PCIE Gen4 16.0GT/s	72.5 to 97.5	—	85
PCIE Gen5 32.0GT/s	72.5 to 97.5	—	85
IEEE 802.3-2022 Ethernet	85 to 100	—	90
HDMI	95 ± 15%	—	95
SDI	—	75	75
DP	95 ± 15%	—	95

1.1.3. S-Parameters for Characterizing the Transmission Line

Reflection coefficient (return loss), forward/reverse transmission coefficient (insertion loss), and S-parameters are used to characterize the transmission line.

The reflection coefficient (Γ) is defined to compute how much of a wave is reflected by an impedance discontinuity in the transmission line.

Its equation is:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

where:

Z_L = load impedance

Z_0 = characteristic impedance

The forward/reverse transmission coefficient (S_{21}/S_{12}) is defined to calculate the gain of the transmission line.

The general S-parameters of a two-port model of a transmission line can be written as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

- **S_{11}** gives the input refection coefficient (Return Loss of port 1).
- **S_{12}** is the reverse transmission coefficient (from port two to port one) (insertion loss from port 2 to port 1).
- **S_{21}** is the forward transmission coefficient (from port one to port two) (insertion loss from port 1 to port 2).
- **S_{22}** is the output reflection coefficient (return loss) (return loss of port 2).
- The source waves in ports one and two are given by a_1 and a_2.
- The reflected waves in ports one and two are given by b_1 and b_2.

1.1.4. PCB Long Transmission Line

The PCB trace needs to be treated as a transmission line if the length of the trace is longer than 1/10 of the signal wavelength. A PCB transmission line is considered a *long* transmission line if its length is longer than 1/4 of the single wavelength. A PCB *long* transmission line needs to be considered in signal integrity simulation because its impedance affects the signal integrity. A *long* transmission needs to be characterized by the VNA (Vector Network Analyzer) or modeled by 3-D simulation tools (Cadence Clarity, Ansys HFSS, ADS, Hyperlynx, etc.). The full channel simulation model can be built after cascading all components' S-parameters. The goal of high-speed design is to build the full channel model, calculate its total loss, and predict the design margin at the receiver.

2. General High-Speed PCB Channel Design Considerations

The PCB *long* transmission line performance may be affected by component fanout, PCB material dielectric loss and skin effect, copper roughness, trace width, transmission line types, ground reference, and power noise. This section covers the design challenges considered to build a high-speed PCB board.

2.1. Design the Right PCB Stack-up for a High-Speed Board

Use the following general recommendations to design the right PCB stack up for a high-speed board:

- The document PCB Layout Recommendations for BGA Packages (FPGA-TN-02024) by Lattice Semiconductor covers the minimum PCB stack-up requirements for BGA fanout. Use it as a reference to calculate the layer number in the new PCB stack-up.
- Select the right PCB material based on the cost target and transmission line loss budget.
- Define trace impedance and calculate trace width and layer thickness.
- Build the full-channel simulation model and check whether the total insertion loss exceeds the design target.
- Calculate the space between transmission channels to meet the NEXT and FEXT crosstalk targets.
- Follow Section 2.4 to define power and ground layers for all power rails.
- Build the stack-up table.
- PCB panel rotation may be required to keep the same electrical properties under the transmission line.

To design the right high-speed PCB stack-up, the following factors need to be considered:

- PCB Material
- Etch Length
- Trace width
- Microstrip vs. Stripline
- Copper roughness(>10GHz)
- BGA fanout

2.1.1. PCB Material

PCB material and etch length affect the channel insertion loss because of dielectric loss and skin effects. The following table lists popular PCB materials used in the communication system:

Table 2.1. Popular PCB Material Used in the Communications System

Vendor	Material	Er	Tangent	Cost	3db Bandwidth	Loss @12 GHz (dB/inch)
Isola group	370HR	4.04	0.021	Low	Up to 1.5 GHz	–1.33
Isola group	FR408	3.67	0.012	Low	Up to 2.5 GHz	–0.83
Panasonic	Megtron2	4.1	0.01	Low	Up to 2.5 GHz	–0.79
TUC	TU872	3.5	0.01	Low	Up to 2.7 GHz	–0.75
Isola group	FR408HR	3.68	0.0092	Medium	Up to 3 GHz	–0.7
Park aerospace Corp	Nelco N4000-13	3.7	0.009	Medium	Up to 3 GHz	–0.7
Panasonic	Megtron4	3.8	0.005	Medium	Up to 3.8 GHz	–0.55
TUC	TU883	3.5	0.0046	high	Up to 4 GHz	–0.51
Rogers	Rogers4350B	3.48	0.0037	high	Up to 4.2 GHz	–0.48
Isola group	Tachyon100G	3.02	0.0021	high	Up to 5 GHz	–0.41
Panasonic	Megtron6(R5775N)	3.4	0.002	high	Up to 5.5 GHz	–0.41
Panasonic	Megtron7(R5785N)	3.4	0.001	high	Up to 7 GHz	–0.33

12-inch, 5-mil microstrip lines are used to compare the insertion loss of the above materials.

The following simulation results illustrate PCB material insertion loss. At 12 GHz, the 12-inch insertion loss of the 370HR is about -16 dB, and the insertion loss of the Megtron 7 is about -4 dB. For high-frequency applications, the dielectric loss of the material has a significant impact.

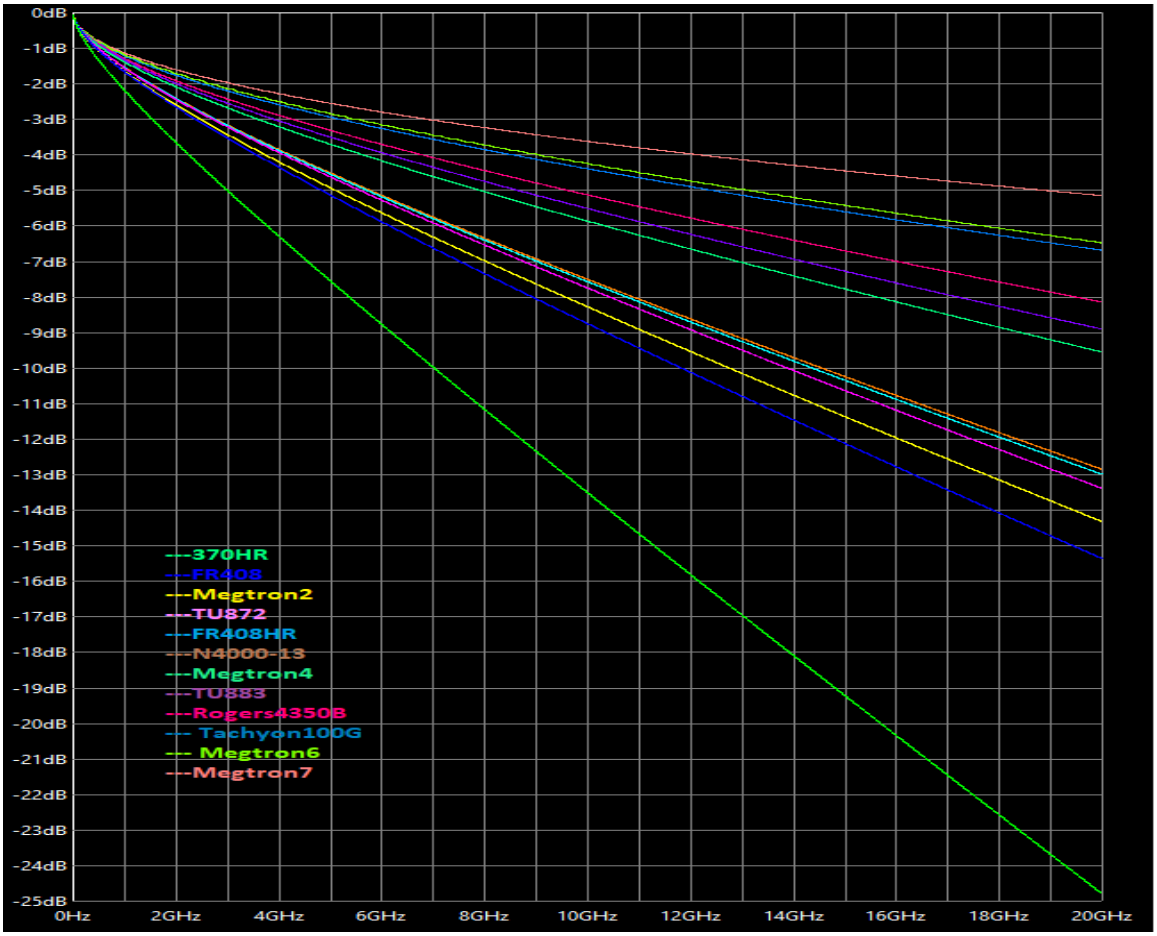


Figure 2.1. 12-inch Insertion Loss Comparison for PCB Materials

2.1.2. Trace Width

A wider trace generally reduces the channel loss. The following figure illustrates 12-inch 10-mil microstrip trace insertion loss (RED) vs. 12-inch 5-mil microstrip trace insertion loss (Green). At 12 GHz, the insertion loss of 10 mil trace is about -2.75 dB, and the insertion loss of 5 mil trace is about -4 dB. The proper PCB stack-up has to balance trace loss with routing density; a wider trace means more routing space is needed. Optimize to get the best tradeoff between loss and routing density.

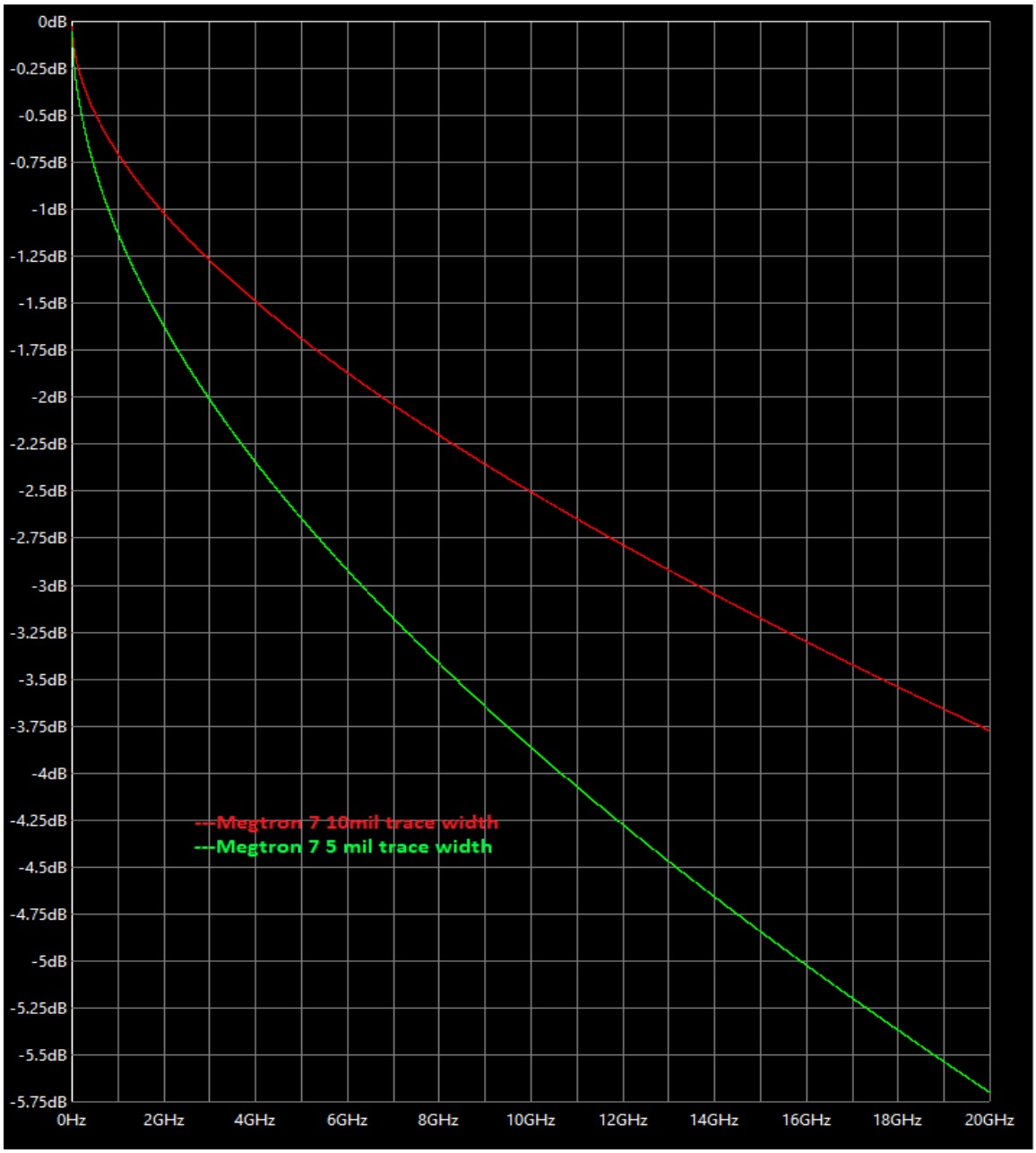


Figure 2.2. 12-inch Insertion Loss Comparison: 10-mil Trace vs. 5-mil Trace Width

2.1.3. Microstrip vs. Stripline

A microstrip line with trace on the surface without a solder mask has less loss per inch compared to a stripline with similar dimensions and material, as the microstrip is surrounded by non-uniform dielectrics that are partially air with no dielectric loss. The following illustrates 12-inch, 5-mil Megtron 7 stripline trace insertion loss (green) and 12-inch, 5-mil Megtron 7 microstrip trace (yellow). At 12 GHz, the insertion loss of the 5-mil stripline trace is about -5.3 dB, and the insertion loss of the 5-mil microstrip trace is about -4.2 dB. However, solder mask coating on top of the microstrip, widely used in production PCBs, significantly increases the loss, especially for the low-loss material, because solder mask coating has a high tangent loss.

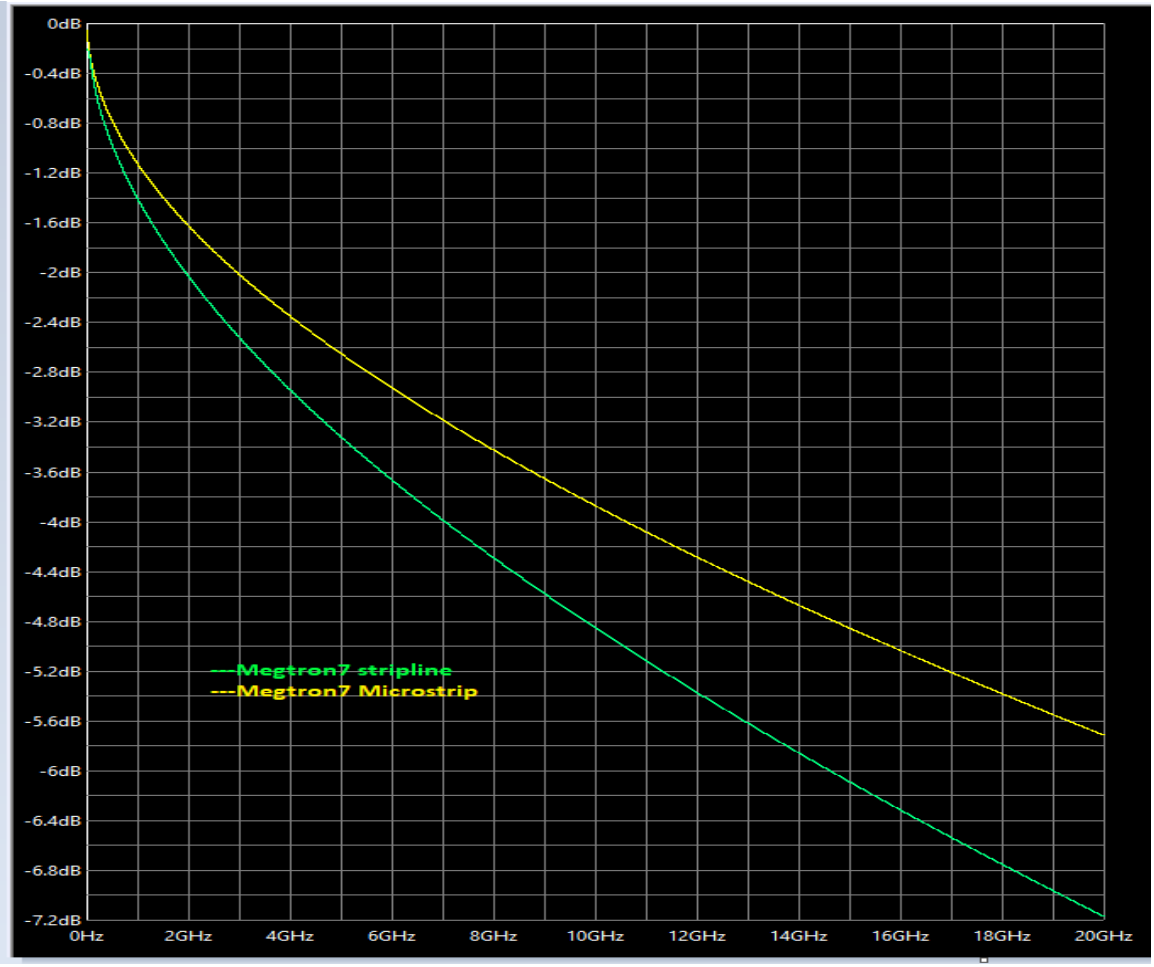


Figure 2.3. 12-inch Insertion Loss of a 5-mil Stripline Trace and 5-mil Microstrip Trace

2.1.4. Copper Foil and Surface Roughness

Reverse Treat Foil (RTF), the most common finish, Very Low Profile (VLP), and Ultra Low Profile (HVLP) copper foils can affect channel loss. The following figure illustrates the insertion loss with HVLP and RTF foils. An increased copper surface can significantly affect loss per inch. This is because the additional skin-effect loss due to the increased copper surface can negate the benefit of low-loss material and significantly affect the loss per inch. Copper roughness must be considered and verified with PCB vendors to get accurate estimates of trace loss.

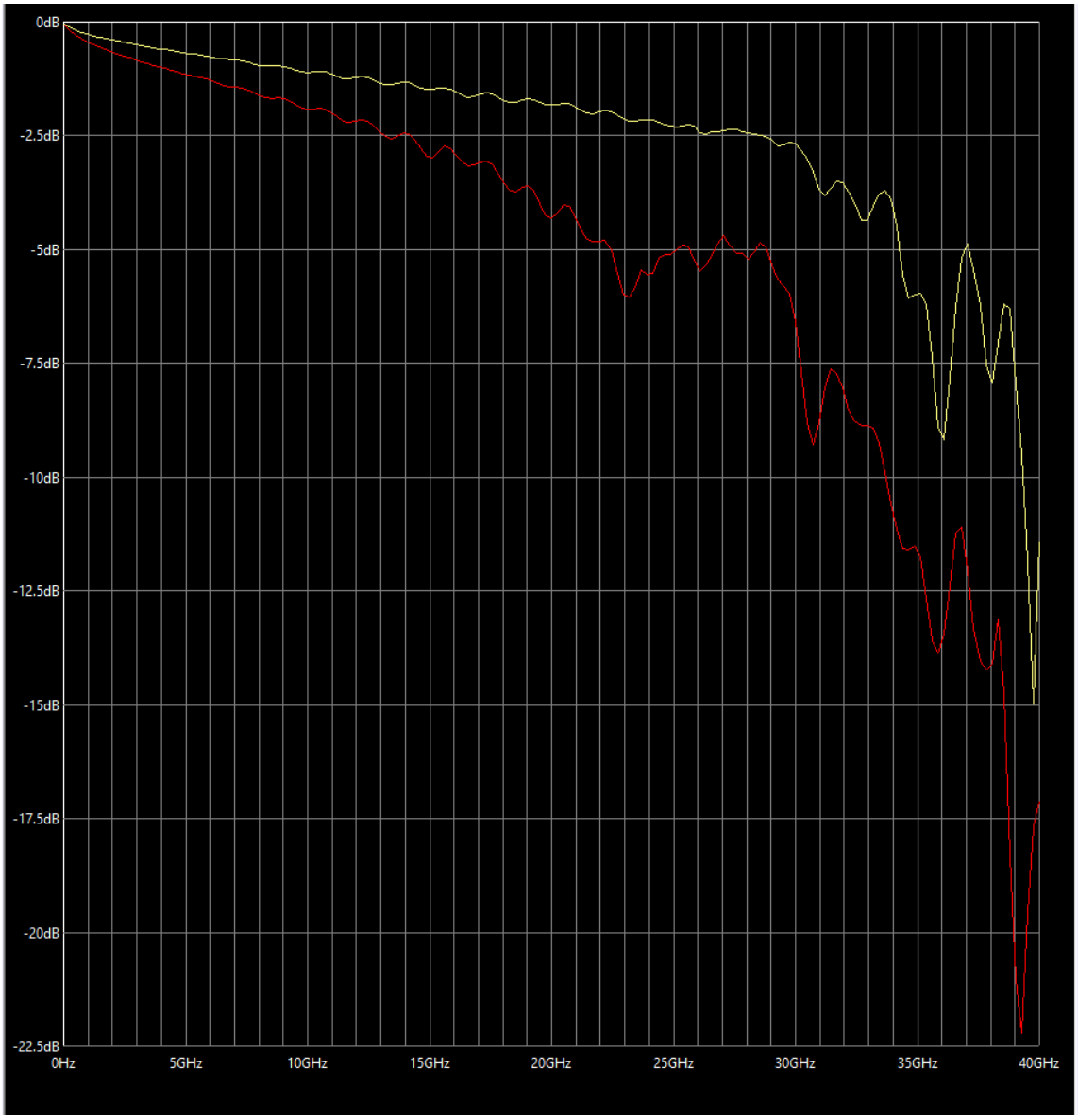


Figure 2.4. Insertion Loss of a VLP Copper Foil (Yellow) and an RTF (Red) Copper Foil

2.2. High-Speed Stack-up Example

The multiple metal layers facilitate high connection density, minimum crosstalk, and good Electromagnetic Compatibility (EMC). These factors are key to achieving good signal integrity for all the signal interconnections. Ideally, all signal layers should be separated from each other by ground or power planes (metal layers). This minimizes crosstalk and provides homogeneous transmission lines with properly controlled characteristic impedance between devices and other board components. This section covers the Avant Versa board stack-up design.

Avant-versa board, a PCIE Gen4x8 full-size form factor board, is a development reference board, and one of the design goals is to minimize trace insertion loss. To achieve this goal, Megtron 7 material is selected in the Avant-Versa stack-up because it has the lowest loss tangent. To fan out the differential traces between BGA balls, an 8-mil via-in pad is used in the BGA area. The anti-pad size of 8 mil via is 25 mil. The differential signal width includes two trace widths, and the space between traces needs to be less than 14 mil. The following pictures indicate the microstrip and stripe line fanouts used in the Avant Versa stack-up.

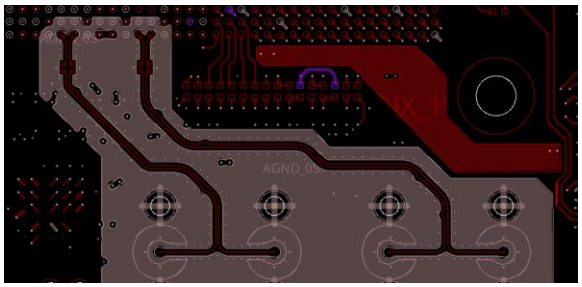
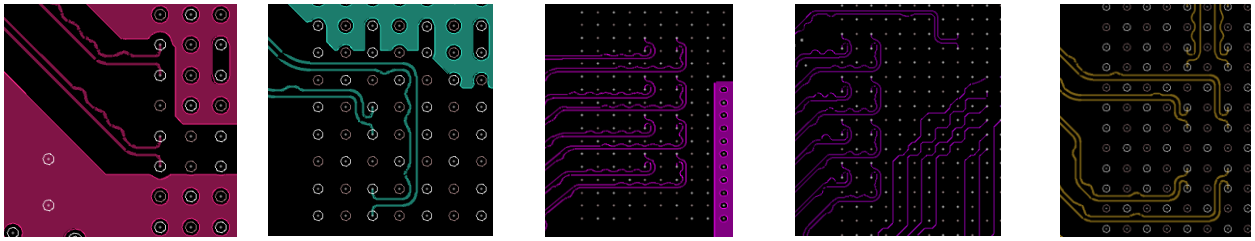


Figure 2.5. Microstrip Fanout—Top Layer



L3 Layer L7 Layer L10 Layer L12 Layer L14 layer

Figure 2.6. 1 mm BGA Format Fanout Used in the Avant Versa Stack-up—Stripline Fanout

The space between high-speed channels is more than six times the PCB dielectric height to avoid crosstalk between channels. A 0.5-ounce HVLP copper foil is selected for signal layers, and two 1-ounce copper foils are used at the L8 and L9 layers to support high-power core current. The hole vias are used to fan out high-speed channels. To avoid stub reflection, the stub is removed by the back drilling, as shown in Figure 2.7.

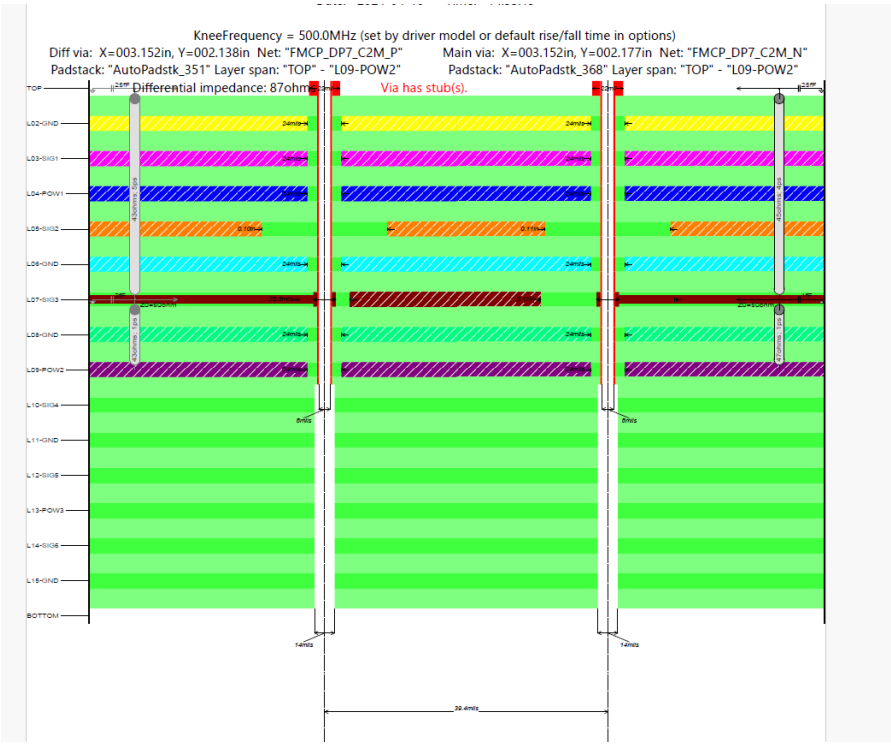


Figure 2.7. Example of the Via Back Drilling

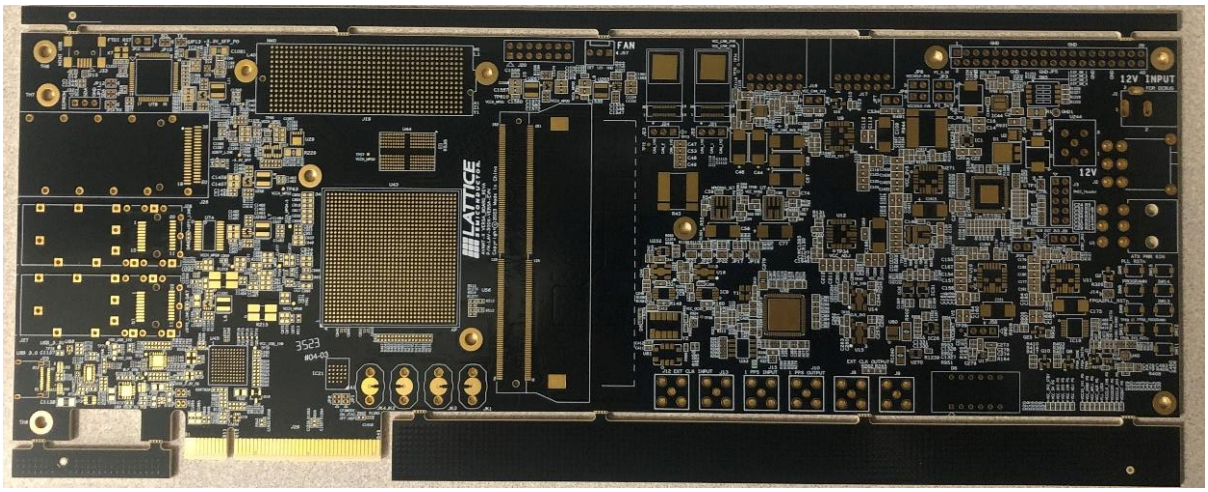


Figure 2.8. Avant Versa PCB Board

The PCIE form factor requires a board thickness of 62 mils ± 5 mils. The thickness of the Avant Versa board stack-up is 58.84 mil. Table 2.2 shows the Avant Versa board, 16-layer stack-up.

Table 2.2. 16-Layer PCIE Form Factor Stack-up

Layer	Material	Thickness (mil)	Er	Tangent
L1(TOP)	Top Mask	0.75	3.2	0.02
	0.5oz+Plating	1.38	—	—
	Prepreg R-5680GN 1080	3.21	3	0.001
L2	0.5oz	0.6	—	—
	Core R-5785GN	3.9	2.75	0.001
L3	0.5oz	0.6	—	—
	Prepreg R-5680GN 1080	2.858	3	0.001
L4	0.5oz	0.6	—	—
	Core R-5785GN	3.9	2.75	0.001
L5	0.5oz	0.6	—	—
	Prepreg R-5680GN 1080	2.896	3	0.001
L6	0.5oz	0.6	—	—
	Core R-5785GN	3.9	2.75	0.001
L7	0.5oz	0.6	—	—
	Prepreg R-5680GN 1080	2.66	3	0.001
L8	1oz	1.2	—	—
	Core R-5785GN	2	2.75	0.001
L9	1oz	1.2	—	—
	Prepreg R-5680GN 1080	2.624	3	0.001
L10	0.5oz	—	—	—
	Core R-5785GN	3.9	2.75	0.001
L11	0.5oz	—	—	—
	Prepreg R-5680GN 1080	2.854	3	0.001

Layer	Material	Thickness (mil)	Er	Tangent
L12	0.5oz	—	—	—
	Core R-5785GN	3.9	2.75	0.001
L13	0.5oz	—	—	—
	Prepreg R-5680GN 1080	2.868	3	0.001
L14	0.5oz	—	—	—
	Core R-5785GN	3.9	2.75	0.001
L15	0.5oz	—	—	—
	Prepreg R-5680GN 1080	3.21	3	0.001
L16(bottom)	0.5oz + plating	1.38	—	—
	Bottom Mask	0.75	3.2	0.02
	Total	58.84	—	—

Based on the simulation, trace impedance targets for each layer are defined in Table 2.3

Table 2.3. 16-Layer Stack-up Trace Impedance Table

Single Layer	Reference Plane	Impedance Type	Impedance Target (Ω)	Trace Width (mil) / Space (mil)
L1	L2	SE	50 ±7%	6.6
L1	L2	SE	40 ±7%	9.8
L1	L2	DE	100 ±7%	4.9/5.2
L1	L2	DE	85 ±7%	6.7/4.8
L1	L2	DE	75 ±7%	8.2/4.1
L1	L2	DE	90 ±7%	6/4.9
L3	L2/L4	SE	50 ±5%	3.89
L3	L2/L4	DE	95 ±5%	4/5.5
L5	L4/L6	SE	50 ±5%	3.89
L5	L4/L6	DE	100 ±5%	3.72/6.48
L7	L6/L8	SE	40 ±7%	5.42
L7	L6/L8	SE	50 ±7%	3.68
L7	L6/L8	DE	75 ±5%	5.48/3.82
L7	L6/L8	DE	95 ±5%	3.83/5.67
L7	L6/L8	DE	100 ±5%	3.55/6.65
L10	L9/L11	SE	40 ±5%	5.4
L10	L9/L11	SE	50 ±5%	3.65
L10	L9/L11	DE	85 ±5%	4.65/5.65
L10	L9/L11	DE	75 ±5%	5.44/3.86
L10	L9/L11	DE	100 ±5%	3.52/6.68
L12	L11/L13	SE	40 ±5%	5.67
L12	L11/L13	SE	50 ±5%	3.85
L12	L11/L13	DE	85 ±5%	4.86/5.44
L12	L11/L13	DE	90 ±5%	4.4/5.5
L12	L11/L13	DE	100+/-5%	3.7/6.5
L14	L13/L15	SE	40 ±5%	5.7
L14	L13/L15	SE	50 ±5%	3.87
L14	L13/L15	DE	60 ±5%	8.2/3.85
L14	L13/L15	DE	75 ±5%	5.66/3.64
L14	L13/L15	DE	95 ±5%	4/5.5

Single Layer	Reference Plane	Impedance Type	Impedance Target (Ω)	Trace Width (mil) / Space (mil)
L14	L13/L15	DE	100 ±5%	3.7/6.5
L16	L15	SE	50 ±7%	6.6
L16	L15	DE	85 ±7%	6.74/4.76
L16	L15	DE	90 ±7%	6/4.9
L16	L15	DE	100 ±7%	4.9/5.2

2.3. Design a Proper Transmission Line

To design a good transmission line, the following factors need to be considered:

- Pad capacitance
- Via reflection
- Via impedance
- Via crosstalk
- Via-in-pad vs. Dogbone

2.3.1. Reduce Pad Capacitance

Pad-to-ground distance needs to be considered in high-speed PCB design. The following examples illustrate the ground cutout under pads of passive components.

0201 Capacitor ZSFP ZQSFP

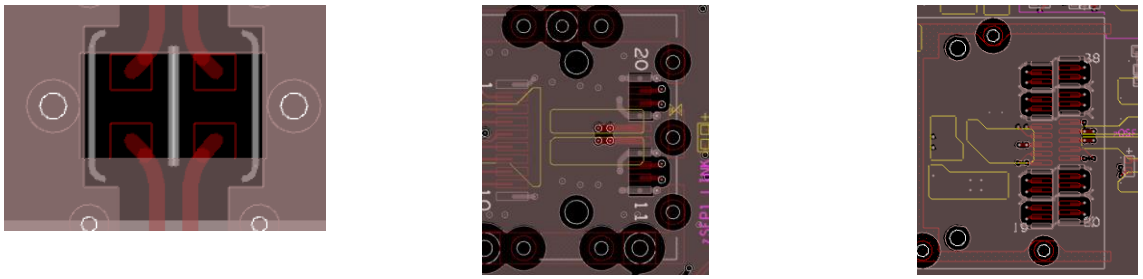


Figure 2.9. PCIE Edge-Fingers copied Figure 77 in PCIE CEM 4.0

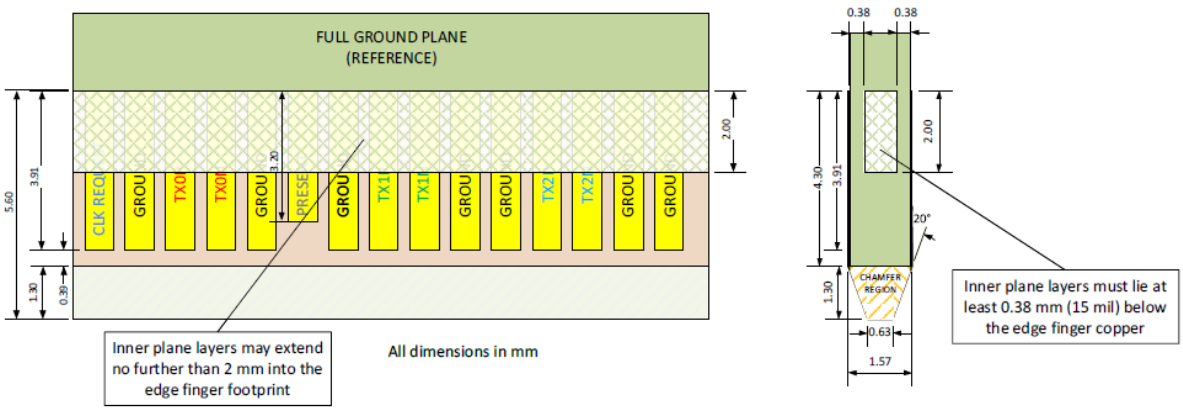


Figure 2.10 Ground Cut Area Under Pads of Passive Components

Capacitance can be generated between two metal plates. The formula for capacitance between two parallel plates is: $C = K \times E_0 \times (A/D)$, where $E_0 = 9.854 \times 10^{-12}$.

where:

K = dielectric constant of the material.

A = overlapping surface area of the plates in m2.

D = distance between the plates in m.

C = capacitance.

To understand the effectiveness of 20-mil pad capacitance, two simulation cases are built:

- In Case 1, the pad-to-ground layer distance is 3.21 mil. Pad capacitance is about 0.07 pF.
- In Case 2, the pad-to-ground layer distance is 6.1 mil. Pad capacitance is about 0.04 pF.

The following figures illustrate the 3D simulation model of Case 1 and Case 2.

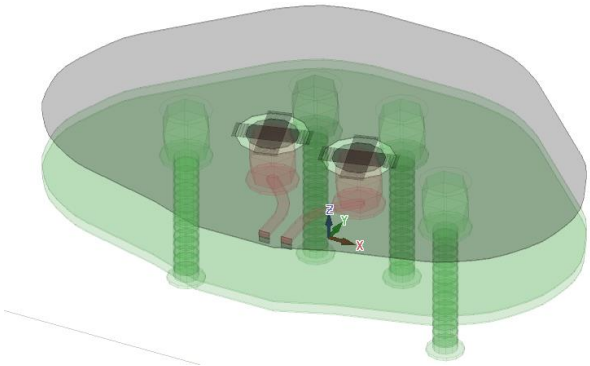


Figure 2.11 3D Simulation Model for Pad Insertion Loss and Return Loss (D = 3.21 mil)

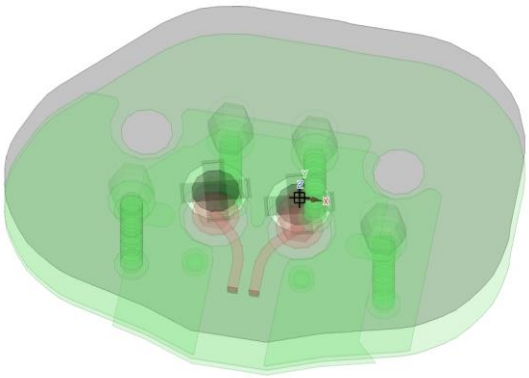


Figure 2.12 3D Simulation Model for Pad Insertion Loss and Return Loss (D = 6.1 mil)

The return loss figure and insertion loss figure are generated by the Hyperlynx full solver.

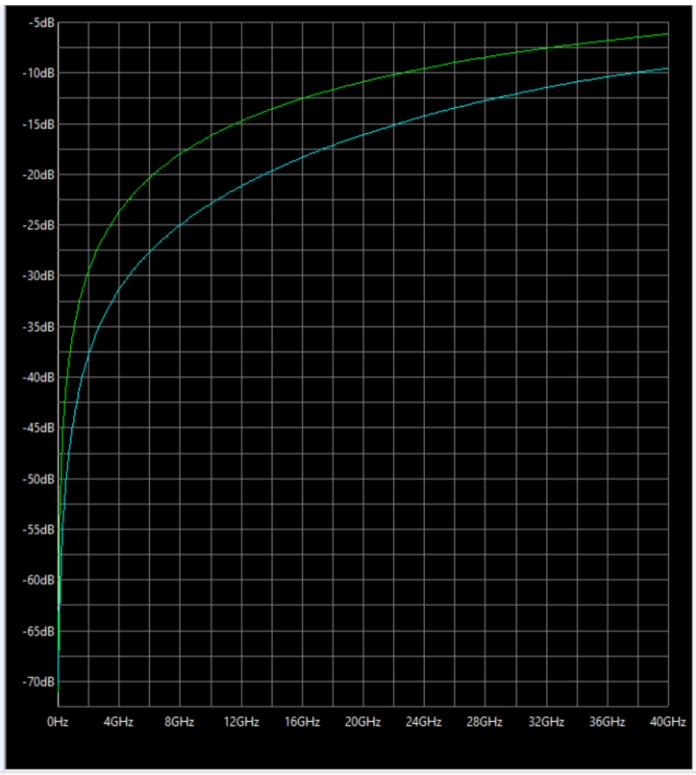


Figure 2.13 Return Loss of 20 mil Pad

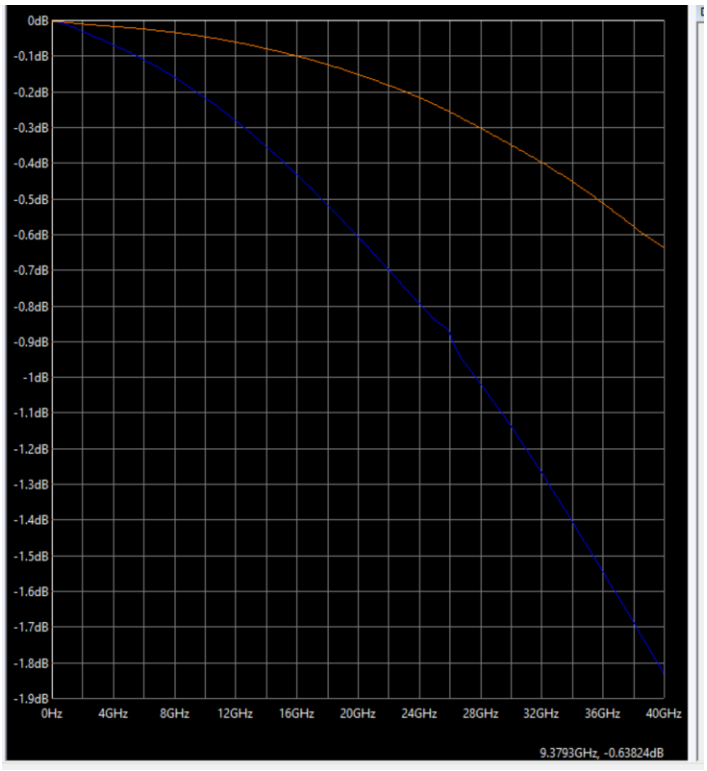


Figure 2.14 Insertion Loss of 20 mil Pad

At 12 GHz, the return loss of case 1 is -5 dB. The return loss in case 2 is -22 dB. The insertion loss of case 1 is -0.3 dB, and the insertion loss of case 2 is -0.05 dB.

Based on the simulation results, we can conclude that higher pad capacitance can result in higher return and insertion losses.

2.3.2. Minimize Via Reflection

A crucial factor for SERDES interconnect design is the discontinuity when a signal travels from the transmitter through packaging, via, connector and arrives at the receiver. Impedance discontinuity is typically caused by a change in trace impedance or a disruption in the return channel, such as when switching from trace to the via. A reflected pulse causes additional ISI (intersymbol interference) and eye closure, which cannot be compensated by the TX and RX equalization circuits. Reflection and return loss must be managed carefully for a link design to be successful.

Via is used to interconnect PCB layers. It is important to understand the via structure. Figure 2.15 illustrates the via structure used in the 0.5-mm-pitch BGA stack-up.

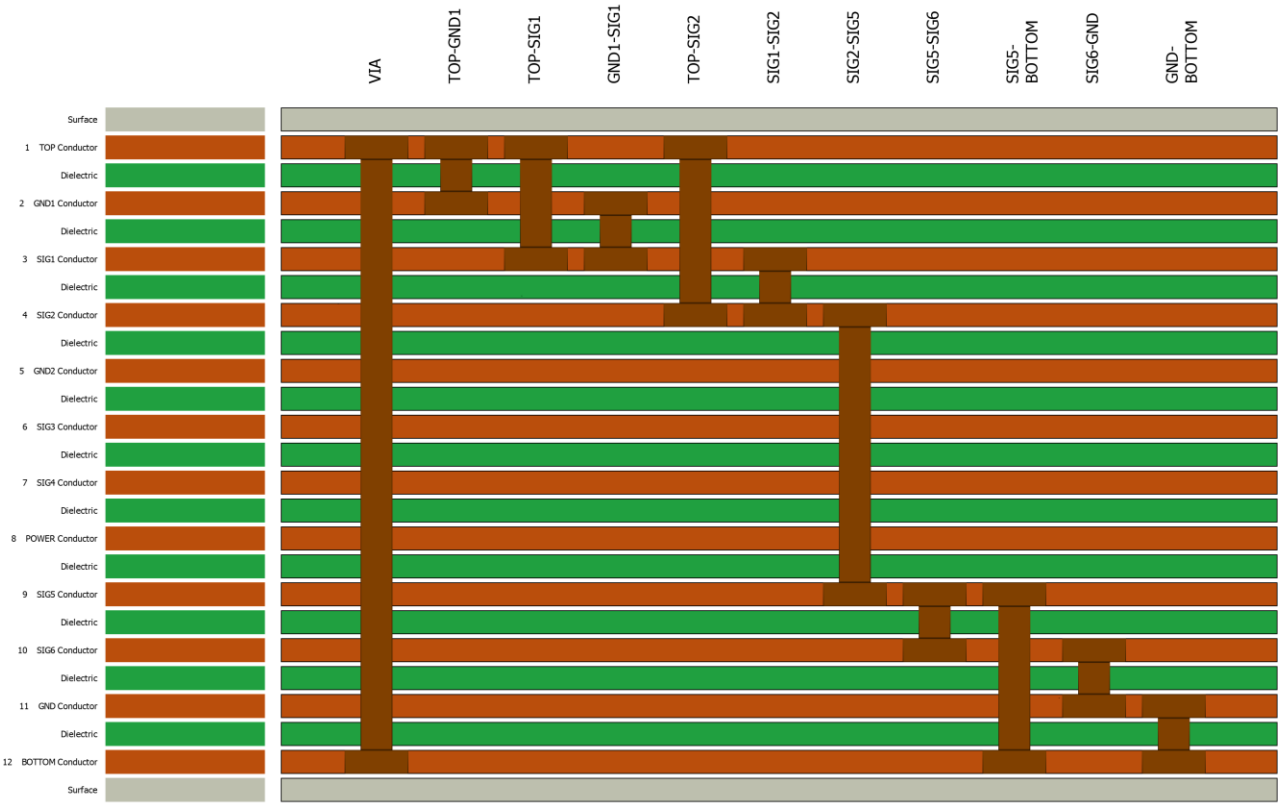


Figure 2.15 Types of PCB Vias

where:

Top-GND1: Micro via

TOP-SIG1: Stacked Micro via between top to layer 3

GND1-SIG1: Buried micro via

SIG2-SIG5: Buried through hole via

Via: Through hole via from Top to Bottom

Micro vias and buried micro vias do not have via stubs. Through-hole vias and buried through-hole vias have via stubs. Table 2.4 lists the cost of the above via structures.

Table 2.4. Performance and Cost of Via Structures

Via Type	Via Stub	Fill	High Speed Performance	Cost
Via in Pad	yes	Yes	10mil stub after back drilling	median
Micro Via	no	Copper fill	No stub	High
Stacked Micro via	no	Copper fill	No stub	High
Buried via	no	Epoxy fill	No stub	High
Through Hole Via	Yes	No	10 mil stubs after back drilling	low

2.3.2.1. Via Cutout

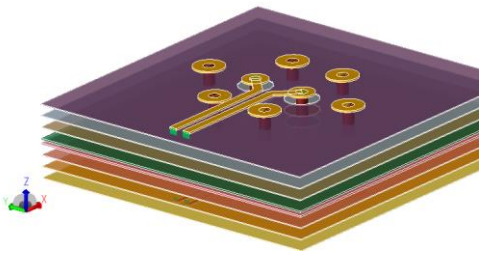
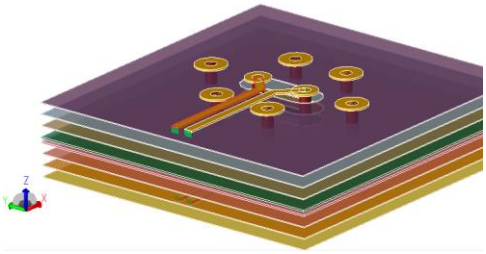
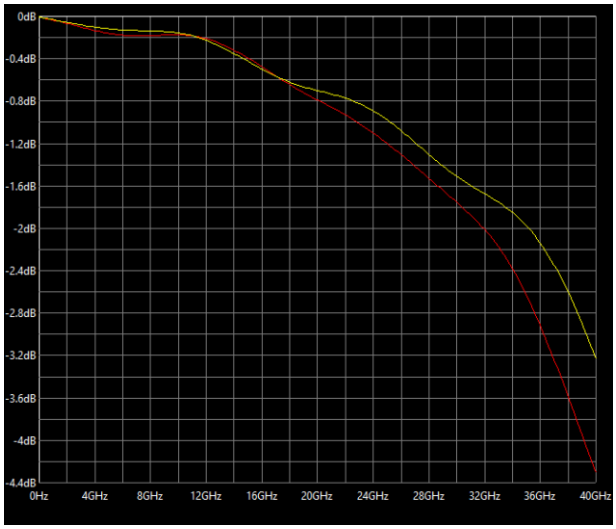
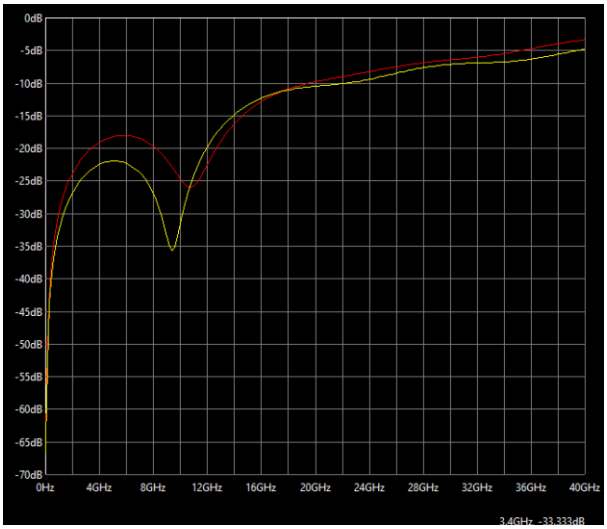
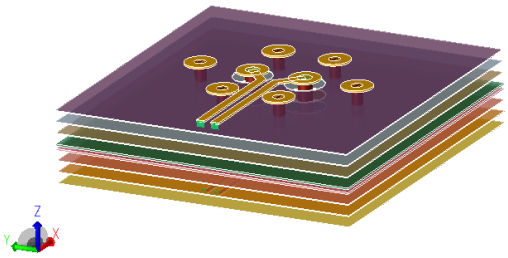
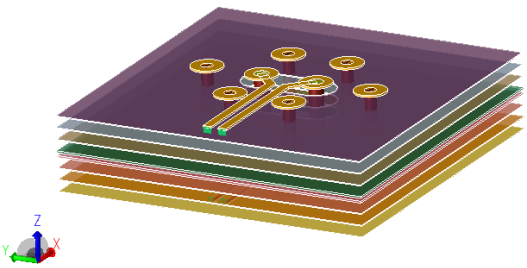
The via impedance is affected by the anti-pad shape. Cutout on the ground and power planes around signal vias (anti-pad) are other factors that can affect reflection. Capacitive coupling between the via pad, the barrel wall, and copper planes increases the capacitance and lowers the equivalent impedance of vias, which results in reflection. When the anti-pad diameter increases, both the capacitive coupling and reflection are reduced. Beyond a threshold of the anti-pad dimension, the benefit gradually decreases.

To understand the effectiveness of via cutout, 8mil and 10 mils vias are constructed in the ADS simulation platform:

- 8-mil Via dimension:
  - Pad size: 18 mil
  - Drill size: 8 mil
  - Anti-pad size: 25 mil
  - Trace feed layers: L1 and L15.
  - The stack-up is shown in Table 2.2. 16-Layer PCIE Form Factor Stack-up
- 10-mil Via dimension:
  - Pad size: 22 mil
  - Drill size: 10 mil
  - Anti-pad size: 28 mil
  - Trace feedback layers: L1 and L15.
  - The stack-up is shown in Table 2.2. 16-Layer PCIE Form Factor Stack-up

Table 2.5 compares the return and insertion loss results of the via with and without a cutout.

Table 2.5. Cutout Reduce the Via Capacitance and Improve the Performance

Via Without Cutout	Via With Cutout
8 mil Via-in Pad Without Cutout (Red line)	8 mil Via-in-Pad With Cutout (Yellow Line)
	
Insertion Loss	Return Loss
Merge Anti-Pad Improve Insertion Loss (Yellow Line)	Merge Anti-Pad Make Return Loss Better (Yellow Line)
	
10 mil Via-in Pad Without Cutout (Red)	10 mil Via-in-Pad With Cutout (Yellow)
	

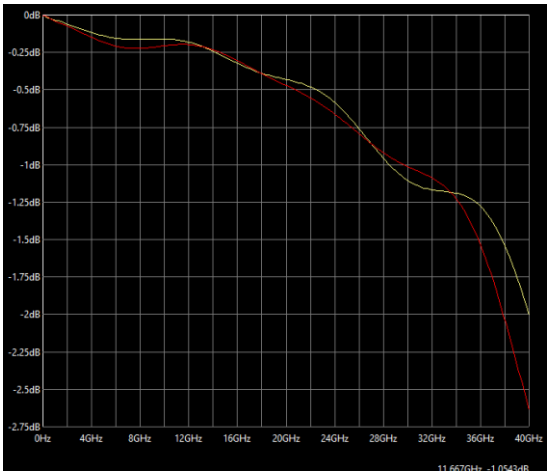
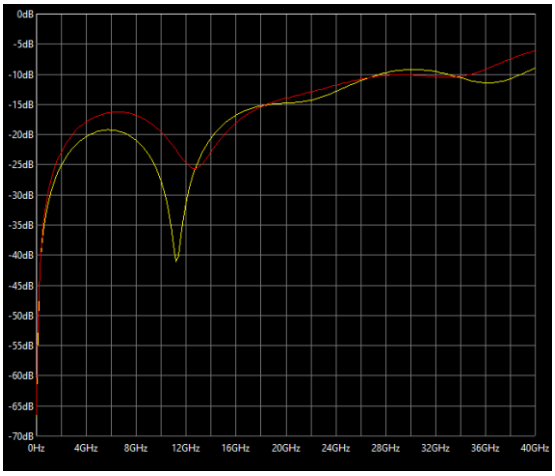
Via Without Cutout	Via With Cutout
Insertion Loss	Return Loss
Merge Anti-Pad Improve Insertion Loss (Yellow Line)	Merge Anti-Pad Make Return Loss Better (Yellow Line)
	

Table 2.5 shows that a merge anti-pad cutout around vias improves return loss by 10 dB. Anti-pad optimization is especially beneficial for long vias in thick PCBs or large vias (e.g., plated through-hole vias for backplane connector pins). Using a 3D full-wave electromagnetic field solver, it is advised to simulate and choose the proper anti-pad dimension considering the via discontinuity, reference plane continuity, and power integrity due to the Swiss cheese effect.

2.3.2.2. Via Stub

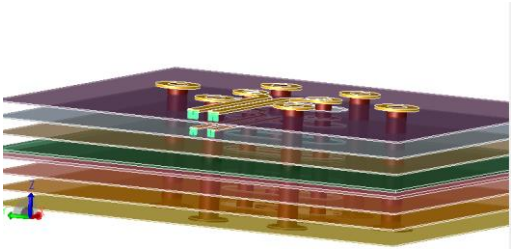
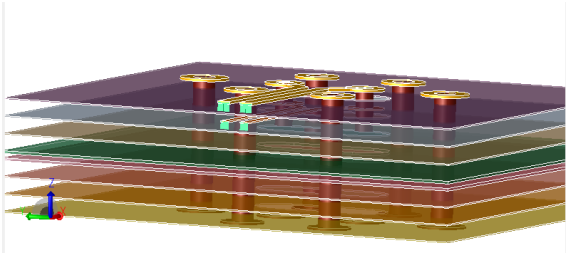
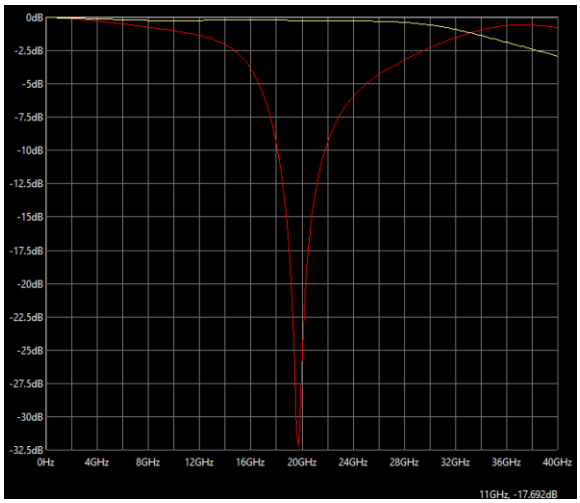
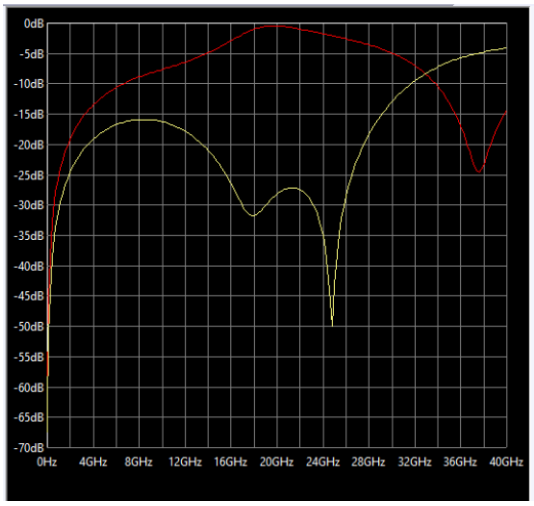
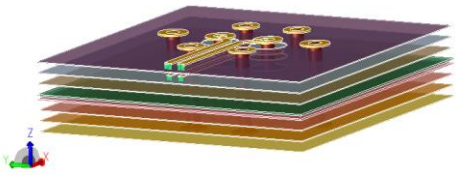
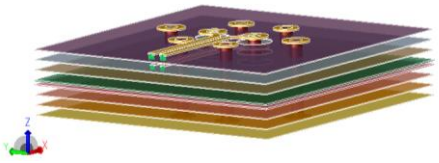
There are stubs in the through-hole-via. The long via stub caused significant reflection and resonance in the insertion loss resulting in a large dip. This resonance frequency is directly linked to the stub length, so the layer where the signal exits and total PCB thickness affect the resonance frequency. For a thick board, for example, a backplane, this resonance frequency shifts to the lower end and causes a worse degradation of insertion loss close to the fundamental frequency of the link and its harmonics.

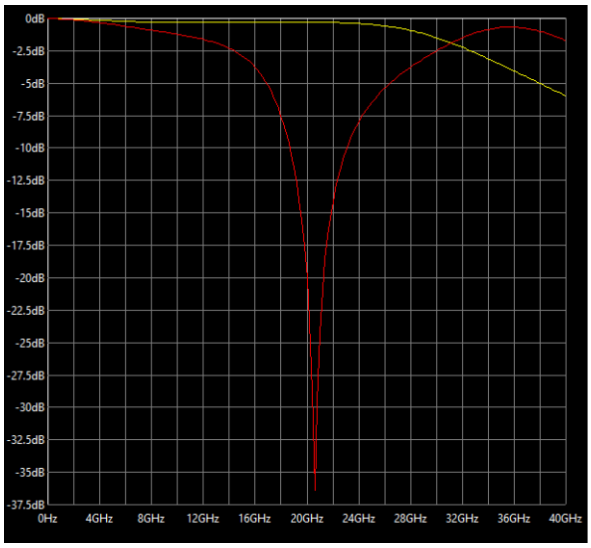
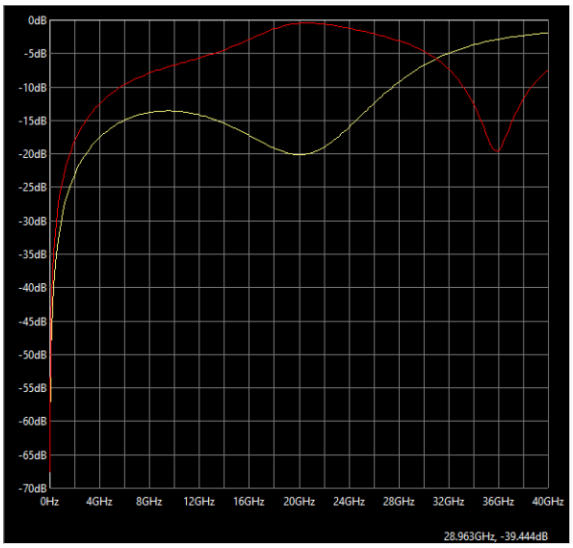
To understand the effectiveness of via stubs, 8 mil and 10 mil vias, (which are commonly used in 60 mil to 120 mil stack-up boards) are built in the ADS simulation platform.

- 8-mil Via dimension:
  - Pad size: 18 mil
  - Drill size: 8 mil
  - Anti-pad size: 25 mil
  - Trace feed layers: L1 and L3.
  - The stack-up is shown in Table 2.2. 16-Layer PCIE Form Factor Stack-up
- 10-mil Via dimension:
  - Pad size: 22 mil
  - Drill size: 10 mil
  - Anti-pad size: 28 mil
  - Trace feedback layers: L1 and L3.
  - The stack-up is shown in Table 2.2. 16-Layer PCIE Form Factor Stack-up

Table 2.6 compares the return and insertion loss results of the via with and without back drilling.

Table 2.6. Back Drilling Reduce the Stub Length and Improves the Transmission Line Performance

Via Without Back Drilling	Via With Back Drilling
8 mil via-in-pad without back drilling (Red line) 	8 mil via-in-pad with back drilling (Yellow line) 
Insertion loss	Return loss
The stub between layer 3 to bottom causes resonant dip at 18 GHz (Red). No resonance after back drilling 	The back drilling from bottom to layer 3 kills the resonant dip at 18 GHz (Yellow) 
10 mil via-in-pad without back drilling (Red Line) 	10 mil via-in-pad with back drilling (Yellow Line) 

Via Without Back Drilling	Via With Back Drilling
Insertion loss	Return loss
The stub between layer 3 to bottom causes resonant dip at 20 GHz (RED). No resonance after back drilling (Yellow)	The back drilling from bottom to layer 3 kills the resonant dip at 20 GHz (yellow)
	

2.3.2.3. Via Crosstalk

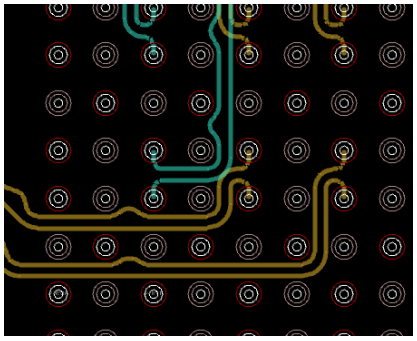
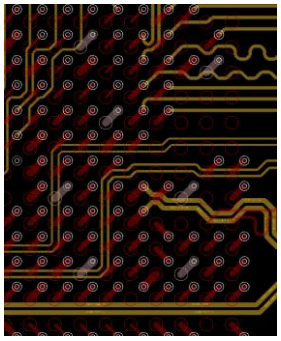
When a signal differential pair moves to another layer, the signal return channel becomes discontinuous, allowing for both near-end and far-end crosstalk during these vertical transitions. If not properly planned, these vertical transitions might result in considerable near-end or far-end crosstalk when compared to signal traces. Follow these guidelines while designing transitions:

- Maintain proper GND reference, for example, GND vias besides signal vias.
- Adequate isolation and spacing of the TX vias and the RX vias are critical to achieving low NEXT.
- Crosstalk is proportional to the length of vias, so shorter vias perform better.

2.3.3. Via-In-Pad BGA Breakout vs. Dogbone BGA Breakout

The controlled impedance trace between the BGA pad and the Dogbone pad is required. The Dogbone breakout is practically used when the BGA pitch is larger than 0.75 mm. The via-in-pad is popularly used to fan out signals if the BGA pitch is smaller than 0.75mm. The cost of the via-in-pad is higher than the Dogbone breakout because epoxy fills are required in the via-in-pad structure. Table 2.7 shows an example of a via-in-pad fanout and a Dogbone fanout.

Table 2.7. Example of Via-In-Pad Fanout and Dogbone Fanout

Via-In-Pad Fanout	Dogbone Fanout
	

2.4. Power Noise Reduction

Power noise directly affects the SNR (signal-to-noise ratio) of the high-speed channel. Proper power noise decoupling is required in the high-speed system design.

For decoupling considerations, use the general checklist below:

1. Follow the hardware checklist provided by Lattice Semiconductor.
2. Identify all high current sources and sinks and identify their return paths. For a load current of more than 10 A, Hyperlynx PDN simulation needs to be used to check IR drop before the PCB layout is released.
3. During layout, maximize the trace width to minimize inductance by mutual coupling. If possible, lay out power supply buses in a grid or a plane. Avoid long serial supply traces.
4. Utilize passive filter networks on analog supplies using series ferrite bead inductors and proper AC decoupling capacitors.
5. Bypass all high-current sources and sinks with capacitors that work well at the frequencies of interest. Ceramic capacitors are good for this application for those capacitors placed very close to the FPGA because they are inexpensive, small, and work well at high frequencies. Use distributed equivalent capacitors to reduce parasitic ESR and ESL. Use tantalum capacitors for counteracting localized power droop. These capacitors work well when placed near the FPGA to provide energy storage.
6. Choose the decoupling elements based on the required isolation and frequency response requirements. If using a simple series inductor, its value should be as small as possible. Avoid high-Q inductors. In this application, a low-Q is desirable.
7. The upper layers should be used for high-priority supplies. Placing high-transient current supplies vertically closer to the device decreases the distance the currents need to travel through vias. Ground planes should also be adjacent to high-transient current power planes to reduce inductance and couple the high-frequency noise.

2.4.1. Decoupling and Bypassing

Traditional methods for providing local power supply decoupling involve placing capacitors near the device in locations that are convenient based on the routing of the board and applying a predetermined ratio of caps to power supply pins. Rule of Thumb provides many cap values in different decades, like 0.1 µF, 0.01 µF, and 10 µF for each power rail, with the smaller two values at each power pin. Unfortunately, the higher switching speeds of complex FPGA designs may render such typical ratios less than useful. Today's high-speed designs produce fast edge rates and large output loads, leaving the decoupling Rule of Thumb guidelines less than optimal. Careful planning and analysis should be performed to ensure that sufficient decoupling is provided. Simulation with a power integrity solver like HyerLynx DC Drop is always a good idea to catch power plane issues and fix them in the PCB layout before you fabricate the PCB.

Among the FPGA device power pins are supplies that source power to the FPGA core, configuration logic, I/O buffers, phase-locked loops, and specialized SERDES power supplies. Depending on the design intent of the FPGA device, a designer must pay strict attention to the PCB power distribution. Understanding that any unintentional coupling between supplies from high-speed switching currents can cause very undesirable performance problems. The FPGA also provides many high-speed, ASIC-like I/O buffers. The interfaces that are used with these buffers are used in a variety of communication protocol bridges and memory interconnections. Some of the interfaces use terminating transmission lines. These terminations pose many concerns that need to be addressed in the power distribution scheme. They include low-impedance output termination voltages and quiet input voltage references. These also need correct decoupling to meet the performance expectations.

2.4.2. Capacitor Selection

Decoupling capacitors are generally chosen based on their individual capacitive properties. However, when capacitors are being selected for high-speed designs, the designer should carefully choose capacitors based on other parasitic characteristics such as inductance and resistance. Local decoupling capacitors should have low-effective series resistance (ESR) and low-equivalent series inductance (ESL) while having a large enough capacitance value to supply current to the IC during switching.

Every capacitor has a narrow frequency band where it is most effective as a decoupling capacitor. The frequency bands of some capacitors are wider than others. The effective frequency bandwidth of a capacitor is determined by the ESR

and (Q) quality factors. Tantalum capacitors generally have a very wide effective band, while the lower ESR of ceramic X7R and X5R chip capacitors typically has a very narrow effective band. The dielectric material and geometry of the capacitor also determine how well the capacitor can suppress switching noise. Mixing several types of capacitors contributes to the total decoupling effectiveness.

In a typical FPGA board design, the capacitor closest to the power supply supplies the lowest-frequency components of the load's varying current. The low-frequency energy is decoupled by large electrolytic capacitors and is traditionally governed by regulated voltage sources. These larger capacitors are employed as a method of low-frequency filtering and to prevent supply droop. The droop is typically due to sections of a design becoming active and covering the lag until the regulator can respond. These big capacitors are usually electrolytic and have a low-frequency response of DC to a couple hundred KHz. Therefore, the close proximity of the capacitor to the FPGA is not critical.

The middle capacitors supply mid-frequency energy with large ceramic or tantalum capacitors. The use of these capacitors, which generally have a very wide effective band, should be in close proximity to the FPGA. These capacitors typically have a response time adequate enough to counteract localized power droop caused by portions of the FPGA becoming active and changing the demand on the supply. Primarily because of their low ESR, ceramic capacitors are often regarded as superior at high frequencies to tantalum capacitors. However, for decoupling, you can use the tantalum capacitors ESR to dampen the resonances that result from interaction between the capacitors' ESLs and the PC board's various capacitances. The high ESR acts as a built-in damping resistor and makes the tantalum capacitor a good choice for decoupling.

As the number of decoupling paths increases, so does the number of voltage drops across them, and this can result in power bus transients along with the associated common mode emissions. This problem can be minimized with proper power plane design in the area of the ICs. The use of adjacent power and ground planes in adjacent layers of the PCB stack-up is capacitively coupled. This power and ground plane act as an effective high-frequency capacitor and, consequently, as an additional energy source that compensates for transient currents.

The number of current transients switching across the power bus increases in complex FPGA designs. These instantaneous current issues are typically associated with simultaneously switching outputs or SSO. Capacitors with very little intervening inductance supply the localized high-frequency energy and are needed to decouple noise from the switching currents of the power bus. The decoupling needed to prevent the instantaneous currents from attacking the device supplies is required to be placed directly by the FPGA. Many smaller caps used in parallel function as local energy storage for the device. Only a small amount of energy is stored in them, and they cannot provide DC power. However, the function of this localized energy storage is to respond very quickly to changing current demands, rather than large capacitors having more storage but poorer response.

2.4.3. Localized Decoupling Considerations

Localized passive filtering is recommended to provide the necessary isolation from high-frequency power supply noise. The filter networks are recommended on the analog and high-speed transceiver (SERDES) supplies. These filter networks should include a series ferrite bead, like Murata BLM41P or BLM18A EMIFIL inductors. The impedance seen by the load is important because a large output impedance causes the load noise current to be translated into a large noise voltage. Typically, the ferrite bead provides good isolation. This limits the energy between the source voltage and the device supply. However, this requires a large bypass capacitor in order to keep the output impedance at a reasonable level. The smallest inductance that gives the required isolation should be used. The filter network should be AC coupled to GND through an appropriate 10–22 µF capacitor.

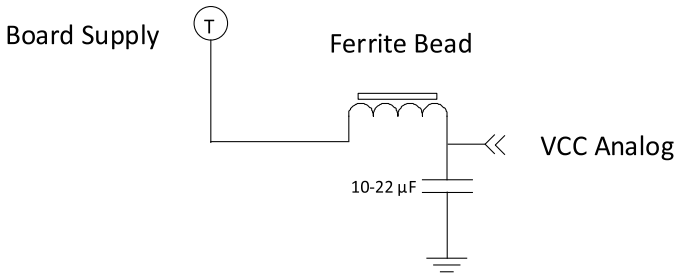


Figure 2.16 Passive Filter Network

Increased spacing between the device and the decoupling capacitor increases the current path distance to the power and ground planes, consequently affecting the inductance of the current path between the device and the capacitor. To optimize the effectiveness of decoupling capacitors, surface-mounted capacitors mounted on the bottom side of the PCB keep the parasitic effects to a minimum. Placing capacitors directly underneath the BGA package improves the high-frequency response of very small-value capacitors.

Using surface-mounted capacitors, the layout should not be allowed to reduce its effectiveness by connecting it through long, skinny traces leading to the power and ground. Use large or multiple smaller vias, and use short and fat traces on capacitors where possible.

Underside routing should be carefully done to place capacitors directly on package ball vias to device power pins. This technique reduces the distance the current path has traveled. The exposed metal on the surface of a PCB where surface-mount devices are soldered or landed should have the shortest possible distance to connect to the device. The best practice is to eliminate any trace connections to capacitors. However, due to PCB assembly limits, this is not always possible. The round-trip delay to the capacitor should be very small. For a particular frequency, the distance to the capacitor should not be greater than one-quarter of a wavelength. If the capacitor placement is greater than one-quarter wavelength, then the energy transferred to the FPGA is negligible.

Use a layout method that hides signal ball vias and creates bottom layer islands that allow ample space to build large low-inductance areas that can accommodate several surface mount capacitors. Figure 2.17 depicts a BGA layout with underside decoupling capacitors.

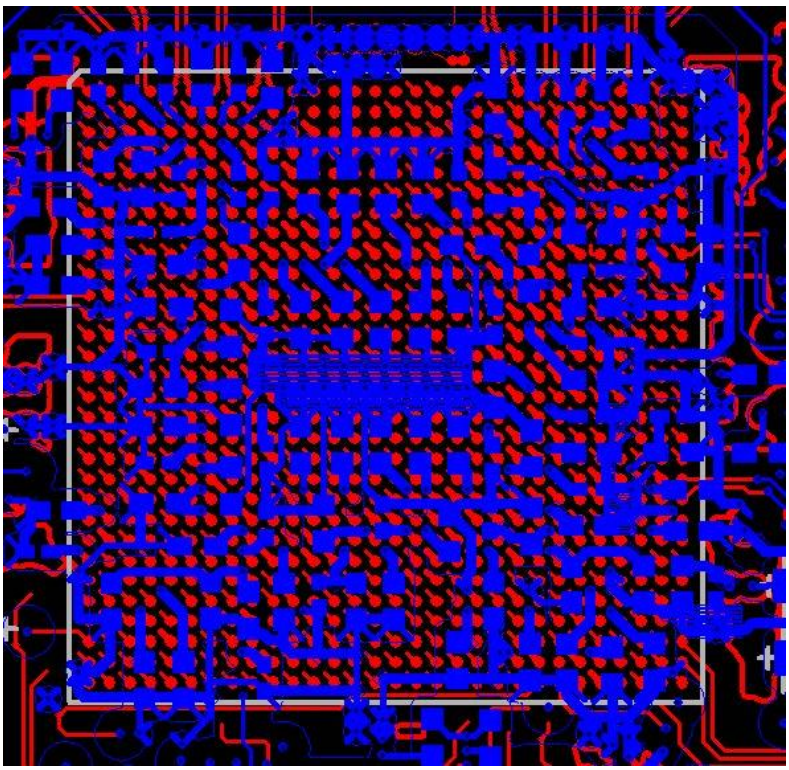


Figure 2.17 Decoupling Capacitors Placement Example

3. Layout Guideline and Fanout Example of High-Speed I/O Interface

Lattice FPGAs support high-speed I/O interfaces, including Double Data Rate (DDR) and Single Data Rate (SDR) interfaces, using the logic built into the Programmable I/O (PIO). SDR applications capture data on one edge of a clock, while DDR interfaces capture data on both the rising and falling edges of the clock, thus doubling the performance. Internal IP core along with the DDR I/O to support DDR3, DDR5, DDR3L, LPDDR2, and LPDDR4 SDRAM memory interfaces. The following section covers a simulation example of the LPDDR4 interface.

3.1. Layout Guidelines of LPDDR4 Interface

The following are the LPDDR4 layout guidelines to meet the JEDEC LPDDR4 specification:

Table 3.1. LPDDR4 Interface Layout Guidelines

Group	Parameter	Condition
Data Bus	Trace Length	< 2inches[1]
	Impedance	40 Ω to 50 Ω
	Connection	Point to point
	Routing Type	Microstrip/Stripline
	Length matching	< ±40mil reference to DQS trace
	DQS P/N matching	< ±4mil
	DQS impedance	80 Ω to 100 Ω
Command/Address, Chip Selection	Trace Length	< 1.5inches[1]
	Impedance	40 to 50 ohm
	Connection	T-point at memory
	Routing type	Microstrip/Stripline
	Length matching	< ±40mil reference to clock trace
Clock	Trace length	< 1.5 inches[1]
	Impedance	100 Ω Differential
	P/N matching	< ±4mil
	External Terminator	100 Ω between PN
	Connection	T-Point, Point to Point

Note:

1. The IP timing needs to be checked to see if the trace length is longer than the specification.

3.1.1. CertusPro-NX LPDDR4-1066 Interface Layout Example

Four signal layers in a 12-layer FR4 stack-up are used to route the LPDDR4 interface signals between the CertusPro-NX memory controller and a NANYA commercial mobile LPDDR4 4Gbit memory.

Two layers are used to route the CA bus, as shown in the following picture. The clock connection is a T-point in memory.

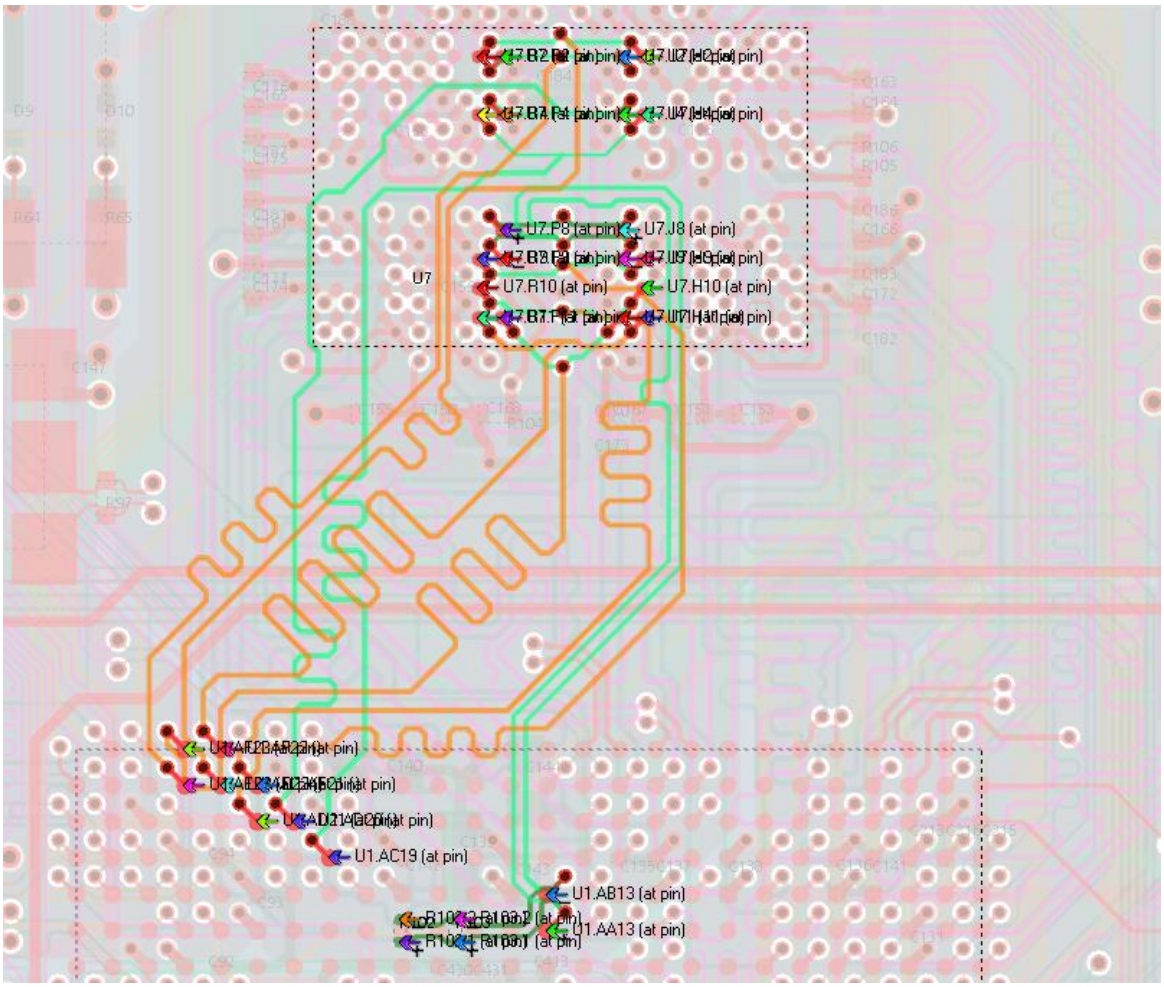


Figure 3.1 LPDDR4 CA Bus Routing Example

Table 3.2. CA Bus Trace Information in the Example Design

Signal name	Layer	Length	Trace Width	Impedance
CA0	L05_SIG2	1.41 inch	6.6 mil	40 Ω
CA1	L05_SIG2	1.41 inch	6.6 mil	40 Ω
CA2	L05_SIG2	1.41 inch	6.6 mil	40 Ω
CA3	L05_SIG2	1.41 inch	6.6 mil	40 Ω
CA4	L05_SIG2	1.41 inch	6.6 mil	40 Ω
CA5	L05_SIG2	1.41 inch	6.6 mil	40 Ω
CKE_A	L08_SIG3	1.41 inch	6.6 mil	40 Ω
CSA	L08_SIG3	1.41 inch	6.6 mil	40 Ω
CAK_A_P/N	L08_SIG3	1.41 inch	6/7.5/6 mil	80 Ω

One layer is used to route the DQ [0..7] and DQ [16..23] buses shown in the following picture:

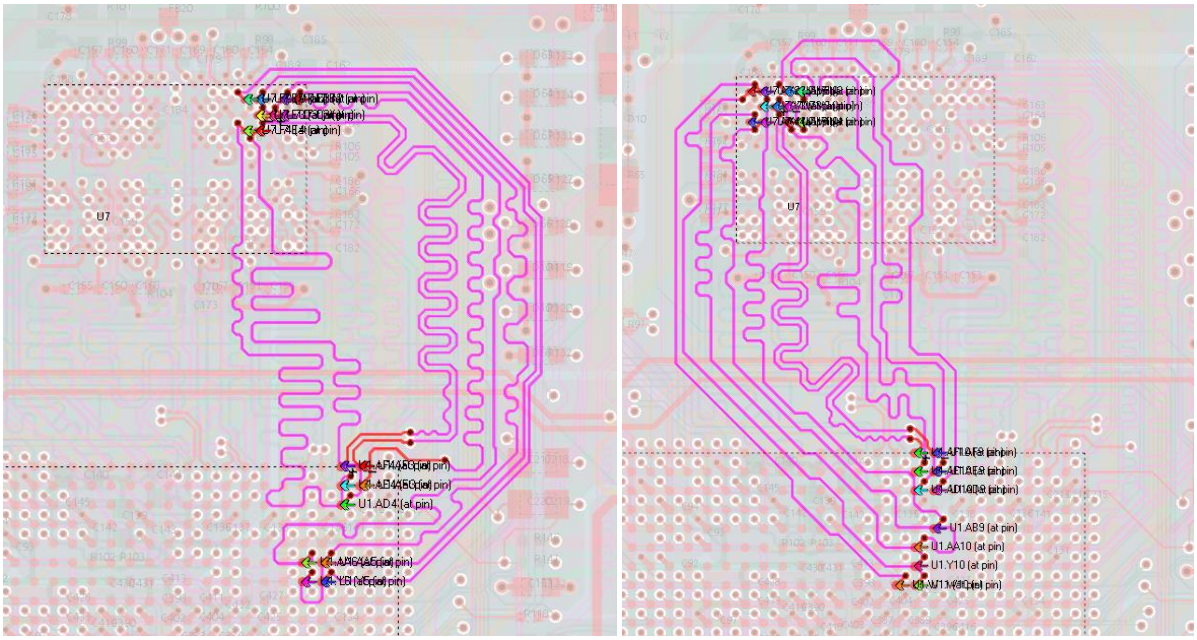


Figure 3.2 LPDDR4 DQ [0..7] and DQ [16..23] Bus Routing Example

Table 3.3. DQ [0..7] and DQ [16..23] Bus Trace Information

Signal name	Layer	Length	Trace Width	Impedance
DQ0	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ1	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ2	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ3	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ4	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ5	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ6	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQ7	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DM0	L03_SIG1	1.95 inch	6.6 mil	40 Ω
DQS0P/N	L03_SIG1	1.95 inch	6/7.5/6 mil	80 Ω
DQ16	L03_SIG1	1.42 inch	6.6 mil	40 Ω
DQ17	L03_SIG1	1.42 inch	6.6 mil	40 Ω
DQ18	L03_SIG1	1.42 inch	6.6 mil	40 Ω
DQ19	L03_SIG1	1.41 inch	6.6 mil	40 Ω
DQ20	L03_SIG1	1.41 inch	6.6 mil	40 Ω
DQ21	L03_SIG1	1.41 inch	6.6 mil	40 Ω
DQ22	L03_SIG1	1.41 inch	6.6 mil	40 Ω
DQ23	L03_SIG1	1.41 inch	6.6 mil	40 Ω
DM2	L03_SIG1	1.41 inch	6.6 mil	40 Ω
DQS2P/N	L03_SIG1	1.42 inch	6/7.5/6 mil	80 Ω

One layer is used to route the DQ[8..15] bus and DQ[24..31] bus, as shown in the following picture:

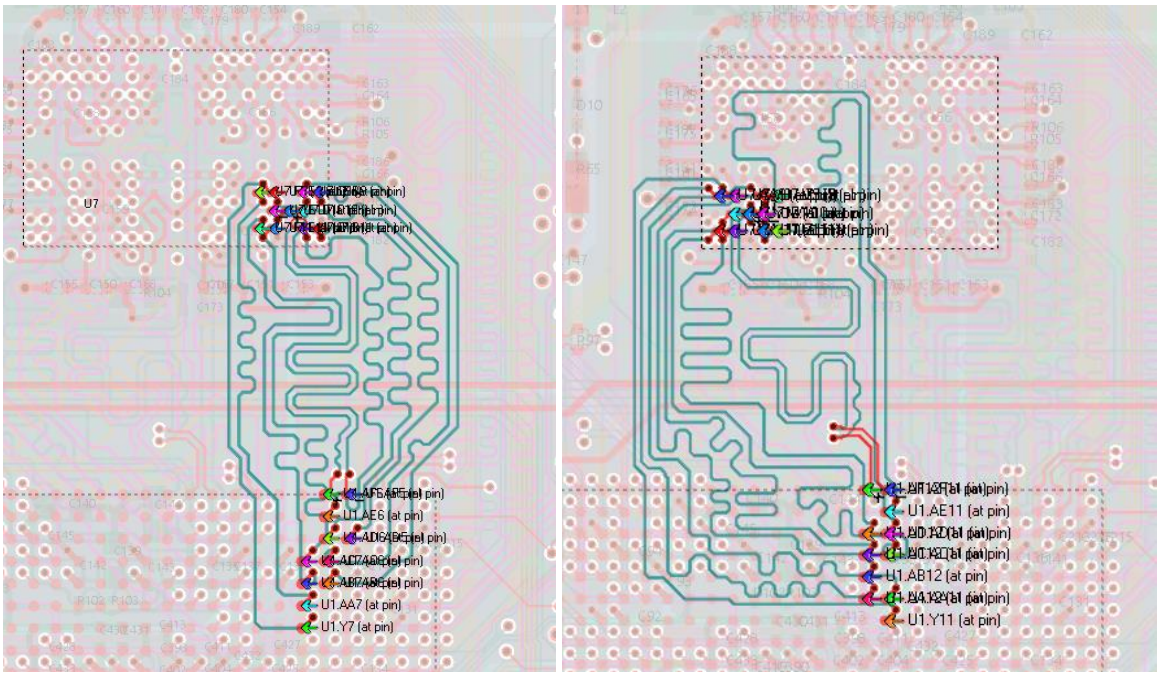


Figure 3.3 LPDDR4 DQ [8..15] and DQ [24..31] Bus Routing Example

Table 3.4. DQ [8..15] and DQ [24..31] Bus Trace Information

Signal name	Layer	Length	Trace Width	Impedance
DQ8	L10_SIG4	1.08 inch	6.6 mil	40 Ω
DQ9	L10_SIG4	1.08 inch	6.6 mil	40 Ω
DQ10	L10_SIG4	1.09 inch	6.6 mil	40 Ω
DQ11	L10_SIG4	1.08 inch	6.6 mil	40 Ω
DQ12	L10_SIG4	1.08 inch	6.6 mil	40 Ω
DQ13	L10_SIG4	1.08 inch	6.6 mil	40 Ω
DQ14	L10_SIG4	1.09 inch	6.6 mil	40 Ω
DQ15	L10_SIG4	1.09 inch	6.6 mil	40 Ω
DM1	L10_SIG4	1.09 inch	6.6 mil	40 Ω
DQS1P/N	L10_SIG4	1.08 inch	6/7.5/6 mil	80 Ω
DQ24	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ25	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ26	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ27	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ28	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ29	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ30	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQ31	L10_SIG4	1.42 inch	6.6 mil	40 Ω
DM3	L10_SIG4	1.41 inch	6.6 mil	40 Ω
DQS3P/N	L10_SIG4	1.41 inch	6/7.5/6 mil	80 Ω

Based on Hyperlynx simulation results, the following is the suggested IP DDR 4 IO configuration for the CertusPro-NX memory controller.

Table 3.5. Suggested IP DDR4 I/O Configuration for CertusPro-NX Memory Controller

Configuration Item	Value
Slew rate for DQ/DM	Fast
Drive Strength for DQ/DQM	10
Slew rate for DQS	Fast
Drive Strength for DQS	8
Slew Rate for CA	Fast
Drive Strength for CA	10
Memory DQ_Vref	40 (ODT=60)
CA _Vref	84(ODT disable)
Controller DQ_vref	97(ODT disable)

3.1.2. Avant LPDDR4-2400 Layout Example

Five signal layers are used to route the Avant 32-bit LPDDR4-2400 interface:

The L07_SIG3 layer in Table 2.2. 16-Layer PCIE Form Factor Stack-up is used to route the CA bus shown in the following picture. The clock routing is a point-to-point connection.

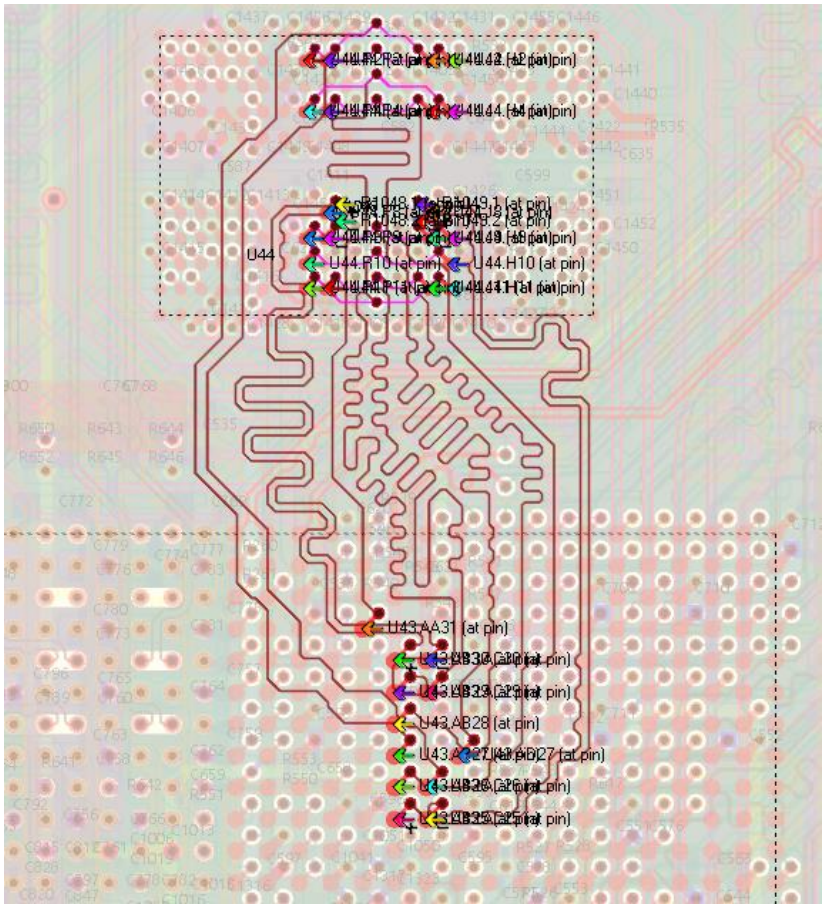


Figure 3.4 Avant LPDDR4 CA Lines Routing Example

Table 3.6. Avant LPDDR4 CA Line Routing Information

Signal name	Layer	Length	Trace Width	Impedance
CA0	L07_SIG3	1.43 inch	3.68mil	50 Ω
CA1	L07_SIG3	1.43 inch	3.68mil	50 Ω
CA2	L07_SIG3	1.43 inch	3.68mil	50 Ω
CA3	L07_SIG3	1.43 inch	3.68mil	50 Ω
CA4	L07_SIG3	1.43 inch	3.68mil	50 Ω
CA5	L07_SIG3	1.43 inch	3.68mil	50 Ω
CKE_A	L07_SIG3	1.43 inch	3.68mil	50 Ω
CSA	L07_SIG3	1.43 inch	3.68mil	50 Ω
CAK_A_P/N	L07_SIG3	1.43 inch	3.55/6.65/3.55mil	100 Ω
CK_B_P/N	L07_SIG3	1.43 inch	3.55/6.65/3.55mil	100 Ω

The L14_SIG6 layer in Table 2.2. 16-Layer PCIE Form Factor Stack-up is used to route the DA[0..7]A bus shown in the following picture.

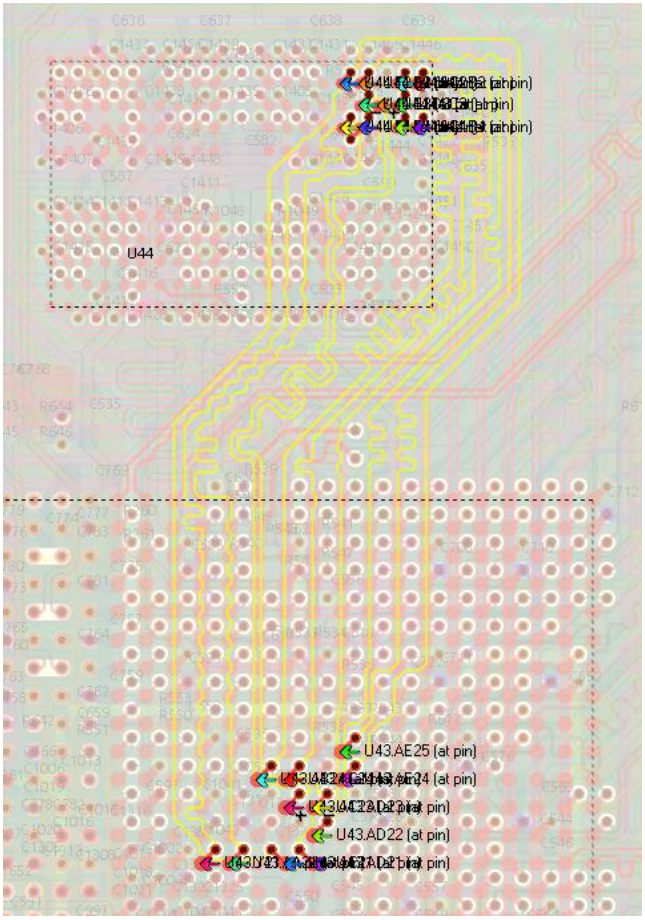


Figure 3.5 Avant DQ [0..7] A Bus Routing Example

Table 3.7. Avant LPDDR4 DQ [0..7] A Bus Trace Information

Signal name	Layer	Length	Trace Width	Impedance
DQ0_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ1_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ2_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ3_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ4_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ5_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ6_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQ7_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DM0_A	L14_SIG6	1.45 inch	3.87mil	50 Ω
DQS0_AP/N	L14_SIG6	1.45 inch	3.7/6.5/3.7mil	100 Ω

L12_SIG5 layer in Table 2.2. 16-Layer PCIE Form Factor Stack-up is used to route DA [8..15] A bus shown in the following picture.

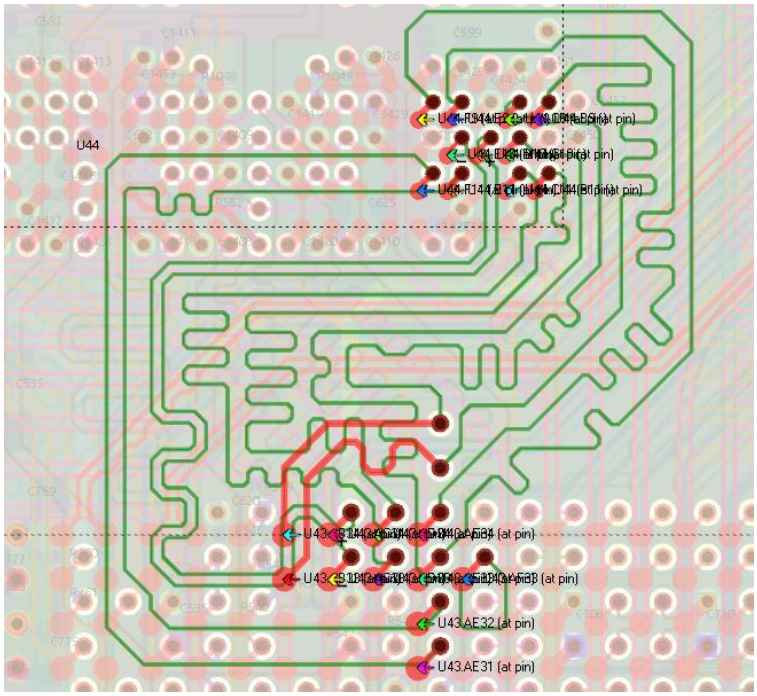


Figure 3.6 Avant DQ [8..15] A Bus Routing Example

Table 3.8. Avant LPDDR4 DQ [8..15] A Bus Trace Information

Signal name	Layer	Length	Trace Width	Impedance
DQ8_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ9_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ10_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ11_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ12_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ13_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ14_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQ15_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DM1_A	L12_SIG5	1.07 inch	3.85mil	50 Ω
DQS1_AP/N	L12_SIG5	1.07 inch	3.7/6.5/3.7mil	100 Ω

The L05_SIG2 layer in Table 2.2. 16-Layer PCIE Form Factor Stack-up is used to route the DA[0..7]B bus shown in the following picture.

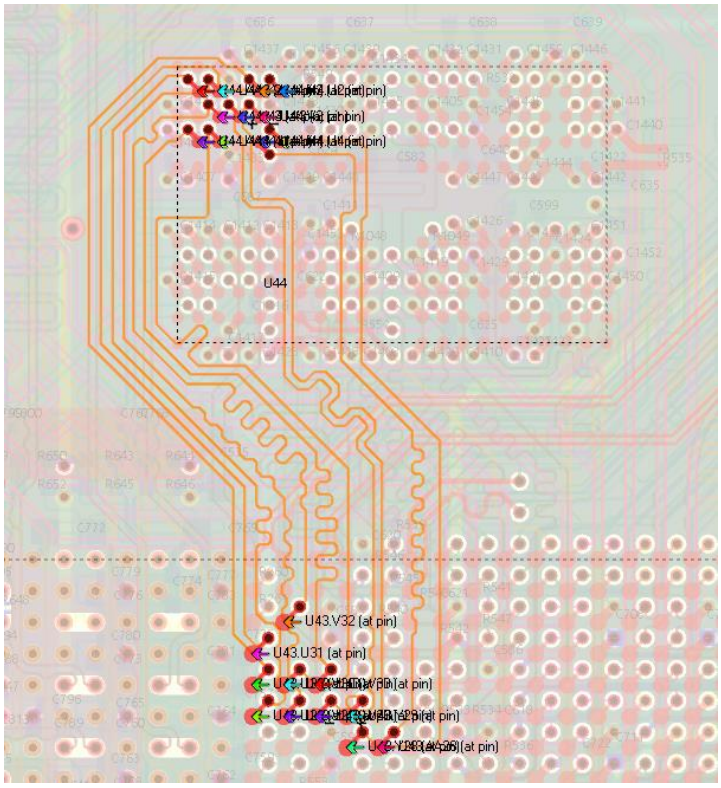


Figure 3.7 Avant DQ [0..7] B Bus Routing Example

Table 3.9. Avant LPDDR4 DQ [0..7] B Bus Trace Information

Signal name	Layer	Length	Trace Width	Impedance
DQ0_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ1_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ2_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ3_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ4_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ5_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ6_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQ7_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DM0_B	L05_SIG2	1.07 inch	3.89mil	50 Ω
DQS3_BP/N	L05_SIG2	1.07 inch	3.7/6.5/3.7mil	100 Ω

The L10_SIG4 layer in Table 2.2. 16-Layer PCIE Form Factor Stack-up is used to route the DA [8..15]B bus shown in the following picture.

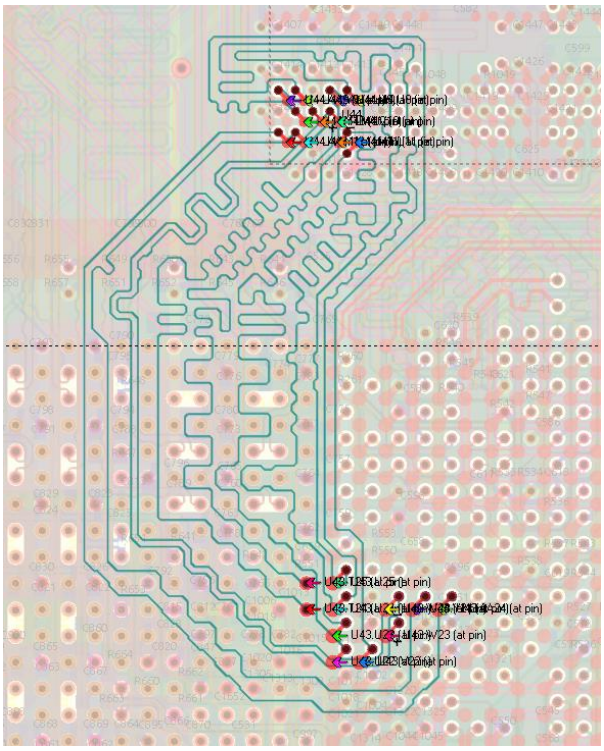


Figure 3.8 Avant DQ [8..15] B Bus Routing Example

Table 3.10. Avant LPDDR4 DQ [8..15] B Bus Trace Information

Signal name	Layer	Length	Trace Width	Impedance
DQ8_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ9_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ10_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ11_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ12_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ13_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ14_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQ15_B	L10_SIG4	1.64 inch	3.85mil	50 Ω
DM1_B	L10_SIG4	1.64 inch	3.65mil	50 Ω
DQS4_BP/N	L10_SIG4	1.64 inch	3.52/6.68/3.52mil	100 Ω

Based on Hyperlynx simulation results, the following is the suggested IP DDR 4 IO configuration for the Avant-versa LPDDR4 interface:

Table 3.11. Suggested IP DDR4 I/O Configuration for the Avant-Versa LPDDR4 Interface

Configuration Item	Value
Slew rate for DQ/DM	Fast
Drive Strength for DQ/DQM	34 Ω
Slew rate for DQS	Fast
Drive Strength for DQS	34 Ω
Slew Rate for CA	SLOW
Drive Strength for CA	34 Ω
Slew Rate for CK/CS	Fast
Drive Strength for CK/CS	34 Ω

Configuration Item	Value
Memory DQ_Vref	34 (ODT=60)
CA _Vref	34(ODT=60)
MC DQ_vref	48 (ODT=60)

4. Layout Guidelines and Simulation Examples of the SERDES Interface

Lattice FPGA supports a range of popular serial protocols, including:

- PCI Express Gen1 (2.5 Gbps), Gen 2 (5.0 Gbps), Gen 3 (8.0 Gbps), and Gen 4 (16.0 Gbps)
- Ethernet
  - 25.78125 Gbps Gigabit Ethernet
  - 40GBase-KR4
  - 10GBASE-R at 10.3125 Gbps
  - SGMII
  - XAUI at 3.125 Gbps per lane
- SLVS-EC at 1.25 Gbps, 2.5 Gbps and 5 Gbps
- DP/eDP at 1.62 Gbps(RBR), 2.7 Gbps (HBR), 5.4 Gbps (HBR2), and 8.1 Gbps (HBR3)
- CoaXPress at 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, and 6.25 Gbps
- JESD204C: Class B 1-12.5 Gbps. Class C 1-25 Gbps
- CPRI:1.2288 Gbps, 2.4576Gbps, 3.072Gbps, 4.915Gbps, 6.144Gbps, 8.11008Gbps, 9.8304Gbps, 10.1276Gbps, 12.16512Gbps,24.300Gbps
- SERDES-only mode allowing direct 8-bit or 10-bit interface to the PCS logic

A SERDES receiver channel can receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8-bit or 10-bit data to the PCS logic. The SERDES transmitter channel can receive parallel 8-bit or 10-bit data from the PCS block or directly from the fabric, serialize the data and transmit the serial bit stream through the differential drivers. The following section covers the simulation example of a 25Gbps high-speed channel.

4.1. Layout Guidelines for 25 Gbps SERDES Channel

The following are the layout guidelines for the 25Gbps high-speed channel:

- Follow the high-speed routing guidelines as indicated in the protocol specification.
- Nominal differential impedance: 85-100 Ω
- Skew within the differential pair: < 1 ps
- Clearly understand the crosstalk specification and choose proper spacing to route the TX and RX signals. When routing on the same layer, ensure that the spacing between the lanes is more than 6 times the PCB dielectric height.
- The return path should be ground-level and continuous. Do not route trace over a plane void or anti-pad.
- Clearly understand the transmission line impedance specification and use simulation tools to tune the differential signal via spacing, anti-pad size, and GND reference via location to minimize reflection and crosstalk. Use ground return vias adjacent to the differential pair vias to minimize crosstalk between the lanes.
- BGA ball pads, AC coupling pad, and large connector finger pads generally introduce high capacitive discontinuities. Carefully tune the anti-pad below the pads to minimize the capacitance.
- Minimize the PCB via stub by choosing the proper routing layer and using blind via or back drilling of via stubs.
- For long channels, generate the right PCB stack-up, simulate the trace loss for each signal layer, and select the right layer to minimize the trace insertion loss.

4.2. Microstrip Layout Example of Avant Versa 25 Gbps Channel

This top layer is used to fanout one Avant 25Gbps TX and RX channel to the Amphenol 50 Ω SMA connector.

The layout follows the IEEE 803.3-2022 25GAUI C2M specification. The PCB insertion loss budget at 12.89 GHz is up to 7.3 dB.

4.2.1. Ground Cutout for BGA Pad and 0201 Capacitor Pad

Based on the simulation, the BGA pad and 0201 AC coupling capacitor pad need ground cutout at layer 2. The following picture illustrates the BGA ground cutout area and 0201 capacitor pad cutout areas used in Figure 4.2.

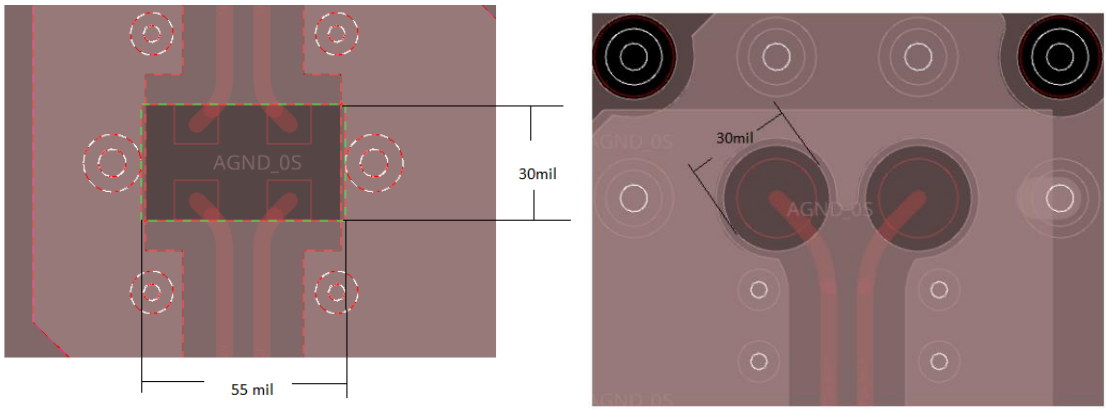


Figure 4.1 0201 Capacitor Pad and BGA Ball Ground Cutout Area

A new ground shape is added to lay03-sig1 in Table 2.2. 16-Layer PCIE Form Factor Stack-up as the new ground reference.

4.2.2. Grounded Wave Guide to Reduce Crosstalk

A grounded wave guide (pink area) is used to reduce crosstalk.

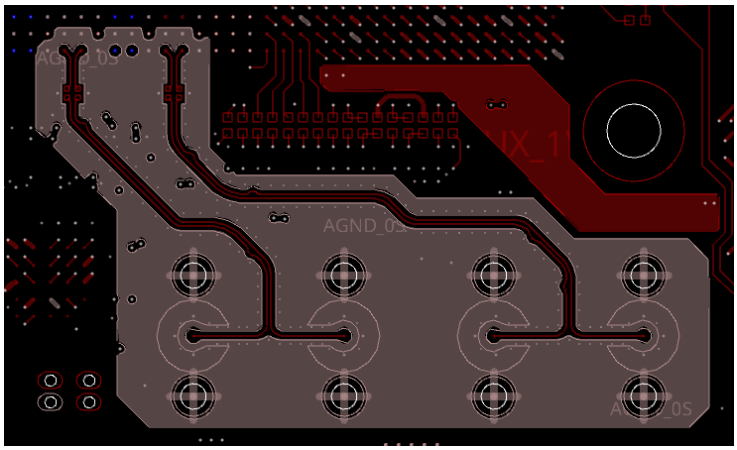


Figure 4.2 Grounded Wave Guide for 25 Gbps Microstrip Channel

4.2.3. Microstrip Channel Simulation Results

The full channel simulation of the microstrip channel meets the IEEE 803.3-2022 25GAUI C2M specification: the insertion line (yellow) is above the spec mask (yellow line mask). The differential return loss (blue) is lower than the spec mask (blue line mask). The common mode return loss (green) is lower than the spec mask (green line mask).

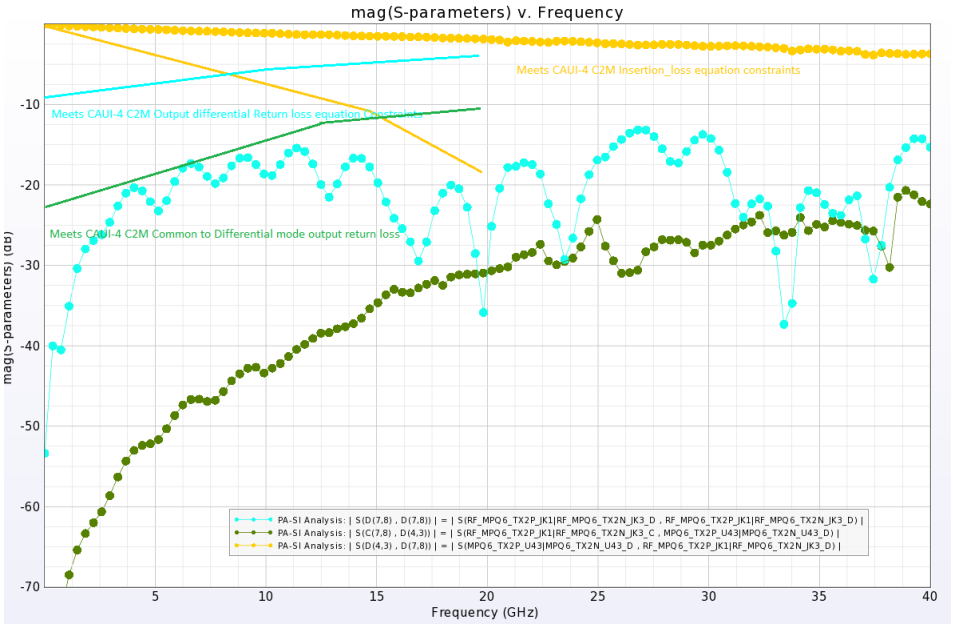


Figure 4.3 Microstrip Line Simulation Results

4.2.4. Microstrip IBIS-AMI Simulation Results

The Keysight ADS platform is used to run the IBIS-AMI simulation. The following is the IBIS AMI simulation schematic. The schematic includes the TX_AMI block, X1 (MPQ6 transmission line S-Parameters), and RX_AMI block.

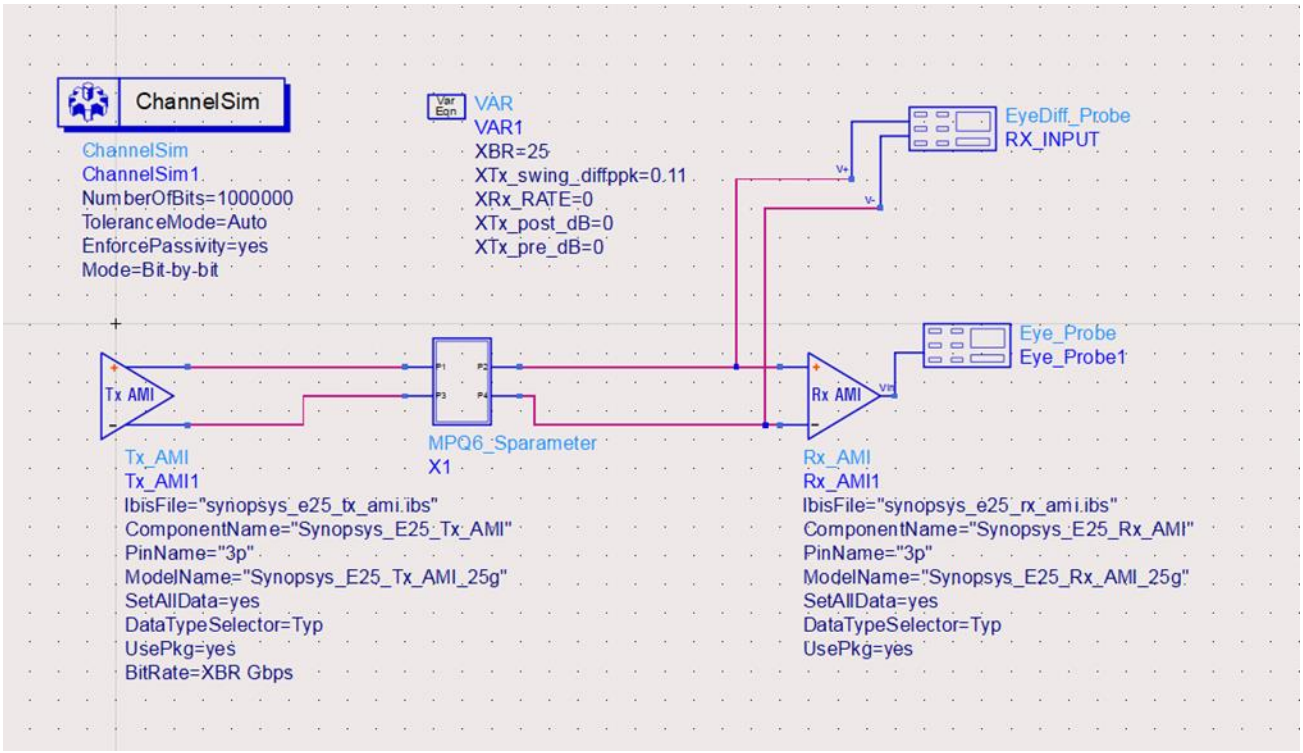
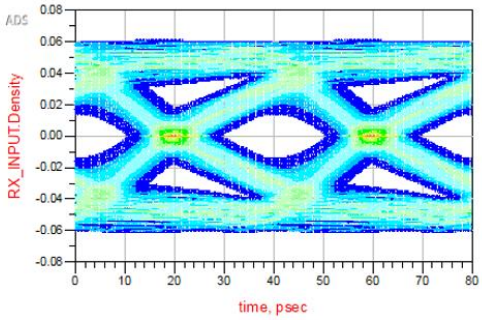
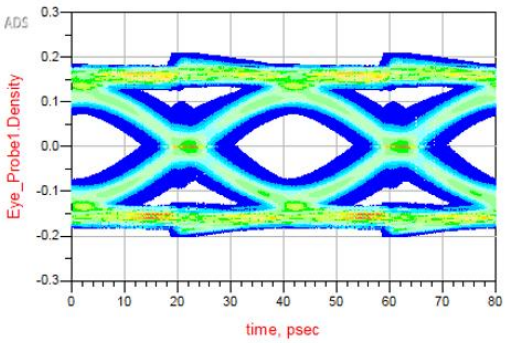


Figure 4.4 Microstrip Line IBIS-AMI Schematic

Eye diagrams and eye measurements outputs after simulation.



measurement	RX_INPUT.Summary
Level1	0.039
Level0	-0.039
Height	0.024
Width	2.040E-11



measurement	Eye_Probe1.Summary
Level1	0.133
Level0	-0.133
LevelMean	-1.894E-5
Amplitude	0.267
Height	0.127
HeightDB	-8.962
Width	2.500E-11
SNR	5.727
RiseTime	2.148E-11
FallTime	2.151E-11
JitterPP	1.840E-11
JitterRMS	2.504E-12
WidthAtBER	1.920E-11
HeightAtBER	0.135

Figure 4.5 Microstrip Line IBIS-AMI Simulation Result

4.3. Stripline Layout Example of the Avant Versa zSFP+ 25 Gbps Channel

This L14-sig6 in Table 2.2. 16-Layer PCIE Form Factor Stack-up is used to route Avant 25Gbps TX and RX channels to the TE ZSFP+ connector.

The layout follows the IEEE 803.3-2022 25GAUI C2M specification. The PCB insertion loss budget at 12.89 GHz is up to 7.3 dB.

4.3.1. Via-in-Pad Through-Hole Via for zSFP+ 25 Gbps Channel Routing

The zSFP+ 25Gbps channel is routed on L14-SIG6 in Table 2.2. 16-Layer PCIE Form Factor Stack-up. The 8-mil Via-in-pad through-hole Via is used to fan out a 25Gbps channel. The anti-pad of 8-mil through hole is 25 mil, so differential trace can be routed between BGA pads. The following picture shows the layout.

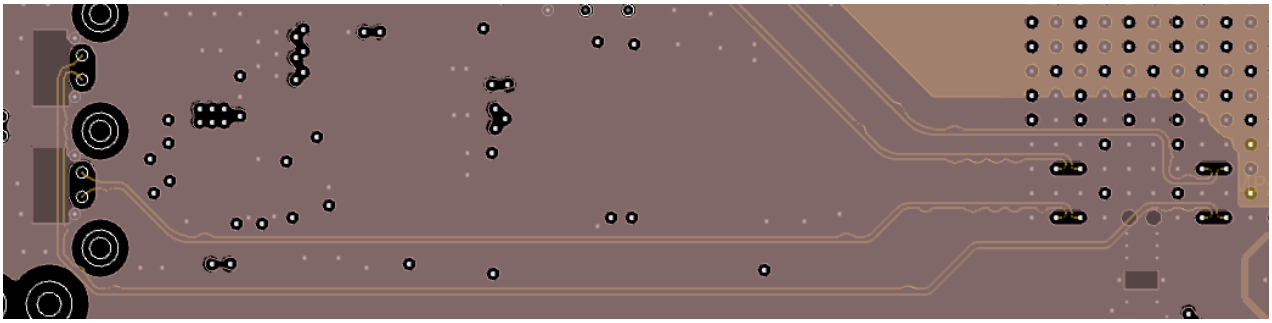


Figure 4.6 zSFP+ 25 Gbps Channel Fanout

4.3.2. Stripline Channel Simulation Results

The full channel simulation of the microstrip channel meets the IEEE 803.3-2022 25GAUI C2M specification: the insertion line (RED) is above the spec mask (Red line mask). The differential return loss (green) is lower than the spec mask (green line mask).

Figure 4.7 Stripline Simulation Results

4.3.3. Stripline IBIS-AMI Simulation Results

The Keysight ADS platform is used to run the IBIS-AMI simulation. The following is the IBIS AMI simulation schematic. The schematic includes the TX_AMI block, X1 (zSFP+ transmission line S-Parameters), and RX_AMI block.

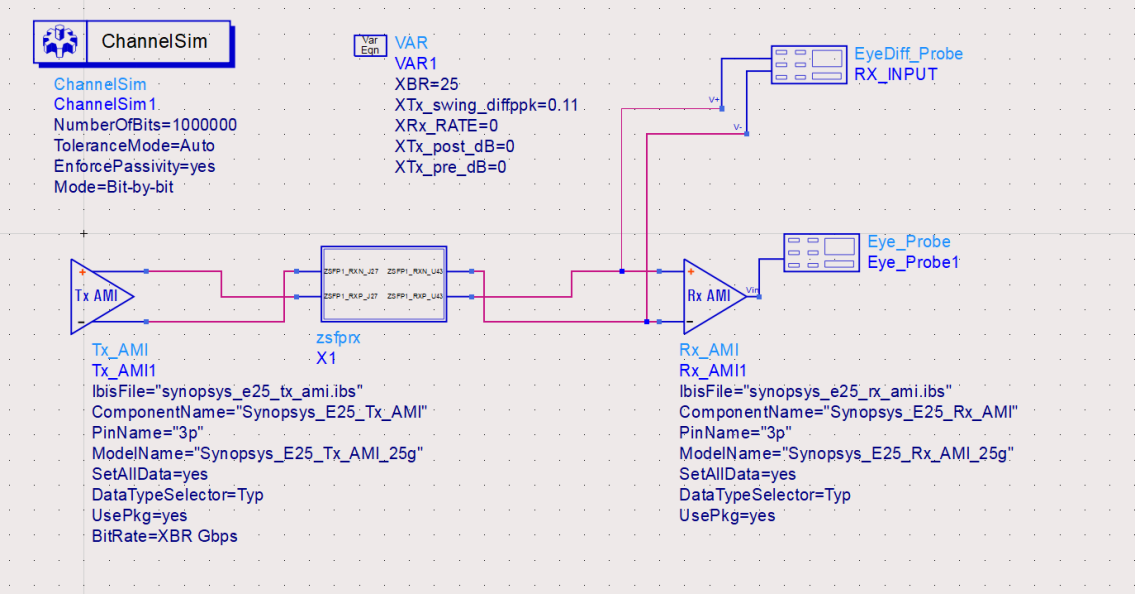
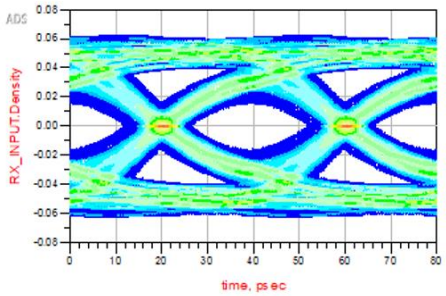
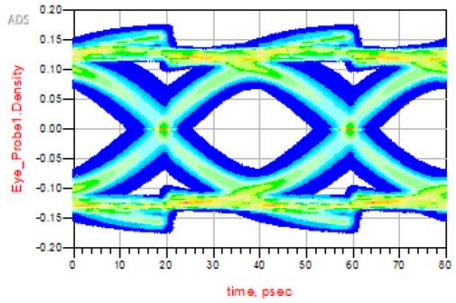


Figure 4.8 Stripline IBIS-AMI model



measurement	RX_INPUT.Summary
Level1	0.040
Level0	-0.040
Height	0.028
Width	2.700E-11



measurement	Eye_Probe1.Summary
Level1	0.111
Level0	-0.111
LevelMean	9.406E-6
Amplitude	0.223
Height	0.129
HeightDB	-8.894
Width	3.000E-11
SNR	7.184
RiseTime	1.801E-11
FallTime	1.803E-11
JitterPP	1.440E-11
JitterRMS	1.687E-12
WidthAtBER	2.280E-11
HeightAtBER	0.130
CrossingLevel	-1.806E-5

Figure 4.9 Stripline IBIS-AMI Simulation Results

References

- CrossLink-NX webpage
- CertusPro-NX webpage
- Mach-NX webpage
- ECP5 and ECP5-5G webpage
- iCE40 UltraPlus webpage
- CrossLink-NX Family Data Sheet (FPGA-DS-02049)
- CertusPro-NX Family Data Sheet (FPGA-DS-02086)
- ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02102)
- iCE40 UltraPlus Family Data Sheet (FPGA-DS-02008)
- Mach-NX Family Data Sheet (FPGA-DS-02084)
- ORTx2G5, ORSOx2G5 and ORSPI4 High-Speed Backplane Measurements (TN-1027)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Transmission of High-Speed Serial Signals Over Common Cable Media (FPGA-TN-1066)
- NANYA Commercial Mobile LPDDR4 2Gb/4Gb SRAM datasheet
- DesignWare Cores SERDES PCB and Packaging Design Guide Version2.40a
- JESD 309 DDR5 Small Outline Dual Inline Memory Module (SODIMM) Common Standard
- JESD209-4D Lower Power Double Data Rate 4 (LPDDR4)
- PCIE Express Card Electromechanical Specification Revision 4.0, Version 1.0
- IEEE Standard for Ethernet—IEEE Std 802.3-2022
- www.eeweb.com/tool
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 6.4, August 2024

Section	Change Summary
All	• Minor editorial fixes. • Removed old sections, *Board Design Practices* and *High-Speed Connectors and IC Packaging*.
Disclaimers	Updated this section.
Inclusive Language	Added this section.
Abbreviations in This Document	• Changed the section title from *Acronyms in This Document to Abbreviations* in This Document. • Updated this section.
Introduction	Reworked section contents.

General High-Speed PCB Design Considerations	• Reworked section contents and updated the section title *to General High-Speed PCB Design Considerations*.
	• Moved the following old sections to this main section:
	  • *Backplane Topology and Overview*
	  • *Point-to-Point Backplane Signal Path Structure*
	  • *Advantages of Differential Signaling*
	  • *PCB Layer Design (Board Stack-Up)*
	  • *Decoupling and Bypassing*

Layout Guidelines and Fanout Example of High-Speed I/O Interface	• Reworked section contents and updated the section title to *Layout Guidelines and Fanout Example of High-Speed I/O Interface*. • Moved old section, *Special Design Considerations at >622 Mbps* to this main section.

Layout Guidelines and Simulation Examples of the SERDES Interface	• Reworked section contents and updated the section title to *Layout Guidelines and Simulation Examples of the SERDES Interface*.
	• Moved following old sections to this main section:
	  • *Special Design Considerations at >2.5 Gbps*
	  • *Special Layout Considerations for Lattice SERDES Devices*
	  • *Pre-Emphasis*
	  • *Receiver Equalization*
	  • *Conclusion*

References	Updated this section.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 6.3, April 2022

Section	Change Summary
Acronyms	Newly added section.
Backplance Topology and Overview	Changed to *This type of backplane interconnection can be used with data rates to 25 Gbps and above*.

Board Design Practices	• In the PCB Trace Impedance Calculation section:
	  • updated the 2D field solver program example to the *Si96000eb program from Polar Instruments* and updated relevant description.
	• In the Examples of PCB Trace Impedance Calculation section:
	  • updated to the latest Product and the latest speed;
	  • updated Figure 5.5 Differential Microstrip Example with Saturn PCB Toolkit Impedance Calculator Tool.
	• In the PCB Design Checklist section:
	  • updated to Use 3 S or 4 S separation rules.

Decoupling and Bypassing	Newly added description about *Rule of Thumb* and *Simulation with a power Integrity solver*.
Special Design Considerations at	• Newly added description about HyperLynx and Tyco RT3 connector.

Section	Change Summary

>622 Mbps	• In the High-Speed Copper Cables section:
	  • newly added description of the latest high speed cable assemblies from TE Connectivity.
	  • newly added Figure 8.1 Insertion Loss Comparison for Flyover Twinax Cables versus Megtron 6 and Megtron 7 with 12 in Traces.

Special Design Considerations at >2.5 Gbps	• In the Board Thickness and Vias section:
	  • newly added These vias need to be top and back drilled to reduce the stub effects.
	• In the Board Material section:
	  • added description regarding new materials increasing the board speed.

Special Layout Considerations for Lattice SERDES Devices	• In the PCB Routing and Board Stack-up section: • added description on how to reduce microstrip losses. • newly added the last paragraph.
High-Speed Connectors and IC Packaging	General update to the first paragraph reflecting the most recent FPGA product information.
Pre-Emphasis**Error! Reference source not found.**	General update to the first paragraph reflecting the most recent FPGA product information.
Conclusion	Updated data rates to 25 Gbps and *allow easy system design at rates to 1066 Mbps parallel interfaces*.
References	Globally updated the list.

Revision 6.2, December 2019

Section	Change Summary
All	• Changed document number from TN1033 to FPGA-TN-02178. • Updated document template.
Disclaimers	Added this section.

Revision 6.1, April 2011

Section	Change Summary
All	Updated for LatticeECP3 FPGA family.

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