RISC-V MC CPU IP Core - Lattice Propel Builder

User Guide

FPGA-IPUG-02114-1.0

May 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AHB-L	ARM High-performance Bus – Lite
CPU	Central processing unit
DMIPS	Dhrystone MIPS (Million Instructions per Second)
FPGA	Field Programmable Gate Array
GDB	Gnu Debugger
HDL	Hardware Description Language
ISA	Instruction Set Architecture
JTAG	Joint Test Action Group
LUT	Lookup-Table
PIC	Programmable Interrupt Controller
RISC-V	Reduced instruction set computer-V (five)

1. Introduction

The Lattice Semiconductor RISC-V MC CPU soft IP contains a 32-bit RISC-V processor core and optional submodules – Timer and Programmable Interrupt Controller (PIC). The CPU core supports the RV32I instruction set, external interrupt, and debug feature, which is JTAG – IEEE 1149.1 compliant. The Timer submodule is a 64-bit real time counter, which compares a real-time register to another register to assert the timer interrupt. The PIC submodule aggregates up to eight external interrupt inputs into one external interrupt. The submodule registers are accessed by the processor core using a 32-bit AHB-L interface.

The design is implemented in Verilog HDL. It can be configured and generated using the Lattice Propel™ Builder software. It can be targeted to MachXO3D™ FPGA devices and implemented using the Lattice Diamond® software Place and Route tool integrated with the Synplify Pro® synthesis tool.

1.1. Features

The RISC-V MC soft IP has the following features:

- RV32I instruction set (RV32C only valid when *PFR_OPT* is unchecked)
- Five stages of pipelines
- Support for the AHB-L bus standard for instruction/data port
- Optional debug through GDB and OpenOCD
- Optional Timer/PIC modules
- Interrupt and exception handling with Machine mode in RISC-V privileged ISA Specification v1.10
- >0.7 DMIPS/MHz performance
- >45 MHz in MachXO3D

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

2. Functional Descriptions

2.1. Overview

The RISC-V MC soft IP processes data and instruction by considering the timer interrupt and external interrupt. As shown in Figure 2.1, the CPU IP core module has a 32-bit processor core and optional submodules. It uses two interfaces, one AHB-L interface (Read-Only) for instruction and one AHB-L interface (Read/Write Access) for data memory. See Table 2.5 and Table 2.6 for the AHB-L Instruction Fetch and Data Accessing ports definition. RISC-V core, PIC, Timer, and AHB-L multiplex are run in the system clock domain. The RISC-V core debug runs in two clock domains: the system clock domain and the JTAG clock domain.

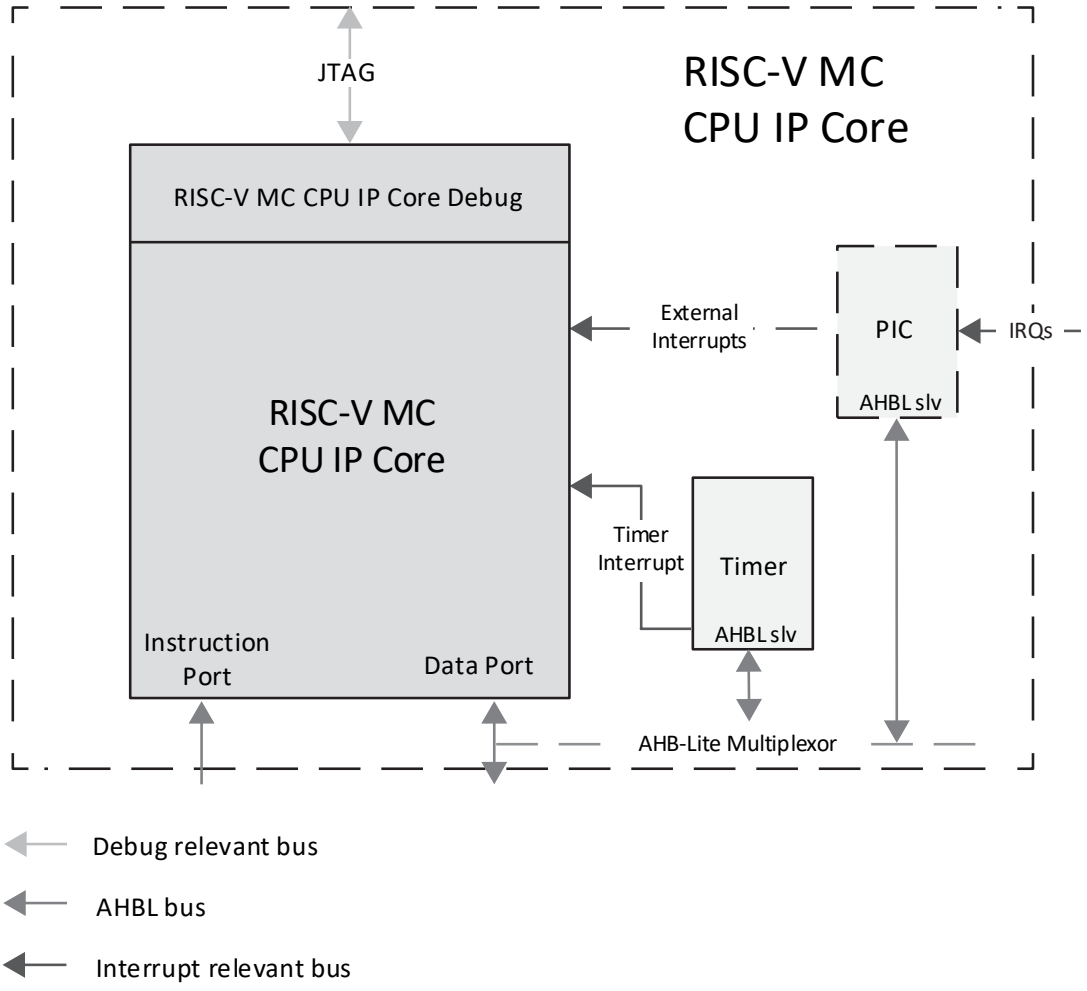

Figure 2.1. RISC-V MC Soft IP Diagram

2.2. Modules Description

2.2.1. RISC-V Processor Core

The processor core follows the RV32I instruction set. Figure 2.2 shows the processor core block diagram.

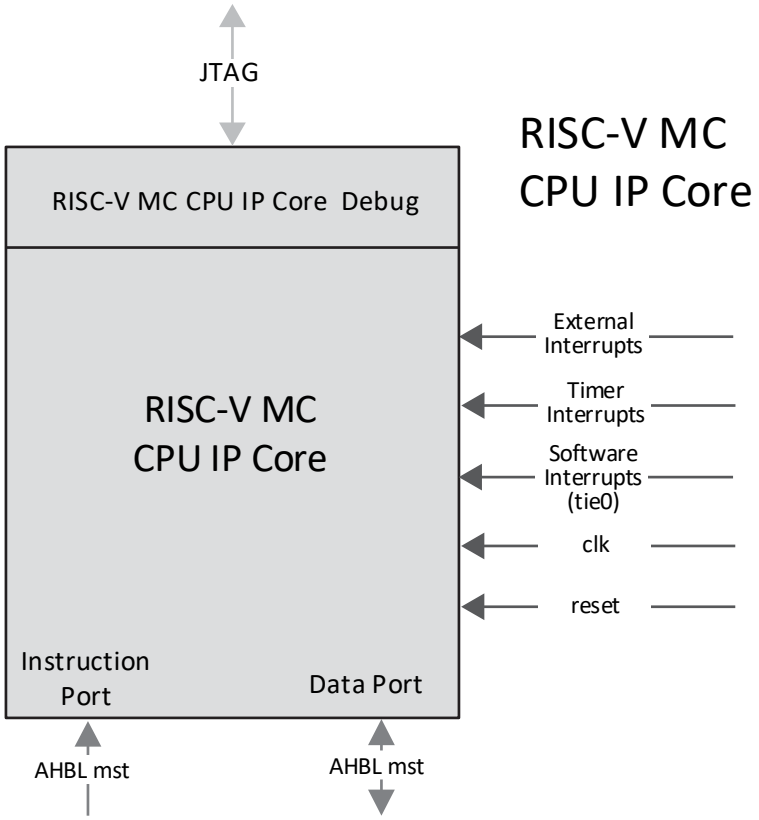

Figure 2.2. RISC-V MC Processor Core Block Diagram

2.2.1.1. Interrupt

Whenever an interrupt occurs, it has to remain in its active level until it is cleared by the processor core interrupt service routine.

If an interrupt occurs before jumping to the interrupt service routine, the processor core stops the prefetch stage and waits for all instructions in the later pipeline stages to complete their execution.

2.2.1.2. Exception

If an exception occurs, the processor core stops the corresponding instruction, flushes all previous instructions, and waits until the terminated instruction reaches the writeback stage before jumping to the exception service routine.

2.2.1.3. Low Power Mode

Processor core (with *PFR_OPT* unchecked) enters into low power mode with *WFI* command, PC halts during low power mode, processor wakes up if there is external/timer interrupt.

2.2.1.4. Debug

The processor core supports the IEEE-1149.1 JTAG debug logic with two hardware breakpoints.

2.2.1.5. Control and status registers

The processor core supports the CSR (control and status registers) listed in Table 2.1.

Table 2.1. RISC-V Processor Core Control and Status Registers

addr	CSR Name	Access	Fields
0x300	mstatus (machine status register)	read/write	bits[12:11] mpp: privilege mode before entering trap , should always be 2'b11 (m mode) bit [7] mpie: updated to mie value when entering to trap bit [3] mie: global interrupt enable
0x304	mie (machine interrupt enable register)	read/write	bit[11] meie: m mode external interrupt enable bit[7] mtie: m mode timer interrupt enable bit[3] msie: m mode software interrupt enable
—	mtvec	cannot be accessed (fixed to 0x20)	bit[31:2]: four byte aligned trap vector base address bit[0]: mode trap vector mode: all traps set the program counter to base
0x341	mepc (machine exception program counter)	read only	bits[31:0]: When trap in taken into m mode, mepc is used to store the address of the instruction that encountered exception.
0x342	mcause (machine cause register)	read only	bit[31]: 1'b1: interrupt 1'b0: exception bit[3:0]: exception code for interrupt : • 3-machine software interrupt • 7-machine timer interrupt • 11- machine external interrupt for exception : 0 – instruction address misaligned 1 – instruction access fault 2 – illegal instruction 4 – load address misaligned 5 – load access fault
0x343	mtval (machine trap value register)	read only	bits[31:0] : When a hardware breakpoint is triggered, or an instruction-fetch, load, or store address is misaligned or access exception occurs, mtval is written with the faulting address. It may also be written with illegal instruction when an illegal instruction exception occurs.
0x344	mip (machine interrupt pending register)	read only	bit[11] meip: m mode external interrupt pending bit[7] mtip: m mode timer interrupt pending bit[3] msip: m mode software interrupt pending

2.2.2. Submodule (PIC/Timer)

The CPU soft IP contains submodules: PIC and Timer. The PIC and Timer share the same start address in memory map and a fixed 2 kB address range is allocated if any of them are enabled.

2.2.2.1. PIC

The PIC aggregates up to eight external interrupt inputs (IRQs) into one interrupt output to processor core. The interrupt status register and can be used to read the values of IRQs. Individual IRQs can be configured by programming the corresponding enable and polarity registers. All registers can be accessed through an AHB-L interface, as shown in Figure 2.3.

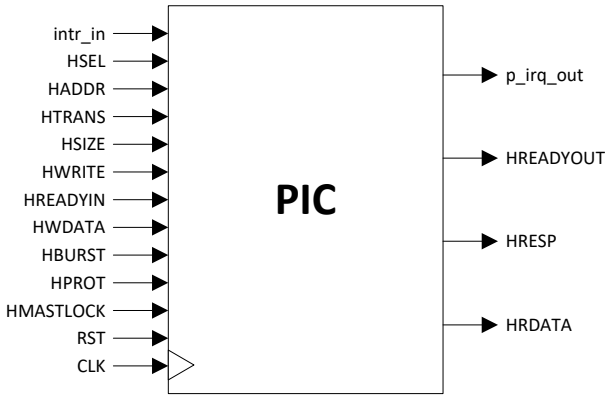

Figure 2.3. PIC Block Diagram

Table 2.2 provides the descriptions of PIC registers.

Table 2.2. PIC Registers

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th></tr>
<tr><td>0x000</td><td>PIC_ISRC</td><td>Interrupt Status Register Clear (write-only)
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_ISRC [N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_ISRC [1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_ISRC [0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table>
</td></tr>
<tr><td>0x004</td><td>PIC_ISRS</td><td>Interrupt Status Register Set (write-only)
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_ISRS [N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_ISRS [1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_ISRS [0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th></tr>
<tr><td>0x008</td><td>PIC_ISR</td><td>Interrupt Status Register (read-only)
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_ISR [N-1]</td><td>R</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_ISR [1]</td><td>R</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_ISR [0]</td><td>R</td><td>1</td><td>0x0</td></tr>
</table></td></tr>
<tr><td>0x010</td><td>PIC_IERC</td><td>Interrupt Enable Register Clear
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_IERC[N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_IERC[1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_IERC[0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table>

PIC_IERC[i]
Enable or Disable the interrupt request (irq[i]) port from the aggregation of interrupts (core_meip).
• 0 – disable irq[i]
• 1 – enable irq[i]</td></tr>
<tr><td>0x014</td><td>PIC_IERS</td><td>Interrupt Enable Register Set
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_IERS[N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_IERS[1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_IERS[0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table></td></tr>
<tr><td>0x018</td><td>PIC_IER</td><td>Interrupt Enable Register
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_IERS[N-1]</td><td>R</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_IERS[1]</td><td>R</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_IERS[0]</td><td>R</td><td>1</td><td>0x0</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th></tr>
<tr><td>0x020</td><td>PIC_POLC</td><td>PIC Interrupt Polarity Register Clear
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_POLC [N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_POLC l[1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_POLC [0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table></td></tr>
<tr><td>0x024</td><td>PIC_POLS</td><td>PIC Interrupt Polarity Register Set
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_POLC [N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_POLC l[1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_POLC [0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table></td></tr>
<tr><td>0x028</td><td>PIC_POL</td><td>PIC Interrupt Polarity register
(Parameterizable width, min=2, max=8)

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N]</td><td>PIC_POLC [N]</td><td>R</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_POLC l[1]</td><td>R</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_POLC [0]</td><td>R</td><td>1</td><td>0x0</td></tr>
</table>
PIC_POLC[i]
Indicates the polarity of interrupt request (irq[i]) port.
• 0 – irq[i] is active high
• 1 – irq[i] is active low</td></tr>
</table>

2.2.2.2. Timer

The Timer module provides a 64-bit real-time counter register (mtime) and time compare register (mtimecmp). An output interrupt signal notices the RISC-V processor core when the value of mtime is greater than or equal to the value of mtimecmp. All registers can be accessed through an AHB-L interface, as shown in Figure 2.4.

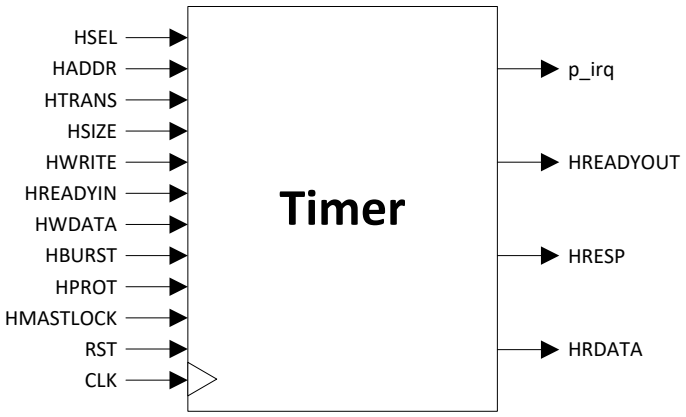

Figure 2.4. Timer Block Diagram

Table 2.3 provides the descriptions of Timer registers.

Table 2.3. Timer Registers

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th></tr>
<tr><td>0x400</td><td>TIMER_CNT_L</td><td>Lower 32 bits of Timer counter register

<table><tr><td>Field</td><td>Name</td><td>Access</td><td>Width</td><td>Reset</td></tr><tr><td>[63:0]</td><td>mtime</td><td>RW</td><td>64</td><td>0x0</td></tr></table>
mtime
A 64 bit real-time counter register. You must set the register to a non-zero value to start the counting process..</td></tr>
<tr><td>0x404</td><td>TIMER_CNT_H</td><td>Higher 32 bits of Timer counter register</td></tr>
<tr><td>0x410</td><td>TIMER_CMP_L</td><td>Lower 32 bit for Timer time compare register.

<table><tr><td>Field</td><td>Name</td><td>Access</td><td>Width</td><td>Reset</td></tr><tr><td>[63:0]</td><td>mtimecmp</td><td>RW</td><td>64</td><td>0x0</td></tr></table>
mtimecmp
This register is used to generate or clear the timer interrupt (mtip). When the value of mtime register is greater than or equal to the value of mtimecmp register, the cpu_mtip_o is asserted and remains asserted until it is cleared by writing to mtimecmp register. Lower 32 bit for Timer time compare register</td></tr>
<tr><td>0x400</td><td>TIMER_CNT_L</td><td>Higher 32 bit for Timer time compare register</td></tr>
</table>

2.3. Signal Description

Table 2.4 to Table 2.7 list the ports of the CPU soft IP in different categories.

2.3.1. Clock and Reset

Table 2.4. Clock and Reset Port

Name	Type	Width	Description
CLK	In	1	RISC-V soft IP clock
RESETN	In	1	Global reset (active high)
SYSTEM_RESETN	Out	1	Combined Global reset and Debug Reset from JTAG

2.3.2. Instruction and Data Interface

Table 2.5. Instruction Port

Name	Type	Width	Description
INSR_HADDR	Out	32	—
INSR_HWRITE	Out	1	Fixed to 1'b0
INSR_HSIZE	Out	3	Fixed to 3'b010
INSR_HPROT	Out	1	Fixed to 4'b1110
INSR_HTRANS	Out	2	—
INSR_HBURST	Out	3	Fixed to 3'b000
INSR_HMASTLOCK	Out	1	Fixed to 1'b0
INSR_HWDATA	Out	32	—
INSR_HRDATA	In	32	—
INSR_HREADY	In	1	—
INSR_HRESP	In	1	—

Table 2.6. Data Port

Name	Type	Width	Description
DATA_HADDR	Out	32	—
DATA_HWRITE	Out	1	—
DATA_HSIZE	Out	3	—
DATA_HPROT	Out	1	Fixed to 4'b1111
DATA_HTRANS	Out	2	—
DATA_HBURST	Out	3	Fixed to 3'b000
DATA_HMASTLOCK	Out	1	—
DATA_HSEL	Out	1	—
DATA_HWDATA	Out	32	—
DATA_HRDATA	In	32	—
DATA_HREADY	In	1	—

Refer to AMBA 3 AHB-Lite Protocol V1.0 for more information.

2.3.3. Interrupt interface

Table 2.7. Interrupt Port

Name	Type	Width	Description
IRQ	In	1~8	Peripheral interrupts
TIMER_IRQ_OUT	Out	1	Timer interrupt , exist only when “TIMER_ENABLE” checked
TIMER_IRQ_IN	In	1	Timer interrupt, exist only when “TIMER_ENABLE” unchecked

2.4. Attribute Summary

The configurable attributes of the RISC-V MC CPU IP are shown in Table 2.8 and are described in Table 2.9.
The attributes can be configured through the Propel Builder software.

Table 2.8. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
SIMULATION	Checked, Unchecked	UnChecked	—
DEBUG_ENABLE	Checked, Unchecked	UnChecked	—
TIMER_ENABLE	Checked, Unchecked	UnChecked	—
PIC_ENABLE	Checked, Unchecked	UnChecked	—
PICTIMER_START_ADDR	0~0xFFFFFE00	0xFFFF0000	Enabled when PIC_ENABLE or TIMER_ENABLE
IRQ_NUM	2~8	8	Enabled when PIC_ENABLE
PFR_OPT	Checked, Unchecked	—	—

Table 2.9. Attributes Description

Attribute	Description
SIMULATION	1: simulation mode for CPU 0: synthesis mode for CPU
DEBUG_ENABLE	1: debug function enable 0: debug function disable
TIMER_ENABLE	1: timer enable 0: timer disable
PIC_ENABLE	1: pic enable 0: pic disable
PICTIMER_START_ADDR	Start address of PIC and Timer
IRQ_NUM	Interrupt number for peripherals
PFR_OPT	Area optimization for LUTs saving for PFR system

3. RISC-V MC CPU IP Generation

This section provides information on how to generate the CPU IP Core module using Propel Builder.

To generate the CPU IP Core module:

1. In Propel Builder, select the CPU package.
2. Enter the module name.
3. Click **Next**. In the example shown in Figure 3.1, the *RISCVSMALL_PACKAGE* is selected.

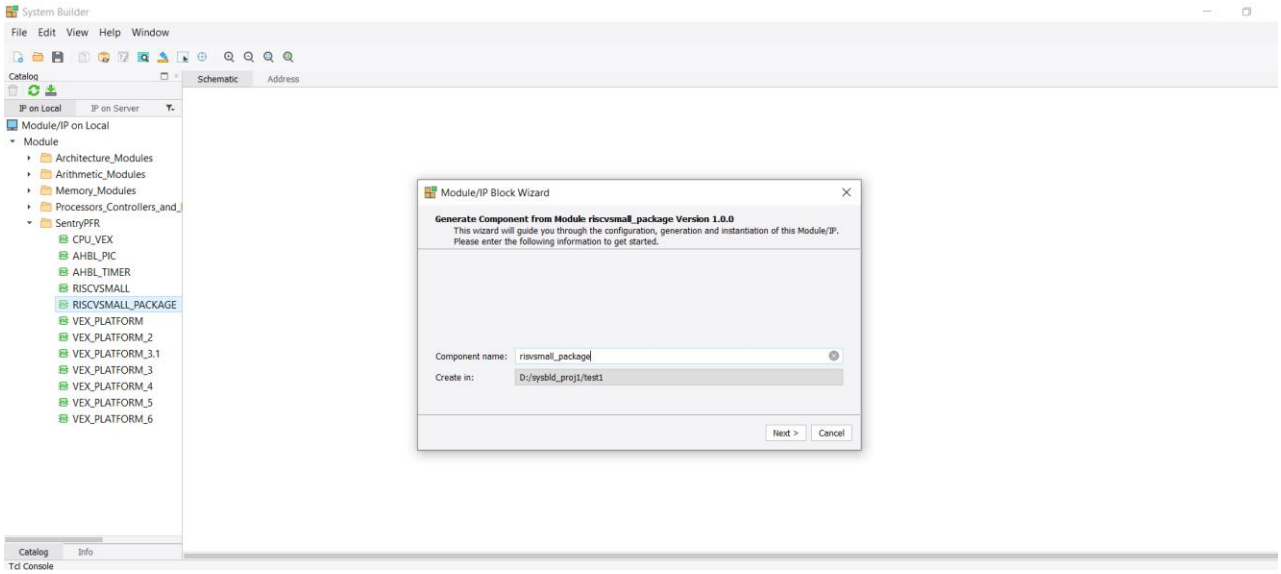

Figure 3.1. Selecting the Package

4. Configure the parameters as needed.
5. Click **Generate**.

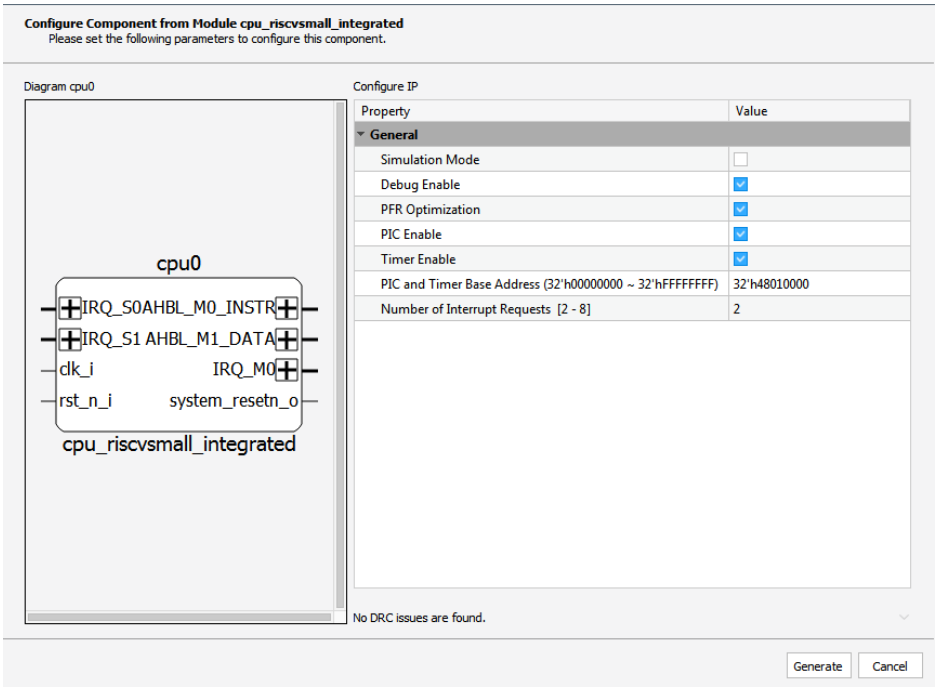

Figure 3.2. Generating the Package

6. Verify the information and click **Finish**.

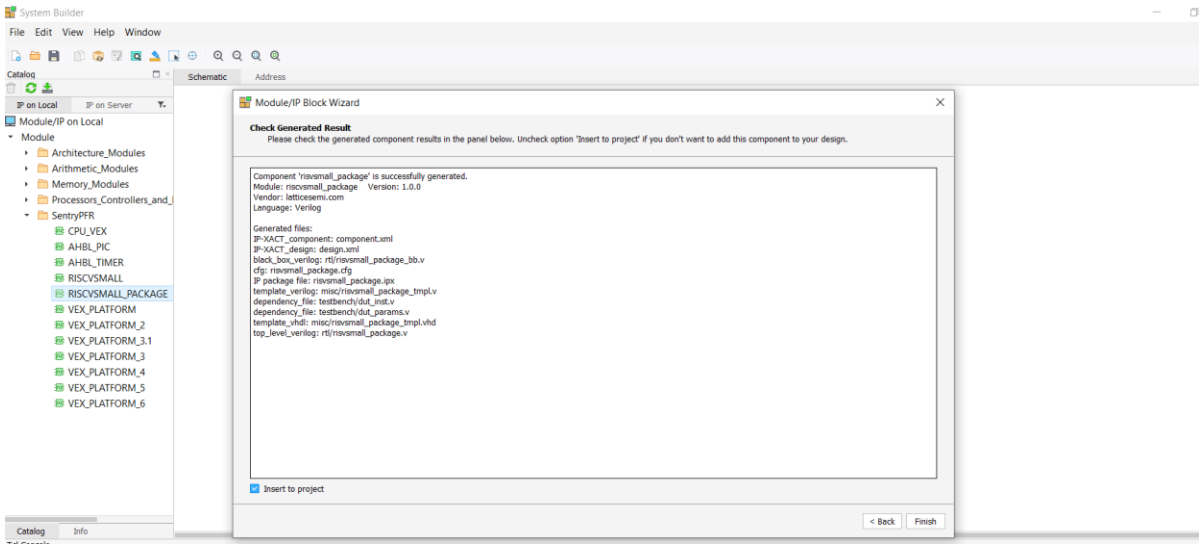

Figure 3.3. Verifying the Result

7. Enter the instance name.
8. Click **OK**.

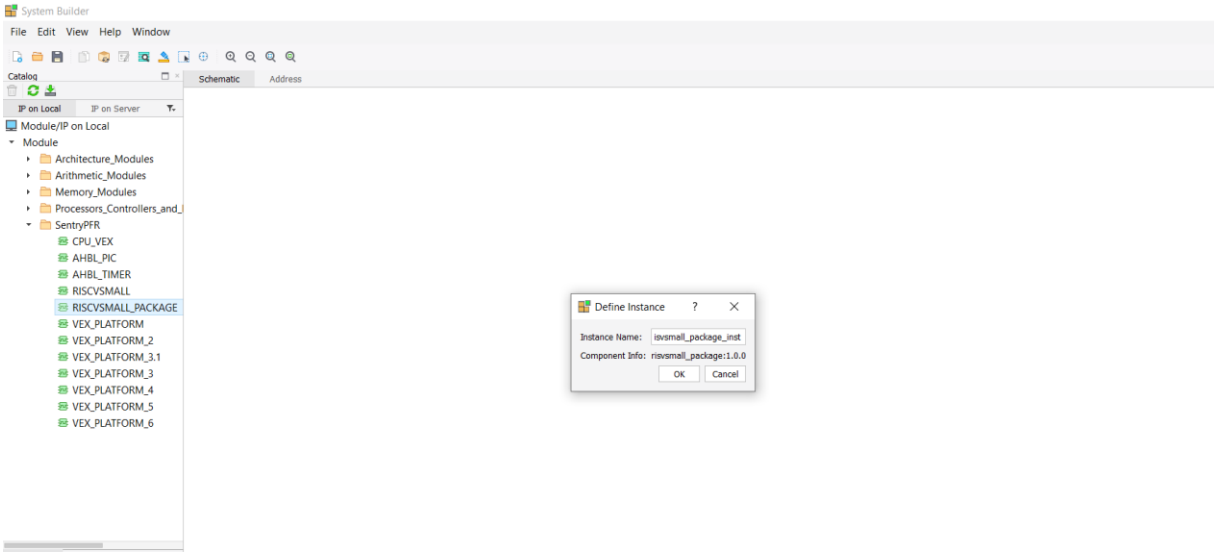

Figure 3.4. Specifying the Instance

The CPU IP instance is successfully generated.

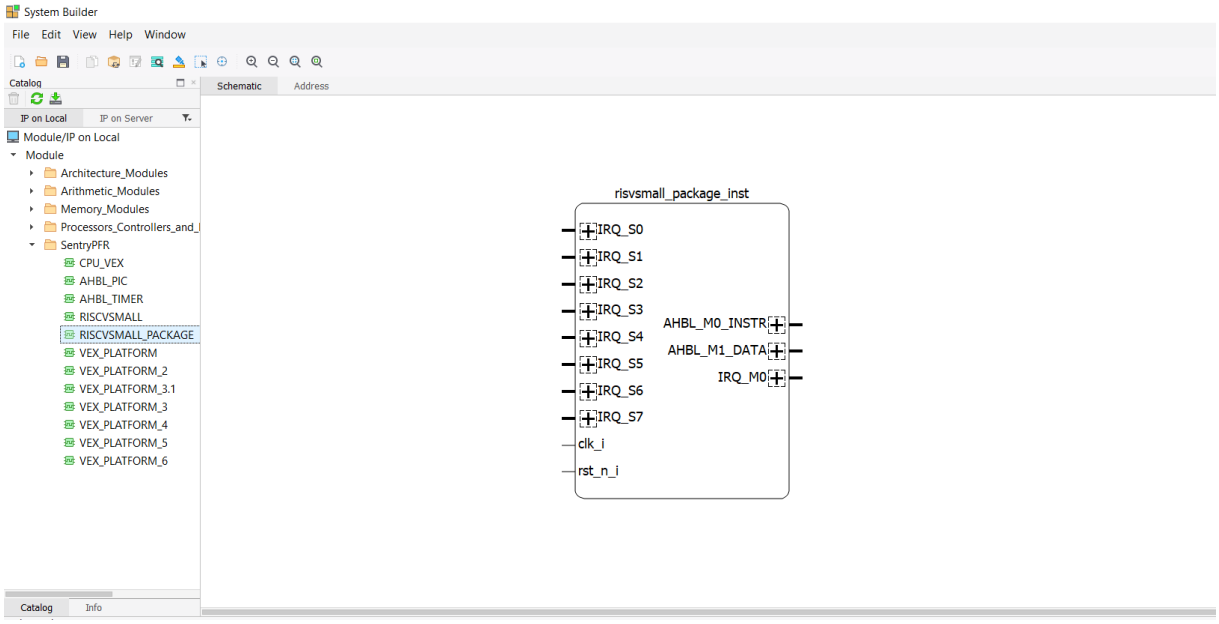

Figure 3.5. Generated Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in MachXO3D

Configuration	Slices	LUTs	Registers	sysMEM EBRs
Processor core only (without debug)	1376	2240	897	0
Processor core only	1699	2599	1257	0
Processor core + PIC	1782	2721	1294	0
Processor core + Timer	2018	3091	1423	0
Processor core + PIC + Timer	2043	3112	1437	0
Processor core only (PFR OPT , without debug)	1097	1645	772	4
Processor core only (PFR OPT)	1425	1993	1142	4
Processor core + PIC (PFR OPT)	1475	2051	1150	4
Processor core + Timer (PFR OPT)	1747	2488	1276	4
Processor core + PIC + Timer(PFR OPT)	1768	2506	1284	4

Note: Resource utilization characteristics are generated using Lattice Diamond software.

References

- MachXO3D FPGA Web Page in latticesemi.com
- Lattice Propel 1.0 User Guide
- Lattice Diamond Software 3.11 User Guide
- AMBA 3 AHB-Lite Protocol V1.0
- RISC-V Privileged Specification (20190608)
- RISC-V Instruction Set Manual (20190608)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.

www.latticesemi.com