Lattice Sentry Embedded Security Block Mux IP Core for MachXO3D - Lattice Propel Builder

User Guide

FPGA-IPUG-02107-1.0

May 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advance Peripheral Bus
ASF	Asynchronous FIFO
CPU	Central Processing Unit
ESB	Embedded Security Block
FIFO	First-In, First-Out
HSP	High Speed Port
PFR	Platform Firmware Resiliency
RISC-V	Reduced Instruction Set Computer-V (five)
SHA	Secure Hashing Algorithm

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1. Introduction

This document describes how to select between the two available logical interfaces of the MachXO3D™ Embedded Security Block (ESB). The ESB has two logical interfaces for sending and receiving data: a WISHBONE register interface and a High Speed Data Port (HSP) FIFO-style interface. These two logical interfaces share one physical data interface with the ESB (one shared 32-bit input port and one shared 32-bit output data port). The WISHBONE interface of the ESB is converted to an APB (Advance Peripheral Bus) interface for RISC-V CPU access.

The design is implemented in Verilog HDL. It can be configured and generated using Lattice Propel™ Builder. It can be targeted to MachXO3D FPGA devices and implemented using the Lattice Diamond® software Place and Route tool integrated with the Synplify Pro® synthesis tool.

1.1. Features

The key features of the ESB Mux IP include:

- Soft wrapper around the ESB to provide separate APB and high-speed port interfaces to user logic
- Support *for* AMBA 3 APB Protocol v1.0

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1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

1.2.3. Host

The logic unit inside the FPGA interacts with the ESB Mux IP through APB.

1.2.4. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

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2. Functional Description

The ESB Mux is a thin wrapper around the ESB, which converts the WISHBONE interface of the ESB to an APB interface. It also provides separate interface ports for the APB and the HSP plus an internal Mux to select between the two. The Mux is controlled by a control register, which is mapped into unused ESB address space. This register is always available through the APB interface, regardless of whether the Mux is set to APB or HSP. When the Mux is set to APB, the external read FIFO status is forced to empty (ASFEMPTYO=1) and FIFO read requests (ASFRDI) are ignored to prevent external logic from initiating FIFO reads, which could cause data conflicts with APB.

2.1. Block Diagram

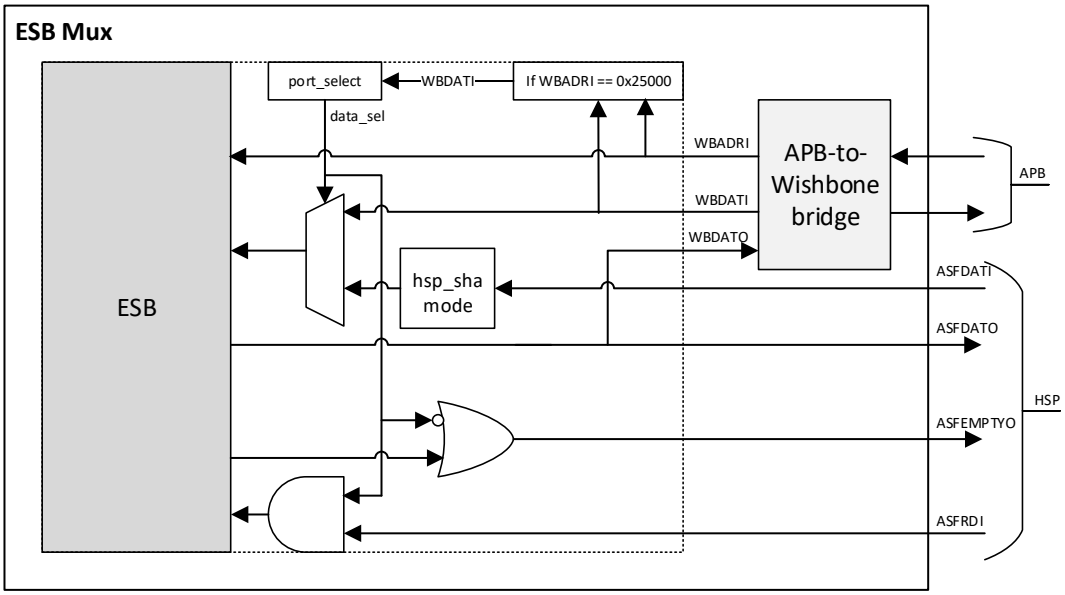

Figure 2.1. ESB Mux Block Diagram

The block diagram for a typical application is demonstrated in Figure 2.2.

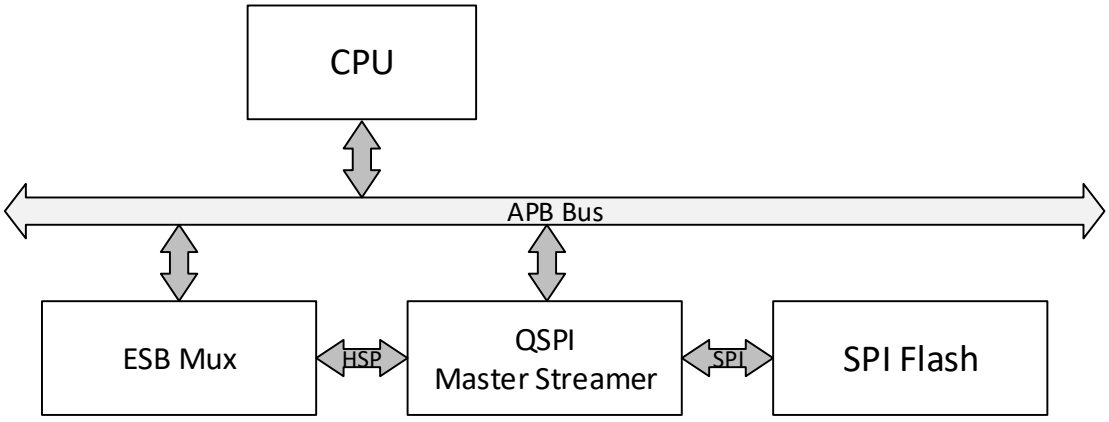

Figure 2.2. ESB Mux in a Typical Application

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2.2. Signal Description

The ESB Mux includes all of the interface ports of the ESBA primitive, with the addition of asf_dat_i[31:0] and asf_dat_o[31:0].

Table 2.1. ESB Mux Signal Description

Port	Width	Direction	Description
System			
reset_n_i	In	1	System Asynchronous Reset
apb_pclk_i	In	1	APB clock
asf_clk_i	In	1	HSP clock
esb_clk_i	In	1	ESB clock; Oscillator input.
APB Interface			
apb_psel_i	In	1	Select signal Indicates that the slave device is selected and a data transfer is required.
apb_paddr_i	In	32	Address signal
apb_pwdata_i	In	32	Write data signal
apb_pwrite_i	In	1	Direction signal Write = 1, Read = 0
apb_penable_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_pready_o	Out	1	Ready signal Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_prdata_o	Out	32	Read data signal
HSP Interface			
asf_dat_i	In	32	HSP Write Data: 32-bit wide input data to write into the ESB FIFO
asf_dat_o	Out	32	HSP Read Data: 32-bit wide output data read from the ESB FIFO
asf_full_o	Out	1	FIFO full status
asf_empty_o	Out	1	FIFO empty status
asf_wr_i	In	1	Write enable
asf_rd_i	In	1	Read enable

2.3. Attribute Summary

The ESB Mux has no RTL parameters for configuring the IP at instantiation time.

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2.4. Register Description

ESB registers are mapped to offsets 0x00000-0x24FFF, and the ESB Mux port_select register is mapped to offset 0x25000.

Table 2.2. Summary of ESB Mux IP Core Registers

Offset	Name	Access	Default Value	Description
0x00000-0x24FFF	ESB registers	—	—	Refer to the MachXO3D Embedded Security Block (FPGA-TN-02091) technical note. To obtain a copy of this document, create a new Technical Support Request through http://www.latticesemi.com/Support and indicate the following: Case Type: Documentation Case Category: App Note/Tech Note Product Family: MachXO3D
0x25000	PORT_SELECT	RW	0	data_sel[0]: • 0 – APB bus • 1 – HSP hsp_sha_mode[1]: • 0 – Data on ASFDATI is for non-SHA operations. • 1 – Data on ASFDATI is for SHA operations.

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3. Ordering Part Number

The Ordering Part Number (OPN) for the Lattice Sentry™ Embedded Security Block Mux IP Core targeting MachXO3D FPGA devices are the following:

- ESBMUX-M3D-U – Project License
- ESBMUX-M3D-UT – Site License

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References

- MachXO3D FPGA Web Page in latticesemi.com
- Lattice Propel 1.0 User Guide
- Lattice Diamond Software 3.11 User Guide

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Revision History

Revision 1.0, May 2020

Section	Change Summary
All	Initial release

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