Lattice Sentry PLD Interface IP Core - Lattice Propel Builder

User Guide

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
AHB-lite	Advanced High-performance Bus - lite
CPU	Central Processing Unit
FPGA	Field-Programmable Gate Array
PLD	Programmable Logic Device
RTL	Register Transfer Language

1. Introduction

The Lattice Semiconductor Customer Programmable Logic Device (PLD) Interface IP implements a register interface, which is used by firmware to send and receive messages to and from the customer's control PLD logic to request system control actions and check status. This user guide defines the hardware and register interface for the firmware and the hardware interface to the customer's logic.

The design is implemented in Verilog HDL. The IP can be configured and generated based on Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
MachXO2™	Lattice Propel™ Builder software	Lattice Diamond® software
MachXO3™	Lattice Propel Builder software	Lattice Diamond software
MachXO3D™	Lattice Propel Builder software	Lattice Diamond software
Mach™-NX	Lattice Propel Builder software	Lattice Diamond software
CrossLink™-NX	Lattice Propel Builder software	Lattice Radiant™ software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the Lattice Sentry Customer PLD IP are:

- Implements a bidirectional mailbox mechanism for sending small (8-bit) messages to the customer PLD logic and receiving messages from the customer PLD logic
- Supports either AMBA 3 APB Protocol v1.0 or AHB-lite Protocol for CPU access

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

1.2.3. Host

The logic unit inside the FPGA interacts with the Customer PLD Interface IP through APB or AHB-lite.

1.2.4. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

The Lattice Semiconductor Customer PLD Interface IP implements a simple mailbox-style message passing mechanism for two-way communication between firmware and the customer PLD Logic. When one side wants to communicate with the other side, the sender writes a message into the corresponding mailbox and sets a flag to indicate that the message is valid. The receiver acknowledges that it has received the message by clearing the valid flag. If the message is a request for action, the receiver performs the action and then sends a return message with the status of the action (success, error, and others) through the mailbox.

2.1. Block Diagram

The Lattice Semiconductor Customer PLD Interface IP block diagram for a typical application is shown in Figure 2.1.

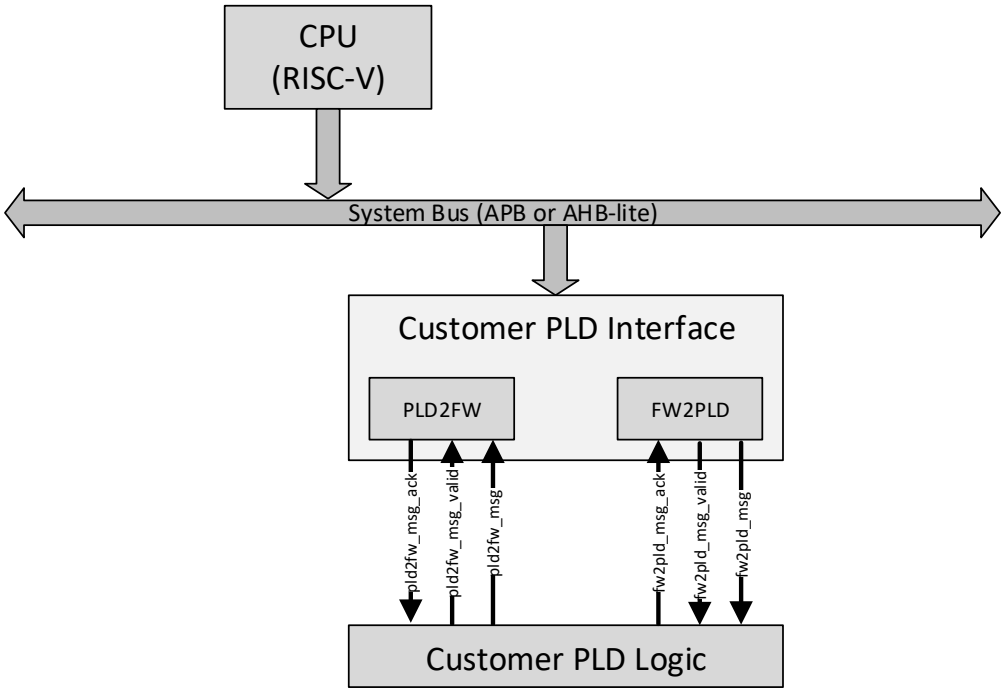

Figure 2.1. Customer PLD Interface IP Module

2.2. Pin Diagram

The interface or pin diagram of the Customer PLD Interface IP is shown in Figure 2.2. The descriptions for the inputs and outputs are shown in Table 2.1.

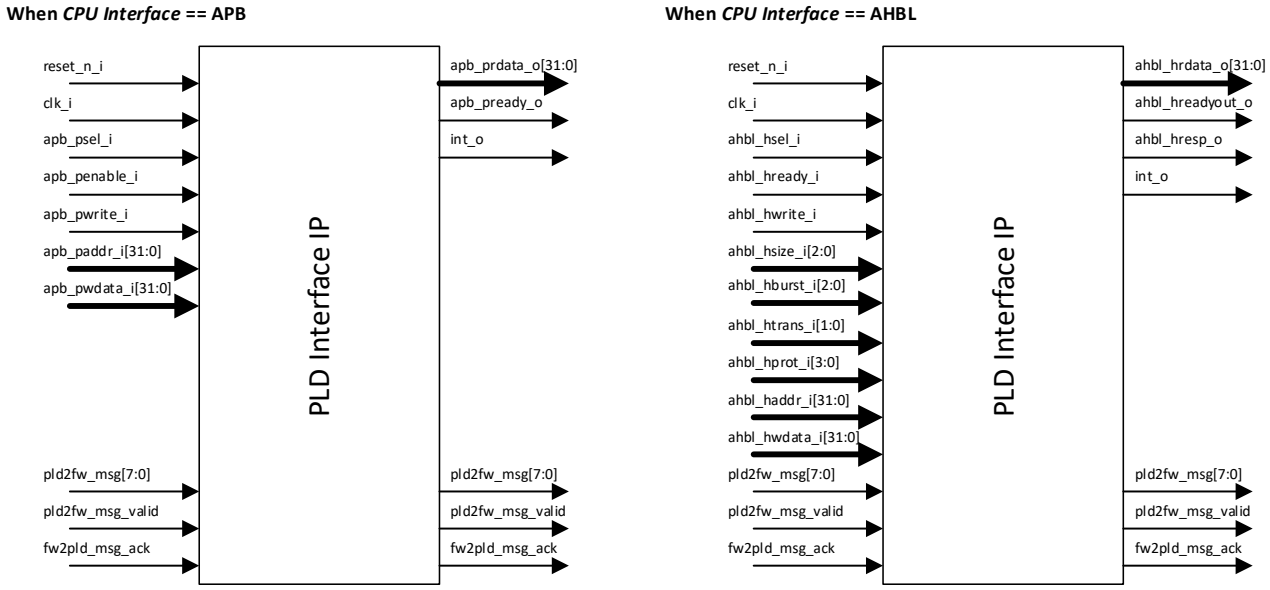

Figure 2.2. Customer PLD Interface Pin Diagram

2.3. Signal Description

Table 2.1. Customer PLD Interface IP Core Signal Description

Port	Width	Direction	Description
System			
reset_n_i	1	Input	Asynchronous reset Active Low
clk_i	1	Input	Master clock input
int_o	1	Output	Interrupt request
APB (*CPU Interface == APB*)			
apb_psel_i	1	Input	Select signal Indicates that the slave device is selected and a data transfer is required.
apb_paddr_i	32	Input	Address signal.
apb_pwdata_i	32	Input	Write data signal.
apb_pwrite_i	1	Input	Direction signal Write = 1, Read = 0
apb_penable_i	1	Input	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_pready_o	1	Output	Ready signal Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_prdata_o	32	Output	Read data signal
AHB-lite *(CPU Interface == AHBL)*			
ahbl_hsel_i	1	Input	Select signal Indicates the device is selected and transder is required.
ahbl_hready_i	1	Input	Ready input signal Indicates data phase of previous transfer is completed.
ahbl_haddr_i	32	Input	Address signal.
ahbl_burst_i	3	Input	Burst Type signal This signal is unused.
ahbl_hsize_i	3	Input	Transfer Size signal Indicates the size of the transfer that is a byte, halfword or word.
ahbl_hprot_i	4	Input	Protection Control signal This signal is unused.
ahbl_htrans_i	2	Input	Transfer Type signal Indicates the transfer type of the current transfer.
ahbl_hwrite_i	1	Input	Direction signal Write = High, Read = Low.
ahbl_hwdata_i	32	Input	Write Data signal
ahbl_hreadyout_o	1	Output	Ready Output signal Indicates transfer completion. Reset value is 1'b1.
ahbl_hrdata_o	32	Output	AHB-Lite Read Data signal Reset value is 0.
ahbl_hresp_o	1	Output	AHB-Lite Transfer Response signal This signal is tied to 1'b0.
PLD Interface			
fw2pld_msg	8	Output	Firmware to PLD message
fw2pld_msg_valid	1	Output	Firmware to PLD message valid
fw2pld_msg_ack	1	Input	Firmware to PLD message acknowledge, which should be synchronous to the clk_i clock domain
pld2fw_msg	8	Input	PLD to firmware message

Port	Width	Direction	Description
pld2fw_msg_valid	1	Input	PLD to firmware message valid, which should be synchronous to the clk_i clock domain.
Pld2fw_msg_ack	1	Output	PLD to firmware message acknowledge

2.4. Attribute Summary

The Customer PLD Interface IP's configurable attributes are shown in Table 2.2 and Table 2.3.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
CPU Interface	"AHBL", "APB"	AHBL	—

Table 2.3. Attribute Description

Parameter	Description
General	
CPU Interface	Selects the interface for register access by the host.

2.5. Register Description

The register map of the Customer PLD Interface IP core is shown in the Table 2.4.

Table 2.4. Summary of Customer PLD Interface IP Core Registers

Offset	Name	Access	Default Value	Description
0x00	FW2PLD_MSG	RW	0	fw2pld_msg [7:0] – Message to send to PLD fw2pld_valid [8] – Write 1 to send message to PLD. Bit is reset to 0 when PLD acknowledges receiving the message. Reserved[31:9]
0x04	PLD2FW_MSG	RW	0	pld2fw_msg [7:0] – Message received from PLD pld2fw_valid [8] – Set to 1 when a new message has been received from the PLD. Bit is reset to 0 when pld2fw_recvd_int interrupt is cleared. Reserved[31:9]
0x10	INT_STATUS	RW	0	Interrupt Status: fw2pld_sent_int [0] – Message Sent to PLD interrupt. Triggered when message is acknowledged by PLD. pld2fw_recvd_int [1] – Message Received from PLD interrupt. Clearing this interrupt triggers message acknowledgement to the PLD. Reserved[31:3] Writing 1 to a bit clears that interrupt
0x14	INT_ENABLE	RW	0	Interrupt Enable: fw2pld_sent_en [0] – Enable Message Sent to PLD interrupt. pld2fw_recvd_en [1] – Enable Message Received from PLD interrupt. Reserved[31:3]
0x18	INT_SET	RW	0	Interrupt Set: fw2pld_sent_set[0] – Set Message Sent to PLD interrupt pld2fw_recvd_set [1] – Set Message Received from PLD interrupt. Reserved[31:3] Writing 1 to a bit sets that interrupt

2.6. Message Definitions

The content and meaning of the messages that are sent between firmware and the Customer PLD logic are determined by the firmware and PLD logic developer. These are not defined in this document.

2.7. Hardware Interface to Customer PLD Logic

The hardware interface to the Customer PLD logic consists of two sets of ports: firmware to PLD (fw2pld) and PLD to firmware (pld2fw). Each set of ports provides xxx_msg[7:0] and xxx_msg_valid signals in one direction and an xxx_msg_ack (acknowledge) signal in the other direction. To send a message, set xxx_msg[7:0] and assert the xxx_msg_valid signal until xxx_msg_ack is asserted after one or more clock cycles. Once xxx_msg_ack is asserted, xxx_msg_valid is de-asserted and xxx_msg [7:0] is undefined. Only one message can be sent at a time. It is your responsibility to wait until a message has been acknowledged before sending the next message. All signals are synchronous and are sampled on the positive edge of the clock. If some or all of the Customer PLD logic is implemented in a different clock domain, it is the Customer PLD logic's responsibility to properly synchronize signals crossing the clock domain boundary in both directions.

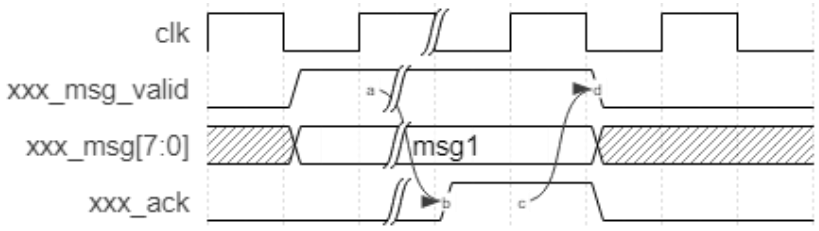

Figure 2.3. Customer PLD Interface Waveform

2.8. Communication Sequence

As shown in Figure 2.4, this sequence diagram illustrates the typical message sequence between firmware and the Customer PLD logic.

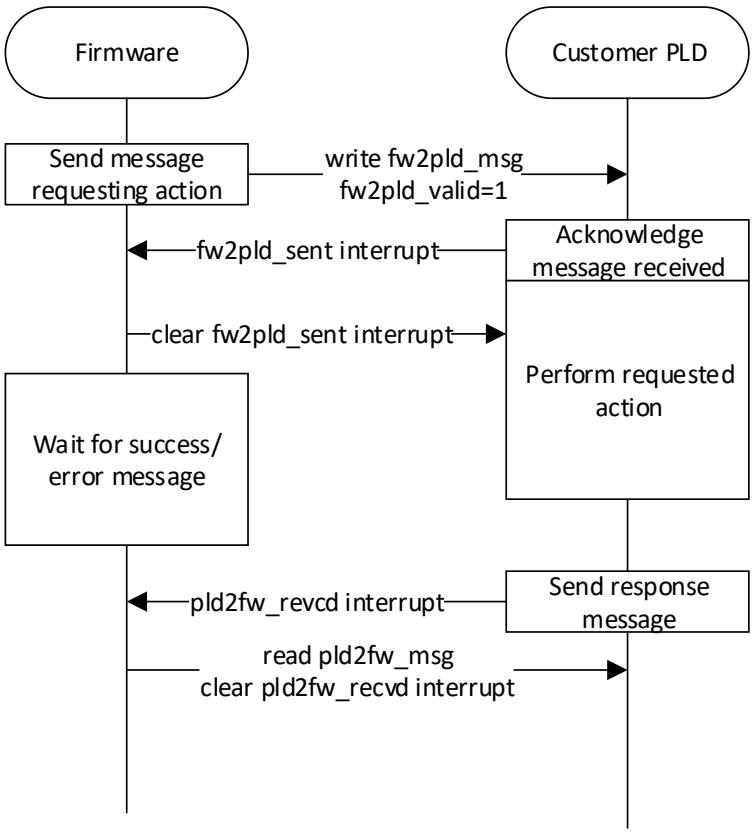

Figure 2.4. Example Message Sequence

References

- MachXO2 Web Page at www.latticesemi.com
- MachXO3 Web Page at www.latticesemi.com
- MachXO3D FPGA Web Page in latticesemi.com
- Mach-NX FPGA Web Page in latticesemi.com
- CrossLink-NX Web Page in latticesemi.com
- Certus-NX Web Page in latticesemi.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, April 2021

Section	Change Summary
Introduction	Updated Table 1.1 to add support for MachXO2 and MachXO3.
References	Added references to MachXO2 and MachXO3.

Revision 1.1, November 2020

Section	Change Summary
All	Changed document name from Lattice Sentry PLD Interface IP Core for MachXO3D – Lattice Propel Builder to *Lattice Sentry PLD Interface IP Core - Lattice Propel Builder*.
Introduction	• Added AHB-Lite support in Features and Host section. • Added Table 1.1.
Functional Description	• Updated Figure 2.1 and Figure 2.2. • Updated Table 2.1 and Table 2.2.
References	Updated content to remove reference links for Lattice Propel and Lattice Diamond user guide; and to add reference links for Mach-NX, CrossLink-NX and Certus-NX web page.

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.

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