EVDK GigE Vision Demo

User Guide

FPGA-UG-02100-1.0

February 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
USB	Universal Serial Bus
GbE	Gigabit Ethernet
I^2C	Inter-Integrated Circuit
LDO	Low Dropout
LED	Light-emitting Diode
LVDS	Low-Voltage Differential Signaling
SPI	Serial Peripheral Interface
VIP	Video Interface Platform

1. Introduction

This document describes the design and setup procedure for the Lattice Embedded Vision Development Kit (EVDK) and the USB3-Gbe VIP I/O Board to demonstrate GigE Vision. GigE Vision is a global camera interface standard for high-performance industrial cameras, which provides a framework for transmitting high-speed video and related control data over Ethernet networks.

1.1. Functional Description

Figure 1.1 shows the top-level diagram of the Helion GigE Vision application. The single camera Mobile Industry Processing Interface (MIPI®) CSI-2 to Gbe demo uses a Sony IMX214 camera to output 1080p video over four MIPI data lanes, each running at 371.25 Mb/s. The CrossLink™ Video Interface Platform (VIP) Input Bridge Board receives the MIPI video stream from the onboard camera sensor and extracts the video pixels. These video pixels from two cameras are merged side-by-side and the combined image data is transmitted to ECP5™ in the form of parallel CMOS interface on the ECP5 video processor board through board-to-board connectors.

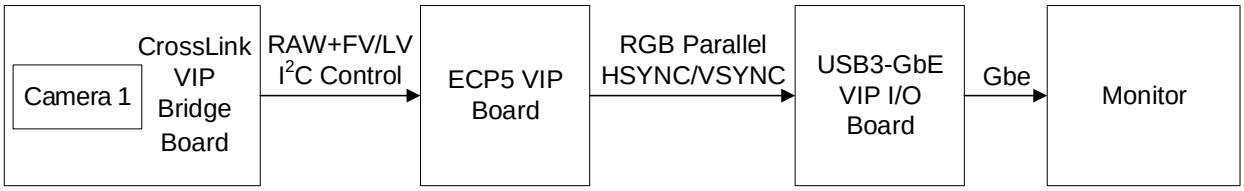

Figure 1.1. 2:1 MIPI CSI-2 to Gbe Bridge System Diagram

The ECP5 FPGA processes the sensor image and sends processed parallel image data to TI DP83867IR Gigabit Ethernet PHY. The data is then transmitted through the RJ45 connector with 10/100/1000 Ethernet speed support, which are in the USB3-Gbe VIP I/O Board. Refer to Figure 1.2.

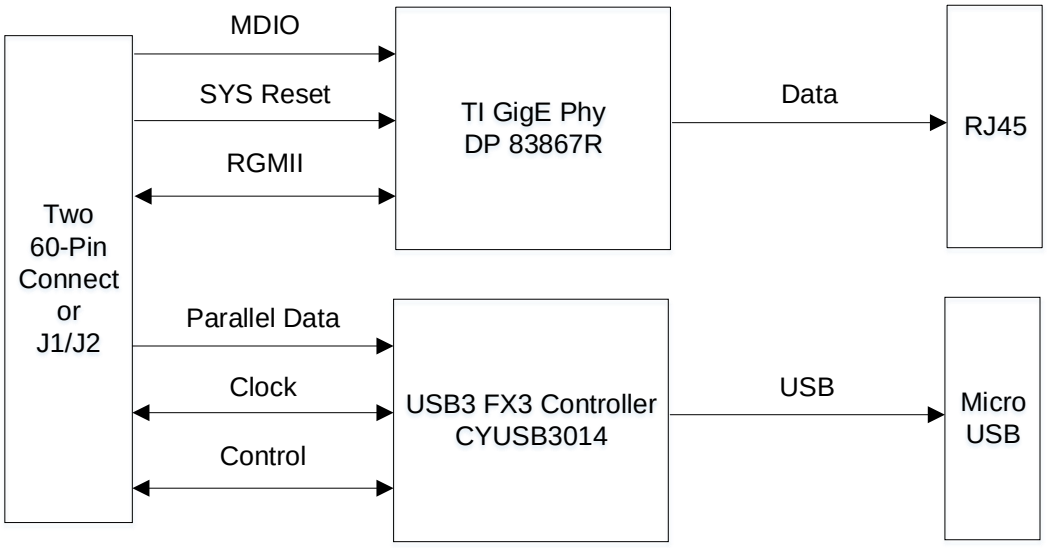

Figure 1.2. 2:1 MIPI CSI-2 to Gbe Bridge System Diagram

1.2. Hardware Requirements

1.2.1. EVDK

Figure 1.3 and Figure 1.4 show the Embedded Vision Development Kit board configuration, which is designed as a stackable modular architecture with 80 mm × 80 mm form factor. The Embedded Vision Development Kit consists of three boards:

- CrossLink VIP Input Bridge Board
- ECP5 VIP Processor Board
- HDMI VIP Output Bridge Board

The figures shown in this document are part of Revision C of the Embedded Vision Development Kit. For more information on the Embedded Vision Development Kit, visit www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/EmbeddedVisionDevelopmentKit.aspx.

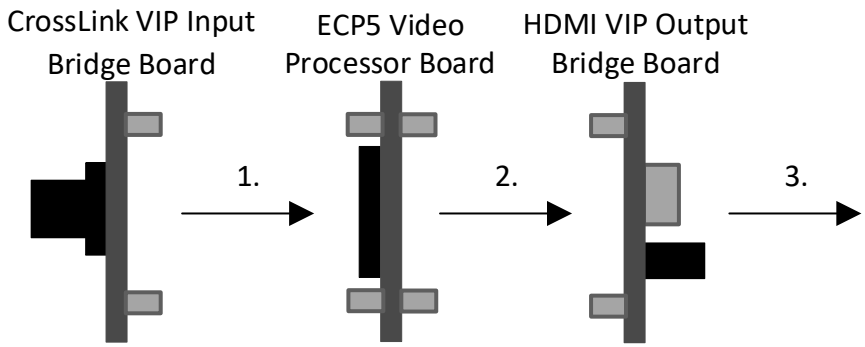

Figure 1.3. EVDK Default Board Configuration

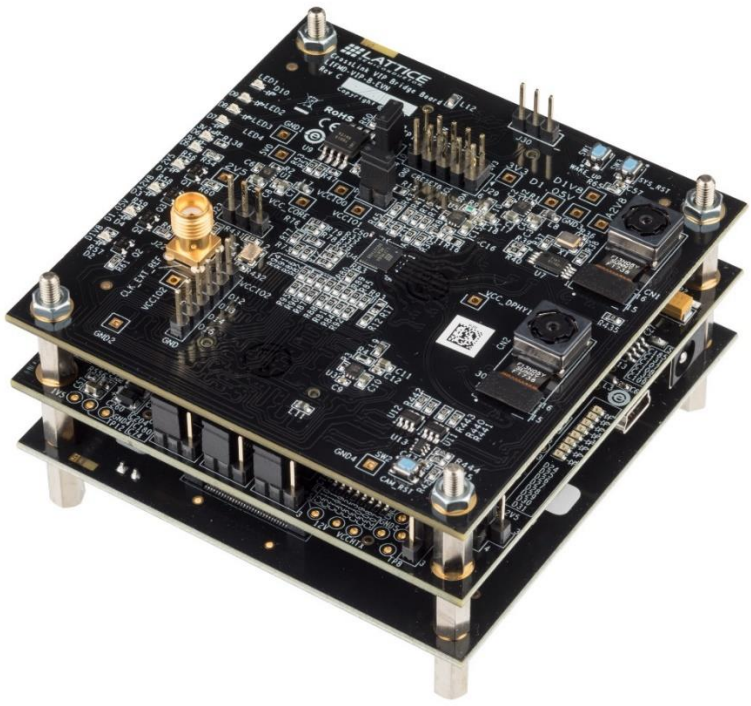

Figure 1.4. Embedded Vision Development Kit Rev C

1.2.2. USB3-GbE VIP IO Board

In addition to the Embedded Vision Development Kit, the following items are required to demonstrate GigE video streaming:

- USB3-GbE VIP IO Board
- Ethernet cable

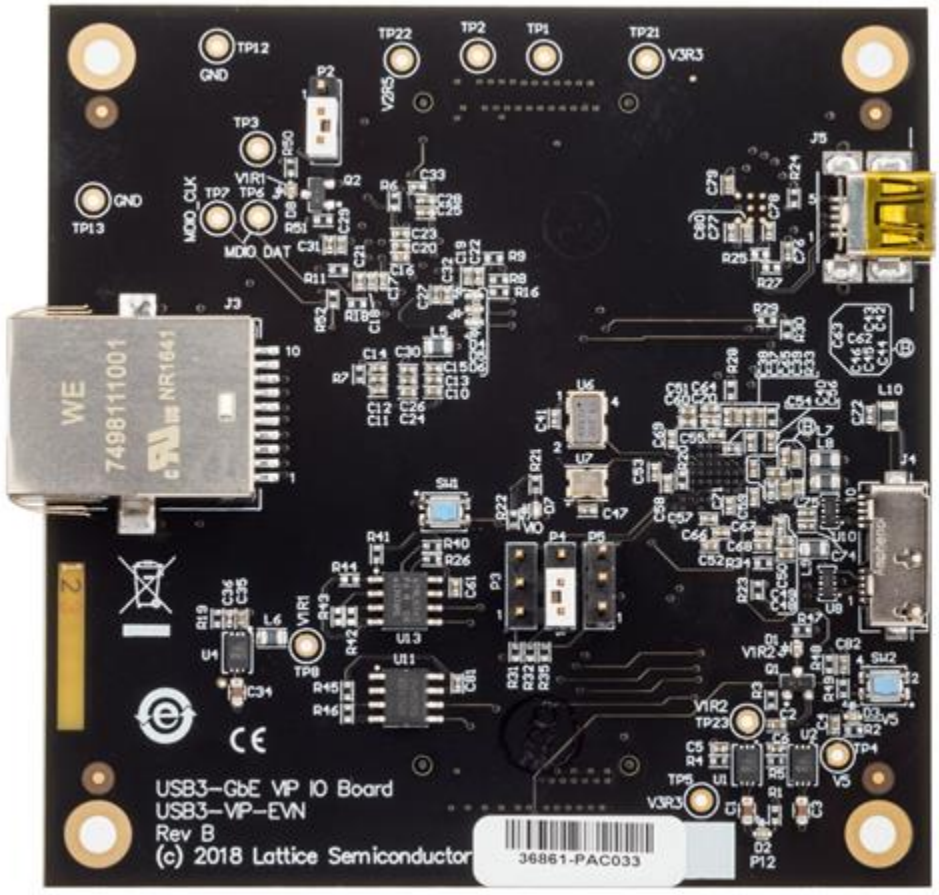

Figure 1.5. USB3-Gbe VIP IO Board Rev B

1.3. Software Requirements

Before proceeding with the demo board setup, download the following software:

- Windows 10 Operating System
- Lattice Diamond® Programmer v3.10 or later
- http://www.latticesemi.com/en/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond
- eBus Player Software
- https://go.pleora.com/Download-eBUS-Player
- http://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/USB3GBeVIPIOBoard

Note: This demo design is tested within the indicated specifications.

2. Demo Board Setup

To perform the GigE video streaming demo, replace the HDMI VIP Output Bridge Board with the USB3-GbE VIP IO Board, as shown in Figure 2.1.

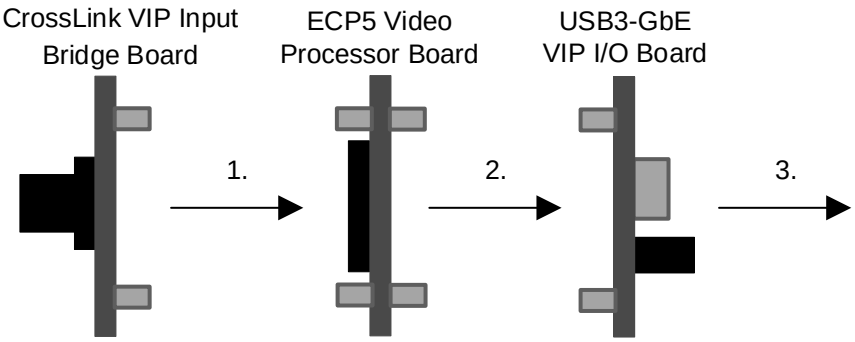

Figure 2.1. Required Board Configuration for the USB3 and GigE Video Streaming Demo

To configure the board:

1. Remove power from the EVDK.
2. Remove the HDMI VIP Output Bridge Board.
3. Install the USB3-GbE VIP IO Board.
   a. Connect J1 (60-pin) connector to J12 of the ECP5 VIP Processor Board.
   b. Connect J2 (60-pin) connector to J13 of the ECP5 VIP Processor Board.

   For pin information details, refer to High-Speed Connectors section of USB3-GigE VIP IO Board User Guide (FPGA-EB-02016).
4. Erase the SRAM and Flash of both the ECP5 device and the CrossLink device before proceeding.
   a. Erase the SRAM of the ECP5 and the CrossLink devices
   b. Erase SPI Flash of the ECP5 and the CrossLink devices
5. Power up the EVDK.
6. Program the SPI flash with the bitstream files as indicated in Table 2.1.

Table 2.1. Bitstream Files

Device	Bitstream file
ECP5UM	GE_Vision_ECP5.bit
CrossLink	GE_Vision_crosslink.bit

Note: For steps how to program, please refer to Demo Requirements and Appendix B section of Lattice Embedded Vision Development Kit (FPGA-UG-02015).

7. Remove power from the EVDK.
8. Plugin the Ethernet cable to J3.
9. Power up the EVDK.

3. Configuring and Running the GigE Video Streaming Demo

The GigE video streaming demo consists bit-streams for the ECP5 FPGA. This demo has its own bit-stream file for Ethernet. It is assumed that the board setup is configured with bitstream for CrossLink and ECP5 as illustrated in the Demo Board Setup section.

The following sections describe the demo.

3.1. Configuring the GigE Demo

To configure the GigE demo:

1. Ensure that you have a video viewer installed on your PC which supports GigE video streaming. This demo uses eBUS Player by Pleora Technologies, which is a Windows based video capture software. Any other software supporting GigE video streaming can be used.
2. Ensure that power is connected to the board.
3. Configure the network parameters of the destination PC with static IP address of 169.254.18.198 and subnet mask 255.255.0.0, as described in Appendix A. The default source IP address of the USB3-GigE VIP IO Board is hard coded in the RTL code to 169.254.0.2.

   Note: It is recommended to write down your original settings so you can restore your PC to its normal settings afterward.
4. Connect the Ethernet cable between the USB3-GigE VIP IO Board and the PC.

3.2. Running the GigE Demo

To set up the board for camera streaming:

1. Power cycle the EVDK
2. Press the reset button on the Crosslink board (SW3).

To set up the eBUS Player for camera streaming:

1. Turn off firewall of the computer.
2. Open the eBUS Player software.

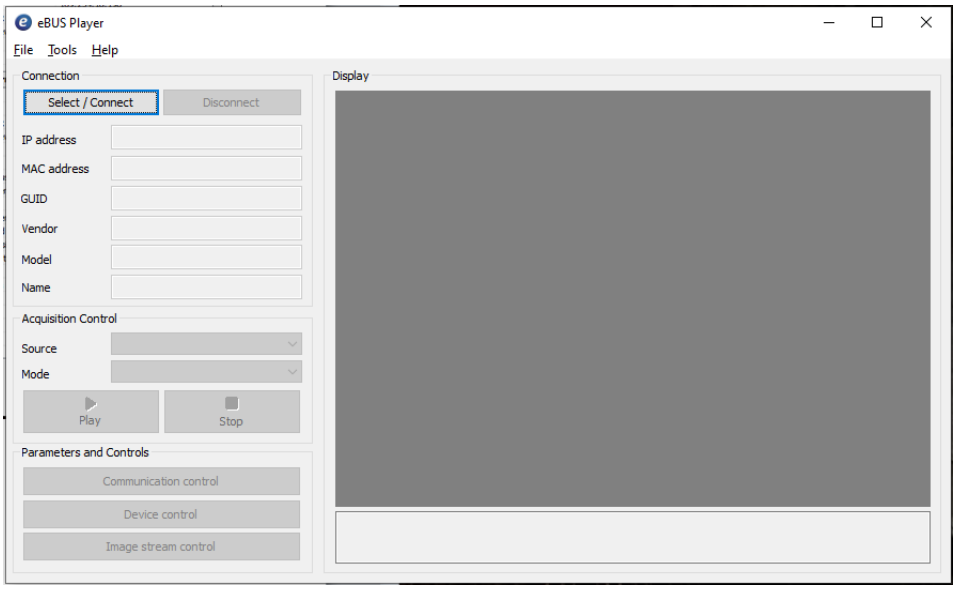

Figure 3.1. eBUS Player GUI

3. Click **Tools > Setup**.
4. Set the parameters as shown in Figure 3.2.

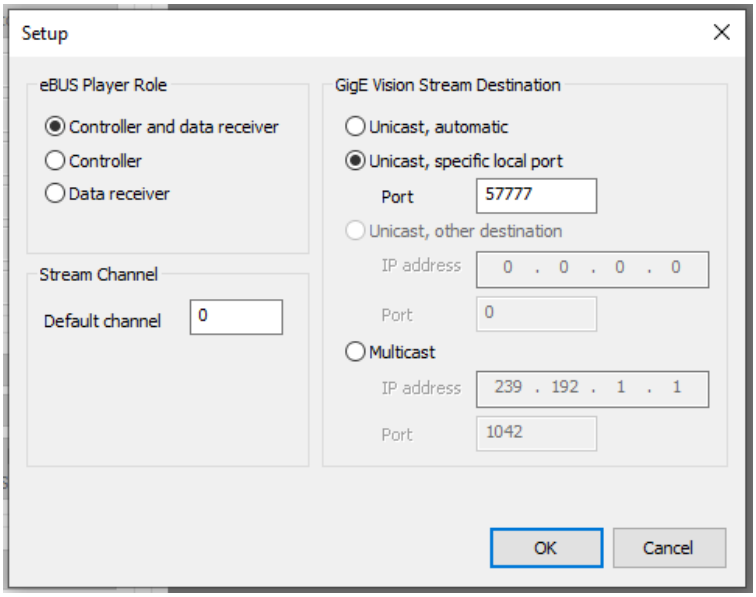

Figure 3.2. eBUS Player Setup Setting

5. Click **OK**.
6. Click **Tools > Buffer Options**.
7. Set the parameters shown in Figure 3.3.

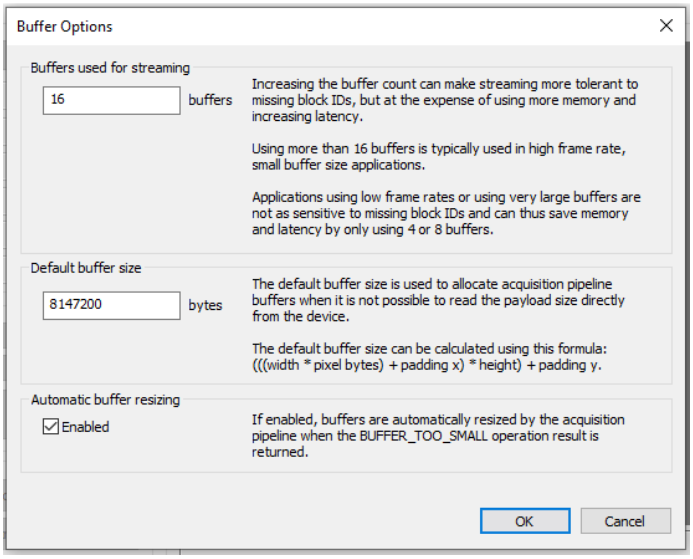

Figure 3.3. eBUS Player Buffer Options Setting

8. Click **OK**.
9. Click **Select/Connect**.
10. Select **AimValley Vizor IP**.

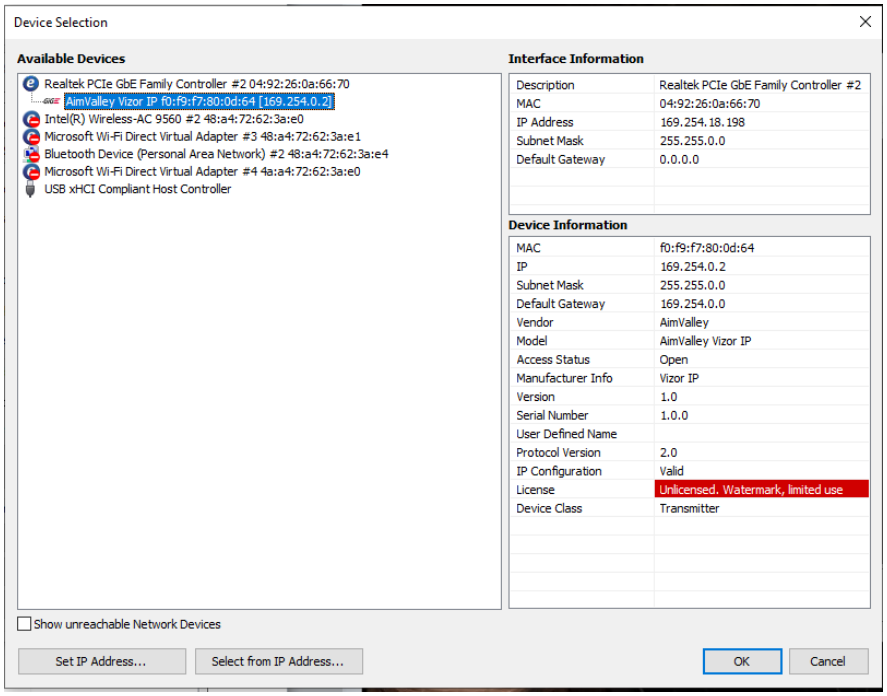

Figure 3.4. eBUS Player Buffer Options Setting

11. Click **OK**. The camera starts streaming.

Figure 3.5. eBUS Player Camera Streaming

12. Click **Image Stream Control** and set **Request Timeout** from **1000 to 100**. Note that this improves the fps.

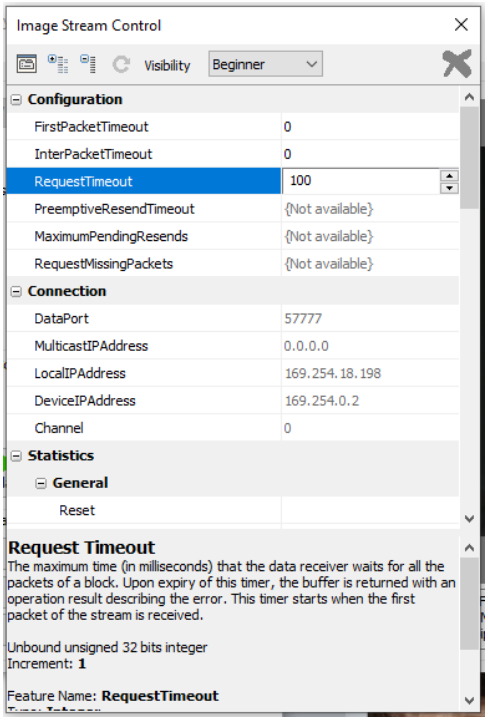

Figure 3.6. Image Stream Control

Appendix A. Changing Network Connection to Static IP Address

To change network connection to static IP address:

1. Select **Control Panel > Network and Sharing Center > Change Adapter Settings**.
2. Disconnect Wireless Connection.
3. Right-click **Local Area Connection** and select **Properties**.
4. Select **Internet Protocol Version 4 (TCP/IPv4)** and select **Properties**.

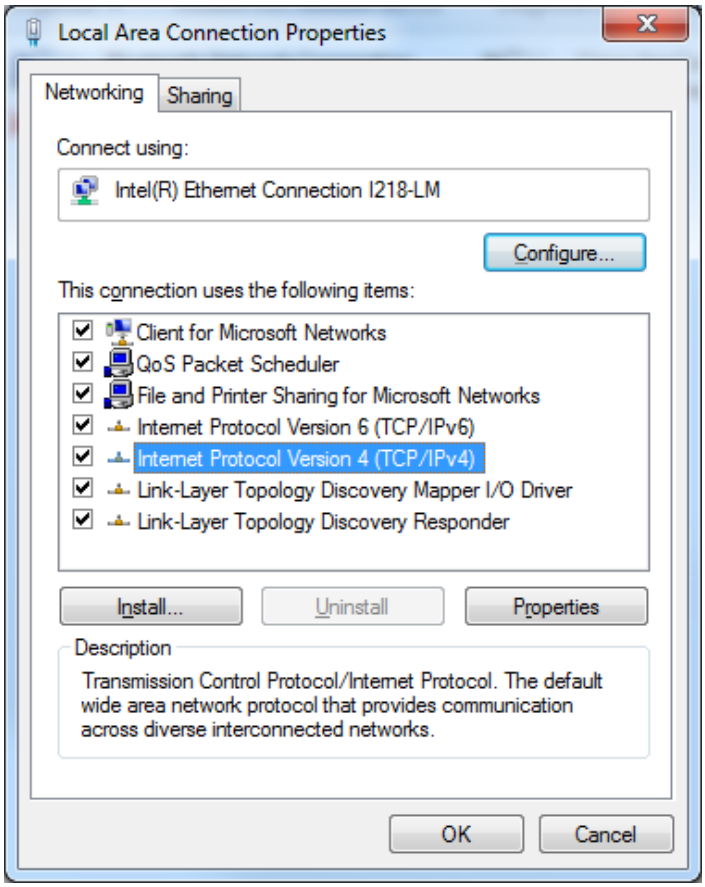

Figure A.1. Setting LAN Properties

5. Select **Use the following IP Address** and set the following values:
   - IP Address: 168.254.18.198
   - Subnet mask: 255.255.0.0

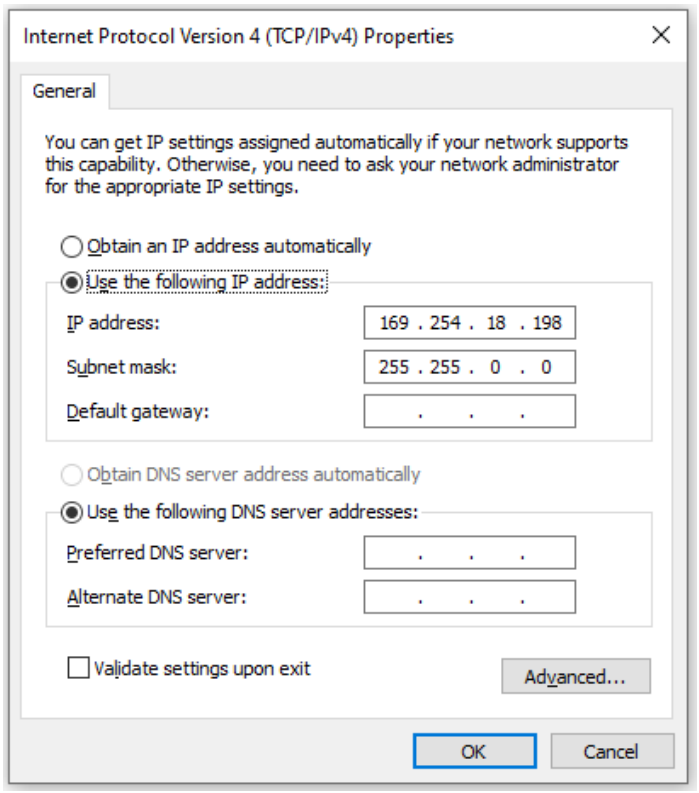

Figure A.2. Setting IP Address

6. Click **OK** to close **Internet Protocol Properties** window.
7. Click **OK** to close the **Local Area Connection** window.

References

For more information, refer to the following documents:

- For more information on boards and kits available for the VIP (Video Interface Platform) system visit www.latticesemi.com/vip.
- For more information on the Embedded Vision Development Kit, visit www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/EmbeddedVisionDevelopmentKit.aspx.
- For details on the Texas Instruments DP83867IR Gigabit Ethernet PHY, visit the Texas Instruments website at http://www.ti.com.
- Lattice Embedded Vision Development Kit User Guide (FPGA-UG-02015)
- For more information on the USB3-Gbe VIP IO Board, http://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/USB3GBeVIPIOBoard

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, February 2020

Section	Change Summary
All	Initial release.

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