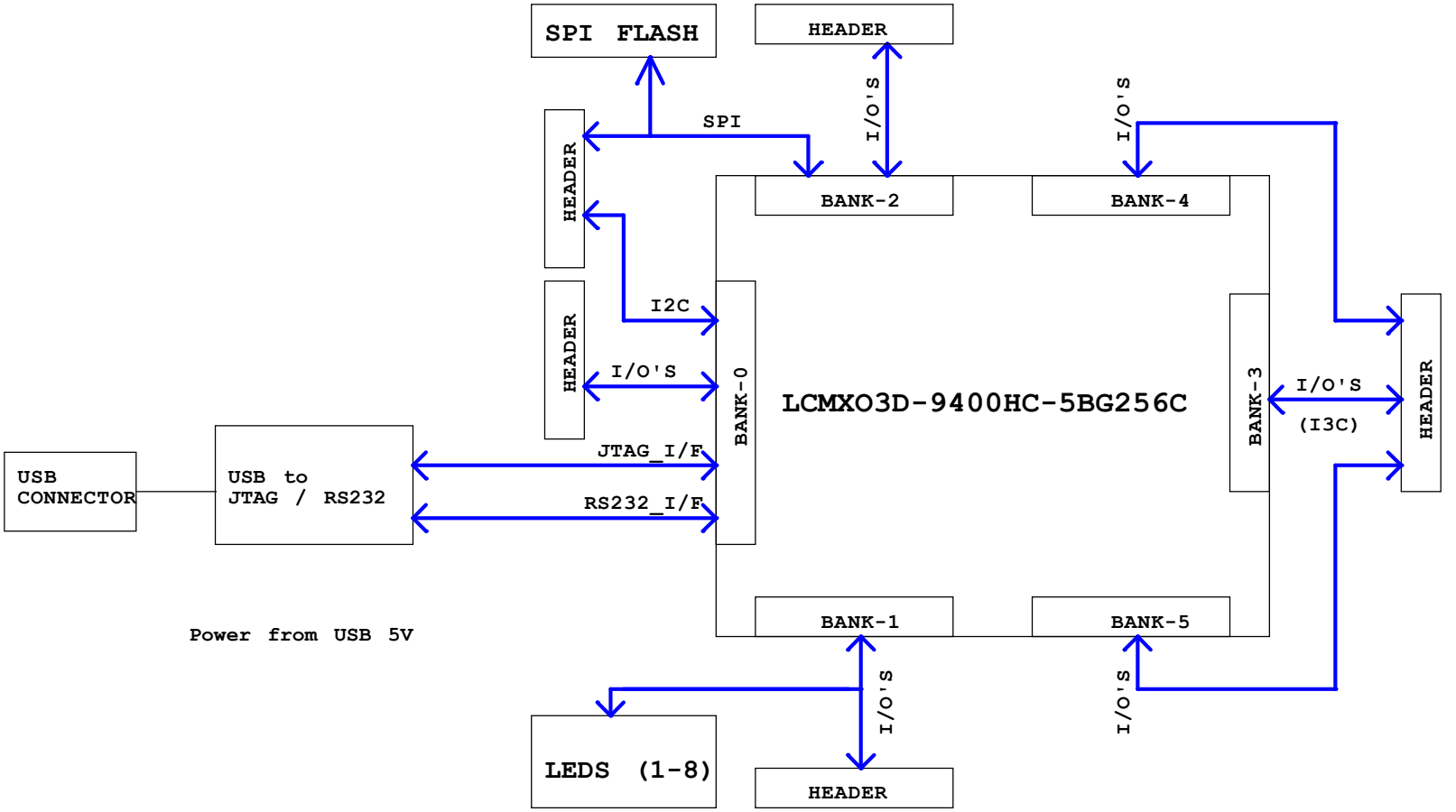
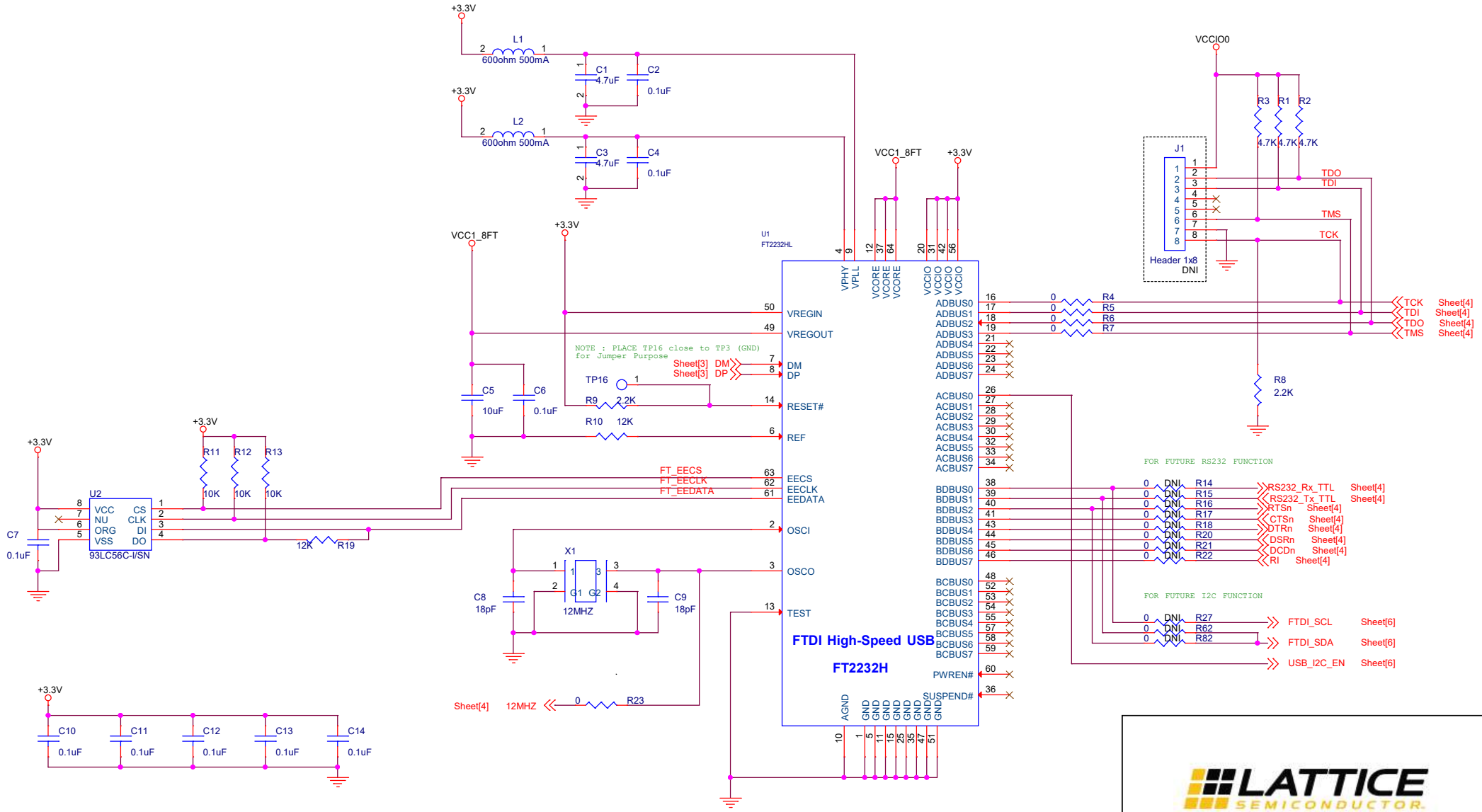


Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

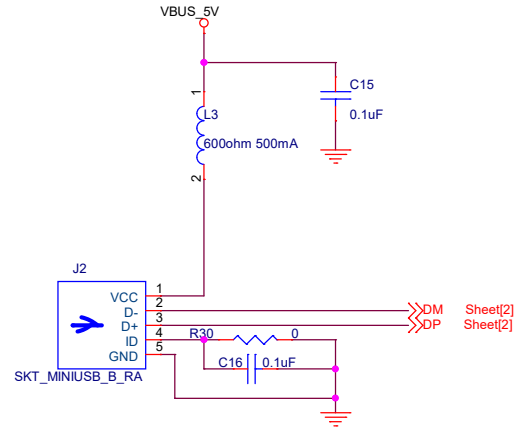
Title: MachXO3D Breakout Board- BLOCK DIAGRAM		
Size: B	Project: MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19	Sheet 1 of 8	

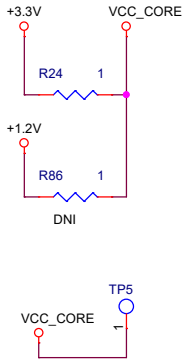


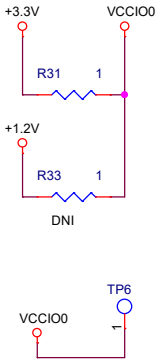
LATTICE SEMICONDUCTOR

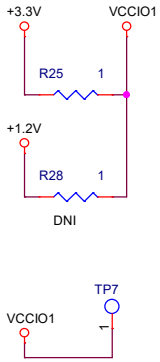
Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

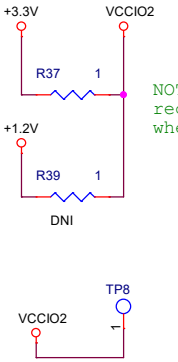
Title	USB to JTAG I/F	
Size B	Project: MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19		Sheet 2 of 8



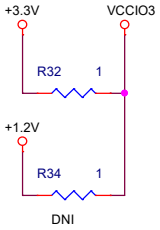


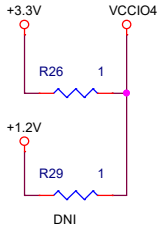


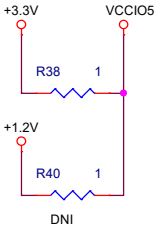


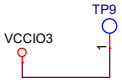


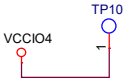
NOTE : Boot from external SPI Flash (U6) requires VCCIO2 set to 3.3V. Use caution when setting VCCIO2 to any other voltage.

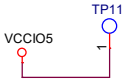


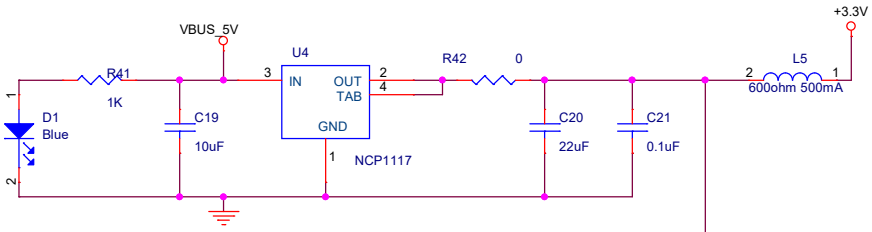


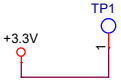


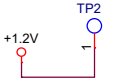


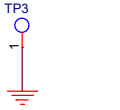


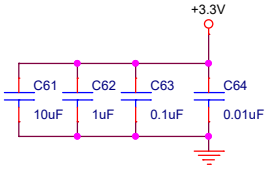


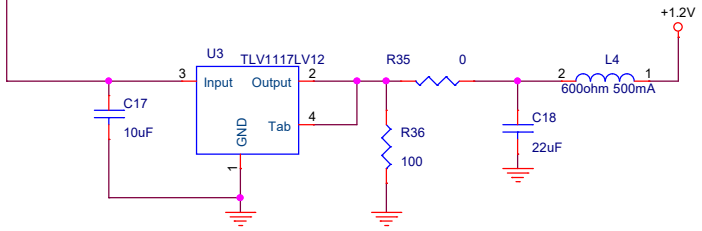






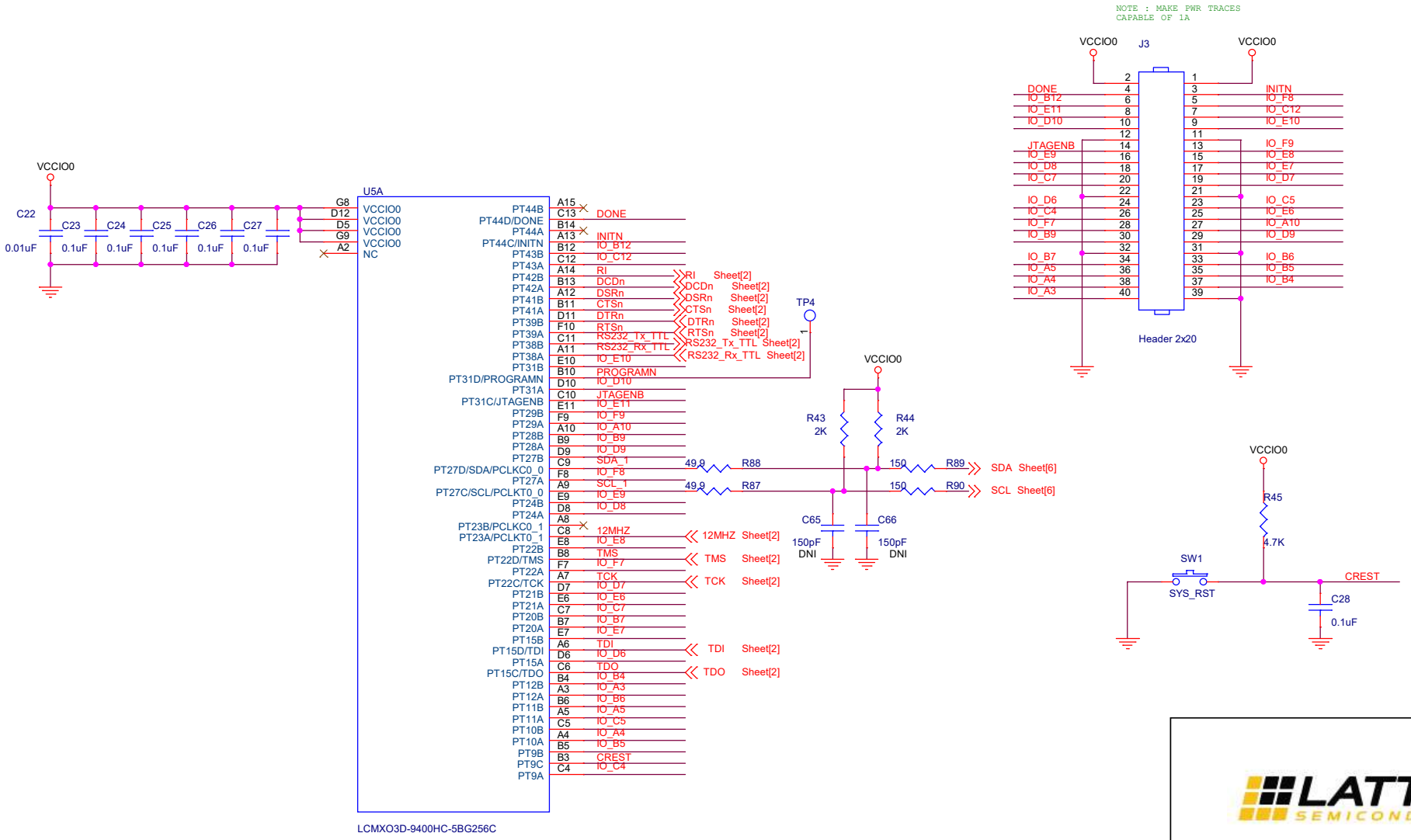






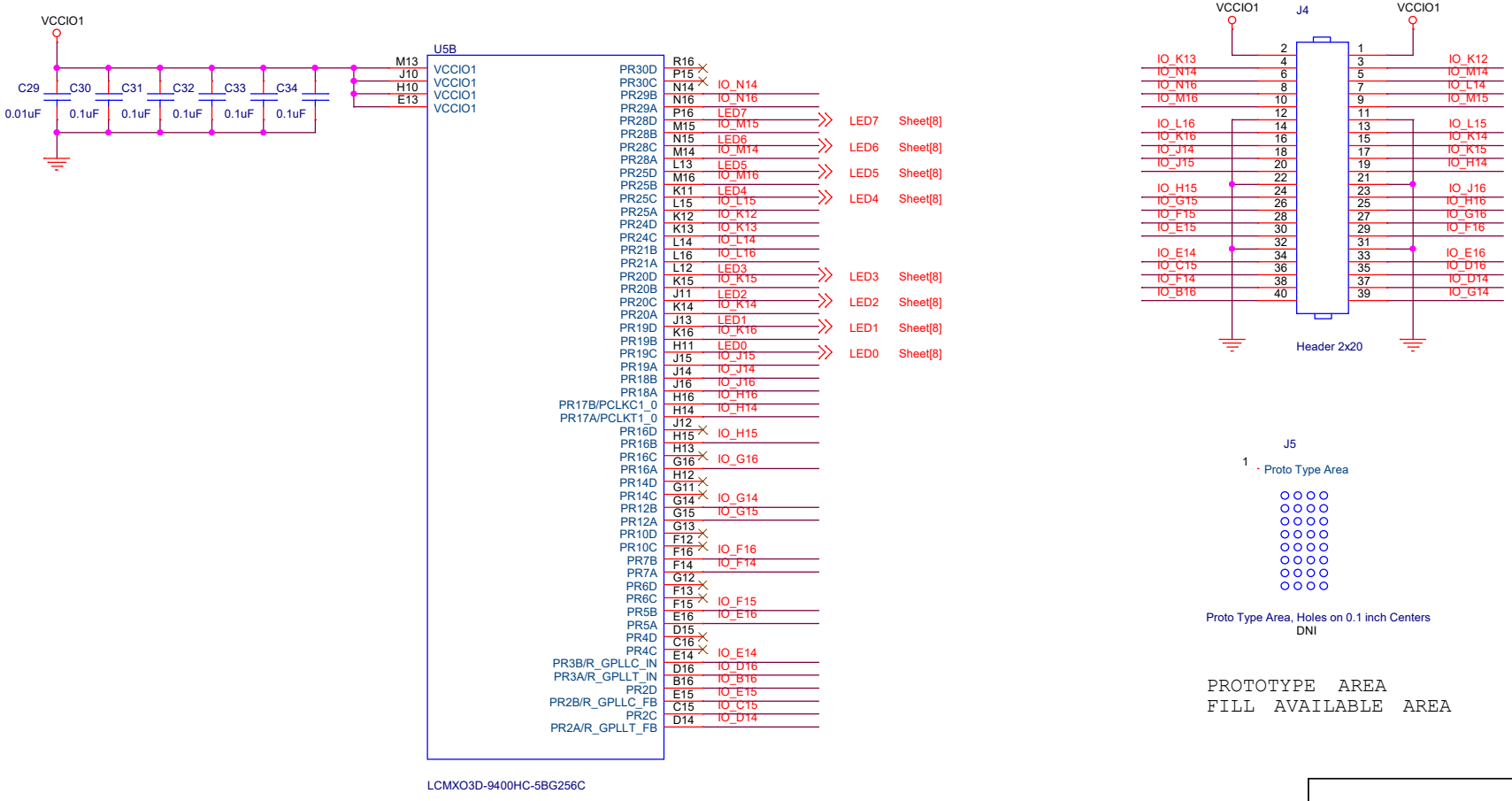
Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title	POWER REGULATORS	
Size B	Project MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19		Sheet 3 of 8



Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

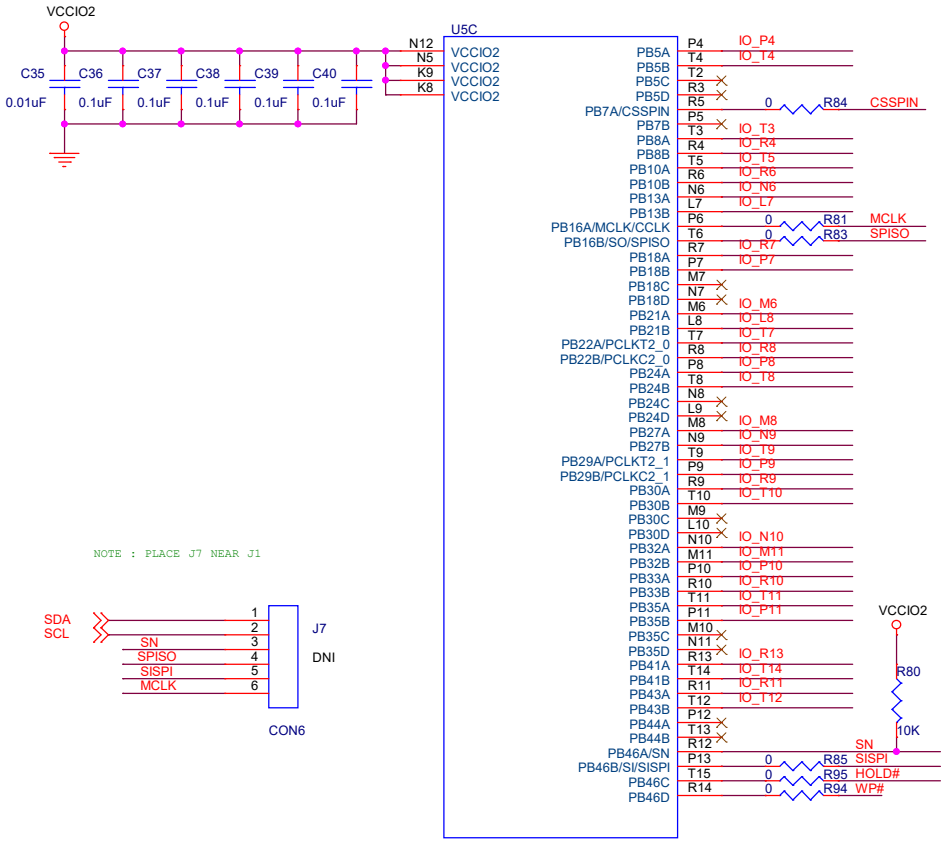
Title: BANK0 I/0		
Size: B	Project: MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19	Sheet 4 of 8	



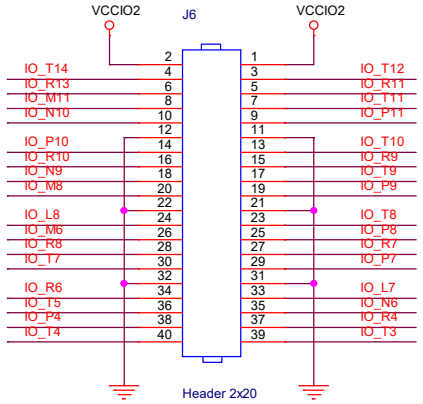
Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title: BANK1 I/O		
Size: B	Project: MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19	Sheet 5 of 8	

NOTE : PLACE R84,R81,R83,R85 CLOSE TO U5



NOTE : MAKE PWR TRACES CAPABLE OF 1A



NOTE : ROUTE J6 TRACES AS 100OHMS, LENGTH MATCHED DIFFERENTIAL PAIRS

IO_P4 IO_T4 R46 DNI 100
IO_T3 IO_R4 R47 DNI 100
IO_T5 IO_R6 R48 DNI 100
IO_N6 IO_L7 R49 DNI 100
IO_R7 IO_P7 R50 DNI 100
IO_M6 IO_L8 R51 DNI 100
IO_T7 IO_R8 R52 DNI 100
IO_P8 IO_T8 R53 DNI 100
IO_M8 IO_N9 R54 DNI 100
IO_T9 IO_P9 R55 DNI 100
IO_R9 IO_T10 R56 DNI 100
IO_N10 IO_M11 R57 DNI 100
IO_P10 IO_R10 R58 DNI 100
IO_T11 IO_P11 R59 DNI 100
IO_R13 IO_T14 R60 DNI 100
IO_R11 IO_T12 R61 DNI 100

NOTE : PLACE ALL THE LVDS DIFF TERMINATION RESISTORS IN TOP AND CLOSE TO U5

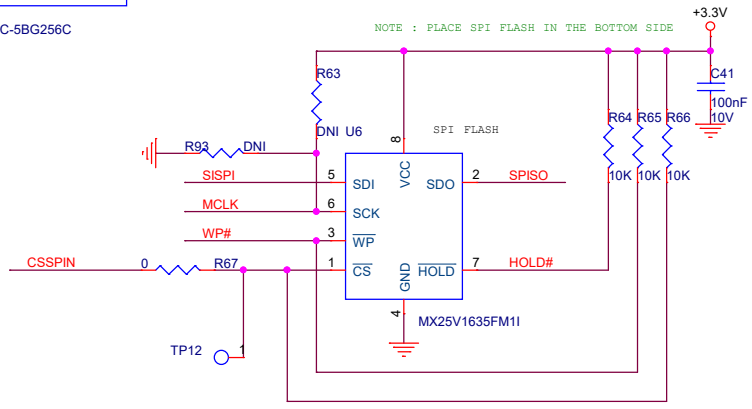
NOTE : PLACE J7 NEAR J1

SDA 0 DNI R91 FTDI_SDA
SCL 0 DNI R92 FTDI_SCL

NOTE : PLACE TEST POINTS NEAR PIN 1 OF J7 AND THE SAME LINE

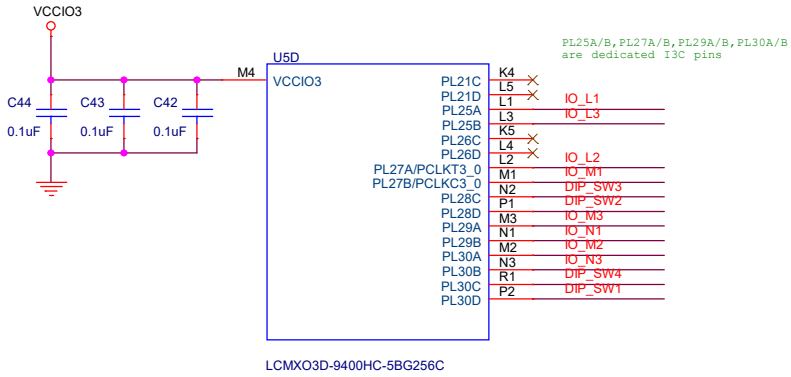
Sheet[2] USB_I2C_EN 1 TP15
Sheet[2] FTDI_SDA 1 TP14
Sheet[2] FTDI_SCL 1 TP13

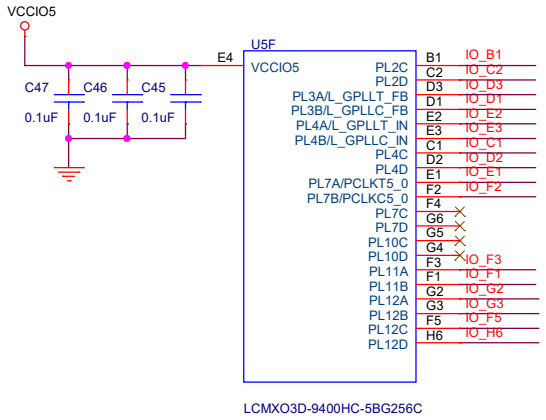
NOTE : PLACE SPI FLASH IN THE BOTTOM SIDE

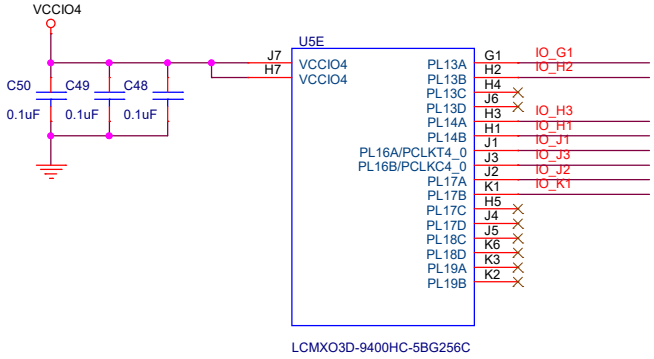


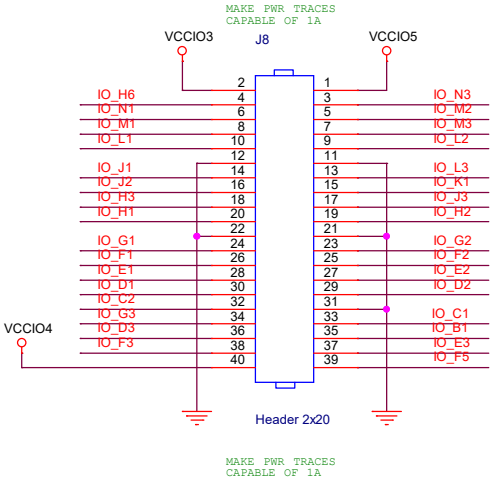
Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

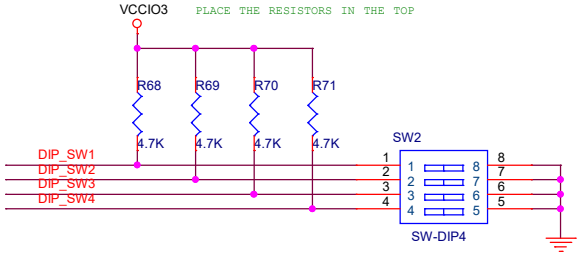
Title: BANK2 I/O		
Size: B	Project: MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19	Sheet 6 of 8	







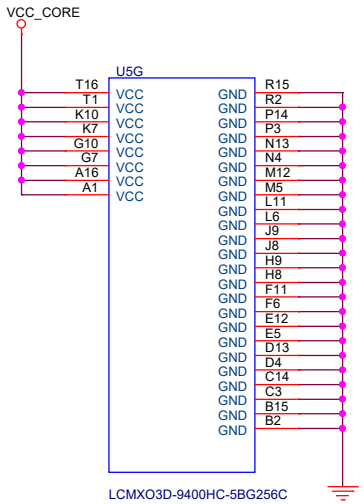


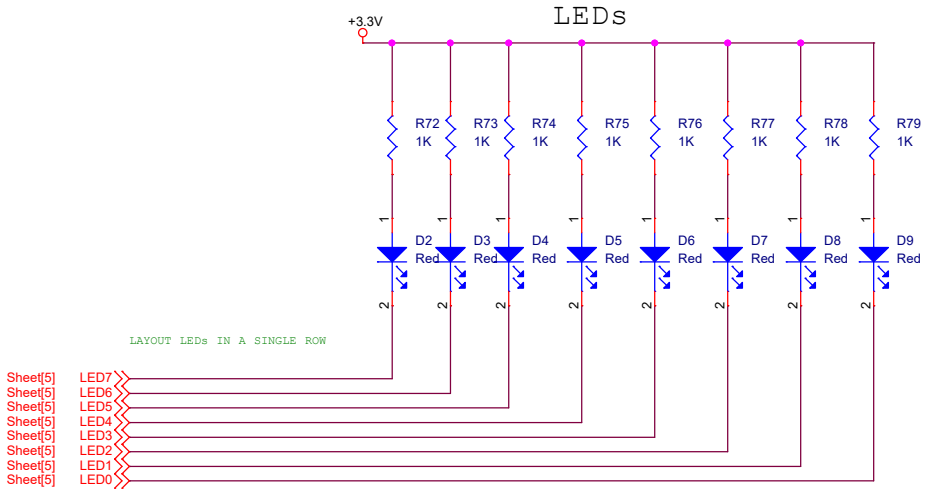


LATTICE SEMICONDUCTOR

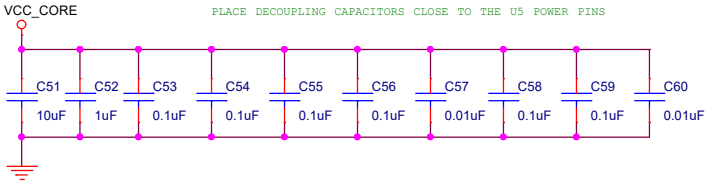
Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title: BANK3,4,5 I/O		
Size: B	Project: MachXO3D Breakout Board	Schematic Rev 1.0
		Board Rev A
Date: 15-APR-19	Sheet 7 of 8	





Note : LEDs are controlled by XO3D I/O Bank 1. When VCCIO1 is set to a voltage less than 3.3V, observe all I/O overdrive requirements. Refer to Lattice Technical Note "MachXO3D sysIO Usage Guide" for more information.



Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title: POWER DECOUPLING AND LED'S		
Size: B	Project: MachXO3D Breakout Board	Schematic Rev 1.0 Board Rev A
Date: 15-APR-19		Sheet 8 of 8