Single Event Upset (SEU) Report for Nexus Platform

Technical Note

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Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CRAM	Configuration RAM
EBR	Embedded Block RAM
ECC	Error Correction Codes
FD-SOI	Fully Depleted Silicon on Insulator
FIT	Failures-in-Time
FPGA	Field-Programmable Gate Array
HP	High Performance
IP	Intellectual Property
JEDEC	Joint Electron Device Engineering Council
JESD89	JEDEC Standard 89
LP	Low Power
LUT	Look Up Table
NYC	New York City
RAM	Random Access Memory
SEC	Soft Error Correction
SED	Soft Error Detect
SEFI	Single Event Functional Interrupt
SER	Soft Error Rate
SEU	Single Event Upset
SRAM	Static Random Access Memory

1. Introduction

This document discusses Single Event Upsets (SEUs), a radiation effect that may be observed during normal operation for Lattice Nexus™ platform, which includes CrossLink™-NX, Certus™-NX, CertusPro™-NX, and MachXO5™-NX product families. SEUs, often referred to as Soft Errors, occur when energetic particles interact with memory components, causing what is observed as a random bit flip.

SRAM is susceptible to SEU and requires characterization according to the JEDEC JESD89 set of standards. Lattice FPGAs typically use SRAM memory in two applications: the Logic Configuration RAM (Config; CRAM) and the User Memory (Embedded Block RAM; EBR).

This document provides Lattice's SEU characterization data for the above-mentioned FPGA families and types of memories, which can be used for estimating failure rates due to radiation effects.

Lattice's FPGA architecture also allows for significant failure derating, primarily due to unused routing resources within designs. Because of these redundant circuits, not all memory bits directly influence design functionality; those that do are known as *critical bits*. Derating guidelines based on critical bit analysis are provided for assessing the Single Event Functional Interrupt (SEFI) rate that is observed during field usage.

Finally, mitigation strategies offered by Lattice for handling SEUs are discussed.

2. Soft Error Rate Data for Nexus Platform FPGA

Table 2.1 summarizes the SEU data collected for Lattice's 28 nm FD-SOI process used for the Nexus platform. The Soft Error Rate (SER) is represented in FIT, meaning the number of upset bits (failures) per billion device-hours. This rate is further normalized to FIT/Mbit of memory to allow for scaling across different devices with varying amounts of memory.

The data is divided by radiation and memory type to allow for use-case customization:

- Radiation Type
  - Neutron – Naturally occurring atmospheric neutrons can cause SEU. Results are scaled to the industry standard flux of NYC Sea-level (14 n/cm2/hr), and can be further scaled based on latitude, longitude, and altitude.
  - Alpha – Device packaging impurities may produce alpha particles as a decay product, which are able to cause SEU. Results are scaled for Ultra-Low Alpha mold compound flux (0.001 a/cm2/hr) and are considered use-case independent.
- SRAM Type
  - Config – Logic configuration memory for controlling FPGA function.
  - EBR – Embedded user memory.
- High Performance versus Low Power Mode
  - HP and LP modes can be considered to effectively modulate the threshold voltage of transistors. In High-Performance mode, the lower effective threshold makes transistors faster and easier to upset with the collected charge from Single Event ionization.

Table 2.1. SEU Data for 28 nm FD-SOI FPGA

Technology	Radiation Type	SRAM Type	SER (FIT/Mbit)
28FDSOI 28 nm	Neutron –LP Mode	Config	2.7
		EBR	6.9
	Alpha – LP Mode	Config	0.4
		EBR	3.35
	Neutron –HP Mode	Config	3.4
		EBR	6.9
	Alpha – HP Mode	Config	0.8
		EBR	3.35

3. Functional Interrupt Rate

Understanding the field impact of SEU is critical for assessing risk and implementing mitigation strategies. The architecture of Lattice FPGAs allows for derating of the above upset rates:

- Config
  - User logic designs implemented on Lattice FPGAs rely on a small fraction of *critical bits* in the Config memory to continue operating properly. A sample of customer design is used to derive typical and worst-case critical bit ratios for assessing the risk of functional failure.
- EBR
  - Lattice FPGAs allow for the implementation of Error Correction Codes (ECC) into the user memory, which can detect and correct flipped bits, eliminating the functional impact of EBR SEU.

Combining these principles allow calculation of the expected field failure rate due to SEU, the SEFI Rate. Table 3.1 shows an example of the Nexus family.

Table 3.1. SEFI Rate by Device Density

Device	Config Memory Size (Mbit)	Typical[1] SEFI Rate (FIT)	Worst-Case[2] SEFI Rate (FIT)
LIFCL-17 LP Mode	2.781	1.7	3.0
LIFCL-17 HP Mode		2.3	4.1
LFD2NX-9 LP Mode		1.7	3.0
LFD2NX-9 HP Mode		2.3	4.1
LFD2NX -17 LP Mode		1.7	3.0
LFD2NX -17 HP Mode		2.3	4.1
LIFCL-33 LP Mode	5.344	3.3	5.8
LIFCL-33 HP Mode		4.5	7.9
LIFCL-33U LP Mode	5.344	3.3	5.8
LIFCL-33U HP Mode		4.5	7.9
LIFCL-40 LP Mode	6.237	3.9	6.8
LIFCL-40 HP Mode		5.2	9.2
LFD2NX-28 LP Mode		3.9	6.8
LFD2NX-28 HP Mode		5.2	9.2
LFD2NX-40 LP Mode		3.9	6.8
LFD2NX-40 HP Mode		5.2	9.2
LFCPNX-50 LP Mode	8.188	5.1	8.9
LFCPNX-50 HP Mode		6.9	12.0
LFCPNX-100 LP Mode	15.073	9.3	16.4
LFCPNX-100 HP Mode		12.7	22.2
LFMXO5-25 LP Mode	4.476	2.8	4.9
LFMXO5-25 HP Mode		3.8	6.6
LFMXO5-15D LP Mode		2.8	4.9
LFMXO5-15D HP Mode		3.8	6.6
LFD2NX-25 LP Mode		2.8	4.9
LFD2NX-25 HP Mode		3.8	6.6
LFD2NX-15 LP Mode		2.8	4.9
LFD2NX-15 HP Mode		3.8	6.6
LFMXO5-55T LP Mode	8.188	5.1	8.9
LFMXO5-55T HP Mode		6.9	12.0
LFMXO5-100T LP Mode	15.005	9.3	16.3
LFMXO5-100T HP Mode		12.6	22.1
LFMXO5-55TD/TDQ LP Mode		9.3	16.3
LFMXO5-55TD/TDQ HP Mode		12.6	22.1

Device	Config Memory Size (Mbit)	Typical[1] SEFI Rate (FIT)	Worst-Case[2] SEFI Rate (FIT)
LFD2NX-65 LP Mode	10.444	6.5	11.4
LFD2NX-65 HP Mode		8.8	15.4
LFD2NX-35 LP Mode		6.5	11.4
LFD2NX-35 HP Mode		8.8	15.4
LFMXO5-65/T LP Mode		6.5	11.4
LFMXO5-65/T HP Mode		8.8	15.4
LFMXO5-35/T LP Mode		6.5	11.4
LFMXO5-35/T HP Mode		8.8	15.4
LFMXO5-30TD/TDQ LP Mode		6.5	11.4
LFMXO5-30TD/TDQ HP Mode		8.8	15.4
LFMXO5-20TD/TDQ LP Mode		6.5	11.4
LFMXO5-20TD/TDQ HP Mode		8.8	15.4

Notes:

1. Typical designs range from 50-70% LUT Utilization based on sample benchmark designs.
2. Worst-Case designs range from 70-90% LUT Utilization based on sample benchmark designs.

4. Customer Down-Time Calculation

System Downtime due to an SEU is a combination of the time that it takes to detect and correct an upset bit, then recover the system to a functioning state. These parameters are highly application dependent.

Downtime per Upsetwn = Detection Time + Correction Time + Recovery Time

The real-world downtime also depends on the probability of a recovery being necessary during a given period.

You can enable SED function to detect soft error events. SED scan happens in the background mode and the duration is variable but does not impact normal device functionality until SED error is detected. Once SED error is detected, Nexus platform devices have the feature to auto-correct single-bit error within a frame via SEC feature. In addition to having an extremely low SEFI rate, the SEC feature of Nexus platform devices make them virtually immune to single event upsets due to Alpha and Neutron particles.

5. Soft Error Event and Repair Sequences

For technical details on SED and SEC features, refer to the documents in the References section.

References

- Soft Error Detection (SED)/Correction (SEC) Usage Guide for Nexus Platform (FPGA-TN-02076)
- A Guide to the Benefits of the Lattice Nexus FPGA Platform for Mission-Critical Applications (WP0028)
- CrossLink-NX web page
- Development Kits and Boards for CrossLink-NX
- IP and Reference Designs for CrossLink-NX
- Certus-NX web page
- Development Kits and Boards for Certus-NX
- IP and Reference Designs for Certus-NX
- CertusPro-NX web page
- Development Kits & Boards for CertusPro-NX
- IP and Reference Designs for CertusPro-NX
- MachXO5-NX web page
- Development Kits and Boards for MachXO5-NX
- IP and Reference Designs for MachXO5-NX
- Lattice Radiant FPGA design software
- Lattice Propel FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Sales Office

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Revision History

Revision 1.8, October 2025

Section	Change Summary
Abbreviations in This Document	Added *FD-SOI*, *HP*, *JEDEC*, *JEDS89*, *LP*, *LUT*, *NYC*, and *RAM*.
Functional Interrupt Rate	Added LFMXO5-20TD/TDQ, LFMXO5-30TD/TDQ, and LFMXO5-55TDQ devices (LP and HP modes) in Table 3.1. SEFI Rate by Device Density.

Revision 1.7, July 2025

Section	Change Summary
All	Made minor editorial changes.
Abbreviations in This Document	Updated section title, introducing sentence, and table header.
Functional Interrupt Rate	Added LFD2NX-15/25/35/65 and LFMXO5-35/T/-65/T devices (LP and HP modes) in Table 3.1. SEFI Rate by Device Density.

Revision 1.6, July 2024

Section	Change Summary
All	Minor editorial fixes.
Functional Interrupt Rate	Added LFD2NX-9 and LFD2NX-28 devices (LP and HP modes) in Table 3.1. SEFI Rate by Device Density.

Revision 1.5, April 2024

Section	Change Summary
Disclaimers	Updated disclaimers.
Functional Interrupt Rate	Added LFMXO5-15D and LFMXO5-55TD devices (LP and HP modes) in Table 3.1. SEFI Rate by Device Density.
References	Added references.

Revision 1.4, August 2023

Section	Change Summary
Functional Interrupt Rate	Added LIFC-33U and LFMXO5-55T devices in Table 3.1. SEFI Rate by Device Density.

Revision 1.3, April 2022

Section	Change Summary
Introduction	Added MachXO5-NX support.
Functional Interrupt Rate	Added LFMXO5-100T device to Table 3.1. SEFI Rate by Device Density.

Revision 1.2, June 2022

Section	Change Summary
Functional Interrupt Rate	Added LIFCL-33 device to Table 3.1. SEFI Rate by Device Density.

Revision 1.1, May 2022

Section	Change Summary
All	• Changed document title to Single Event Upset (SEU) Report for Nexus Platform. • Added Nexus platform/Certus-NX, CertusPro-NX, and MachXO5-NX support.
Soft Error Rate Data for Nexus Platform FPGA	Updated section heading.
Functional Interrupt Rate	• Added High Performance versus Low Power Mode under EBR. • Added LFD2NX, LFCPNX, and LFMXO5 devices to Table 3.1. SEFI Rate by Device Density.
Customer Down-Time Calculation	Added information on System Downtime due to an SEU computation.

Section	Change Summary
References	Updated referenced document title to *Soft Error Detection (SED)/Correction (SEC) Usage Guide for Nexus Platform*. Added *A Guide to the Benefits of the Lattice Nexus FPGA Platform for Mission Critical Applications* white paper.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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