Introduction

The Edge of the network is rapidly becoming a critical part of the future of AI processing. Connectivity is going to become even more pervasive with 5G set to connect billions of devices to the Internet. There's an increasing interest across markets in leveraging AI and machine learning (AI/ML) and there's a large demand for low power high-tech devices with AI/ML processing capabilities to operate at the network Edge. Advanced processing at the Edge is important to reduce latency to end points and end users, and to maintain better user privacy. In addition, intelligent Edge devices filter data traffic to the cloud, reducing network costs and bandwidth.

Many of these intelligent Edge devices use image sensors to support various embedded vision applications and include AI/ML-driven applications such as object counting or presence detection. Supporting embedded vision applications at the Edge, however, requires devices offer certain design and performance characteristics: low power consumption, high performance, high reliability and a small form factor. For these applications, Lattice has built a new family of FPGAs under the Lattice CrossLink-NX™ brand. Lattice's new chips are designed to address the latest trends in video processing: mixing multiple sensors and displays, higher resolution video, multiple interfaces, and Edge AI processing.

CrossLink meets Nexus

To help developers support new and existing embedded vision systems, Lattice Semiconductor created the CrossLinkPlus™ family of specialized, small-footprint, low-power FPGAs.

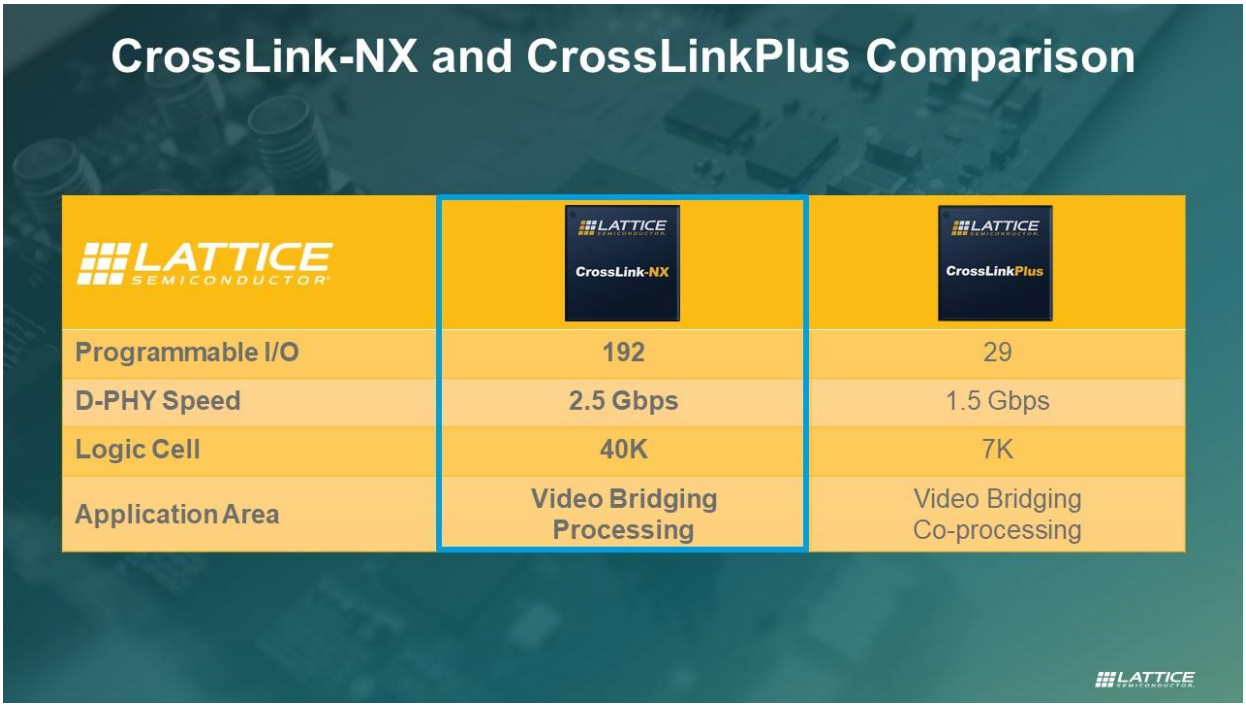

Figure 1 CrossLinkPlus compared with CrossLink-NX

With programmable logic capabilities to handle processing needs and support for a wide range of interface standards, CrossLinkPlus is a compelling design choice for video signal aggregation and image co-processing in Edge applications. CrossLinkPlus FPGAs are manufactured using a 40 nm bulk CMOS technology.

For embedded vision systems requiring higher levels of performance, Lattice released the CrossLink-NX family of FPGAs. They're the first FPGAs implemented on Lattice's new FPGA platform, Lattice Nexus™, and the industry's first low power mainstream FPGA platform to use 28nm fully depleted silicon-on-insulator (FD-SOI) planar process technology. Thanks to the 28nm FD-SOI process and a new FPGA architecture optimized for low power and new small form factor packaging options, CrossLink-NX expands on the capabilities of the CrossLink FPGA family. The CrossLink-NX gives developers an innovative choice for video and sensor processing that outperforms similar competing FPGAs by offering lower power, smaller form factor packages, higher performance, higher reliability, and new tools for ease of use.

Crosslink-NX Markets: Automotive, Mobile, Industrial, and More

The Crosslink-NX family is flexible enough to address several different segments in the video switching and image processing market. Many of these applications require support for bridging and/or aggregation of data streams between multiple displays, camera and sensors (image sensors and others). In addition, these parts can be used for simultaneous video processing and AI/ML inferencing. The FPGAs are very power efficient, so they can be used in mobile, battery-powered devices, yet are still powerful enough to use in computing and industrial control applications.

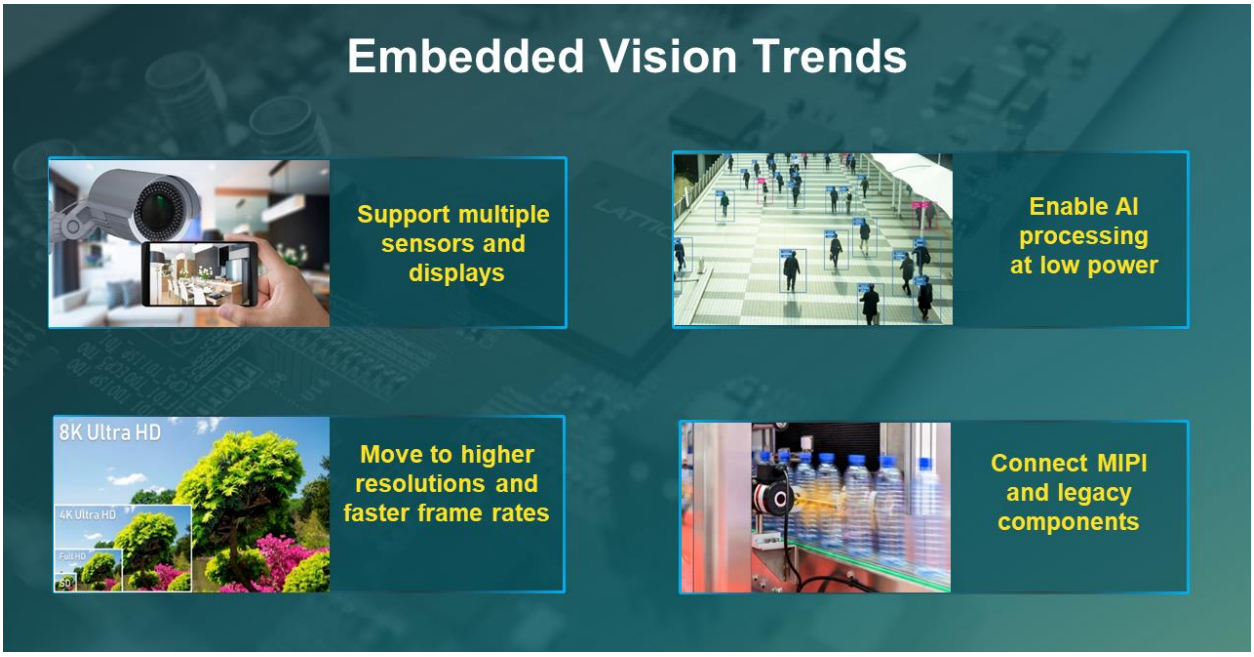

Figure 2. Embedded Vision Trends *Source: Lattice*

In video surveillance and security applications, CrossLink-NX can be used for sensor aggregation and bridging, in addition to powering AI inferencing to preprocess the sensor data with functions such as facial recognition or presence detection.

The chip can be used as an embedded vision co-processor to merge up to 14 sensors. It can also be used for video scaling, rotation, and color space conversions. With this chip, one sensor stream can be sent to multiple locations, which is useful in applications such as automotive, where cameras need to feed multiple processing units.

In the following sections of this white paper, several comparisons are made between CrossLink-NX and competing FPGAs with similar logic cell densities and I/O support. The comparisons are based on performance and power usage tests conducted by Lattice.

Crosslink-NX Performance for Edge AI

While it is often thought that AI processing will be done in the cloud, it is becoming more important that local AI functionality be available at the Edge to ensure better user privacy, reduce data traffic to the cloud, and lower data latency to improve device response times.

A number of factors make supporting Edge AI/ML challenging for the hardware developer. For example, to boost the accuracy of AI/ML results or enable new applications, embedded vision developers are adding more sensors and/or higher resolution/faster frame rate cameras to their systems. At the same time, embedded vision designers are looking to use components compliant with the MIPI standard. Originally developed for the mobile market, developers across a growing array of applications are looking for ways to capitalize on the high performance and economies of scale afforded by MIPI components like application processors.

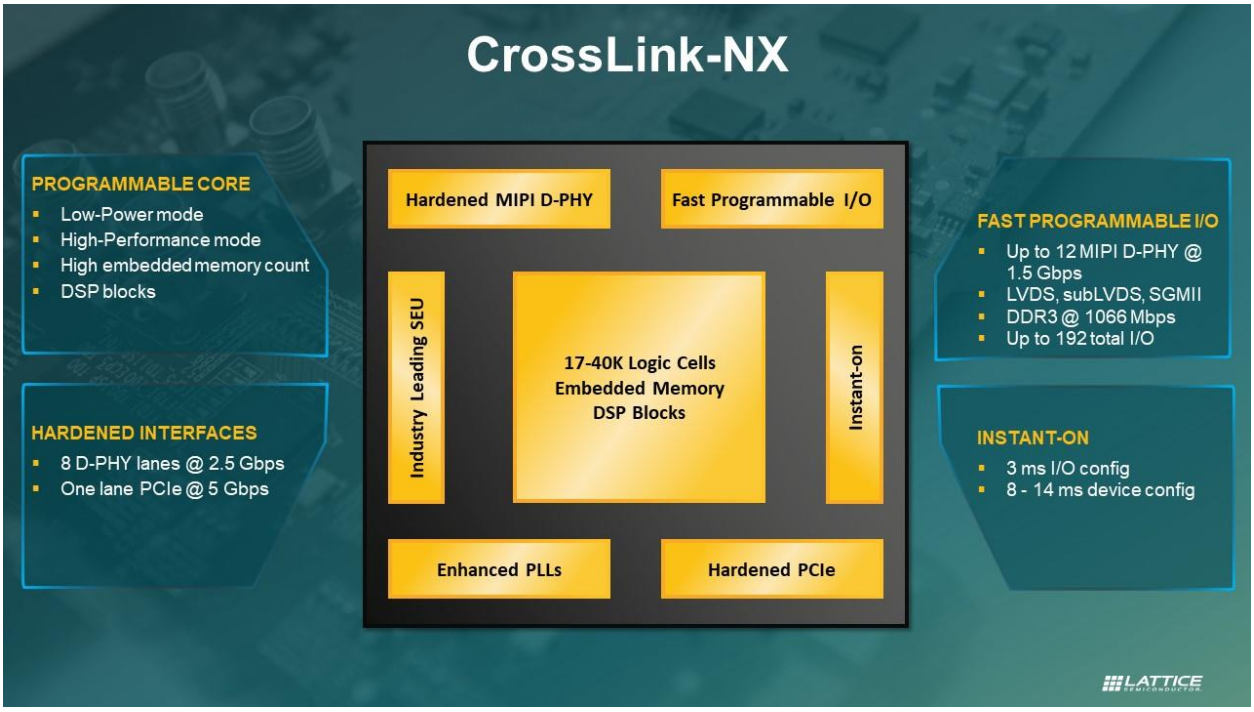

Figure 3. CrossLink-NX Block Diagram *Source: Lattice*

CrossLink-NX FPGAs have the necessary resources to process multiple video streams and perform AI compute functions on the fly and it can support legacy interfaces.

To serve video and display applications, the family includes multiple MIPI D-PHY interfaces and CSI-2 camera interfaces. There are two hardened D-PHY interfaces each of which supports four lanes at up to 2.5 Gbps speeds (10 Gbps in total), while additional soft MIPI D-PHY configurations can support up to another 12 MIPI data streams at 1.5 Gbps. Other I/Os include a hardened 5 Gbps PCIe Gen2 and LPDDR3 DRAM at 1,066 Mbps.

The hardened DSP blocks in the CrossLink-NX can be used to locally process neural nets (NN). This family offers the most embedded memory per logic block of any FPGA in its class (170 bits per logic cell). The FPGAs' large on-chip SRAM, ranging from 1 to 2.5MB, can store the NN activations/weights.

FD-SOI Enables Innovative New Power Modes and Higher Reliability

The use of FD-SOI allowed Lattice to create an innovative way for developers to manage power. The process allows the application of a voltage on the back side of the die (back-bias) that changes the threshold voltage. This allows Lattice to offer two operating modes – lower power mode and a higher performing mode. With power optimizations, the operating power at higher frequencies can be in the 200mW range, with only a few 10's of mW static leakage. Power consumption for CrossLink-NX FPGAs is up to 75 percent lower than other competing devices of a similar class.

The FD-SOI process adds an additional benefit in that it is more immune to soft errors – a phenomenon where high energy particles striking transistors on an FPGA disrupt operation. With FD-SOI, there is smaller physical area on the chip that is susceptible to soft errors. To ensure the SRAM-based LUTs are performing reliably, there is also software error checking with memory block error correcting codes. All told, the soft error rate (SER) for the CrossLink-NX in FD-SOI is up to 100x lower than similar competing FPGA solutions manufactured in bulk CMOS processes.

Crosslink-NX Smaller Footprint

Mobile applications can have very tight space constraints. Lattice will have two family members offering different levels of logic support (17K or 40K logic cells). An advantage of the CrossLink-NX family is that it will support very small spaces, down to a 3.7 mm x 4.1mm package size (for the smaller 17K logic cells version). The devices in the CrossLink-NX family are pin compatible, so the same board design can be used for different applications or provide a performance upgrade to future versions of devices that use them.

Instant-On Performance

For configuration files, CrossLink-NX FPGAs use a quad-SPI flash. The I/O pins can be configured first in 3 milliseconds, then the fully configured logic is available in less than 14

milliseconds. These features enable instant-on performance to reduce possible operational issues in many applications.

Crosslink-NX Offers Ease of Use

CrossLink-NX FPGAs are supported by a growing software library that includes the Lattice Radiant design tool (which was recently updated to include new functionality including on-chip debugging, signal integrity analysis and an engineering change order editor) and a collection of IP cores widely used in embedded visions applications (MIPI D-PHY, format conversion, PCIe, SGMII and OpenLDI). Development boards and reference designs for common applications like camera aggregation are also available, with more planned for future releases.

Conclusion

With the CrossLink-NX FPGA family, Lattice has combined programmability with high-performance processing and fast I/O connectivity. These devices will give developers a wide range of options for intelligent embedded vision applications where flexibility, power efficiency, programmability, small footprint, and fast video interfaces are needed. These are just the first products available based on the Lattice Nexus FPGA platform.

CrossLink-NX Family Reference: