CrossLink-NX Hardware Checklist

Technical Note

FPGA-TN-02149-1.7

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ADC	Analog to Digital Converter
BGA	Ball Grid Array
CML	Current-Mode Logic
DLL	Delay-Locked Loop
FPGA	Field Programmable Gate Array
GPLL	General-Purpose Phase-Locked Loop
HCSL	High-Speed Current Steering Logic
HPIO	High-Performance Input/Output
I/O	Input/Output
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IBIS	I/O Buffer Information Specification
JTAG	Joint Test Action Group
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POR	Power-On-Reset
RST	Reset
SCL	Serial Clock Line
SDA	Serial Data Line
SERDES	Serializer/Deserializer
SPI	Serial Peripheral Interface
SSPI	Secondary Serial Peripheral Interface
SSTL	Stub Series Terminated Logic
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
WLCSP	Wafer Level Chip Scale Package
WRIO	Wide-Range Input/Output

1. Introduction

When designing complex hardware using the CrossLink™-NX device, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the CrossLink-NX device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that the reader is familiar with the CrossLink-NX device features as described in CrossLink-NX Family Data Sheet (FPGA-DS-02049). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to CrossLink-NX Family Data Sheet (FPGA-DS-02049) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the CrossLink-NX power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: You should refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL/DLL Design and User Guide for Neus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097)
- Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SerDes (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SerDes Jitter (TN1084)
- HSPICE SerDes simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- CrossLink-NX-related pinout information can be found on the Lattice CrossLink-NX web page.
- ADC User Guide for Nexus Platform (FPGA-TN-02129)

2. Power Supplies

The V_{CC}, V_{CCAUXA}, and V_{CCIOX} power supplies are monitored to determine the CrossLink-NX internal Power Good condition during power-up. These supplies need to be at a valid and stable level before the device becomes operational. All other supplies are not monitored during power-up, but need to be at valid and stable level before the device configuration is complete and enters User Mode. Several other supplies are used in conjunction with onboard D-PHYs, SerDes Blocks, and ADCs on CrossLink-NX devices.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Single-Ended I/O Standards

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCAUXA}	1.8 V	Auxiliary Supply Voltage for Core logic. Required for Power Good condition.
V_{CCAUX}	1.8 V	Auxiliary power supply voltage for internal analog circuitry Banks 0, 1, 2, 6, and 7.
$V_{CCAUXH[5:3]}$	1.8 V	Auxiliary power supply voltage for internal analog circuitry Banks 3, 4, and 5.
$V_{CCIO[7:0]}$	Banks 0, 1, 2, 6, 7: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply: V_{CCIO0} and V_{CCIO1} are used in conjunction with pins dedicated and shared with device configuration, and are required for Power Good condition.
$V_{CCDPHY[1:0]}$	1.0 V	Digital Supply Voltage for D-PHY. Should be isolated from excessive noise.
$V_{CCADPHY[1:0]}$	1.8 V	Analog Supply Voltage for D-PHY. Should be isolated from excessive noise.
$V_{CCPLLDPHY[1:0]}$	1.0 V	PLL Supply voltage for D-PHY. Should be isolated from excessive noise.
$V_{CCADC18}$	1.8 V	ADC Block power supply. Should be isolated from excessive noise.
ADC_REFP[1:0]	1.0 V to 1.8 V Typical	ADC External Reference. Should be isolated from excessive noise and have high accuracy (< 0.1%).
V_{CCSD0}	1.0 V	SerDes Block Core power supply voltage. Should be isolated from excessive noise.
$V_{CCPLLSD0}$	1.8 V	SerDes Block PLL power supply voltage. Should be isolated from excessive noise.
$V_{CCAUXSD}$	1.8 V	SerDes Block Auxiliary power supply voltage. Should be isolated from excessive noise.

The CrossLink-NX FPGA device has a power-on-reset state machine that depends on several of the power supplies.

These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies have reached their minimum operating voltages.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noises.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR × expected current draw
- Expected voltage drops due to current measuring resistor's ESR × expected current draw

With 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is especially sensitive to noise as every 10 mV is 1% of the rail voltage. For SerDes differential power rails, it is recommended to target a maximum 1% peak noise. For PLLs, target less than 0.25% peak noise.

3. CrossLink-NX MIPI D-PHY, SerDes, and PLL Power Supplies

There are supplies dedicated to the operation of the CrossLink-NX MIPI® D-PHYs, SerDes Blocks, and ADCs. These supplies are also paired with dedicated ground pins. Providing a quiet supply is critical for these blocks. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins.

For the best jitter performance, careful pin assignment keeps noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk to sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require a cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies; however, a robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	10 µF x 3 + 100 nF per pin	Core logic. 1.0 V
V_{CCAUXA}	120 FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for Core logic. 1.8 V
V_{CCAUX} and $V_{CCAUXH[5:3]}$ Combined Together	120 Ω FB + 10 µF x 2 + 100 nF per pin	Auxiliary power supply pin for internal analog circuitry V_{CCAUX} Banks 0, 1, 2, 6, 7. $V_{CCAUXH[5:3]}$ Banks 3, 4, 5. 1.8 V
$V_{CCIO[7:0]}$	10 µF + 100 nF per pin	Bank I/O. Unused banks can replace the 10 µF with a 1.0 µF. For banks with lots of outputs or large capacitive loading replace the 10 µF with a 22 µF (or add one additional 10 µF). Banks 0, 1, 2, 6, 7 = 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4, 5 = 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.
$V_{CCDPHY[1:0]}$	120 Ω FB + 10 µF + 100 nF per pin	D-PHY digital. If DPHYx Block is not used, leave open. 1.0 V
$V_{CCADPHY[1:0]}$	120 Ω FB + 10 µF + 100 nF per pin	D-PHY analog. If DPHYx Block is not used, leave open. 1.8 V
$V_{CCPLLDPHY[1:0]}$	220 Ω or 120 Ω FB + 2.2 µF + 100 nF per pin	D-PHY PLL. If DPHYx Block is not used, leave open. 1.0 V
$V_{CCADC18}$	120 Ω FB + 10 µF + 100 nF per pin	ADC Block. If ADC Block is not used, leave open. 1.8 V
ADC_REFP[1:0]	220 Ω or 120 Ω FB + 1 µF + 100 nF per pin	ADC External Reference. Must have very low noise and high accuracy (< 0.1%). Voltage source/regulator should be filtered by 220 Ω or 120 Ω FB + 1 µF. If ADC Block is not used, connect to board ground. 1.0 V to 1.8 V Typical

Power Input	Recommended Filter	Notes
V_{CCSD0}	120 Ω FB + 10 µF + 100 nF per pin	SerDes Block Core. If SerDes Block is not used, leave open. 1.0 V
$V_{CCPLLSD0}$	220 Ω FB + 47 µF + 470 nF per pin IMPORTANT: Connect capacitor grounds only to FPGA pin SDx_REFRET	SerDes Block PLL. If SerDes Block is not used, leave open. Bypass capacitor grounds go only to SDx_REFRET. 1.8 V
$V_{CCAUXSD}$	120 Ω FB + 10 µF + 100 nF per pin	SerDes Block Auxiliary. If SerDes Block is not used, leave it open. Bypass capacitor grounds go only to SDx_REFRET. 1.8 V

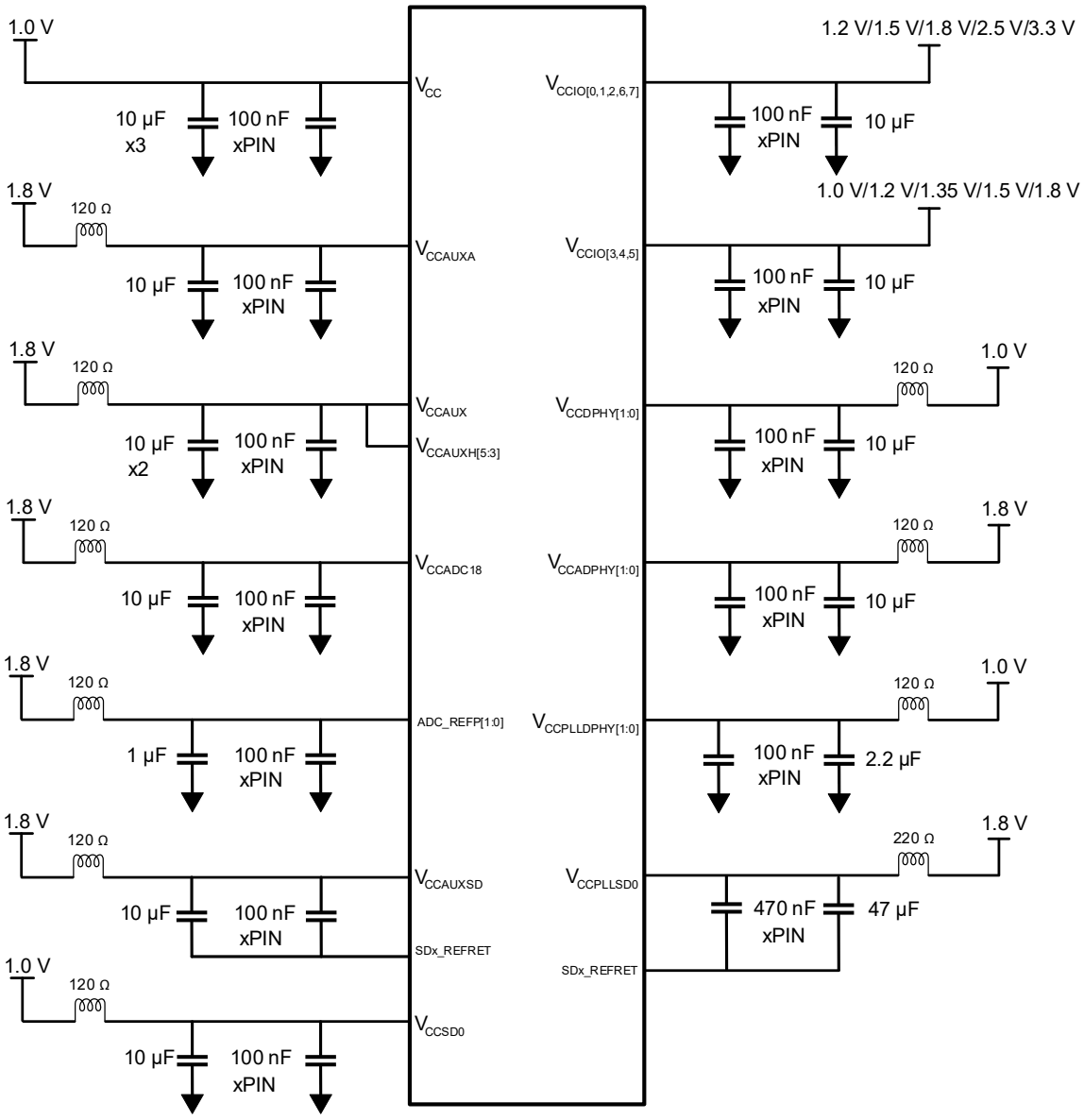

Figure 3.1. Recommended Power Filters

3.2. Ferrite Bead Selection Notes

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR * CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.025 Ω and 0.10 Ω depending on current load.
- PLL rails are low current which allow ferrite beads with ESR ≤ 0.3 Ω.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

3.3. Ground Pins

- All ground pins need to be connected to the board's ground plane.
- V_{SSSD0}, V_{SSADC}, and $V_{SSADPHY}$ pins are sensitive to noise and should be isolated from fast switching high current pathways on the ground plane. Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.
- SD0_REFRET — Input SerDes Reference Return Input. This pin should be AC coupled (bypassed) to the $V_{CCPLLSD0}$ supply.

3.4. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator is recommended.

3.5. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the power supply pins as possible. Good quality capacitors for bypassing generally meet the requirements discussed in the following subsections.

3.5.1. Dielectric

Use dielectrics such as X5R, X7R and similar ones which have good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U and similarly poor capacitance-controlled dielectrics.

3.5.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the voltage rail (maximum). Example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.5.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size-related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0603
4.7 µF	0603	0402
10 µF	0603	0805
22 µF	0805	1206

3.6. Unused Bank V_{CCIOx}

Connect unused V_{CCIO}s to a power rail, Do not leave them open.

3.7. Unused ADC Blocks

Connect V_{SSADC}, ADC_REFPx, ADC_DPx, and ADC_DNx pins to board ground. Leave $V_{CCADC18}$ floating (not connected).

3.8. Unused SerDes Blocks

Connect V_{SSSD}, Rx Differential Inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET, and SDx_REXT to board ground. Leave V_{CCSD0}, $V_{CCPLLSD0}$, V_{CCAUX}, and Tx Differential Pair Outputs open.

3.9. Unused DPHY Banks

Leave $V_{CCADPHYx}$, $V_{CCDPHYx}$, $V_{CCPLLDHYx}$, and DPHY I/O floating (not connected).

4. Power Sequencing

There is no power up sequence required for the CrossLink-NX device.

5. Power Estimation

Once the CrossLink-NX device density, package, and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant® design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current and maximum DC and AC current for the given system environmental conditions.
- The ability for the system environment and CrossLink-NX device packaging to be able to support the specified maximum operating junction temperature. By determining these two criteria, the CrossLink-NX device power requirements are taken into consideration early in the design phase.

6. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024). WLCSP packages are similar to other BGA (ball grid array) packages with regard to the PCBs the packages are to be mounted on. For application-specific assembly guidance, consult the design guidelines of the assembly service provider.

The CrossLink-NX device includes provisions to configure the FPGA via the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 6.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI/SI	4.7 kΩ pull-up to V_{CCIO1}
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
TDO/SO	4.7 kΩ pull-up to V_{CCIO1}
TCK/SCLK	2.2 kΩ pull-down to GND

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO1} and ground.

External resistors are necessary if the configuration signals are used to handshake with other devices. Recommended pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground should be used on the following pins. External pull-resistors are not necessary on individual configuration pins if the signal pin has not persisted.

Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO0}
INITN	4.7 kΩ pull-up to V_{CCIO0}
DONE	4.7 kΩ pull-up to V_{CCIO0}
MCLK	1.0 kΩ to GND (Not installed by default) 1.0 kΩ to V_{CCIO0} (Not installed by default)
MCSN	4.7 kΩ pull-up to V_{CCIO0}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
SCL/SDA*	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO1}

***Note:** Pull-up resistors are not required in Target I3C configuration mode.

Table 6.3. Configuration Pins Needed per Programming Mode[1]

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
MSPI	0	(Default)	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
JTAG	1	JTAG_EN pin[2]	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key[2]	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

Notes:

1. Leave unused Configuration ports open.
2. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

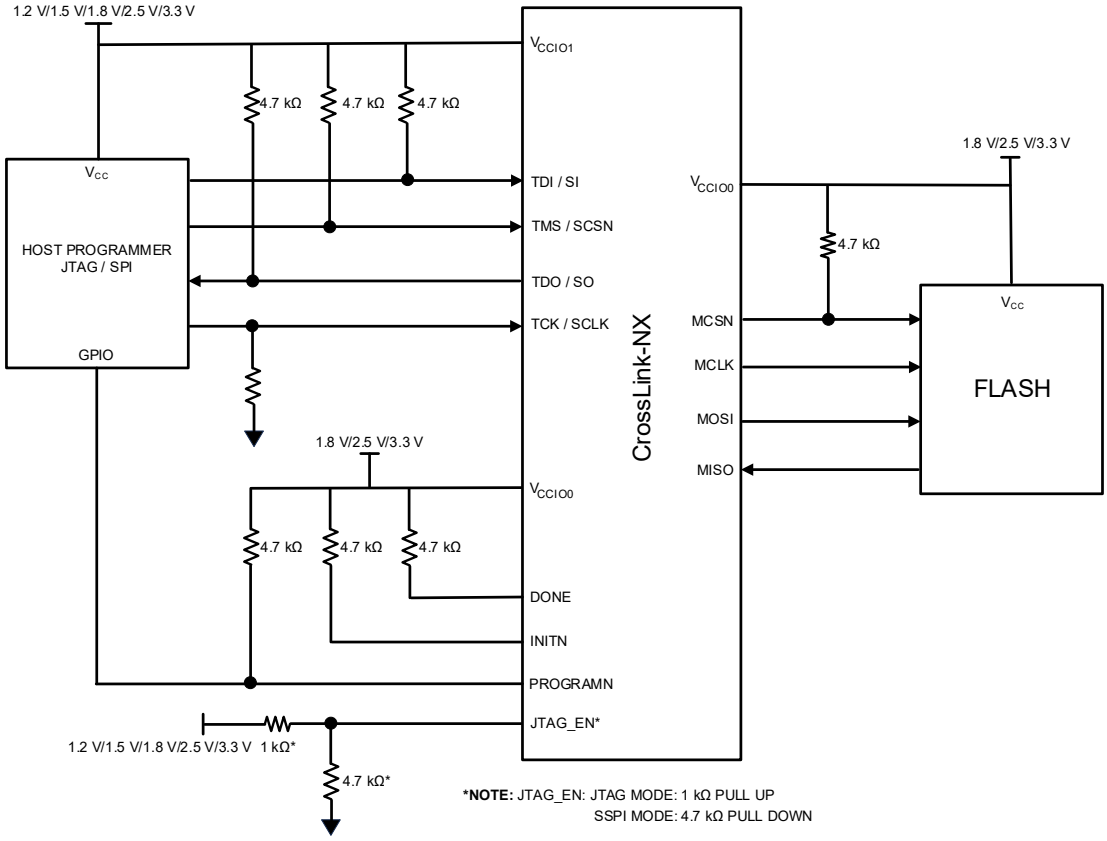

Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI

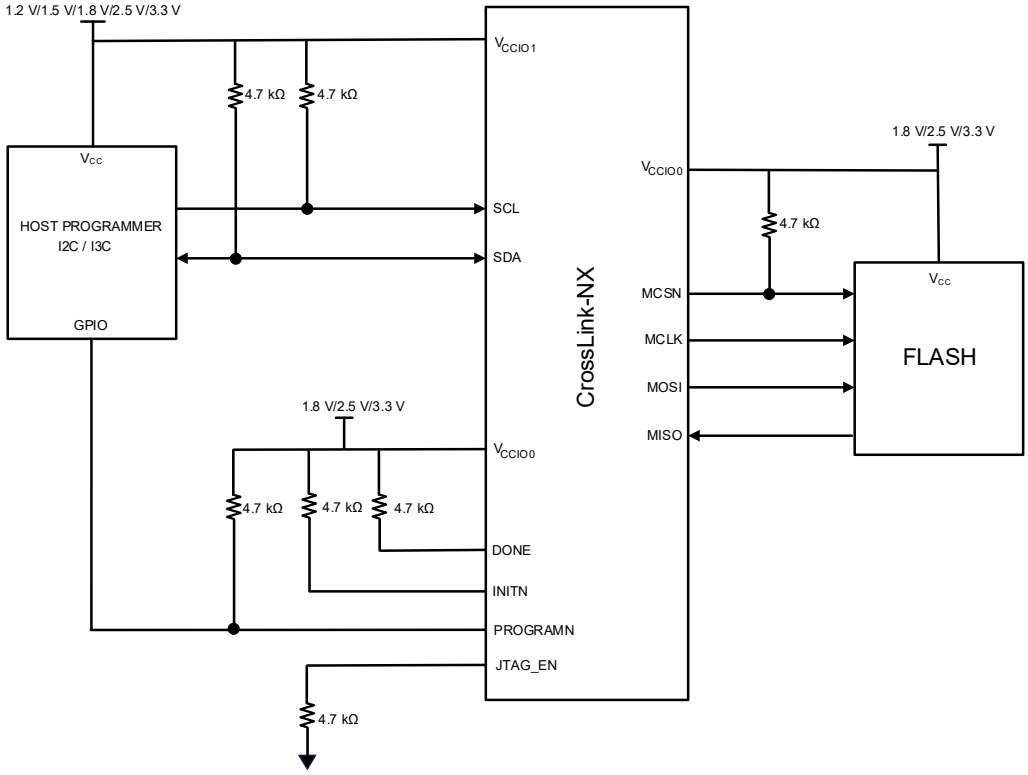

Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C

Some architectures require Bank 0 and Bank 1 to have different bank voltages. One such architecture is illustrated in Figure 6.3. In the event a control signal, such as PROGRAMN, originates in one voltage domain but is terminated in another, a voltage translating device or circuit must be implemented to reduce excess current leakage or possible device damage. Figure 6.3 shows a voltage translator utilized for PROGRAMN, allowing a 3.3 V driver to drive the 1.8 V bank 0 input buffer safely and efficiently.

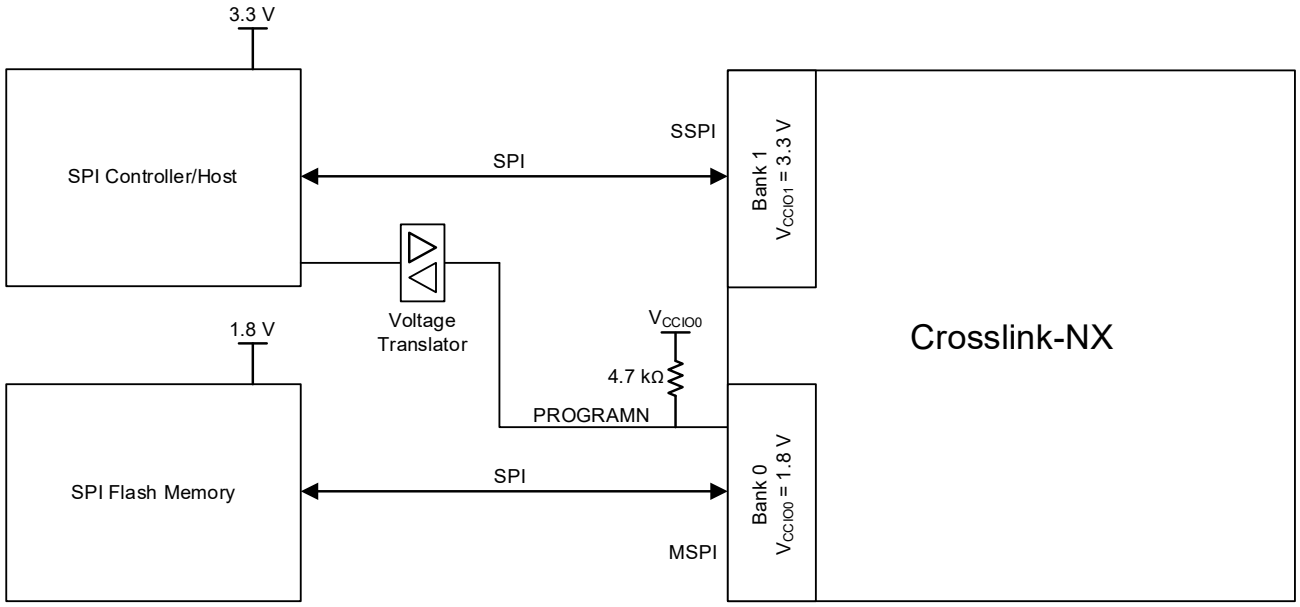

Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks

7. External SPI Flash

The SPI Flash voltage should match the V_{CCIO0} voltage.

It is recommended to use SPI Flash devices that are supported by the Lattice Radiant Programmer.

You can view the list of supported devices by searching for *SPI Flash support* in the Lattice Radiant Programmer Help menu. For SPI Flash devices that are not listed in the *SPI Flash support*, using the **custom flash** option may allow non-supported devices to work.

8. I/O Pin Assignments

Assembly and rework parameters for WLCSP packages are similar to other BGA packages. Refer to Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041), which outlines the reflow parameters for all the various package styles offered, including WLCSP.

The $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ provide a *quiet* supply for the SerDes blocks. For the best jitter performance, careful pin assignment keeps *noisy* I/O pins away from *sensitive* pins. The leading causes of PCB related SerDes crosstalk are related to FPGA outputs located in close proximity to the sensitive SerDes power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

Although coupling has been reduced in the device packages of CrossLink-NX devices where little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to SerDes data, reference clock, and power pins as well as other critical I/O pins such as clock signals. Electrical Recommendations for Lattice SerDes (FPGA-TN-02077) provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they cause problems.

It is a common practice for designers to select pinouts for their system very early in the design cycle. This requires a detailed knowledge of the targeted FPGA device for the FPGA designers. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

9. sysI/O

Crosslink-NX device provides you the flexibility to configure each I/O according to your requirement. These pins can be configured as input, output, and tri-state. Attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can also be set up.

You can set Pull-up and Pull-down resistors for PULLMODE. The implementation of this resistor is set by using a constant current that has values as specified in Table 9.1.

Table 9.1. Weak Pull-up/Pull-down Current Specifications

Configuration	Parameter	Condition	Min	Max	Unit
Pull-up	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	–30	–150	µA
Pull-down	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	150	µA

Crosslink-NX device also provides special I/O like HPIO and WRIO that can be used for high-speed communication. Figure 9.1 shows the block diagram for HPIO and Figure 9.2 shows the block diagram for WRIO.

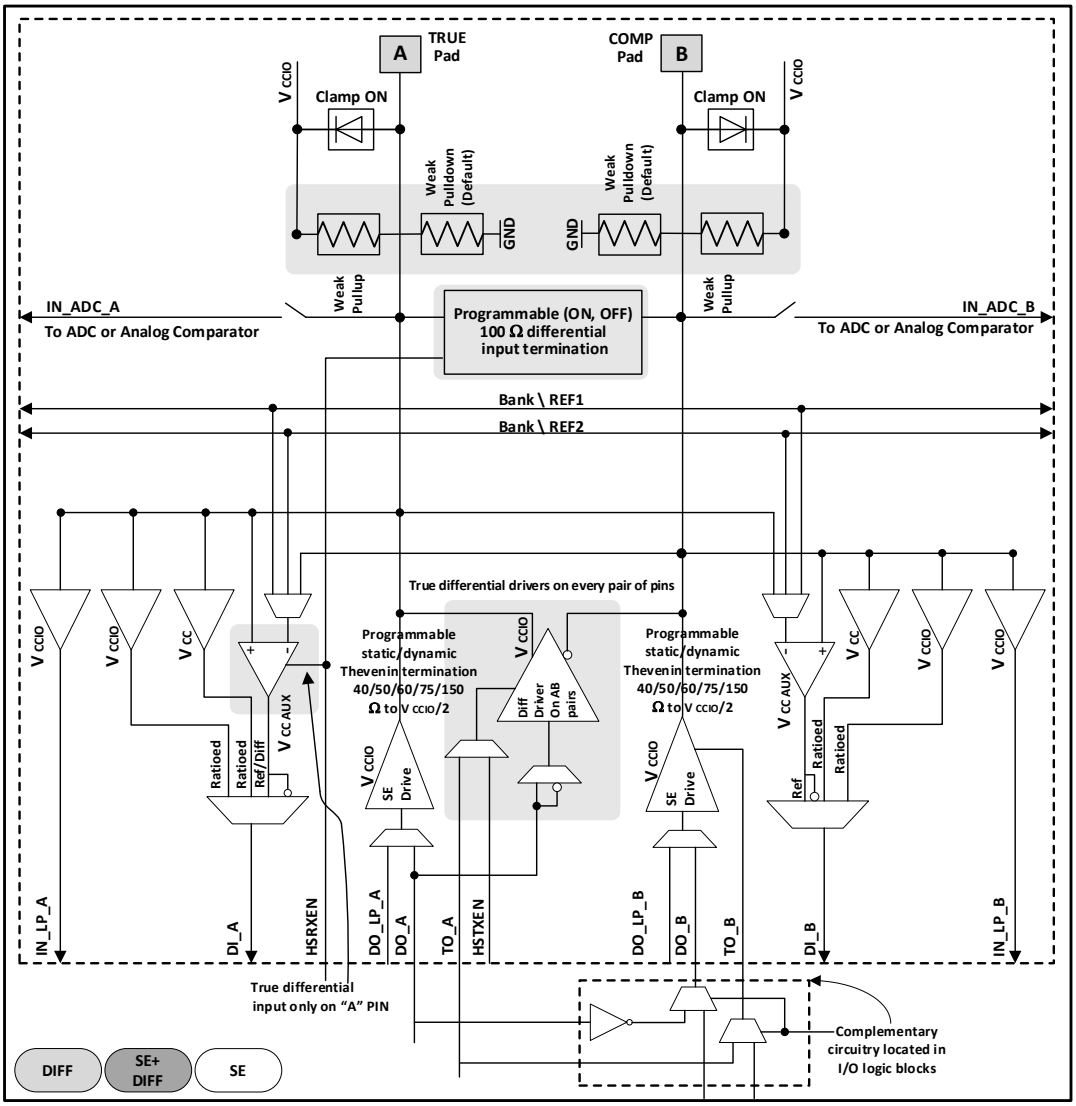

Figure 9.1. High-Performance sysI/O Buffer Pair for Bottom Side

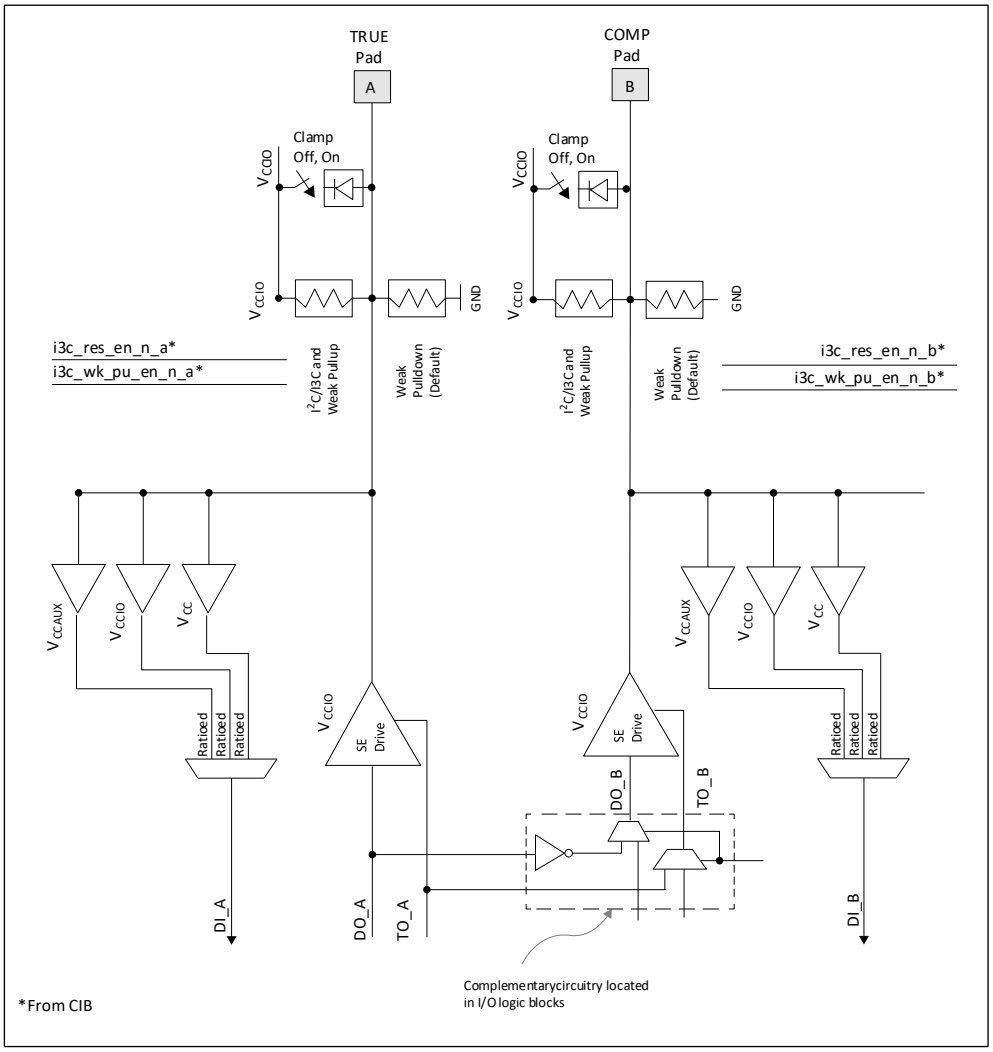

Figure 9.2. Wide-Range sysI/O Buffer for Top and Left/Right Sides

10. Clock Inputs

The CrossLink NX device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O. When these pins are used for clocking purpose, you need to pay attention to minimize signal noise on these pins. Refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).

These shared clock input pins, typically labeled GPLL and PCLK, can be found under the *Dual Function* column of the *pinlist csv* file. High speed differential interfaces (such as MIPI) received by the FPGA device must route their differential clock pair into a pair of inputs that support differential clocking, labeled as PCLKTx_y (+true) and PCLKCx_y (–complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA device, you have to ensure that the oscillator's output voltage to the FPGA device does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

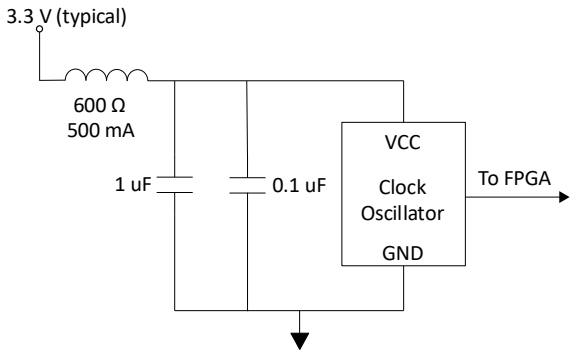

Figure 10.1. Clock Oscillator Bypassing

It is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO} for differential clock inputs to banks with V_{CCIO} voltage of 1.5 V and lower. An LVDS oscillator can also be used if AC coupled and then DC biased at half of the V_{CCIO} voltage. An example of a dual footprint design supporting HCSL and LVDS is as shown in Figure 10.2.

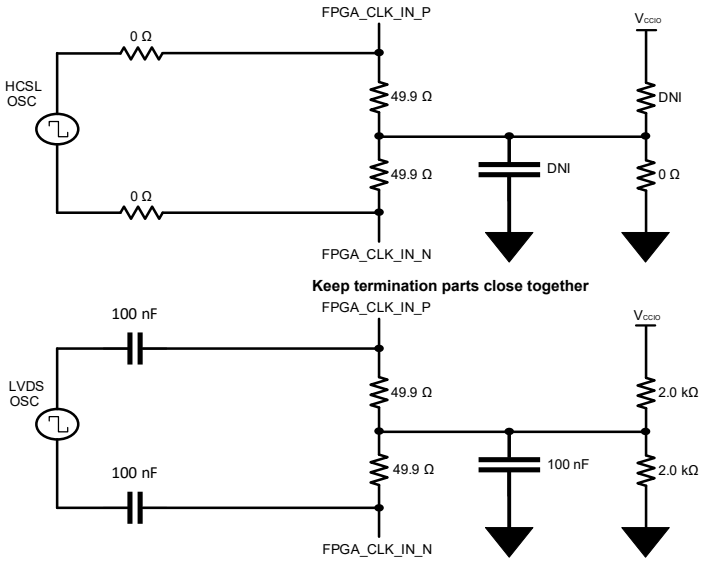

Figure 10.2. PCB Dual Footprint Design Supporting HCSL and LVDS Oscillators

10.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enabled pin is shown in Figure 10.3.

Note: External board oscillators typically require 5 to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

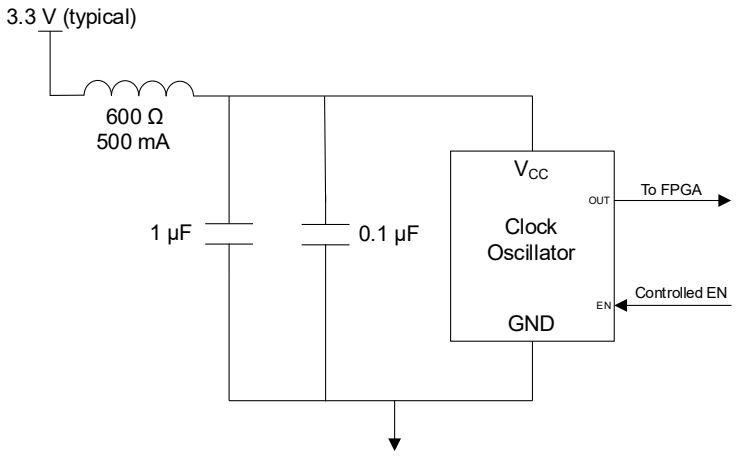

Figure 10.3. Clock Oscillator with Controlled Enable Pin

11. Pinout Considerations

The CrossLink-NX device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097) for rules pertaining to these interface types.

12. LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins on the bottom side of the devices. Top, left, and right side I/O banks do not support True LVDS standard, but can support emulated LVDS outputs. True LVDS input pairing on bottom banks can be found under the High-Speed column in the pinlist csv file.

Emulated LVDS output is available on pairs around all banks, but this requires external termination resistors. This is described in CrossLink-NX Family Data Sheet (FPGA-DS-02049).

13. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards require an external reference voltage. HSUL and SSTL are supported on the device bottom banks only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

14. DPHY and SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly matched differential routing with very few discontinuities.

The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. Refer to High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance.

15. Layout Recommendations

A good design from schematic should also reflect with a good layout for the system design to work without any issues on noise and power distribution. Below are some recommended layouts in general:

1. All power should come from power planes to ensure good power delivery and thermal stability.
2. Each power pin should have its own decoupling capacitor, typically 100 nF, and should be placed as close as possible to each other.
3. Placement of analog circuits must be away from digital circuits or high switching components.
4. High speed signals should have a clearance of five times trace width from other signals.
5. High speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are ground. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}). See Figure 15.1 for details.

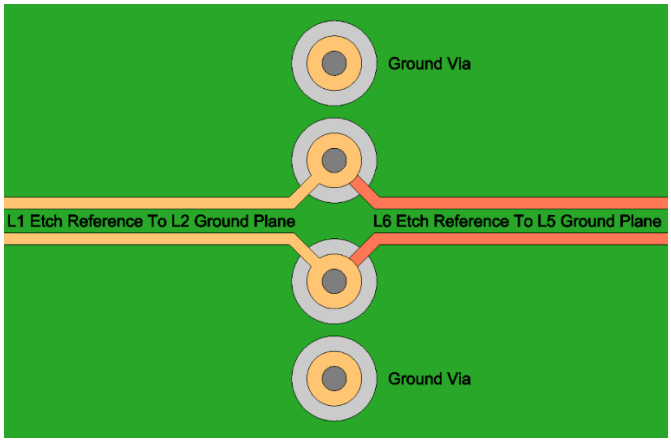

Figure 15.1. Ground Vias Implementation

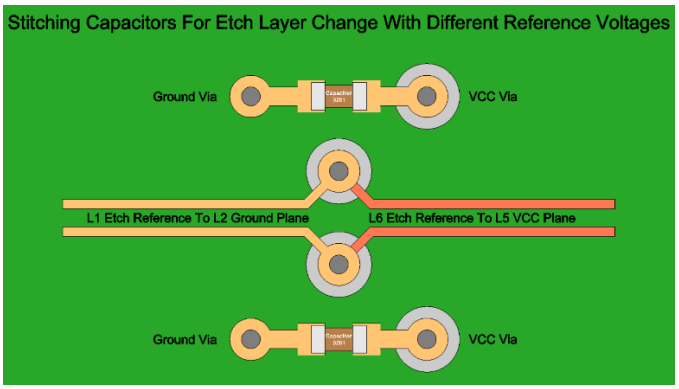

Figure 15.2. Stitching Vias Implementation

6. High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.
7. For differential pairs, make sure to match the length as close as possible. A good rule of thumb is to match up to ±5 mils.

Refer to the following documents for further information on layout recommendations:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

16. Checklist

Table 16.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{CC} core at 1.0 V ±5%		
1.1.2	Use a PCB plane for V_{CC} core with proper decoupling		
1.1.3	V_{CC} core sized to meet power requirement calculation from software		
1.1.4	V_{CCAUX} and $V_{CCAUXH3/H4/H5}$ at 1.8 V –3%/+5%		
1.1.5	V_{CCAUXA} at 1.8 V at 1.8 V –3%/+5%		
1.1.6	V_{CCAUXA} *quiet* and *isolated*		
1.1.7	V_{CCAUXA} pins should be ganged together. A solid PCB plane is recommended, and this plane should not have adjacent non- SerDes signals passing above or below. It should also be isolated from the V_{CC} core power plane.		
1.2	I/O Supplies		
1.2.1	All *Wide Range* V_{CCIO} (Banks 0,1,2,6,7) are between 1.2 V to 3.3 V		
1.2.2	All *High Performance* (Bank 3,4,5) V_{CCIO} are between 1.0 V to 1.8 V		
1.2.3	All Configuration V_{CCIO} (Banks 0,1), when used with configuration interfaces (for example, memory devices), need to match specifications.		
1.2.4	$V_{CCIO[7:2]}$ used based on user design		
1.3	DPHY power supplies		
1.3.1	$V_{CCDPHY[1:0]}$ are 1.0 V +5%		
1.3.2	$V_{CCADPHY[1:0]}$ are 1.8 V +5%		
1.3.3	$V_{CCADPHY[1:0]}$ *quiet* and *isolated*		
1.3.4	$V_{CCPLLDPHY[1:0]}$ are 1.0 V +5%		
1.3.5	$V_{CCPLLDPHY[1:0]}$ *quiet* and *isolated*		
1.4	ADC power supplies		
1.4.1	$V_{CCADC18}$ is 1.8 V +5%		
1.4.2	$V_{CCADC18}$ *quiet* and *isolated*		
1.5	SerDes Power Supplies		
1.5.1	V_{CCSD0} are at 1.0 V ±5%		
1.5.2	$V_{CCPLLSD0}$ and $V_{CCAUXSD}$ are 1.8 V +5%		
1.5.3	$V_{CCPLLSD0}$ and $V_{CCAUXSD}$ *quiet* and *isolated* from each other and other 1.8 V supplies		
2	**JTAG**		
2.1	Pull-up or Pull-down on JTAG_EN, per Table 6.2.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development		
2.4	Pull-down on TCK per Table 6.1.		
2.5	Pull-up on TMS per Table 6.1.		
3	**Configuration**		
3.1	Pull-ups or pull-downs on persisted configuration specific pins per Table 6.1 and Table 6.2		
3.2	V_{CCIO0}, V_{CCIO1} bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
4	**Special Pin Assignments**		
4.1	VREF assignments followed for single-ended SSTL inputs		
4.2	Properly decouple the VREF source		

	Item	OK	NA
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.		
5.4	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
6	**DDR3, DDR3L, and LPDDR2 Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
6.2	Maintain a maximum of ±50 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
6.3	All data groups must reference a ground plane within the stack-up.		
6.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
6.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed)		
6.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched at ±10 mil.		
6.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
6.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched within 10 mil.		
6.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
6.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
6.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
6.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		
7	**External Flash**		
7.1	Flash voltage should match V_{CCIO0} voltage.		
8	**SerDes**		
8.1	Dedicated reference clock input from clock source meets the DC and AC requirements		
8.2	External AC coupling caps may be required for compatibility to common-mode levels		
8.3	Ref clock termination resistors may be needed for compatible signaling levels		
8.4	Maintain good high-speed transmission line routing		
8.5	Continuous ground reference plane to serial channels		
8.6	Tightly length matched differential traces		
8.7	Do not pass other signals on the PCB above or below the high-speed SerDes without isolation.		
8.8	Keep non- SerDes signal traces from passing above or below the VCCA power plane without isolation.		
9	**ADC**		
9.1	When using ADC function, use the Lower Right Corner PLL.		

	Item	OK	NA
10	**Clock Input**		
10.1	External clock source must be connected to PCLK or GPLL pins.		
10.2	PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the PLL Reference Clock Locking section for more details.		

References

- CrossLink-NX web page
- CrossLink-NX Family Data Sheet (FPGA-DS-02049)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL/DLL Design and User Guide for Neus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097)
- Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SerDes (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SerDes Jitter (TN1084)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase

Revision History

Revision 1.7, October 2025

Section	Change Summary
All	Minor editorial fixes.
Abbreviation in This Document	• Replaced *Acronyms* with *Abbreviations*. • Updated section contents.
Introduction	• Added, *Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists*, after the first paragraph of this section. • Removed the statement, *The device family consists of FPGA densities ranging from 17K to 40K Logic Cells.*
CrossLink-NX MIPI D-PHY, SerDes, and PLL Power Supplies	• Updated the ADC_REFP[1:0] notes from If ADC Block not used, *leave it open* to *connect to board ground* in Table 3.1. Recommended Power Filtering Groups and Components. • Updated the Unused SERDES Blocks section. • Moved SDx_REXT to board ground.
Clock Inputs	• Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads.* • Added the PLL Reference Clock Locking section.
Layout Recommendations	Replaced Figure 15.1. Recommended Layout with Figure 15.1. Ground Vias Implementation and Figure 15.2. Stitching Vias Implementation.
Checklist	• Added item 5.4, For single-ended I/Os, use only PCLKT pins as primary CLK pads. • Added *Clock Inputs* under *item 10.*

Revision 1.6, June 2024

Section	Change Summary
All	• Minor editorial fixes. • Changed *I^2C to I2C*. • Changed *Master to Controller*. • Changed *Slave to Target*.
Inclusive Language	Added this section.
CrossLink-NX MIPI D-PHY, SerDes, and PLL Power Supplies	• Updated the recommended filter of VCCPLLSD0 to 220 Ω FB + 47 µF + 470 nF per pin in Table 3.1. Recommended Power Filtering Groups and Components. • Added *Bypass capacitor grounds go only to SDx_REFRET* to VCCAUXSD in Table 3.1. Recommended Power Filtering Groups and Components. • Updated Figure 3.1. Recommended Power Filters to align with the changes of VCCPLLSD0 and VCCAUXSD in Table 3.1. Recommended Power Filtering Groups and Components.

Revision 1.5, April 2024

Section	Change Summary
All	Minor editorial fixes.
CrossLink-NX MIPI D-PHY, SerDes, and PLL Power Supplies	Updated the Unused ADC Blocks to *Connect V_{SSADC}, ADC_REFPx, ADC_DPx, and ADC_DNx pins to board ground. Leave $V_{CCADC18}$ floating (not connected)*.

Revision 1.4, March 2024

Section	Change Summary
Disclaimers	Updated boilerplate.
Acronyms in This Document	Added *ADC*, *FPGA*, *HPIO*, *I/O*, *MIPI*, *PCB*, *WLCSP*, and *WRIO* to the list of acronyms.
Introduction	Added ADC User Guide for Nexus Platform (FPGA-TN-02129) to the list of documents for detailed recommendations.
Power Supplies	Updated the *Voltage* value for the *ADC_REFP[1:0]* in Table 2.1. Single-Ended I/O Standards.

CrossLink-NX MIPI D-PHY, SerDes, and PLL Power Supplies	• Updated the *Recommended Filter* and *Notes* in Table 3.1. Recommended Power Filtering Groups and Components for the following *Power Inputs*:
	  • *ADC_REFP[1:0]*
	  • $V_{CCPLLSD0}$
	• Replaced previous *Figure 3.1. Clock Oscillator Bypassing* with new Figure 3.1. Recommended Power Filters.
	• Removed the following sentences from Clock Oscillator Supply Filtering section:
	  • *A typical bypassing circuit is shown below in Figure 3.1. Clock Oscillator Bypassing.*
	  • *When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the clock oscillator supply pins as practically possible.*
	  • *Good quality capacitors for bypassing generally meet the following requirements:*
	• Moved Dielectric, Voltage Rating, and Size subsections into newly added Capacitor Selection section.
	• Updated the heading numbers of remaining section headers after Capacitor Selection section.
	• Updated the paragraphs of Unused SerDes Blocks section.

Configuration Considerations	• Updated Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins:
	  • Updated *PCB Connection* recommendations for *MCLK* pin .
	  • Added a *Note* for *SCL/SDA* pin.
	• Updated the *Notes* section for Table 6.3. Configuration Pins Needed per Programming Mode1.
	• Added Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI and Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C.
	• Updated the figure number of Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks.

External SPI Flash	Added this section and updated the heading numbers of remaining sections accordingly.
sysI/O	Added this section and updated the heading numbers of remaining sections accordingly.
Clock Inputs	• Updated the paragraphs of this section. • Added Figure 10.1. Clock Oscillator Bypassing and Figure 10.2. PCB Dual Footprint Design Supporting HCSL and LVDS Oscillators.
Layout Recommendations	Added this section and updated the heading numbers of remaining sections accordingly.
Checklist	• Added checklist items *7. External Flash* and *9. ADC*. • Updated checklist number for item *8. SERDES*.
References	Added this section.

Revision 1.3, June 2023

Section	Change Summary
All	Changed SERDES to SerDes.
Checklist	Updated Table 13.1. Hardware Checklist to change row 6 from 'LPDDR3 and DDR3 Interface Requirements' to 'DDR3, DDR3L, and LPDDR2 Interface Requirements'.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Revision 1.2, February 2022

Section	Change Summary
DPHY and SerDes Pin Considerations	Added a line to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.
Checklist	Added a row in Table 13.1 to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.

Revision 1.1, November 2020

Section	Change Summary
Introduction	Updated the titles of some referenced technical notes.

CrossLink-NX MIPI D-PHY, SerDes, and PLL Power Supplies	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  • Added *Combined Together* to V_{CCAUX} and $V_{CCAUXH[5:3]}$ power input.
	  • Updated notes for $V_{CCDPHY[1:0]}$, $V_{CCADPHY[1:0]}$, $V_{CCPLLDPHY[1:0]}$, $V_{CCADC18}$, ADC_REFP[1:0], V_{CCSD0}, $V_{CCPLLSD0}$, and $V_{CCAUXSD}$.
	• Updated descriptions of the following sections: Unused ADC Blocks; Unused SerDes Blocks; and Unused DPHY Banks.

Configuration Considerations	Added paragraph and Figure 6.1. Accommodation for Mixed Voltage Across Configuration Banks.
I/O Pin Assignments	Updated information on power supply pins.
LVDS Pin Assignments	Updated the referenced document and removed the incorrect sentence information.
—	Minor formatting adjustments.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

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