CrossLink-NX Hardened D-PHY Usage Guide

Technical Note

FPGA-TN-02081-1.1

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CIL	Control and Interface Logic
CMOS	Complementary Metal-Oxide Semiconductor
CSI	Camera Serial Interface
DDR	Double Data Rate
DSI	Display Serial Interface
ECLK	Edge Clock
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
PCLK	Primary Clock
PLL	Phase Locked Loops

1. Introduction

The Lattice Semiconductor CrossLink-NX™ device family is specially designed for control, edge processor assist, and edge image bridging and processing. The top of the CrossLink-NX device has two Hardened MIPI® D-PHY interfaces that can be configured as CSI-2 or DSI interface as part of an image bridging and processing solution. These interfaces are pre-defined and characterized and can be generated using the Lattice Radiant® Software. This document describes how to implement the MIPI D-PHY interfaces.

2. MIPI D-PHY Interface

The key video bridging building block in the CrossLink-NX device family are the two Hardened MIPI D-PHY blocks. The Hardened blocks follow MIPI D-PHY specification revision 1.2. The usage of the D-PHY blocks is described in detail in the MIPI D-PHY Receive Interfaces and in the MIPI D-PHY Transmit Interfaces section. The Hardened D-PHY block is referred to as the DPHY primitive in the following discussions. The D-PHY block is automatically configured to transmit or receive based on the Lattice Radiant Software IP Catalog user interface selection.

The features of the integrated D-PHY blocks include:

- Transmit and receive support for both DSI and CSI-2
- Data rate up to 10 Gb/s per quad (2.5 Gb/s per lane)
- Integrated PLL for Transmitter frequency synthesis
- Dynamic switching between high-speed (HS) and low-power (LP modes)
- Integrated serializer and deserializer for 8:1 or 16:1 interfacing with FPGA fabric
- Support for both continuous clock and non-continuous clock (low-power) Receiver and Transmitter modes

The D-PHY blocks contain all the necessary components to move data to/from DSI and CSI-2 data links and the FPGA fabric. In addition to the FPGA fabric, CrossLink-NX includes additional on-chip building blocks such as:

- Generic DDR interface blocks
- General purpose PLL
- Flexible LVDS I/O
- Embedded memory resources

The flexible LVDS banks can also be used to implement D-PHY Tx and Rx, as well as a variety of LVDS and CMOS based standards. By combining these blocks with functions such as Mux, Merge, Duplicate, Scale, and Split implemented in the FPGA fabric and memory resources, CrossLink-NX can support a wide variety of video bridging applications.

3. MIPI D-PHY Receive Interfaces

The CrossLink-NX device family provides two Hardened D-PHY blocks, which support both Receiver and Transmitter.

3.1. MIPI DSI Receive Interface – Hardened D-PHY Module

The Hardened D-PHY blocks can be configured as DSI Receive interfaces based on the Lattice Radiant Software IP Catalog user interface selection.

- The DPHY primitive is used to receive MIPI DSI data (up to four lanes) and clock.
- The HS_RX_EN_I signal is used to enable high-speed mode.
- Figure 3.1 and Figure 3.2 show the signals connected to the fabric when the Hardened D-PHY is configured for DSI receive mode. The Lattice Radiant Software IP Catalog user interface settings automatically power down unused lanes of the Hardened D-PHY.
- The gearing mode of x8 and x16 are available and is selected through the Lattice Radiant Software IP Catalog user interface.
- The D-PHY outputs the received, deserialized data on the HS_RX_DATA_O port. The width of this port depends on the number of data lanes and the gearing ratio. This data should be connected to the fabric and synchronized to the CLK_BYTE_O signal.
- The Hardened D-PHY includes an integrated PLL block. This is powered down when in DSI receive mode.
- The PD_DPHY_I port can be used to power down the D-PHY.

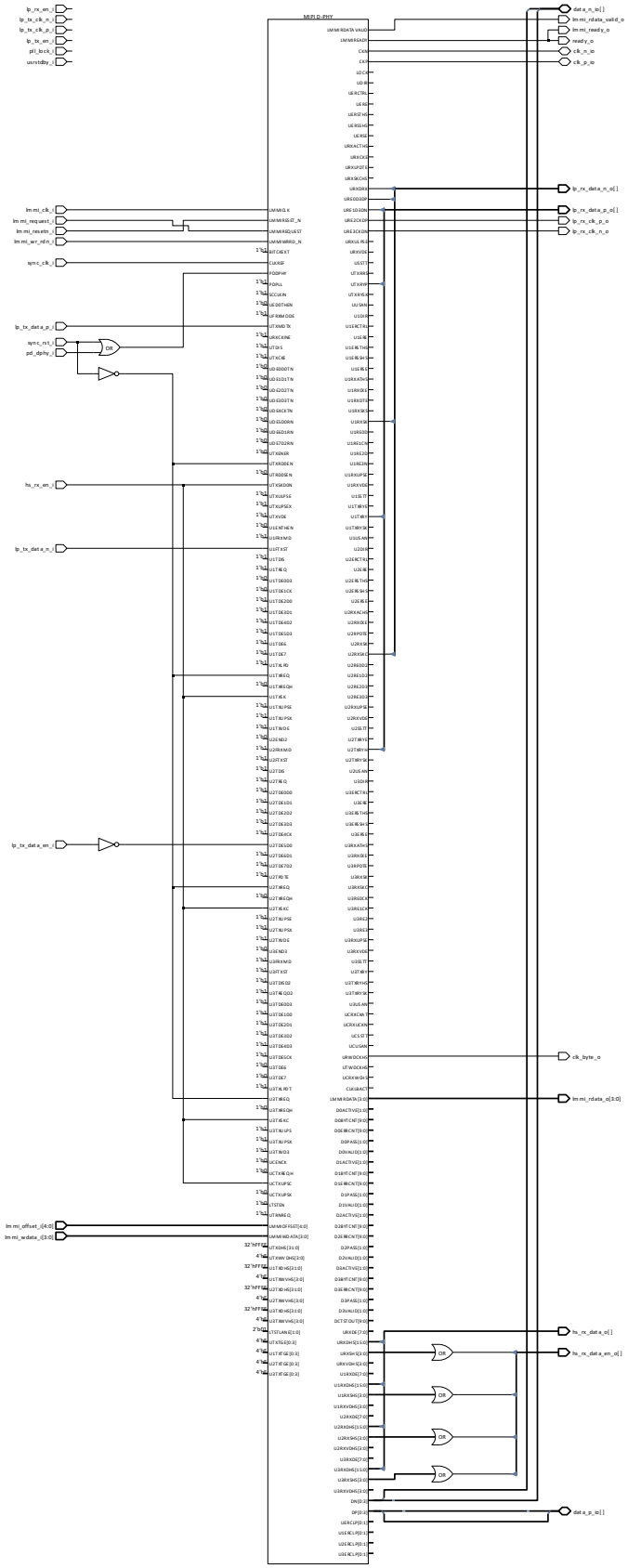

Figure 3.1. MIPI DSI Receive Interface with No CIL – Hardened D-PHY Module

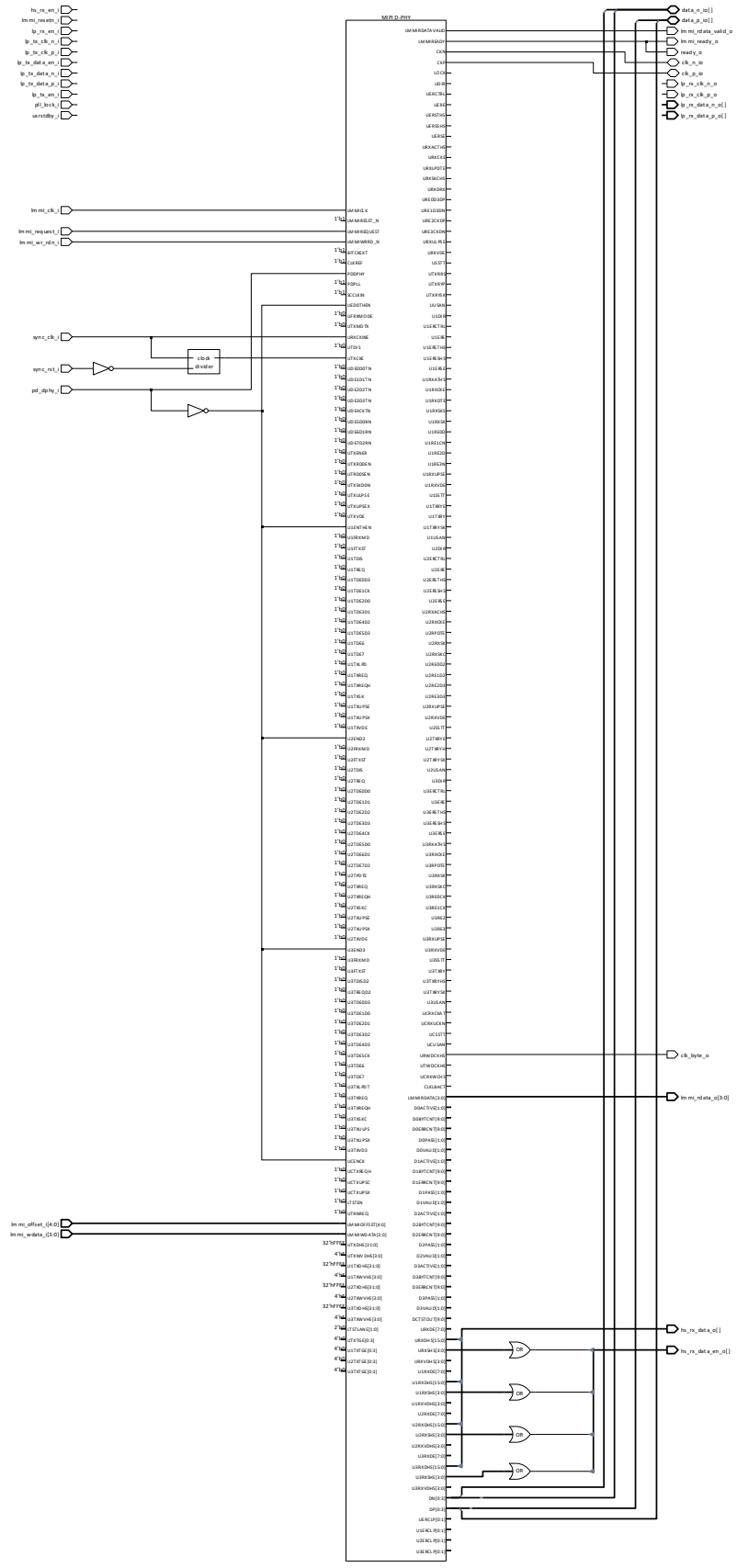

Figure 3.2. MIPI DSI Receive Interface with CIL – Hardened D-PHY Module

Table 3.1. Hardened MIPI DPHY – DSI Receive Interface Port List

Pin Name	I/O	Description	CIL	NO CIL
HS_RX_EN_I	I	High speed receiver enable signal	√	√
LMMI_CLK_I	I	LMMI interface clock	√	√
LMMI_OFFSET_I	I	Register offset, starting at offset 0	√	√
LMMI_REQUEST_I	I	Start transaction	√	√
LMMI_RESETN_I	I	Active LOW. Reset the configuration registers	√	√
LMMI_WDATA_I	I	Write data	√	√
LMMI_WR_RDN_I	I	Write = HIGH, Read = LOW	√	√
LP_RX_EN_I	I	Low power receiver enable signal	—	√
LP_TX_CLK_N_I	I	Low power transmitter negative data input	√	√
LP_TX_CLK_P_I	I	Low power transmitter positive data input	√	√
LP_TX_DATA_EN_I	I	Low power transmitter enable signal	√	√
LP_TX_DATA_N_I	I	Low power transmitter negative data input	√	√
LP_TX_DATA_P_I	I	Low power transmitter positive data input	√	√
LP_TX_EN_I	I	Low power transmitter enable signal	√	√
PD_DPHY_I	I	Active HIGH. Power down input for PHY.	√	√
PLL_CLKOP_I	I	PLL main output clock input	√	√
PLL_CLKOS_I	I	PLL output clock input	√	√
PLL_LOCK_I	I	PLL lock input	√	√
SYNC_CLK_I	I	Clocks GDDR_SYNC	√	√
SYCN_RST_I	I	Active HIGH. Synchronized reset for GDDR_SYNC.	√	√
CLK_BYTE_O	O	Geared down byte clock from D-PHY clock. Only active when the data lanes are in high-speed mode.	√	√
CLK_N_IO	I/O	MIPI input/output negative clock	√	√
CLK_P_IO	I/O	MIPI input/output positive clock	√	√
DATA_N_IO	I/O	MIPI input/output negative data	√	√
DATA_P_IO	I/O	MIPI input/output positive data	√	√
HS_RX_DATA_O	O	High-Speed receive data	√	√
HS_RX_DATA_SYNC_O	O	Receiver synchronization observed	√	√
LMMI_RDATA_O	O	Read data	√	√
LMMI_RDATA_VALID_O	O	Read transaction completed. LMMI_RDATA_O contains valid data.	√	√
LMMI_READY_O	O	Ready to start a new transaction	√	√
LP_RX_CLK_N_O	O	Low power receiver negative clock output	—	√
LP_RX_CLK_P_O	O	Low power receiver positive clock output	—	√
LP_RX_DATA_N_O	O	Low power receiver negative data output	—	√
LP_RX_DATA_P_O	O	Low power receiver positive data output	—	√
READY_O	O	Indicates the state of GDDR_SYNC	√	√

Interface Requirements:

- The DPHY primitive should be mapped to one of the available Hardened D-PHY blocks on the CrossLink-NX device. This is done using the *ldc_set_location* preference shown below.
- ldc_set_location –site *Pin_Number* [get_ports *Port_Name*]
- Example Constraint for LIFCL-17 csfBGA121 MIPI DPHY0:

```
ldc set location -site {C11} [get ports clk p i]
ldc set location -site {C10} [get ports clk n i]
ldc set location -site {D11} [get ports d0 p i]
ldc_set_location -site {D10} [get_ports d0_n_i]
```

  See Appendix A. Hardened D-PHY Pinout for the DPHY pinout for different packages.
- The output of the module CLK_BYTE_O should be connected to primary clock tree.

3.2. MIPI CSI-2 Receive Interface – Hardened D-PHY Module

The Hardened D-PHY blocks can be configured as CSI-2 Receive interfaces based on the Lattice Radiant Software IP Catalog user interface selection.

- The DPHY primitive is used to receive MIPI CSI-2 data (up to four lanes) and clock.
- The HS_RX_EN_I signal is used to enable high-speed mode.
- Figure 3.3 and Figure 3.4 show the signals connected to the fabric when the Hardened D-PHY is configured for CSI-2 receive mode. The Lattice Radiant Software IP Catalog user interface settings automatically powers down unused lanes of the Hardened D-PHY.
- The gearing mode of x8 and x16 are available and the gearing mode is selected through the Lattice Radiant Software IP Catalog user interface.
- The D-PHY outputs the received, deserializes data on HS_RX_DATA_O port. The width of this port depends on the number of data lanes and the gearing ratio. This data should be connected to the fabric and synchronized to the CLK_BYTE_O signal.
- The Hardened D-PHY includes an integrated PLL block. This is powered down when in CSI-2 receive mode.
- The PD_DPHY_I port can be used to power down the D-PHY.

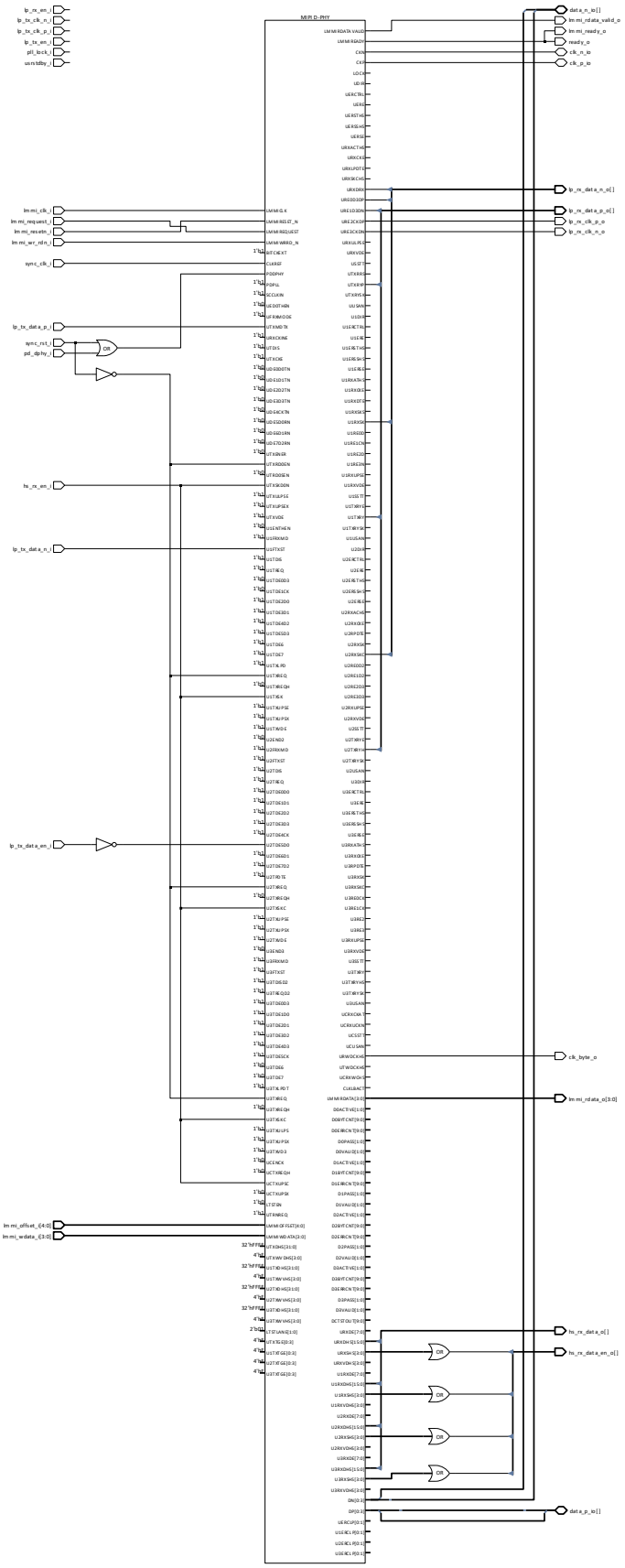

Figure 3.3. MIPI CSI-2 Receive Interface with No CIL – Hardened D-PHY Module

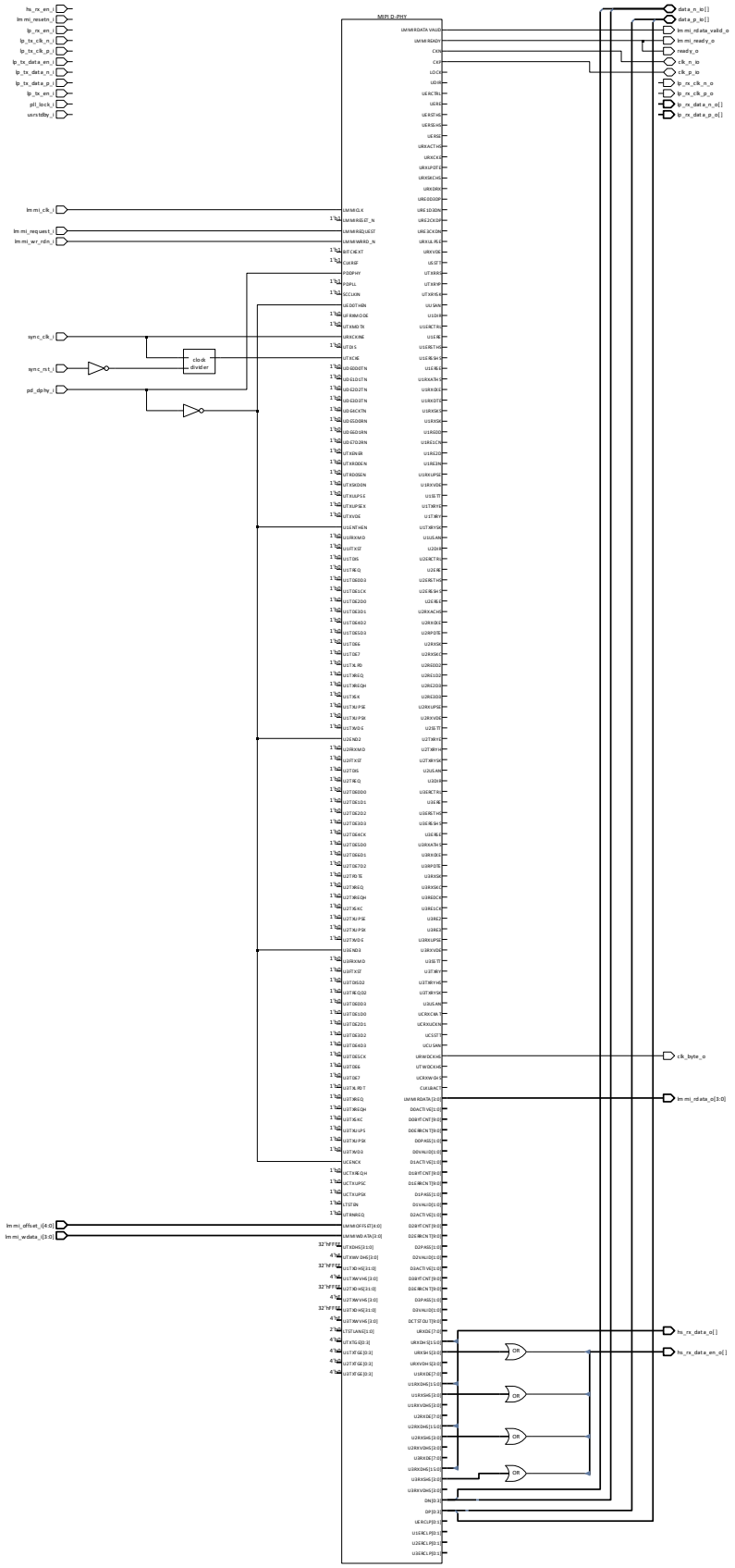

Figure 3.4. MIPI CSI-2 Receive Interface with CIL – Hardened D-PHY Module

Table 3.2. Hardened MIPI DPHY – CSI-2 Receive Interface Port List

Pin Name	I/O	Description	CIL	NO CIL
HS_RX_EN_I	I	High speed receiver enable signal	√	√
LMMI_CLK_I	I	LMMI interface clock	√	√
LMMI_OFFSET_I	I	Register offset, starting at offset 0	√	√
LMMI_REQUEST_I	I	Start transaction	√	√
LMMI_RESETN_I	I	Active LOW. Reset the configuration registers	√	√
LMMI_WDATA_I	I	Write data	√	√
LMMI_WR_RDN_I	I	Write = HIGH, Read = LOW	√	√
LP_RX_EN_I	I	Low power receiver enable signal	—	√
PD_DPHY_I	I	Active HIGH. Power down input for PHY	√	√
PLL_CLKOP_I	I	PLL main output clock input	√	√
PLL_CLKOS_I	I	PLL output clock input	√	√
PLL_LOCK_I	I	PLL lock input	√	√
SYNC_CLK_I	I	Clocks GDDR_SYNC	√	√
SYCN_RST_I	I	Active HIGH. Synchronized reset for GDDR_SYNC.	√	√
CLK_BYTE_O	O	Geared down byte clock from D-PHY clock. Only active when the data lanes are in high-speed mode.	√	√
CLK_N_IO	I/O	MIPI input/output negative clock	√	√
CLK_P_IO	I/O	MIPI input/output positive clock	√	√
DATA_N_IO	I/O	MIPI input/output negative data	√	√
DATA_P_IO	I/O	MIPI input/output positive data	√	√
HS_RX_DATA_O	O	High-Speed receive data	√	√
HS_RX_DATA_SYNC_O	O	Receiver synchronization observed	√	√
LMMI_RDATA_O	O	Read data	√	√
LMMI_RDATA_VALID_O	O	Read transaction completed. LMMI_RDATA_O contains valid data.	√	√
LMMI_READY_O	O	Ready to start a new transaction	√	√
LP_RX_CLK_N_O	O	Low power receiver negative clock output	—	√
LP_RX_CLK_P_O	O	Low power receiver positive clock output	—	√
LP_RX_DATA_N_O	O	Low power receiver negative data output	—	√
LP_RX_DATA_P_O	O	Low power receiver positive data output	—	√
READY_O	O	Indicates the state of GDDR_SYNC	√	√

Interface Requirements:

- The DPHY primitive should be mapped to one of the available Hardened D-PHY blocks on the CrossLink-NX device. This is done using the *ldc_set_location* preference shown below.
- ldc_set_location –site *Pin_Number* [get_ports *Port_Name*]
- Example Constraint for LIFCL-17 csfBGA121 MIPI DPHY0:

```
ldc_set_location -site {C11} [get_ports clk_p_i]
ldc_set_location -site {C10} [get_ports clk_n_i]
ldc_set_location -site {D11} [get_ports d0_p_i]
ldc_set_location -site {D10} [get_ports d0_n_i]
```

  See Appendix A. Hardened D-PHY Pinout for the DPHY pinout for different packages.
- The output of the module CLK_BYTE_O should be connected to primary clock tree.

4. MIPI D-PHY Transmit Interfaces

4.1. MIPI DSI Transmit Interface – Hardened D-PHY Module

The Hardened D-PHY blocks can be configured as DSI Transmit interfaces based on the Lattice Radiant Software IP Catalog user interface selection.

- The DPHY primitive is used to transmit MIPI DSI data (up to 4 lanes) and clock.
- The HS_TX_EN_I signal is used to enable high-speed mode.
- Figure 4.1 and Figure 4.2 show the signals connected to the fabric when the Hardened D-PHY is configured for DSI transmit mode. The Lattice Radiant Software IP Catalog user interface settings automatically powers down unused lanes of the Hardened D-PHY.
- The gearing mode of x8 and X16 are available and the gearing mode is selected through the Lattice Radiant Software IP Catalog user interface.
- The D-PHY serializes and transmits data from the HS_TX_DATA_I port. The width of this port depends on the number of data lanes and the gearing ratio. This data should be driven from the fabric and should be synchronized to the CLK_BYTE_O signal.
- The Hardened D-PHY includes an integrated PLL block. The PLL is used to generate clocks required to transmit the data and the clock. The PLL settings are generated automatically by the MIPI D-PHY IP. A reference clock is provided to the PLL input. The reference clock may be sourced from an external dedicated pin or a primary clock net on the device. The PLL also provides a PLL_LOCK_O indicator signal.
- The USRSTDBY_I port can be used to power down the D-PHY.

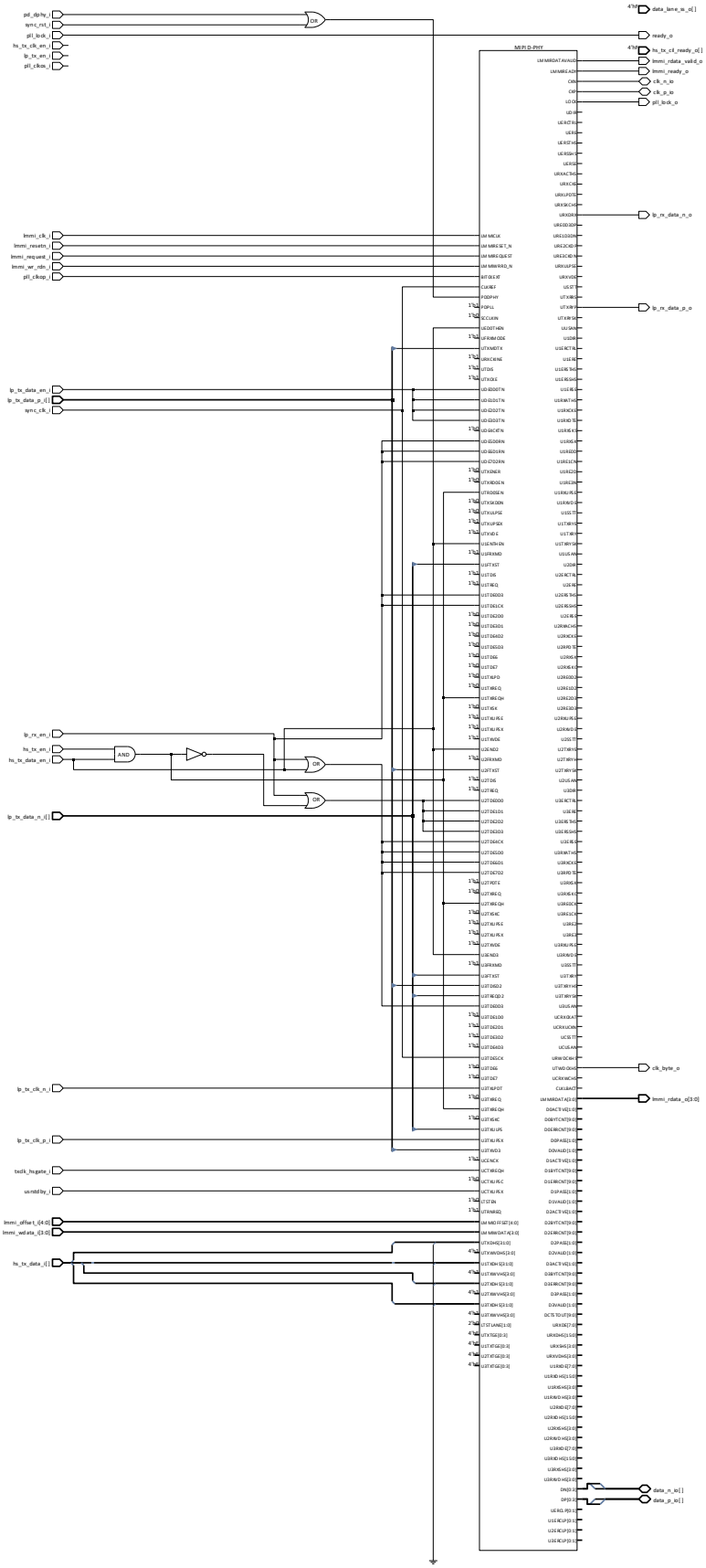

Figure 4.1. MIPI DSI Transmit Interface with No CIL – Hardened D-PHY Module

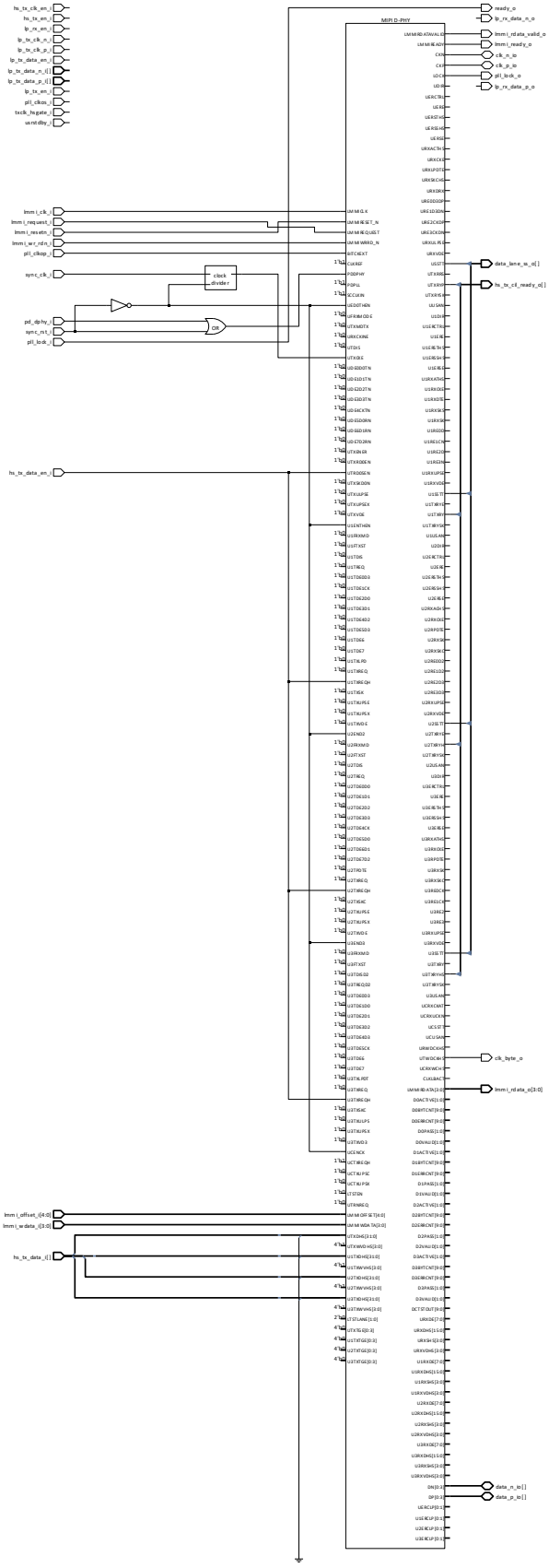

Figure 4.2. MIPI DSI Transmit Interface with CIL – Hardened D-PHY Module

Table 4.1. Hardened MIPI DPHY – DSI Transmit Interface Port List

Pin Name	I/O	Description	CIL	NO CIL
HS_TX_DATA_EN_I	I	High speed transmit data enable	√	√
HS_TX_DATA_I	I	High speed transmit data	√	√
HS_TX_EN_I	I	High speed transmit mode enable	√	√
LMMI_CLK_I	I	LMMI interface clock	√	√
LMMI_OFFSET_I	I	Register offset, starting at offset 0	√	√
LMMI_REQUEST_I	I	Start transaction	√	√
LMMI_RESETN_I	I	Active low signal to reset the configuration registers	√	√
LMMI_WDATA_I	I	Write data	√	√
LMMI_WR_RDN_I	I	Write = HIGH, Read = LOW	√	√
LP_RX_EN_I	I	Low power receiver mode enable	—	√
LP_TX_CLK_N_I	I	Low power transmit negative clock lane	√	√
LP_TX_CLK_P_I	I	Low power transmit positive clock lane	√	√
LP_TX_DATA_EN_I	I	Low power transmit data enable	√	√
LP_TX_DATA_N_I	I	Low power transmitter negative data input	√	√
LP_TX_DATA_P_I	I	Low power transmitter positive data input	√	√
PD_DPHY_I	I	Power down for D-PHY	√	√
PLL_CLKOP_I	I	PLL main output clock input	√	√
PLL_CLKOS_I	I	PLL output clock input	√	√
PLL_LOCK_I	I	PLL lock input	√	√
SYNC_CLK_I	I	GDDR SYNC reference clock	√	√
SYNC_RST_I	I	GDDR SYNC reset	√	√
USRSTDBY_I	I	User standby for PLL and D-PHY	√	√
CLK_BYTE_O	O	Byte clock	√	√
CLK_N_IO	I/O	MIPI input/output negative clock	√	√
CLK_P_IO	I/O	MIPI input/output positive clock	√	√
DATA_N_IO	I/O	MIPI input/output negative data	√	√
DATA_P_IO	I/O	MIPI input/output positive data	√	√
LMMI_RDATA_O	O	Read data	√	√
LMMI_RDATA_VALID_O	O	Read transaction is complete and LMMI_RDATA_O contains valid data.	√	√
LMMI_READY_O	O	Slave is ready to start a new transaction. Slave can insert wait states by holding this signal low.	√	√
LP_RX_DATA_N_O	O	Low power receive data negative	—	√
LP_RX_DATA_P_O	O	Low power receive data positive	—	√
PLL_LOCK_O	O	PLL ready	√	√
READY_O	O	Ready from D-PHY or PLL	√	√
DATA_LANE_SS_O	O	Active high signal indicates that the corresponding lane is currently in STOP state	√	—
HS_TX_CIL_READY_O	O	Active high signal indicates that TxDataHS is accepted by the corresponding lane to be serially transmitted	√	—

Interface Requirements:

- The DPHY primitive should be mapped to one of the available Hardened D-PHY blocks on the CrossLink-NX device. This is done using the *ldc_set_location* preference shown below.
- ldc_set_location –site *Pin_Number* [get_ports *Port_Name*]
- Example Constraint for LIFCL-17 csfBGA121 MIPI DPHY0:

```
ldc_set_location -site {C11} [get_ports clk_p_o]
ldc_set_location -site {C10} [get_ports clk_n_o]
ldc_set_location -site {D11} [get_ports d0_p_o]
ldc_set_location -site {D10} [get_ports d0_n_o]
```

  See Appendix A. Hardened D-PHY Pinout for the DPHY pinout for different packages.
  The CLK_BYTE_O output of the module should be connected to the primary clock tree.
- The D-PHY reference clock input can come from one the following sources:
  - I/O pin with MIPI_CLK function
  - Primary clock net

4.2. MIPI CSI-2 Transmit Interface – Hardened D-PHY Module

The Hardened D-PHY blocks can be configured as CSI-2 Transmit interfaces based on the Lattice Radiant Software IP Catalog user interface selection.

- The DPHY primitive is used to transmit MIPI CSI-2 data (up to 4 lanes) and clock.
- The HS_TX_EN_I signal is used to enable high-speed mode.
- Figure 4.3 and Figure 4.4 show the signals connected to the fabric when the Hardened D-PHY is configured for CSI-2 transmit mode. The Lattice Radiant Software IP Catalog user interface settings automatically powers down unused lanes of the Hardened D-PHY.
- The gearing mode of x8 and x16 are available and the gearing mode is selected through the Lattice Radiant Software IP Catalog user interface.
- The D-PHY serializes and transmits data from the HS_TX_DATA_I port. The width of this port depends on the number of data lanes and the gearing ratio. This data should be driven from the fabric and should be synchronized to the CLK_BYTE_O signal.
- The Hardened D-PHY includes an integrated PLL block. The PLL is used to generate clocks required to transmit the data and the clock. The PLL settings are generated automatically by the MIPI D-PHY IP. A reference clock is provided to the PLL input. The reference clock may be sourced from an external dedicated pin or a primary clock net on the device. The PLL also provides a PLL_LOCK_O indicator signal.
- The USRSTDBY_I port can be used to power down the D-PHY.

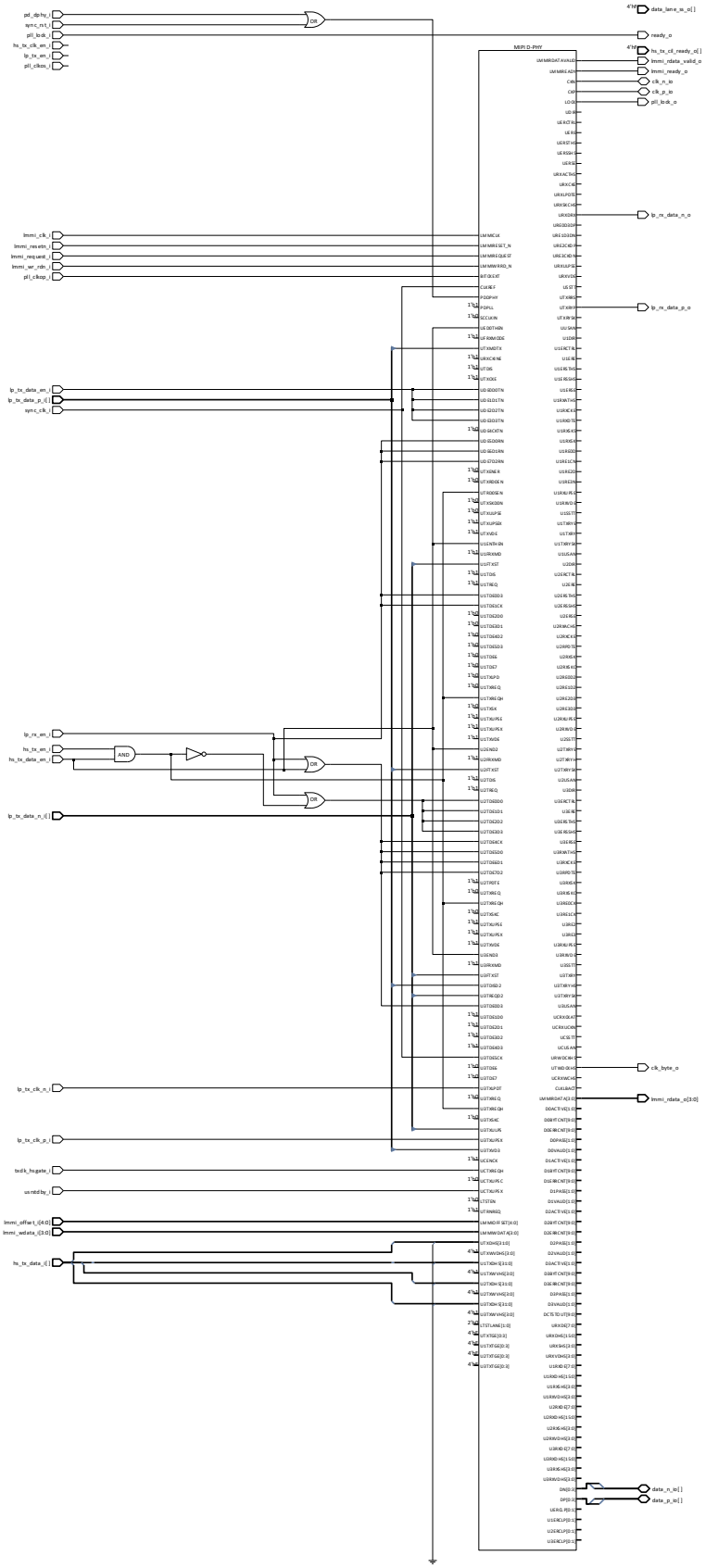

Figure 4.3. MIPI CSI-2 Transmit Interface with No CIL – Hardened D-PHY Module

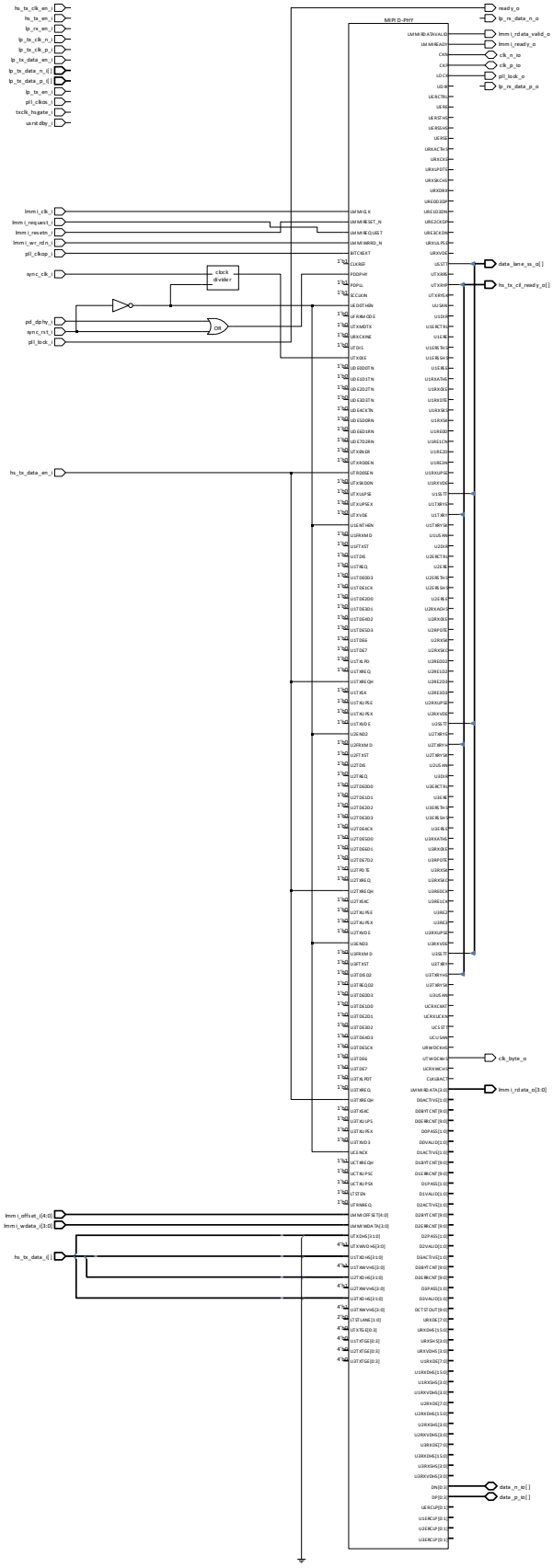

Figure 4.4. MIPI CSI-2 Transmit Interface with CIL – Hardened D-PHY Module

Table 4.2. Hardened MIPI DPHY – CSI-2 Transmit Interface Port List

Pin Name	I/O	Description	CIL	NO CIL
HS_TX_DATA_EN_I	I	High speed transmit data enable	√	√
HS_TX_DATA_I	I	High speed transmit data	√	√
HS_TX_EN_I	I	High speed transmit mode enable	√	√
LMMI_CLK_I	I	LMMI interface clock	√	√
LMMI_OFFSET_I	I	Register offset, starting at offset 0	√	√
LMMI_REQUEST_I	I	Start transaction	√	√
LMMI_RESETN_I	I	Active low signal to reset the configuration registers	√	√
LMMI_WDATA_I	I	Write data	√	√
LMMI_WR_RDN_I	I	Write = HIGH, Read = LOW	√	√
LP_TX_CLK_N_I	I	Low power transmit negative clock lane	√	√
LP_TX_CLK_P_I	I	Low power transmit positive clock lane	√	√
LP_TX_DATA_EN_I	I	Low power transmit data enable	√	√
LP_TX_DATA_N_I	I	Low power transmitter negative data input	√	√
LP_TX_DATA_P_I	I	Low power transmitter positive data input	√	√
PD_DPHY_I	I	Power down for D-PHY	√	√
PLL_CLKOP_I	I	PLL main output clock input	√	√
PLL_CLKOS_I	I	PLL output clock input	√	√
PLL_LOCK_I	I	PLL lock input	√	√
SYNC_CLK_I	I	GDDR SYNC reference clock	√	√
SYNC_RST_I	I	GDDR SYNC reset	√	√
USRSTDBY_I	I	User standby for PLL and D-PHY	√	√
CLK_BYTE_O	O	Byte clock	√	√
CLK_N_IO	I/O	MIPI input/output negative clock	√	√
CLK_P_IO	I/O	MIPI input/output positive clock	√	√
DATA_LANE_SS_O	O	Active high signal indicates that the corresponding lane is currently in STOP state	√	—
DATA_N_IO	I/O	MIPI input/output negative data	√	√
DATA_P_IO	I/O	MIPI input/output positive data	√	√
HS_TX_CIL_READY_O	O	Active high signal indicates that TxDataHS is accepted by the corresponding lane to be serially transmitted	√	—
LMMI_READY_O	O	Slave is ready to start a new transaction. Slave can insert wait states by holding this signal low.	√	√
LMMI_RDATA_O	O	Read data	√	√
LMMI_RDATA_VALID_O	O	Read transaction is complete and LMMI_RDATA_O[3:0] contains valid data.	√	√
PLL_LOCK_O	O	PLL ready	√	√
READY_O	O	Ready from D-PHY or PLL	√	√

Interface Requirements:

- The DPHY primitive should be mapped to one of the available Hardened D-PHY blocks on the CrossLink-NX device. This is done using the *ldc_set_location* preference shown below.
- ldc_set_location –site *Pin_Number* [get_ports *Port_Name*]
- Example Constraint for LIFCL-17 csfBGA121 MIPI DPHY0:

```
ldc_set_location -site {C11} [get_ports clk_p_o]
ldc_set_location -site {C10} [get_ports clk_n_o]
ldc_set_location -site {D11} [get_ports d0_p_o]
ldc_set_location -site {D10} [get_ports d0_n_o]
```

  See Appendix A. Hardened D-PHY Pinout for the DPHY pinout for different packages.
- The CLK_BYTE_O output of the module should be connected to the primary clock tree.
- The D-PHY reference clock input can come from one the following sources:
  - I/O pin with MIPI_CLK function
  - Primary clock net

5. Building MIPI D-PHY Interface Modules

The MIPI D-PHY interfaces are built using Hardened MIPI D-PHY blocks on the top side of the device.

To build MIPI D-PHY Interfaces:

1. In Lattice Radiant Software, go to **IP Catalog.**
2. Select **MIPI_DPHY** under **Module/IP on Local > Module > Architecture_Modules > IO**.
3. Enter instance name and then click **Next** to open the **Module/IP Block Wizard**. Figure 5.1 shows the **Module/IP Block Wizard** for **MIPI_DPHY**.
4. Enter the instance name and click **Next** to configure the IP.

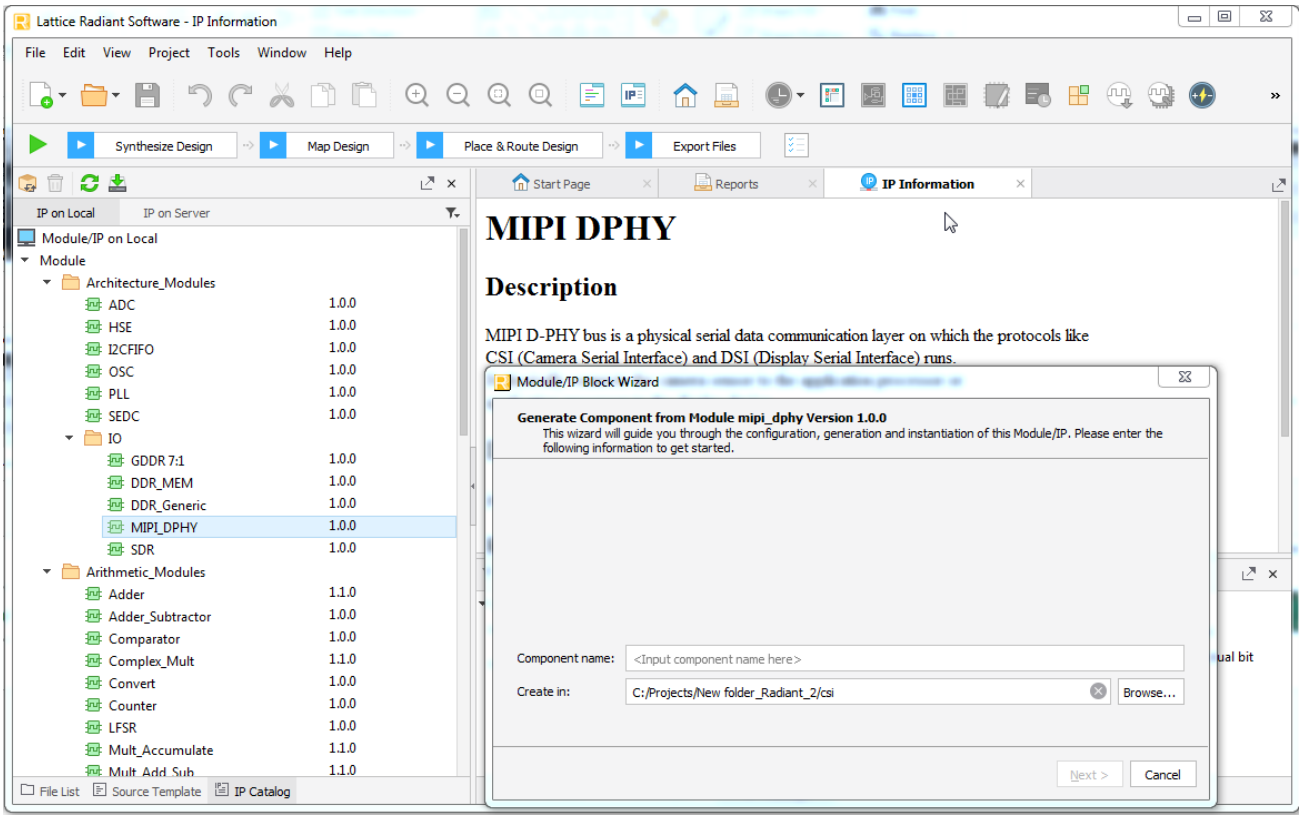

Figure 5.1. MIPI DPHY Selected in IP Catalog

Figure 5.2 shows the main configuration window for MIPI D-PHY interface modules.

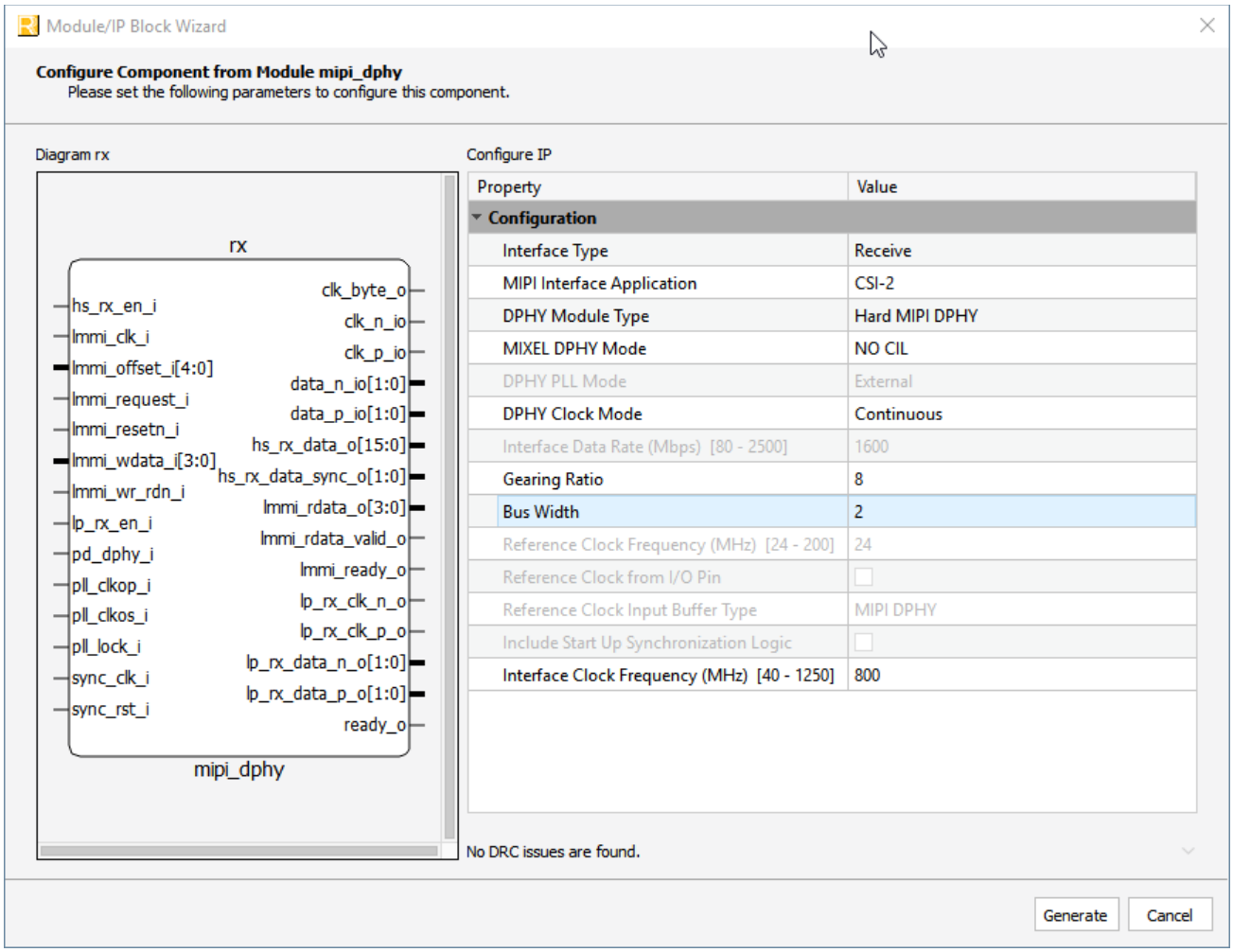

Figure 5.2. MIPI D-PHY Configuration

Table 5.1 lists all the MIPI D-PHY Configurations that can be set in IP Catalog.

Table 5.1. MIPI D-PHY Configuration Parameters

User Interface Option	Description	Values
Interface Type	Direction of MIPI Interface	Transmit, Receive
MIPI Interface Application	Type of MIPI Application	CSI-2, DSI
DPHY Module Type	Type of implementation for MIPI DPHY	Hard MIPI DPHY, Soft MIPI DPHY
MIXEL DPHY Mode	Enable or disable Control & Interface Logic	NO CIL, CIL
DPHY Clock Mode	Continuous (HS) clock or switches between High-Speed and Low-Power modes	Continuous, Non-Continuous
Gearing Ratio	Gearing Ratio selection for the D-PHY Interface	8, 16
Bus Width	Total number of Data Lanes for the D-PHY Interface	1, 2, 4
Interface Clock Frequency	Clock frequency of the Interface	40 MHz – 1250 MHz

Appendix A. Hardened D-PHY Pinout

Table A.1. LIFCL-17 Hardened MIPI DPHY0 Pin Assignment

LIFCL-17	caBGA256	csfBGA121	WLCSP72	QFN72
DPHY0_CKP	D1	C11	A8	68
DPHY0_CKN	D2	C10	B8	69
DPHY0_DP0	E1	D11	A9	4
DPHY0_DN0	E2	D10	B9	3
DPHY0_DP1	C1	B11	B7	66
DPHY0_DN1	C2	B10	C7	67
DPHY0_DP2	F1	E11	C8	1
DPHY0_DN2	F2	E10	C9	2
DPHY0_DP3	B1	A11	C6	64
DPHY0_DN3	B2	A10	D6	65

Table A.2. LIFCL-17 Hardened MIPI DPHY1 Pin Assignment

LIFCL-17	caBGA256	csfBGA121	WLCSP72	QFN72
DPHY1_CKP	A5	A7	N/A	N/A
DPHY1_CKN	B5	B7	N/A	N/A
DPHY1_DP0	A4	A8	N/A	N/A
DPHY1_DN0	B4	B8	N/A	N/A
DPHY1_DP1	A6	A6	N/A	N/A
DPHY1_DN1	B6	B6	N/A	N/A
DPHY1_DP2	A3	A9	N/A	N/A
DPHY1_DN2	B3	B9	N/A	N/A
DPHY1_DP3	A7	A5	N/A	N/A
DPHY1_DN3	B7	B5	N/A	N/A

Table A.3. LIFCL-40 Hardened MIPI DPHY0 Pin Assignment

LIFCL-40	caBGA400	csBGA289	caBGA256	csfBGA121	QFN72
DPHY0_CKP	A2	D1	D1	C11	68
DPHY0_CKN	B1	E2	D2	C10	69
DPHY0_DP0	B2	E1	E1	D11	4
DPHY0_DN0	C1	F2	E2	D10	3
DPHY0_DP1	A3	C1	C1	B11	66
DPHY0_DN1	B3	D2	C2	B10	67
DPHY0_DP2	C2	F1	F1	E11	1
DPHY0_DN2	D1	G2	F2	E10	2
DPHY0_DP3	A4	B1	B1	A11	64
DPHY0_DN3	B4	C2	B2	A10	65

Table A.4. LIFCL-40 Hardened MIPI DPHY1 Pin Assignment

LIFCL-40	caBGA400	csBGA289	caBGA256	csfBGA121	QFN72
DPHY1_CKP	A8	A4	A5	A7	N/A
DPHY1_CKN	B8	B4	B5	B7	N/A
DPHY1_DP0	A7	A3	A4	A8	N/A
DPHY1_DN0	B7	B3	B4	B8	N/A
DPHY1_DP1	A9	A5	A6	A6	N/A
DPHY1_DN1	B9	B5	B6	B6	N/A
DPHY1_DP2	A6	A2	A3	A9	N/A
DPHY1_DN2	B6	B2	B3	B9	N/A
DPHY1_DP3	A10	A6	A7	A5	N/A
DPHY1_DN3	B10	B6	B7	B5	N/A

References

For more information, refer to the following documents:

- CrossLink-NX Family Data Sheet (FPGA-DS-02049)
- CrossLink-NX Hardware Checklist (FPGA-TN-02149)
- CrossLink-NX sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02095)
- CrossLink-NX sysI/O Usage Guide (FPGA-TN-02067)
- CrossLink-NX Memory Usage Guide (FPGA-TN-02094)
- Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075)
- CrossLink-NX I2C Hardened IP Usage Guide (FPGA-TN-02142)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, June 2021

Section	Change Summary
MIPI D-PHY Receive Interface	Updated Interface Requirements sections.
MIPI D-PHY Transmit Interface	Corrected syntax for mapping the DPHY primitive to one of the Hardened D-PHY blocks. Changed *get_ports* to *get_cells*.
Appendix A. Hardened D-PHY Pinout	Added this section.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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