CrossLinkPlus Programming and Configuration User Guide

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CRC	Cyclic Redundancy Check
EBR	Embedded Block RAM
GOE	Global Output Enable
GSR	Global Set Reset
GWDIS	Global Write Disable
I^2C	Inter-Integrated Circuit
LUT	Look Up Table
MSPI	Master Serial Peripheral Interface
OTP	One Time Programmable
POR	Power On Reset
SDM	Self Download Mode
SRAM	Static Random-Access Memory
SSPI	Slave Serial Peripheral Interface
SVF	Serial Vector Format

1. Overview

Lattice Semiconductor CrossLinkPlus™ is an SRAM-based Programmable Logic device that includes an internal Flash Memory, as well as flexible SPI and I^2C configuration modes. CrossLinkPlus provides a rich set of features for the programming and configuration of the FPGA. Many options are available for building the programming solution that fits user needs. This document describes each of the options in detail.

2. CrossLinkPlus Features

The key programming and configuration features of CrossLinkPlus devices include:

- Instant-On configuration from internal Flash – powers up in milliseconds
- Single-chip, secure solution
- Multiple programming and configuration interfaces
  - Self download
  - Slave SPI
  - Master SPI
  - Slave I^2C
- Optional dual boot with external SPI memory
- Optional security bits for design protection

3. Definition of Terms

This document uses the following terms to describe common functions:

- **BIT** – The BIT file is the configuration data for CrossLinkPlus that is stored in an external SPI Flash. It is a binary file and is programmed unmodified into the SPI Flash.
- **Configuration** – Configuration refers to a change in the state of the CrossLinkPlus SRAM memory cells.
- **Configuration Data** – This is the data read from the non-volatile memory and loaded into the FPGA SRAM configuration memory. This is also referred to as a bitstream, or device bitstream.
- **Configuration Mode** – The configuration mode defines the method the CrossLinkPlus device uses to acquire the configuration data from the non-volatile memory.
- **Dummy Byte** – A dummy byte is any data in which the numeric value is considered to be “don’t care”. In some cases, external devices controlling the resident FPGA scan in dummy bytes as a requirement of the protocol.
- **Internal Flash** – The JED file can be programmed directly into the internal Flash. User do not need to know where an actual page of the configuration data starts. The CrossLinkPlus configuration engine handles the parsing of the Flash to SRAM transfer.
- **Number Formats** – The following nomenclature is used to denote the radix of numbers:
  - 0x: Numbers preceded by *0x* are hexadecimal
  - b (suffix): Numbers suffixed with *b* are binary
  - All other numbers are decimal
- **Port** – A port refers to the physical connection used to perform programming and some configuration operations. Ports on the CrossLinkPlus device include SPI and I^2C physical connections.
- **Programming** – Programming refers to the process used to alter the contents of the internal or external non-volatile configuration memory.
- **User Mode** – CrossLinkPlus is in User Mode when configuration is complete, and the FPGA is performing the logic functions it was programmed to perform.
- **XFLASH** – Background programming mode used to program the embedded flash while the device is still in user mode

4. Configuration Process and Flow

Before it is operational, the FPGA goes through a sequence of states, including initialization, configuration, and wake up. Figure 4.1 shows the configuration flow.

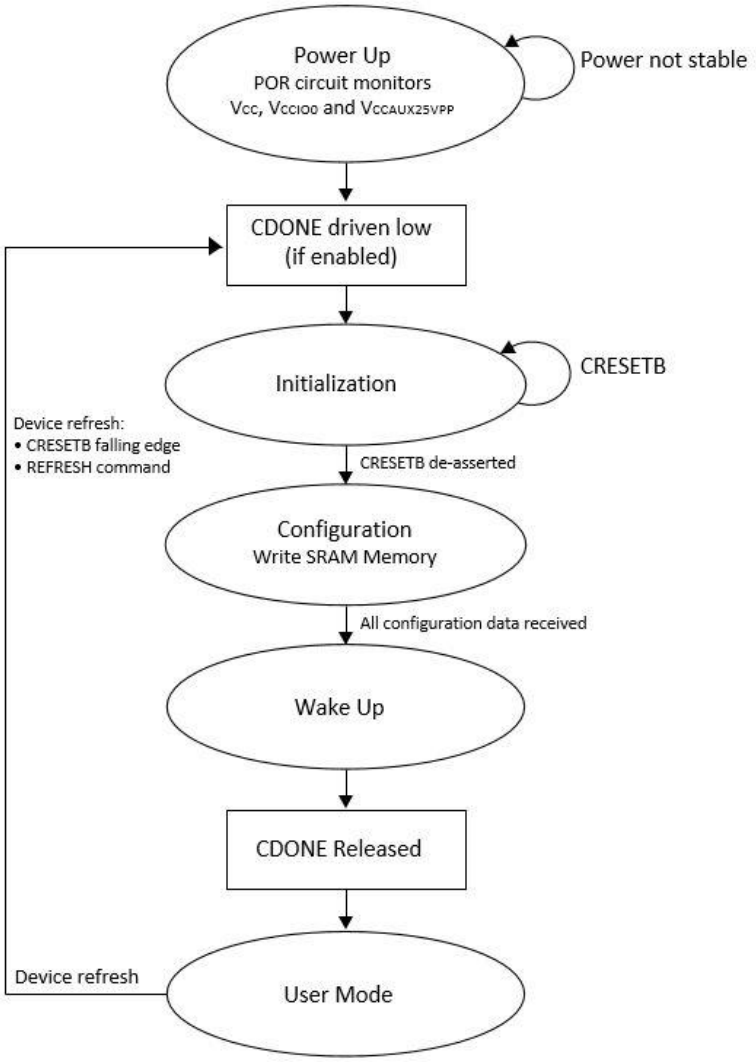

Figure 4.1. Configuration Flow

The CrossLinkPlus sysCONFIG ports provide industry standard communication protocols for programming and configuring the FPGA. Each protocol provides a way to access the CrossLinkPlus device internal Flash, or to load its configuration SRAM.

The sysCONFIG ports capable of accessing the internal Flash have a priority order. The MSPI configuration port does not have the ability to alter the internal Flash space, and as a result is not a factor in the sysCONFIG port priority scheme.

4.1. Power-up Sequence

Power must be applied to the CrossLinkPlus device for it to operate. For a short period of time, as the voltages applied to the system rise, the FPGA has an indeterminate state. Upstream sources should not enable their output until the CrossLinkPlus device has completed its configuration to ensure that the CrossLinkPlus device is operating in a known state.

As power continues to ramp, a Power On Reset (POR) circuit inside the FPGA becomes active. The POR circuit, once active, ensures that the external I/O pins are in a high-impedance state. It also monitors the VCC, VCCIO0, and VCCAUX input rails. Refer to CrossLinkPlus Family Data Sheet (FPGA-DS-02054) for exact Power On Voltage levels.

When POR conditions are met, the POR circuit releases an internal reset strobe, allowing the device to begin its initialization process. CrossLinkPlus drives CDONE LOW during the initialization process.

4.2. Initialization

The CrossLinkPlus device enters the memory initialization phase immediately after the Power On Reset circuit drives the CDONE status pin LOW. The purpose of the initialization state is to clear all of the SRAM memory inside the FPGA.

The FPGA remains in the initialization state until the CRESET_B pin is deasserted HIGH or until after the Slave SPI/Slave I^2C (SSPI/SI^2C) activation code is received.

4.3. Configuration Ports Default Behavior and Arbitration

During power up or when CRESET_B pin toggles from LOW to HIGH, the Configuration Logic puts the device into Master Configuration mode and boots from internal Flash.

The blank CrossLinkPlus device, without any software re-configuration, employs the default BOOT_UP_SEQUENCE of CFG (boot from internal Flash) where the configuration engine attempts to boot from the internal Flash.

Holding CRESET_B LOW postpones the Master Configuration event and allows the slave configuration ports (Slave SPI or Slave I^2C) to detect a *Slave Active* condition.

1. During power up, CRESETB must be asserted (LOW) within 9.5 ms of Power-On-Reset supplies reaching the POR thresholds to prevent the CrossLinkPlus device from entering Master Configuration Mode.
   a. CRESETB can be kept low prior to power up to prevent it from entering Master Configuration Mode.
   b. The activation keys can be sent at any time while CRESETB is asserted (LOW).
2. While in User Mode, CRESETB can be toggled from HIGH to LOW at any time to re-enter Configuration Mode.
   a. The activation key can be sent at any time while CRESETB is asserted (LOW).

Slave Active condition means that the slave port is addressed, the Slave Configuration Port Activation Key (as listed in Table 4.1) is sent, and the Activation Key matches the pre-defined key code. If any slave port declares active before CRESET_B is released HIGH, the device is activated for slave configuration. If no Activation Key is received and CRESETB pin is released HIGH, the device enters Master Configuration Mode and boots from the location specified in the BOOT_UP_SEQUENCE preference.

Table 4.1. Slave Configuration Port Activation Key

Configuration Port	Header	Activation Key
Slave SPI Port	N/A	0xA4C6F48A
Slave I^2C Port	Slave I^2C Port Address Write[1]	0xA4C6F48A

Note: The slave I^2C address could be either 7 bits or 10 bits address.

The I^2C and SPI pins are intentionally shared (MCK/SPI_SCK/SDA and CSN/SPI_SS/SCL) in such a manner as to prevent unintentional activation of either port. For example, a valid I^2C interface can never inadvertently activate the SPI port and vice versa.

4.4. Configuration

The FPGA is able to accept the configuration bitstream created by the Lattice Diamond® development tools.

CrossLinkPlus begins fetching configuration data from non-volatile memory, either the internal Flash, or an external SPI Flash.

The configuration data may be retrieved from the internal Flash, if the BOOT_UP_SEQUENCE is set to CFG, EXT-CFG or CFG-EXT. The configuration data may be retrieved from the external SPI Flash, if the BOOT_UP_SEQUENCE is set to EXT, CFG-EXT, or EXT-CFG.

Note: The MSPI persistence has no effect with the availability of MSPI mode to the configuration engine during device configuration.

CrossLinkPlus does not leave the Configuration state if there are no memories with valid configuration data. In this case, only the SSPI and I^2C modes may be used to program the device when it is in a blank/erased state. An external SPI Master or I2C Master needs to write the Activation Key to the FPGA.

4.5. Wake-up

Wake-up is the transition from the configuration mode to the User Mode. The CrossLinkPlus fixed four-phase Wake-up sequence starts when the device has correctly received all of its configuration data. When all configuration data is received, the FPGA asserts an internal DONE status bit. The assertion of the internal DONE causes a Wake-up state machine to run that sequences the following four controls strobes:

- External CDONE
- Global Write Disable (GWDIS)
- Global Output Enable (GOE)
- Global Set/Reset (GSR)

In the first phase of the Wake-up process at default software settings, the CrossLinkPlus device releases the Global Output Enable and asserts the Global Write Disable.

When Global Output Enable is asserted, it permits the FPGA I/O to exit a high-impedance state and take on their programmed output function. The FPGA inputs are always active. The input signals are prevented from performing any action on the FPGA flip-flops by the assertion of the Global Set/Reset (GSR).

The Global Write Disable is a control that overrides the write enable strobe for all RAM logic inside the FPGA. The inputs on the FPGA are always active, as mentioned in the Global Output Enable section. Keeping GWDIS asserted prevents accidental corruption of the instantiated RAM resources inside the FPGA.

The second phase of the Wake-up process releases the Global Set/Reset and the Global Write Disable controls.

The Global Set/Reset is an internal strobe that, when asserted, causes all I/O flip-flops, Look Up Table (LUT) flip-flops, distributed RAM output flip-flops, and Embedded Block RAM output flip-flops that have the *GSR enabled* attribute to be set/cleared per their hardware description language definition.

The last phase of the Wake-up process is to assert the external CDONE pin. The CDONE pin may also be held LOW externally to delay the User Mode entry in order to synchronize with other devices. This behavior is configurable. See the sysCONFIG Pins**Error! Reference source not found.** section for details on the CDONE pin.

When the final Wake-up phase is complete, the FPGA enters User Mode.

4.6. User Mode

The CrossLinkPlus device enters User Mode immediately when the Wake-up sequence has completed. User Mode is the point in time when CrossLinkPlus begins performing the logic operations designed. The CrossLinkPlus device remains in this state until one of the following occurs:

- CRESET_B input pin is asserted (LOW)
- REFRESH command is received
- ISC_ENABLE command is received
- Power is lost

4.7. Clearing the Configuration Memory and Re-initialization

The current User Mode configuration of CrossLinkPlus remains in operation until it is actively cleared, or power is lost. Several methods are available to clear the CrossLinkPlus internal configuration memory:

- Power cycle the CrossLinkPlus device.
- Execute an ERASE command while in programming mode.

- Toggle the CRESET_B pin from HIGH to LOW. Note that only a HIGH to LOW transition creates a REFRESH command. Keeping CRESET_B LOW does not create a REFRESH event.
- Reinitialize the memory through a REFRESH command. Any active configuration port can be used to send a REFRESH command.

Invoking one of these methods causes the CrossLinkPlus device to drive CDONE LOW. The CrossLinkPlus device enters the initialization state as described earlier.

4.8. Bitstream/PROM Sizes

The CrossLinkPlus device is an SRAM based FPGA. The SRAM configuration memory must be loaded from a non-volatile memory that can store all of the configuration data. The size of the configuration data is variable. It is based on the amount of logic available in the FPGA, and the number of pre-initialized Embedded Block RAM (EBR) components. A CrossLinkPlus design with every EBR pre-initialized with unique data values requires the largest amount of storage (Table 4.2).

Table 4.2. Maximum Configuration Bits

Device	Bitstream Size Without Pre-Initialized EBR	Bitstream Size With Maximum Number of Pre-Initialized EBR	Units
LIF-MDF6000	1.24	1.59	Mb

4.9. Internal Flash Programming

CrossLinkPlus internal Flash can be programmed in two different modes, offline programming, and background programming.

4.9.1. Offline Programming

Offline Programming requires the device to enter into programming mode. When in programming mode, the device stops working until the programming is completed. When using Lattice Diamond Programmer, select Flash Programming Mode under Access Mode. The operations start with FLASH. Unless noted by the operation, the Flash sectors accessed are feature, configuration, and UFM.

4.9.2. Background Programming

Background Programming allows the device to continue operating in User Mode while the configuration logic programs the internal Flash memory. When the internal Flash memory programming is completed, the configuration data can be downloaded into the SRAM with a REFRESH instruction. When using Lattice Diamond Programmer, select Flash Background Mode under Access Mode. The operations starts with XFLASH. Unless noted by the operation, the Flash sectors accessed are configuration and UFM.

4.10. Lock Bits

CrossLinkPlus devices contain security bits that, when set, can control the access of the SRAM configuration and internal Flash spaces. CrossLinkPlus device provides read, write, and erase permission control for each internal Flash sector and SRAM. The Lattice Diamond Programmer GUI allows the following lock options:

- Erase Lock
- Read Lock
- Write Lock

Once one of these options is selected, the corresponding operation is prohibited. The only way to unlock an option is not to lock the Erase Lock. Leaving erase unlock allows one to erase the bitstream and unlock the read and write operations.

4.11. Password

CrossLinkPlus devices support a password-based security access feature that uses a password key to protect the internal Flash. The password key feature requires that a device accessing the CrossLinkPlus device through a sysConfig port to provide a valid digital password to unlock the device and allow configuration or programming operation to proceed. Without a valid password key, the user can only perform rudimentary non-configuration operations, such as Read Device ID.

4.12. sysCONFIG Pins

The CrossLinkPlus device provides a set of sysCONFIG I/O pins to program and configure the FPGA. The sysCONFIG pins are grouped together to create ports, SSPI, I^2C, MSPI, that are used to interact with the FPGA for programming, configuration, and access of resources inside the FPGA. The sysCONFIG pins in a configuration port group may be active, and used for programming the FPGA, or they can be reconfigured to act as general purpose I/O.

Recovering the configuration port pins for use as general purpose I/O requires adhering to the following guidelines:

- User must DISABLE the unused port. User can accomplish this by using the Global Preferences tab of the Diamond Spreadsheet View. Each configuration port is listed in the sysCONFIG options tree.

Table 4.3 lists the default state of the shared sysCONFIG pins. A device with an erased/HW default Feature Row has the Slave SPI port enabled. Upon entry to User Mode, the state of the SSPI and I^2C ports is determined by the sysCONFIG port settings. The software default sysCONFIG port setting is SSPI enabled while I^2C is disabled. This means user lose the ability to program the CrossLinkPlus device using I^2C when using the default sysCONFIG port settings. User must assert CRESET_B to program over I^2C in that case. To retain the I^2C sysCONFIG pins in User Mode, be sure to ENABLE them using the Diamond Spreadsheet View editor.

The sysCONFIG pins are powered by the V_{CCIO0} voltage. It is important to take this into consideration when provisioning other logic attached to Bank 0.

The function of each sysCONFIG pin is described in Table 4.3. The default state of each sysConfig Port is shown in Table 4.4.

Table 4.3. Default State of sysCONFIG Pins

Pin Name	Associated sysCONFIG Port	Pin Function in Feature Row Blank Mode (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function in User Mode (Software Default State)
CRESET_B	SDM	CRESET_B	Input with weak pull up	CRESET_B
CDONE	SDM	I/O	I/O with weak pull up	User-defined I/O
SPI_SCK/MCK/SDA	SSPI/MSPI/I^2C	SSPI/I^2C	Input with weak pull up	SSPI
SPI_SS/CSN/SCL	SSPI/MSPI/IC	SSPI/I^2C	Input with weak pull up	SSPI
MOSI	SSPI/MSPI	SSPI	Input	SSPI
MISO	SSPI/MSPI	SSPI	Output	SSPI

Note: All pins are in Configuration Mode until the device is configured and enters User Mode.

Table 4.4. Default State in Lattice Diamond for Each Port

sysConfig Port	Diamond Default[1]
CDONE_PORT	CDONE_USER_IO
SLAVE_SPI_PORT	Enable
I2C_PORT	Disable
MASTER_SPI_PORT	Disable[2]

Notes:

1. This default setting can be modified in the Global Preferences tab of the Diamond Spreadsheet View.
2. The MASTER_SPI_PORT setting does not influence the behavior during configuration. For details, see the Configuration section.

4.12.1. Self-Download Port Pins

CRESET_B

CRESET_B is an active LOW input with a weak internal pull-up resistor used for configuration of the FPGA. When CRESET_B is asserted LOW, the FPGA exits User Mode and starts a device configuration sequence at the Initialization phase, as described in Table 4.1. Holding the CRESET_B pin LOW during power up (Figure 4.2) keeps the CrossLinkPlus device in the Initialization phase. This LOW period allows an external SPI Master or I^2C Master to write the Activation Key to the FPGA to enter into slave configuration mode. See **Error! Reference source not found.** section for addition d etails. The CRESET_B pin has a minimum pulse width assertion period (Figure 4.3) in order for it to be recognized by the FPGA. The minimum time can be found in the AC timing section of the CrossLinkPlus Family Data Sheet (FPGA-DS-02054).

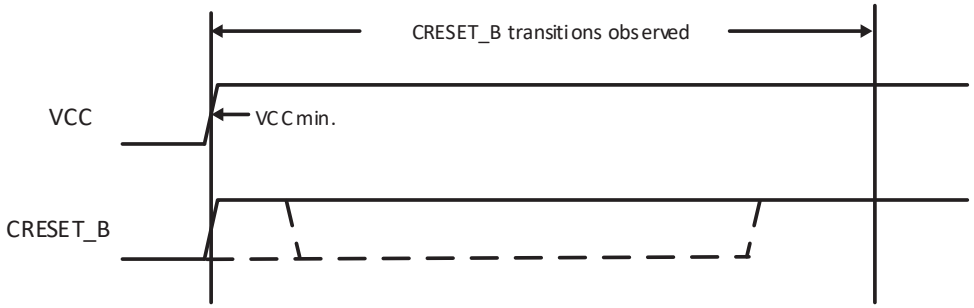

Figure 4.2. Period CRESET_B is Always Observed

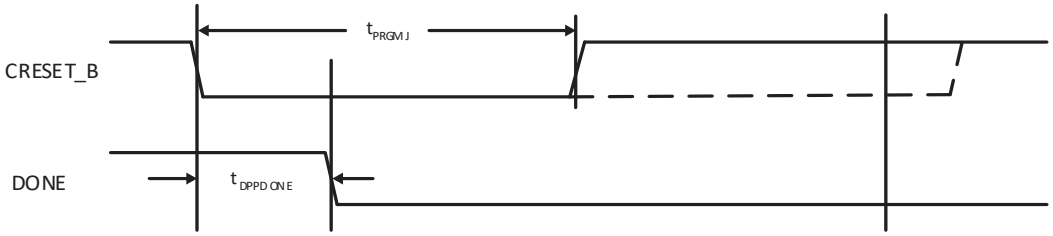

Figure 4.3. Configuration from CRESET_B Timing

If an error is detected when reading the bitstream, the internal DONE bit is not set, the CDONE pin stays LOW, and the device does not wake up. The device configuration fails when the following occurs:

- The bitstream CRC error is detected.
- The invalid command error is detected.
- A timeout error is encountered when loading from the internal Flash.
- The program DONE command is not received when the end of on-chip SRAM configuration or internal Flash is reached.
- Device ID code mismatch.

CDONE

The CDONE pin is a bi-directional open drain with a weak pull-up that signals the FPGA is in User Mode. CDONE is first able to indicate entry into User Mode only after an internal DONE bit is asserted. The internal DONE bit defines the beginning of the FPGA Wake-up state.

The CDONE output pin is controlled by the CDONE_PORT and DONE_EX configuration parameters that are modified in the Diamond Spreadsheet View. By default, the CDONE pin is a general purpose I/O when the CrossLinkPlus device is in the Feature Row HW Default Mode state. The default mode causes the CrossLinkPlus device to automatically pass through the Wake-up sequence after the internal DONE bit is asserted. The FPGA does not delay waking up waiting for the CDONE pin to be asserted high.

The FPGA can be held from entering User Mode indefinitely by having an external agent keep the CDONE pin asserted LOW. In order to use CDONE to delay entering User Mode, the CDONE_PORT must be set to CDONE_ONLY and the DONE_EX set to ON. These settings may be modified from Diamond Spread Sheet View. If DONE_EX = ON, the device waits for CDONE to be driven high by an external signal to wake up. A common reason for keeping CDONE driven LOW is to allow multiple FPGAs to be completely configured. As each FPGA reaches the DONE state, it is ready to begin operation. The last FPGA to be configured can trigger all the FPGAs to start in unison.

The CDONE pin drives LOW when the FPGA enters Initialization Mode. As described earlier, this condition happens when power is applied, CRESET_B is asserted through HIGH to LOW transition or a REFRESH command is received via an active configuration port. Note that CRESET_B is no longer level sensitive.

4.12.2. Master and Slave SPI Configuration Port Pins

Table 4.5. Master SPI Configuration Port Pins

Pin Name	Function	Direction	Description
MCK	MCK	Output with weak pullup	Master clock used to time data transmission/reception from the CrossLinkPlus Configuration Logic to a slave SPI PROM.
CRESET_B	CRESET_B	Input with weak pullup	CRESET_B is used to initiate programming/configuration Optional: Tie HIGH for MSPI mode
MOSI	MO	Output	This is the Master output which carries configuration commands to the external SPI PROM.
MISO	MI	Input	This is the input to the Master which carries output data from the slave SPI PROM to the CrossLinkPlus Configuration Logic.
CSN	CSN	Output	CrossLinkPlus Master SPI chip select output pin for external SPI Flash.

Table 4.6. Slave SPI Configuration Port Pins

Pin Name	Function	Direction	Description
SPI_SCK	SPI_SCK	Input with weak pullup	Clock used to time data transmission/reception from an external SPI master device to the CrossLinkPlus Configuration Logic.
CRESET_B	CRESET_B	Input with weak pullup	CRESET_B is used to initiate programming / configuration Optional: Tie to GND for SSPI mode
MOSI	SI	Input	This is the input to the slave which receives data from the external SPI master to the CrossLinkPlus Configuration Logic.
MISO	SO	Output	This is the output from the slave which carries output data from the CrossLinkPlus Configuration Logic to the external SPI master.
SPI_SS	SPI_SS	Input with weak pullup	CrossLinkPlus Configuration Logic slave SPI chip select input.

MCK/SPI_SCK

The MCK/SPI_SCK pin is a multi-function pin (GPIO/SPI_SCK/MCK/SDA). The MCK/SPI_SCK, when active, are clocks used to sequentially load the configuration data for the FPGA.

The MCK/SPI_SCK pin default state for CrossLinkPlus in the Feature Row HW Default Mode state is to act as the SPI_CLK configuration clock. This allows an external Master SPI controller to program CrossLinkPlus. The maximum SPI_SCK frequency and the data setup/hold parameters can be found in the AC timing section of the CrossLinkPlus Family Data Sheet (FPGA-DS-02054). The SLAVE_SPI_PORT must be set to ENABLE if user want to use the port to reprogram the CrossLinkPlus device after it enters User Mode.

The MCK/SPI_SCK pin functions as a Master Clock (MCK) when the CrossLinkPlus device is configured in Dual Boot or External Boot mode. The MCK becomes an output and provides a reference clock for an SPI Flash connected to the CrossLinkPlus Master SPI Configuration port. MCK actively outputs a clock until all of the configuration data has been received. When the CrossLinkPlus device enters User Mode, the MCK output is tri-stated. This allows MCK to become a

general purpose I/O. MCK is reserved for use, in most post-configuration applications, as the reference clock for performing memory transactions with the external SPI PROM.

The CrossLinkPlus device generates MCK from an internal oscillator. The initial frequency of the MCK is nominally 2 MHz. The MCK frequency can be altered by modifying the MCCLK_FREQ parameter in Diamond Spreadsheet View. Following is a complete list of supported MCCLK frequencies:

- 2 MHz
- 3 MHz
- 6 MHz
- 12 MHz
- 24 MHz

During the initial stages of device configuration, the frequency value specified using MCCLK_FREQ is loaded into the FPGA. The MCLK output is updated after the CrossLinkPlus device accepts the new MCCLK_FREQ value.

Ensure that the selected MCCLK_FREQ does not exceed the frequency specification of the design configuration memory or PCB. Refer to the CrossLinkPlus AC specifications in the CrossLinkPlus Family Data Sheet (FPGA-DS-02054) when selecting the MCCLK_FREQ value.

SPI_SS

The SPI_SS pin is a multi-function pin (GPIO/SPI_SS/CSN/SCL) that serves as the Slave SPI port's chip select when in Slave SPI Mode. An external SPI bus master asserts the SPI_SS pin (active LOW) in order to perform actions using CrossLinkPlus Programming and Configuration Logic. The SPI_SS pin is available when the CrossLinkPlus device is in User Mode when the SLAVE_SPI_PORT is set to the ENABLE setting. The SPI_SS pin is a general purpose I/O in User Mode when the Slave SPI port is set to the DISABLE setting.

Proper operation of the CrossLinkPlus device depends upon maintaining the SPI_SS pin in the correct state:

- SPI_SS must be asserted LOW when configuring the CrossLinkPlus device using Slave SPI mode. SPI_SS signal needs to be clean during power up. Noise on SPI_SS pin may cause errors when the external SPI Master is attempting to write to the CrossLinkPlus device.
- SPI_SS must be deasserted HIGH when the CrossLinkPlus device is in User Mode.
- The Master SPI port and the Slave SPI port share four common pins, MOSI, MISO, MCK/SPI_SCK and CSN/SPI_SS. They are not permitted to be accessed at the same time. Diamond Software process flow fails if both of these ports are enabled through the Global Preferences tab of Lattice Diamond Spreadsheet View.

Lattice recommends the SPI_SS pin to be pulled high externally to augment the weak internal pull-up.

Note: In case of CrossLinkPlus, the SPI_SS pin is shared with I2C SCL line. The startup sequence for the CrossLinkPlus device decides Slave SPI and Slave I2C pins while the device is in configuration mode. The Startup state machine determines if either the I2C or the SPI slave mode is activated, and if so, identifies which one is activated. When one is activated, the other is locked out until the next refresh event or power cycle and so are its concerned pins.

CSN

The CSN pin is a multi-function pin (GPIO/SPI_SS/CSN/SCL) that serves as an active LOW chip select used by the Master SPI configuration mode to enable an external SPI Flash. When the CrossLinkPlus device is programmed to configure in either External or Dual Boot mode, the CSN pin is asserted LOW to the attached SPI Flash. The CrossLinkPlus device asserts CSN LOW until all configuration data bytes have been loaded, at which time the CSN enters a high impedance state.

When the CrossLinkPlus device is in the Feature Row HW Default Mode state, the CSN is SPI_SS with a weak pullup. It must have an external pullup resistor when the External and Dual Boot configuration modes are used. CSN must ramp in tandem with the external SPI PROM V_{CC} input. It remains SPI_SS when the FPGA enters User Mode in software default state. The Master SPI port must be set to ENABLE in the Global Preferences tab of the Spreadsheet View to reserve CSN function for use by the internal SPI Master logic.

When configuring from an external SPI Flash, ensure that the SPI Flash V_{CC} and the CrossLinkPlus V_{CCIO0} are at the same level. Ensure that the SPI Flash V_{CC} is at the recommended operating level.

Some SPI PROM manufacturers require the chip select input of the PROM ramp in unison to the PROMs V_{CC} rail. The CSN pin, by default, has a weak pull-up resistor internally. Adding a 4.7 kΩ to 10 kΩ pull-up resistor to the CSN pin on the CrossLinkPlus device is recommended.

MOSI

MOSI is a dual function (GPIO/MOSI) bi-directional pin. The direction depends upon whether a Master or Slave mode is active. MOSI is an input data pin when using the Slave SPI mode and is an output data pin when using the Master SPI mode. In Master SPI mode, CrossLinkPlus drives MOSI until all configuration data bytes have been loaded, at which time the MOSI enters a high impedance state.

At least one of the sysCONFIG preferences, MASTER_SPI_PORT or SLAVE_SPI_PORT, must be set to ENABLE in order to preserve this pin as MOSI and allow access to the SPI interface.

MISO

MISO pin is a dual function (GPIO/MISO) bi-directional pin. The direction depends upon whether a Master or Slave mode is active. MISO is an input data pin when using the Master SPI mode and is an output data pin when using the Slave SPI mode.

At least one of the sysCONFIG preferences, MASTER_SPI_PORT or SLAVE_SPI_PORT, must be set to ENABLE in order to preserve this pin as MISO and allow access to the SPI interface.

CRESET_B

CRESET_B is a configuration reset pin. When CRESET_B is asserted through a HIGH to LOW transition, the FPGA exits User Mode and starts a device configuration sequence at the Initialization phase, as described in this Technical Note. Holding the CRESET_B pin LOW prevents the CrossLinkPlus device from leaving the Initialization phase. An external SPI Master can also write the Activation Key to the FPGA during this LOW time to enter slave configuration mode. See Configuration Ports Default Behavior and Arbitration section for addition details.

4.12.3. I^{2}C Configuration Port Pins

SCL

The SCL pin is a multi-function pin (GPIO/SPI_SS/CSN/SCL) that the CrossLinkPlus device provides for an I^{2}C configuration port. SCL is the bi-directional I^{2}C Serial Clock pin, and is used to initiate and time transactions on the I^{2}C bus. SCL requires an external pull-up resistor in order to operate.

The SCL pin assumes the SPI_SS function when the CrossLinkPlus device is in the Feature Row HW Default Mode state. User must ENABLE the I2C_PORT for the configuration access to continue to be available in User Mode. See the I2C Configuration Mode section for details. The SCL pin becomes a general purpose I/O if user do not ENABLE the I2C_PORT, SLAVE_SPI_PORT and MASTER_SPI_PORT. The configuration SCL pin is not shared with the I2C0 USER_SCL pin. The I2C0 and I2C1 User Mode I^{2}C blocks operate independently of the configuration I^{2}C block.

SDA

The SDA pin is pin is a multi-function pin (GPIO/SPI_SCK/MCK/SDA) that the CrossLinkPlus device provides for an I^{2}C configuration port. SDA is the I^{2}C serial data input/output pin. It is bi-directional, open-drain, and requires an external pull-up resistor in order to operate. The pin changes direction dynamically during data transactions on the I^{2}C bus. The current state depends on the current bus master and the operation being performed by that master.

The SDA pin assumes the SPI_SCK function when the CrossLinkPlus device is in the Feature Row HW Default Mode state. User must ENABLE the I2C_PORT for the configuration access to be available in User Mode. See the I2C Configuration Mode section for details. The SDA pin becomes a general purpose I/O if user do not ENABLE the I2C_PORT, SLAVE_SPI_PORT and MASTER_SPI_PORT. The configuration SDA pin is not shared with the I2C0 USER_SDA pin.

5. Configuration Modes

The CrossLinkPlus device provides multiple options for loading the configuration SRAM from a non-volatile memory. The previous section describes the physical interface necessary to interact with the CrossLinkPlus Configuration Logic. This section describes the functionality of each of the different configuration modes. Descriptions of important settings required in the Diamond Spreadsheet View are also discussed. See the Configuration section for details on the default configuration behavior of the device.

5.1. SDM Mode

Self-Download Mode (SDM) is the primary configuration method for the CrossLinkPlus device where it retrieves the configuration data from the internal Flash. SDM is triggered when power is applied, a REFRESH command is received, or by asserting the CRESET_B pin from HIGH to LOW. The advantages of SDM include:

- **Speed**: The CrossLinkPlus device is ready to run in a few milliseconds.
- **Security**: The configuration data is never seen outside the device during the loading of the SRAM. It prevents the internal memory from being read.
- **Reduced cost**: Eliminate the need to purchase an external Flash specifically for programming the CrossLinkPlus device.
- **Reduced board space**: Eliminating the external Flash allows for a reduction in board size.

5.2. Master SPI Configuration Mode

Master SPI (MSPI) configuration mode is the only other self-controlled configuration mode available to the CrossLinkPlus device. Lattice recommends having a secondary configuration port available that is active when the CrossLinkPlus device is in Feature Row HW Default Mode state (blank state). The secondary port allows the CrossLinkPlus device to recover in the event of a programming error.

For a CrossLinkPlus device to operate correctly using the MSPI configuration mode, ensure the following:

- The POR of the external SPI Flash device is lower than the POR of CrossLinkPlus or the external SPI Flash is powered first.
- External SPI Flash F_{max} is greater than CrossLinkPlus MCK F_{max}.

Table 5.1. Master SPI Configuration Port Pins

Pin Name	Function
MCK	Clock output from the CrossLinkPlus Configuration Logic and Master SPI controller. Connect MCK to the SCLK input of the Slave SPI device.
MOSI	Serial Data output from CrossLinkPlus Configuration Logic to the Slave SPI SI input.
MISO	Serial Data input to the CrossLinkPlus Configuration Logic from the Slave SPI SO output.
CSN	Chip select output from the CrossLinkPlus Configuration Logic to the external Slave SPI Flash holding configuration data for CrossLinkPlus.

Table 4.2 provides information about the amount of memory needed for CrossLinkPlus configuration data. Select an external SPI Flash that accepts 03 hex Read Opcodes. CrossLinkPlus is only able to use the 03 hex Read Opcode.

The CrossLinkPlus device begins retrieving configuration data from the external SPI Flash when power is applied or the CRESET_B pin HIGH to LOW to HIGH transition (without receiving an Activation Key), which puts the FPGA into Master SPI configuration mode. The MCK/SPI_SCK I/O takes on the Master Clock (MCK) function, and begins driving a nominal 2 MHz clock to the external SPI Flash SCLK input. CSSPIN is asserted LOW, commands are transmitted to the external Flash over the MOSI output, and data is read from the external Flash on the MISO input pin. When all of the configuration data is retrieved from the external Flash, the CSSPIN pin is deasserted HIGH and the MSPI output pins are tri-stated.

The MCK frequency always starts downloading the configuration data at the nominal 2 MHz frequency. The MCCLK_FREQ parameter, accessed using the Spreadsheet View, can be used to increase the configuration frequency.

The configuration data in the external Flash has some padding bits, and then the data altering the MCK base frequency is read. The CrossLinkPlus device reads the remaining configuration data bytes using the new MCK frequency.

After the CrossLinkPlus device enters User Mode, the Master SPI configuration port pins are tri-stated. This permits background programming of or access to the external SPI Flash. To set the CrossLinkPlus device for operation using the MSPI configuration mode:

- Store the entire configuration data in an external SPI Flash.
- The data must start at offset 0x000000 within the external SPI Flash.
- Set the preferences as listed in Table 5.2.
- Enable Bitstream File creation in the Diamond Process Pane.
- Run the Export Files process to build the design.

Table 5.2. Master SPI Configuration Software Settings

Preference	Setting
MASTER_SPI_PORT	ENABLE
BOOT_UP_SEQUENCE	EXT

The Export Files process generates a JEDEC file, a PROM file, and a BIT file. The BIT file must be programmed into the external SPI Flash. There are several ways to get the data into the external SPI Flash:

- Diamond Programmer can transmit the SPI Flash data using a download cable.
- An on-board SOC can program the external SPI Flash.
- Automatic test equipment can program the external SPI Flash.
- Pre-programmed SPI Flash memories can be pre-assembled onto the printed-circuit board.

The configuration can be tested when CrossLinkPlus Feature Row is programmed and the external SPI Flash contains the configuration data. Toggle the CRESET_B pin through HIGH to LOW to HIGH transition, transmit a REFRESH command, or cycle power to the board, and the CrossLinkPlus device is configured from the external SPI Flash.

5.3. Dual Boot Configuration Mode

Dual Boot Configuration Mode is a combination of Self Download Mode and Master SPI Configuration Mode. When set up in Dual Boot Mode, the CrossLinkPlus device tries to configure first from a primary image stored in the external SPI Flash or internal Flash. If the primary image configuration fails, the CrossLinkPlus device attempts to configure itself using a fail-safe golden image stored in either the external SPI Flash or internal Flash. The load order can be changed by setting the BOOT_UP_SEQUENCE preference.

The primary image can fail in one of several ways:

- A bitstream CRC error is detected during configuration.
- A time-out error is encountered when loading the configuration SRAM.
- A Device ID mismatch occurs during configuration.
- An illegal command is asserted which can cause failure.

A CRC error is caused by incorrect data being written into the internal Flash or external SPI Flash. The configuration data is read out in rows. Each row data entering the Configuration Engine is checked for CRC consistency before the data enters the Configuration SRAM. Any incorrect CRC causes the device to erase the Configuration SRAM and retrieve configuration data from the fail-safe image.

There is a corner case where it is possible for the data to be correct from a CRC calculation perspective, but not functionally correct. In this instance, the internal DONE bit never becomes active. The CrossLinkPlus device counts the number of master clock pulses it provided after the Power On Reset signal is released. When the count expires without DONE becoming active, the FPGA attempts to get its configuration data from the fail-safe image.

The external SPI Flash must have a lower Power-On-Reset (POR) voltage supply level than the CrossLinkPlus POR to ensure proper configuration.

Dual boot configuration mode typically requires two configuration data files. One of the two configuration data files is a fail-safe image that is rarely, if ever, updated. The second configuration data file is a working image (also called primary

image) that is routinely updated. The fail-safe image can be stored in either the external SPI Flash or the internal Flash. In dual boot scenarios where only one image is stored in the external SPI Flash (BOOT_UP_SEQUENCE = CFG-EXT or EXT-CFG), the external image is stored in the SPI Flash starting at address 0x000000. One Lattice Diamond project or implementation can be used to create both the working and the fail-safe configuration data files. The external SPI Flash memory file for dual boot can be generated using the Lattice Diamond Deployment Tool. Use the External Memory: Dual Boot option in Deployment Tool to generate the dual boot image.

Refer to the Lattice Diamond Online Help for more information about using Diamond implementations.

User can use the following preferences listed in Table 5.3 to build a dual-boot design.

Table 5.3. Dual-Boot Configuration Settings

Preference	Dual-Boot Setting
CONFIGURATION	CFG
MASTER_SPI_PORT	ENABLED
BOOT_UP_SEQUENCE	CFG-EXT, EXT-CFG

5.4. Slave SPI Mode

CrossLinkPlus provides a Slave SPI (SSPI) configuration port that allows user to access features provided by the Configuration Logic. It is necessary to send a REFRESH command to load a new internal Flash image into the SRAM.To enter SSPI mode, CRESET_B pin should be held LOW while an external SPI Master writes the Activation Key (Table 4.1) to the FPGA. See Configuration Ports Default Behavior and Arbitration section for additional details.

Table 5.4. Slave SPI Port Pins

Pin Name	Description
SPI_SCK	Configuration clock input that is driven by a SPI Master controller.
MOSI	Serial Data Input to the CrossLinkPlus Configuration Logic for command and data.
MISO	Serial Data Output from the CrossLinkPlus Configuration Logic.
SPI_SS	Chip select to enable the CrossLinkPlus Configuration Logic.

In the Slave SPI mode, the MLK/SPI_SCK pin becomes SPI_SCK (Configuration clock). Input data is read into the CrossLinkPlus device on the MOSI pin at the rising edge of SPI_SCK. Output data is valid on the MISO pin at the falling edge of SPI_SCK. The SPI_SS acts as the chip select signal. When SPI_SS is HIGH, the SSPI interface is deselected and the MISO pin is tri-stated.

Commands can be written into and data read from CrossLinkPlus when SPI_SS is asserted (LOW). The CrossLinkPlus SSPI port only accepts Mode 0 (CPHA = 0 and CPOL = 0) bus transactions to the Configuration Logic.

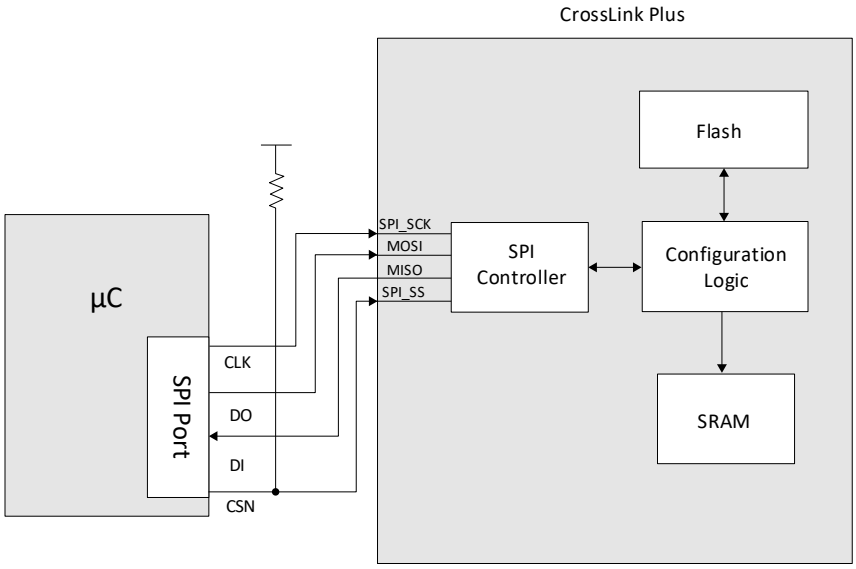

Figure 5.1. Slave SPI Configuration Mode

The SSPI port is active in User Mode when the CrossLinkPlus device is in Feature Row HW Default Mode state (blank/erased state). Lattice Diamond Software default preference for the SLAVE_SPI_PORT parameter is to ENABLE the port. Use the Spreadsheet View to make changes to the preference.

The SSPI port is used to program and verify the internal Flash or to configure the SRAM. The SSPI port can issue a REFRESH command to make a newly programmed image active. Programming the CrossLinkPlus device using the SSPI port is complex. Lattice provides C source code called SSPIEmbedded to circumvent the complexity of programming the CrossLinkPlus device. Use SSPIEmbedded to reprogram the CrossLinkPlus internal Flash. SSPIEmbedded can be found in the Diamond installation directory under the embedded_source folder. To modify the SSPIEmbedded code per the user-specific environment, refer to the Programming Tools User Guide document.

5.5. I²C Configuration Mode

The CrossLinkPlus device has an I²C Configuration port for use in accessing the Configuration Logic. An I²C Master can communicate with the Configuration Logic using 10-bit or 7-bit addressing modes to reprogram the internal Flash, configure the SRAM, or access status/control registers within the Configuration Logic block. Note that only one of the SPI or I²C interfaces can be enabled at a time. When the I²C interface is activated, all subsequent communication to the SPI port is ignored, even if in the middle of an active communication.

Table 5.5. I²C Port Pins

Pin Name	Description
SCL	I²C bus clock
SDA	I²C bus data line

The default state set for the I2C_PORT in Lattice Diamond design software is to place the I2C_PORT in the DISABLE state. User must ensure the I2C_PORT is set to the ENABLE state to leave the I²C interface active in User Mode.

To enter Slave I²C mode, CRESET_B pin should be held LOW while an external I²C Master writes the Activation Key (Table 4.1) to the FPGA. See Configuration Ports Default Behavior and Arbitration section for additional details.

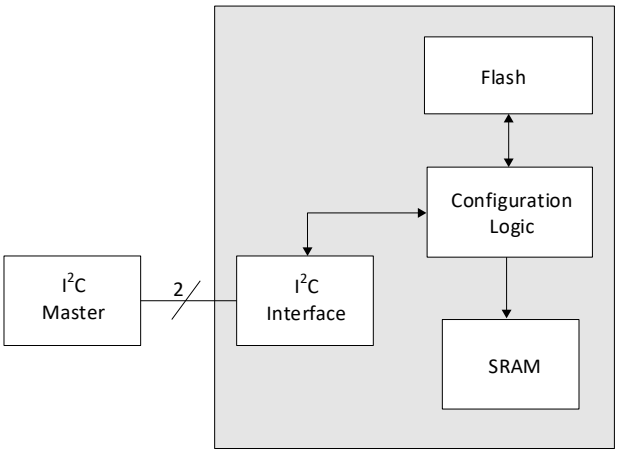

Figure 5.2. I²C Configuration Logic

An external I²C Master accesses the Configuration Logic using address 1000000b (7-bit mode) or 1111000000b (10-bit mode) unless the I²C base address has been modified.

Table 5.6 lists the address decoding used to access the I²C resources in the CrossLinkPlus device.

Table 5.6. Slave Addresses for I²C Ports

Slave Address	I²C Function
yyyxxxxx00b	Primary I²C Controller Configuration Logic address. Always responds to 7-bit or 10-bit addresses.
yyyxxxxx11b	Primary I²C Configuration Logic Reset. Always responds to 7-bit or 10-bit addresses.

Note: Although there are four possible combinations of the reserved address bits 1000 0XXb, only the two combinations listed above are used. The remaining two addresses are reserved for future I²C bus enhancements.

The CrossLinkPlus I²C controller supports two separate slave addresses as listed in Table 5.6. These are determined by the two least significant bits in the slave address – 00b corresponds to the Configuration Logic, while 11 corresponds to a reset port. In some instances, an I²C memory transaction to the Configuration Logic may be interrupted or abandoned.

It is possible for a command to be accepted by the Configuration Logic that causes the Configuration Logic to respond with data. In the event that the I²C memory transaction is interrupted or abandoned, the Configuration Logic continues to return the queued data.

New incoming I²C commands may be considered padding bytes or may be misinterpreted. Clear this condition by writing any value to the address with least significant bits 11b. The Configuration Logic command interpreter is reset, any queued data is flushed, and subsequent I²C memory transactions to the Configuration Logic operates correctly.

5.6. TransFR Operation

The CrossLinkPlus device, like other Lattice FPGAs, provides for the TransFR™ capability. TransFR is described in Minimizing System Interruption During Configuration Using TransFR Technology (TN1087).

Figure 5.3 shows how user can update bitstream in the CrossLinkPlus device by using the TransFR feature.

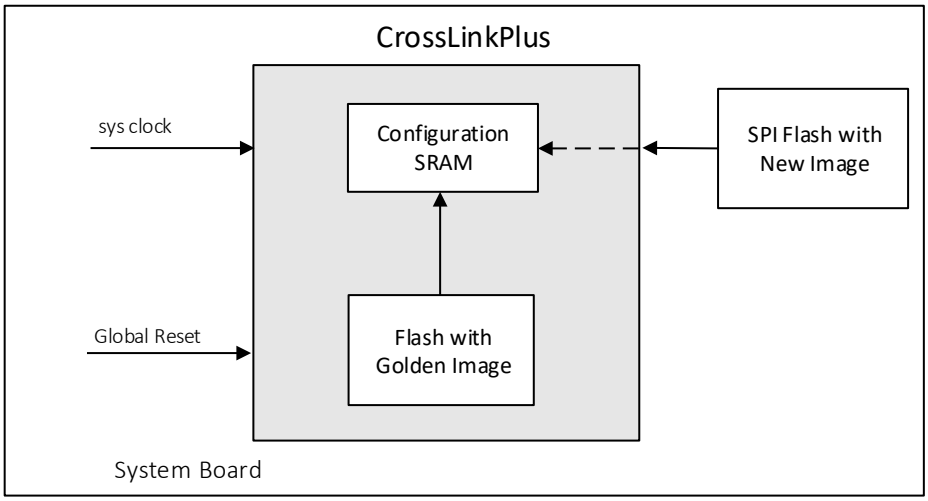

Figure 5.3. Bitstream Update Using TransFR

The example assumes the golden image is stored in the internal Flash to initiate the system, and then uses an external SPI Flash as a resource for image updates without disturbing the system. Figure 5.4 shows the process flow for performing this task.

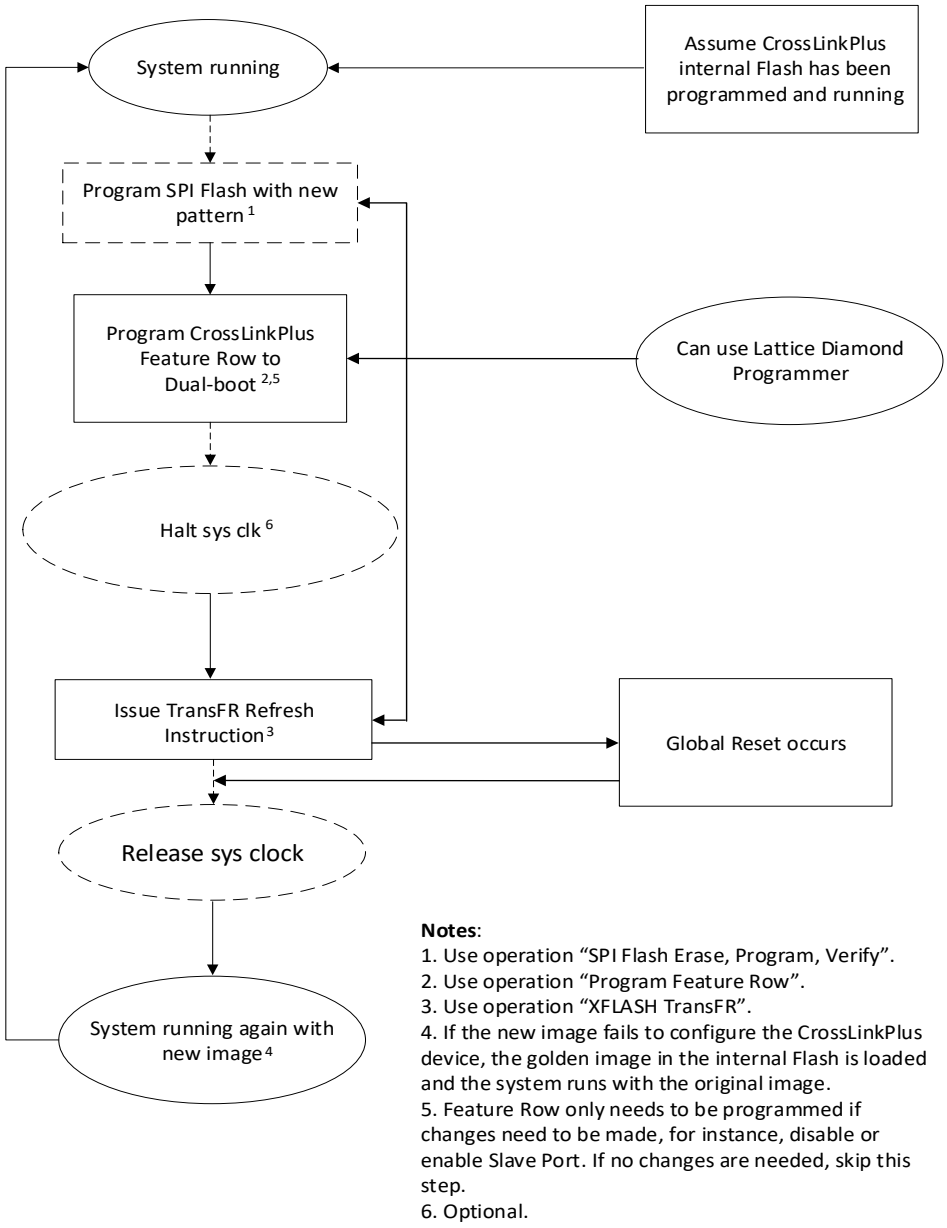

Figure 5.4. Example Process Flow

Caution when using the above process flow:

As a Global Reset is triggered during device wake-up after REFRESH instruction is issued, attention needs to be given in designing I/O with following conditions:

- Register output pins
- Impact on the system board level when value changes (may shut off the board, for instance)
- Register is set/reset by global reset

For the I/O in the example above, the state of the I/O is not changed during the TransFR refresh, but may change when the device gets into User Mode right after the TransFR refresh. Following are design tips to avoid this:

- For critical I/O, do not use global reset.
- For critical I/O, if user have to use global reset, use the set/reset option so that when GSR occurs, the state of the I/O pin does not trigger a system crash.

6. Software Selectable Options

The operation of the CrossLinkPlus Configuration Logic is managed by options selected in the Lattice Diamond design software. Other FPGAs provide dedicated I/O pins to select the configuration mode. The CrossLinkPlus devices uses the non-volatile Feature Row to select how it configures. The Feature Row default state needs to be modified in almost every design. Use the Lattice Diamond Spreadsheet View to make the changes to the operation of the CrossLinkPlus Feature Row which alters the operation of the Configuration Logic.

The Configuration Logic preferences are accessed using the Spreadsheet View. Click the Global Preferences tab and look for the sysCONFIG tree. Figure 6.1 shows the sysCONFIG section. The sysCONFIG preferences are divided into three categories:

- Configuration mode and port related
- Bitstream generation related
- Security related

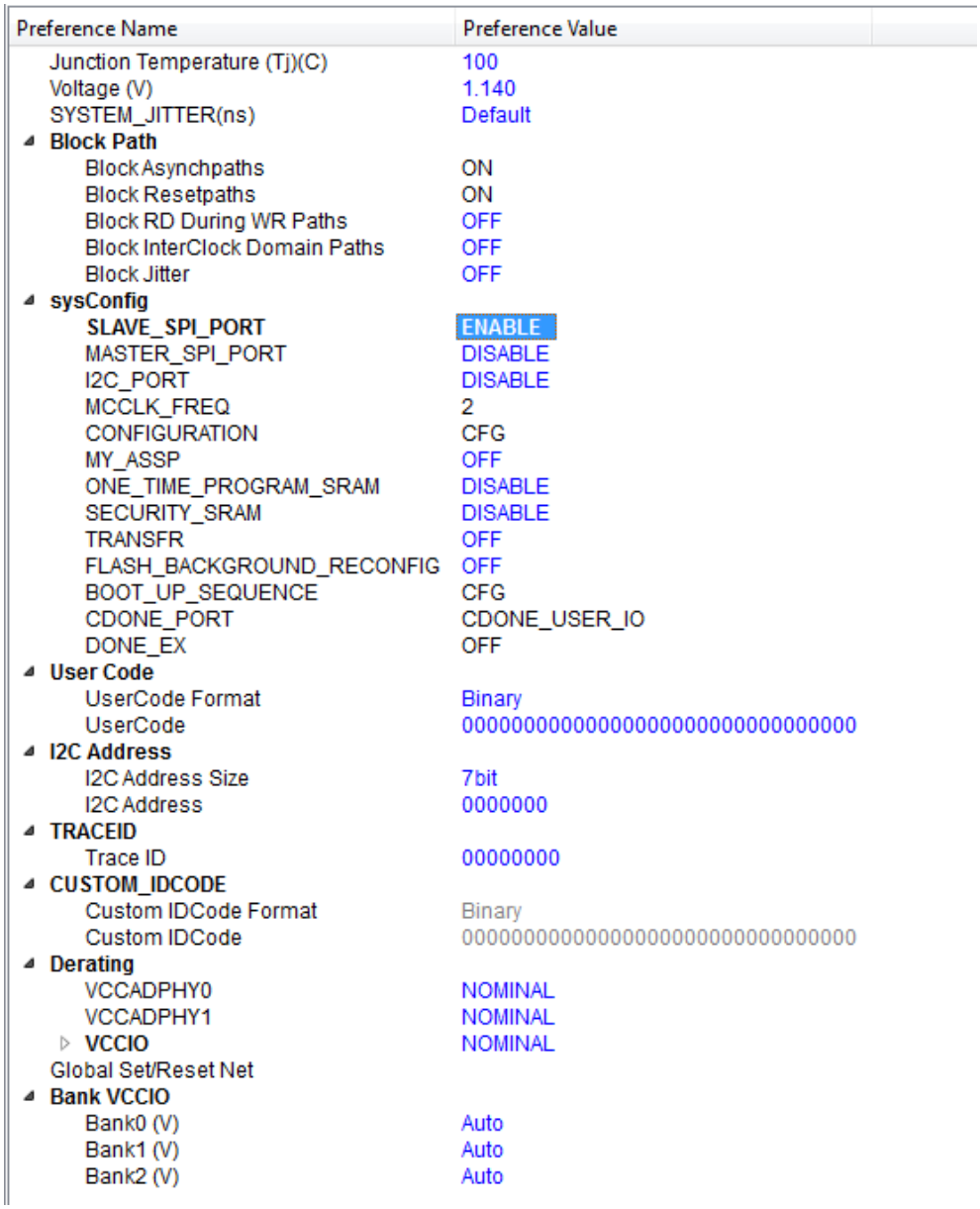

Figure 6.1. sysCONFIG Preferences in Global Preferences Tab of Lattice Diamond Spreadsheet View

6.1. Configuration Mode and Port Options

The configuration and port options allow user to set which configuration ports continue to operate after the CrossLinkPlus device enters User Mode. User can also control the availability of status pins, as well as the speed at which configuration data is read from an external Flash.

The configuration and port options can be used in any combination.

Table 6.1. Configuration Mode/Port Options

Option Name	Default Setting	All Settings
SLAVE_SPI_PORT	ENABLE	DISABLE, ENABLE
MASTER_SPI_PORT	DISABLE	DISABLE, ENABLE
I2C_PORT	DISABLE	DISABLE, ENABLE
MCCLK_FREQ	2	2,3,6,12,24
TRANSFR	OFF	OFF,ON
CDONE_PORT	CDONE_USER_IO	CDONE_ONLY, CDONE_USER_IO

SLAVE_SPI_PORT

The SLAVE_SPI_PORT allows user to preserve the Slave SPI configuration port after the CrossLinkPlus device enters User Mode. The SLAVE_SPI_PORT preference can be set in two states:

- **ENABLE** — This setting preserves the Slave SPI port I/O when the CrossLinkPlus device is in User Mode. When the pins are preserved, an external SPI master controller can interact with the Configuration Logic. Choosing ENABLE also prevents user from using these port pins as general purpose IO.
- **DISABLE** — This setting disconnects the SPI port pins from the Configuration Logic. By itself it does not make the port pins general purpose I/O. Both SLAVE_SPI_PORT and MASTER_SPI_PORT must be disabled to configure the MISO and MOSI port pins as general purpose I/O. SLAVE_SPI_PORT, MASTER_SPI_PORT and I2C_PORT must all be disabled to configure SPI_SS/CSN/SCL and SPI_SCK/MCK/SDA port pins as general purpose I/O.

MASTER_SPI_PORT

The MASTER_SPI_PORT allows user to preserve the Master SPI configuration port after the CrossLinkPlus device enters User Mode. The MASTER_SPI_PORT preference can be set in two states:

- **ENABLE** — This setting preserves the Master SPI port I/O when the CrossLinkPlus device is in User Mode. Choosing ENABLE also prevents user from using these port pins as general purpose I/O.
- **DISABLE** — This setting disconnects the SPI port pins from the Configuration Logic. By itself it does not make the port pins general purpose I/O. Both SLAVE_SPI_PORT and MASTER_SPI_PORT must be disabled to configure the MISO and MOSI port pins as general purpose I/O. SLAVE_SPI_PORT, MASTER_SPI_PORT and I2C_PORT must all be disabled to configure SPI_SS/CSN/SCL and SPI_SCK/MCK/SDA port pins as general purpose I/O.

I2C_PORT

The I2C_PORT allows user to preserve the I^2C configuration port after the CrossLinkPlus device enters User Mode. The I2C_PORT preference can be set in two states:

- **ENABLE** — This setting preserves the I^2C port I/O when the CrossLinkPlus device is in User Mode. Choosing ENABLE also prevents user from using these port pins as general purpose I/O.
- **DISABLE** — This setting disconnects the I^2C port pins from the Configuration Logic. SLAVE_SPI_PORT, MASTER_SPI_PORT, and I2C_PORT must all be disabled to configure SPI_SS/CSN/SCL and SPI_SCK/MCK/SDA port pins as general purpose I/O.

MCCLK_FREQ

The MCCLK_FREQ preference allows user to alter the MCCLK frequency used to retrieve data from an external SPI Flash when using EXT or Dual Boot configuration modes. The MCCLK_FREQ value is stored in the incoming configuration data, not in the Feature Row. The CrossLinkPlus device reads a series of padding bits, a *start of data* word (0xBDB3) and a control register value. The control register contains the new MCCLK_FREQ value. The CrossLinkPlus device switches to the new clock frequency shortly after receiving the MCCLK_FREQ value.

The MCCLK_FREQ has a range of possible frequencies available from 2 MHz up to 24 MHz (see the list on page 16). Do not exceed the maximum clock rate of user SPI Flash, or of user's printed circuit board.

Lattice recommends having a back-up configuration port available in case user specify a clock frequency that is out of specification.

TRANSFR

The TransFR function used by the CrossLinkPlus device requires the configuration data loaded into the configuration SRAM and any future configuration data file loaded into the external SPI Flash to have the TRANSFR set to the ENABLE state. See the TransFR Operation section and refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for more information about using TransFR with the CrossLinkPlus device.

6.2. Bitstream Generation Options

The Bitstream Generation options allow user to decide how the Lattice Diamond development tools create the configuration data for the CrossLinkPlus device. The CONFIGURATION, USERCODE, and CUSTOM_IDCODE settings are saved in the Feature Row and remain in effect until the Feature Row is erased. The other options allow user to control the BIT files that are generated by Diamond.

CONFIGURATION

The BOOT_UP_SEQUENCE preference allows user to control the boot up sequence. The BOOT_UP_SEQUENCE preference has four possible settings:

- **CFG** — The internal Flash setting is the Software default mode for building configuration data. The configuration bitstream is stored in the internal Configuration Flash. This is the Hardware default mode for a blank device.
- **CFG-EXT** — This setting boots up the system using the internal Flash first. If an error occurs, the system boots up with the golden image in the External SPI Flash.
- **EXT-CFG** — This setting boots up the system using the external SPI Flash first. If an error occurs, the system boots up with the golden image in the internal Flash.
- **EXT** — This preference generates configuration data that is stored in the external SPI Flash.

UserCode

The CrossLinkPlus Configuration Flash sector contains a 32-bit register for storing a user-defined value. The default value stored in the register is 0x00000000. The UserCode preference allows user to assign any value to a register. Suggested uses include the configuration data version number, a manufacturing ID code, and date of assembly among others.

The format of the UserCode field is controlled using the *UserCode Format* preference. Data entry can be performed in either Binary, Hex, or ASCII formats.

UserCode Format

The *UserCode Format* preference sets the format for the data field used to assign a value in the UserCode preference. The *UserCode Format* has three options:

- **Binary** — UserCode is set using 32 *1* or *0* characters.
- **Hex** — UserCode is set using eight hexadecimal digits that is 0-9A-F.
- **ASCII** — UserCode is set using up to four ASCII characters.

CDONE_PORT

CDONE and a GPIO are bonded to a shared package ball. This option enables the feature in the software.
If CDONE_PORT = CDONE_ONLY, the GPIO becomes unavailable to the user. If CDONE_PORT = CDONE_USER_IO, the GPIO becomes available to the user.

DONE_EX

If ON, the device waits for CDONE to be driven high by an external signal to wake up. A common reason for keeping CDONE driven LOW is to allow multiple FPGAs to be completely configured. As each FPGA reaches the DONE state, it is ready to begin operation. The last FPGA to be configured can trigger all the FPGAs to start in unison.

If the default setting is OFF, the CDONE pin is asserted by the device when the internal DONE bit is set. When set to OFF, the device wakes up regardless of the external signal state on CDONE.

6.3. Security Options

Security Options allows user to select from a range of options for tracking or securing the CrossLinkPlus device. Table 6.2 provides a summary of these options.

Table 6.2. Configuration Mode/Port Options

Option Name	Default Setting	All Settings
Trace ID	<all zeros>	8-bit arbitrary
MY_ASSP	OFF	OFF, ON
CUSTOM_IDCODE	<all zeros>	32-bit arbitrary
Custom IDCode Format	Binary	Binary, Hex, ASCII
SECURITY_SRAM	DISABLE	DISABLE, ENABLE
ONE_TIME_PROGRAM_SRAM	DISABLE	DISABLE, ENABLE

TRACEID

TRACEID stamps each CrossLinkPlus device with a unique 64-bit ID. No two CrossLinkPlus devices have the same TraceID value even when they are loaded with the same configuration data. This differs from a UserCode which is present in the configuration data. Every device that receives the configuration data using a UserCode receives the same UserCode value.

The Trace ID is 64 bits long with the least significant 56 bits being immutable data. The most significant eight bits are provided and stored in the Feature Row. The TRACEID is changed using Lattice Diamond Spreadsheet View. User enter a unique 8-bit binary value in the TraceID field and generate configuration data.

MY_ASSP

The MY_ASSP preference permits user to change the value returned when the IDCode is read from the FPGA. Turning the MY_ASSP ON enables the Custom_IDCode preference.

CUSTOM_IDCODE

The CUSTOM_IDCODE is the value user assign to override the default IDCode in the CrossLinkPlus device. User are only allowed to enter a 32-bit hexadecimal, ASCII or binary value when the MY_ASSP preference is ON.

Overriding the IDCode prevents the Lattice programming software from being able to identify the CrossLinkPlus device, and as a result, prevents Programmer from being able to directly program the CrossLinkPlus device. It is necessary to migrate to generating Serial Vector Format (SVF) files in order to program MY_ASSP enabled CrossLinkPlus devices.

Custom IDCode Format

The Custom IDCode Format preference selects the format for the data field used to assign a value in the CUSTOM_IDCODE preference. The Custom IDCode Format has three options:

- **Binary** — CUSTOM_IDCODE is set using 32 *1* or *0* characters.
- **Hex** — CUSTOM_IDCODE is set using eight hexadecimal digits that is 0-9A-F.
- **ASCII** — CUSTOM_IDCODE is set using up to four ASCII characters

SECURITY_SRAM

When this preference is set to ON for SRAM Fast Configuration Operation, the read-back of the SRAM memory is blocked. The CrossLinkPlus device cannot be read back.

ONE_TIME_PROGRAM_SRAM

The CrossLinkPlus device has One Time Programmable (OTP) fuses that can be used to prevent the SRAM from being erased or programmed through any slave configuration interfaces

7. Device Wake-up Sequence

When configuration is completed and SRAM is loaded, the device wakes up in a predictable fashion. If the CrossLinkPlus device is the only or the last device in the chain, the Wake-up process begins when configuration is completed and the internal DONE bit is set. Upstream sources should not enable their outputs until the CrossLinkPlus device has completed its configuration to ensure that the CrossLinkPlus device is operating in a known state.

7.1. Wake-up Signals

Three internal signals, GSR, GWDIS, and GOE, determine the Wake-up sequence.

- GSRN is used to set and reset the core of the device. GSR is asserted (LOW) during configuration and de-asserted (high) in the Wake-up sequence.
- When the GWDIS signal is LOW, it safeguards the integrity of the RAM Blocks and LUTs in the device. This signal is LOW before the device wakes up. This control signal does not control the primary input pin to the device but controls specific control ports of EBR and LUTs.
- When GOE is LOW, it prevents the device I/O buffers from driving the pins. The GOE only controls output pins. When the internal DONE is asserted the CrossLinkPlus device responds to input data.

When CDONE pin is HIGH, it indicates that configuration is complete and that no errors are detected.

Appendix A. CrossLink SSPI SRAM Configuration Flow

		Shift In			Shift Out		
Steps	**Configuration Step**	**Signal**	**Clocks**	**Value**	**Signal**	**Value**	**Description**
1	Initialize	CRESETB		LOW			
		Wait 1 ms					
		SN		LOW			
		SI	40	0xFF A4 C6 F4 8A			Shift in Activation Key
		SN		HIGH			
		CRESETB		HIGH			
2	Delay	Wait 1 ms					
3	Check IDCODE (Optional)	SN		LOW			
		SI	32	0xE0 00 00 00			Shift in IDCODE_PUB (0xE0) opcode
		SI	32	0x00 00 00 00	SO	DEVICE_ID	Shift out DEVICE_ID & compare to expected value
		SN		HIGH			
4	Enable Programming Mode	SN		LOW			
		SI	32	0xC6 00 00 00			Shift in ISC ENABLE (0xC6) instruction
		SN		HIGH			
5	Delay	Wait 1 ms					
6	Erase the device	SN		LOW			
		SI	32	0x0E 00 00 00			Shift in ISC ERASE (0x0E) instruction
		SN		HIGH			
7	Delay	Wait 200 ms					
8	Program Fuse Map	SN		LOW			
		SI	32	0x0E 00 00 00			Shift in LSC_INIT_ADDRESS (0x46) instruction
		SN		HIGH			
		SN		LOW			
		SI	32	0x7A 00 00 00			Shift in LSC_BISTREAM_BURST (0x7A) instruction
		SI		Full Bitstream			Shift in bitstream (.bit) generated in Diamond Software
		SN		HIGH			
9	Delay	Wait 10 ms					
10	Read the status bit	SN		LOW			
		SI	32	0x3C 00 00 00			Shift in LSC_READ_STATUS (0x3C) instruction
		SI	32	0x00 00 00 00	SO	Status Register Value	Expected Value from SO: 0x00000100 with the Mask: 0x00003100 [Bit-8 DONE = 1, Bit-12 Busy = 0, Bit-13 Fail = 0]
		SN		HIGH			
11	Exit Programming Mode	SN		LOW			
		SI	32	0x26 00 00 00	SO	Status Register Value	Shift in ISC DISABLE (0x26) instruction
		SN		HIGH			

		Shift In			Shift Out		
Steps	**Configuration Step**	**Signal**	**Clocks**	**Value**	**Signal**	**Value**	**Description**
		Wait 200 ms					
		SN		LOW			
		SI	32	0xFF FF FF FF			Shift in NO-OP (0xFF) instruction
		SN		HIGH			

Appendix B. CrossLink Slave I2C SRAM Configuration Flow

Steps	Signal	Configuration Step	Read/Write	Value	Description
1	CRESETB			LOW	
		Wait 1 s			
		Initialize	W	0xA4 0xC6 0xF4 0x8A	Shift in Activation Key
	CRESETB			HIGH	
		Wait 10 ms			
2		Check IDCODE (Optional)	W	0xE0 0x00 0x00 0x00	Shift in IDCODE (0xE0) opcode
			R	Byte 1 – Byte 2 – Byte 3 – Byte 4	Shift out DEVICE_ID & compare expected value
3		Enable SRAM Programming Mode	W	0xC6 0x00 0x00 0x00	Shift in ENABLE (0xC6) instruction
		Wait 1 ms			
4		Erase SRAM	W	0x0E 0x00 0x00 0x00	Shift in ERASE (0x0E) instruction
		Wait 5 s			
5		Read Status Register	W	0x3C 0x00 0x00 0x00	Shift in LSC_READ_STATUS (0x3C) instruction
			R	Byte 1 – Byte 2 – Byte 3 – Byte 4	Expected Value: 0x00000000 with the Mask: 0x00003000 [Bit-12 Busy = 0, Bit-13 Fail = 0]
6		Program SRAM	W	0x46 0x00 0x00 0x00	Shift in LSC_INIT_ADDRESS (0x46) instruction
			W	0x7A 0x00 0x00 0x00	Shift in LSC_BITSTREAM_BURST (0x7A) instruction
				Byte 1 – Byte 2 – … - Byte N	Shift in bitstream (.bit) generated by Diamond Software
		Wait 10 ms			
7		Verify USERCODE (Optional)	W	0xC0 0x00 0x00 0x00	Shift in USERCODE (0xC0) instruction
			R	Byte 1 – Byte 2 – Byte 3 – Byte 4	Read USECODE
8		Read Status Register	W	0x3C 0x00 0x00 0x00	Shift in LSC_READ_STATUS (0x3C) instruction
			R	Byte 1 – Byte 2 – Byte 3 –Byte 4	Expected Value from 0x00000100 with the Mask: 0x00003100 [Bit-8 DONE = 1, Bit-12 Busy = 0, Bit-13 Fail = 0]
9		Exit Programming Mode	W	0x26 0x00 0x00 0x00	Shift in DISABLE (0x26) instruction

Appendix C. CrossLink Slave I2C SRAM Configuration Flow

CrossLinkPlus SSPI Flash Configuration Flow		Shift In			Shift Out		
Steps	**Configuration Step**	**Signal**	**Clocks**	**Value**	**Signal**	**Value**	**Description**
1	Initialize	CRESETB		LOW			
		Wait 1 ms					
		SN		LOW			
		SI	40	0xFF A4 C6 F4 8A			Shift in Activation Key
		SN		HIGH			
		CRESETB		HIGH			
2	Delay	Wait 1 ms					
3	Check IDCODE (Optional)	SN		LOW			
		SI	32	0xE0 00 00 00			Shift in IDCODE_PUB (0xE0) opcode
		SI	32	0x00 00 00 00	S0	DEVICE_ID	Shift out DEVICE_ID & compare to expected value
		SN		HIGH			
4	Enable Programming Mode	SN		LOW			
		SI	32	0xC6 08 00 00			Shift in ISC ENABLE (0xC6) instruction
		SN		HIGH			
5	Delay	Wait 3 ms					
6	Check Password Protect	SN		LOW			
		SI	32	0x46 00 00 00			Set address pointer to the beginning of Flash CFG memory sector 0
		SN		HIGH			
		SN		LOW			
		SI	32	0x3C 00 00 00			Shift in LSC_READ_STATUS (0x3C) instruction
		SI	32	0x00 00 00 00	SO	Status Register Value	Expected Value from SO: 0x00000000 with the Mask: 00000020 Bit-5 Protected = 1
		SN		HIGH			
7	Delay	Wait 1 ms					
8	Erase the device	SN		LOW			
		SI	32	0x0E 00 00 00			Shift in ISC ERASE (0x0E) instruction
		SN		HIGH			
9	Delay	Wait 200 ms					
10		SN		LOW			
		SI	32	0x46 00 00 00			Set address pointer to the beginning of Flash CFG memory sector 0 46 01 00 00: For memory sector 1 46 02 00 00: For memory sector 2
		SN		HIGH			
		SN		LOW			
		SI	32	0x70 04 00 00			Shift in LSC_PROG_INCR_NV
		SI		JED file			Shift in .jed file generated in

CrossLinkPlus SSPI Flash Configuration Flow		Shift In			Shift Out		
Steps	**Configuration Step**	**Signal**	**Clocks**	**Value**	**Signal**	**Value**	**Description**
							Diamond Software
		SN		HIGH			
11	Delay	Wait 10 ms					
12	Read the status bit	SN		LOW			
		SI	32	0x3C 00 00 00			Shift in LSC_READ_STATUS (0x3C) instruction
		SI	32	0x00 00 00 00	SO	Status Register Value	Expected Value from SO: 0x00000100 with the Mask: 0x00003100 [Bit-8 DONE = 1, Bit-12 Busy = 0, Bit-13 Fail = 0]
		SN		HIGH			
13	Exit Programming Mode	SN		LOW			
		SI	32	0x26 00 00 00	SO	Status Register Value	Shift in ISC DISABLE (0x26) instruction
		SN		HIGH			
		Wait 200 ms					
		SN		LOW			
		SI	32	0xFF FF FF FF			Shift in NO-OP (0xFF) instruction
		SN		HIGH			

References

For more info on this FPGA device, refer to the following:

- CrossLinkPlus Family Data Sheet (FPGA-DS-02054)
- CrossLinkPlus High-Speed I/O Interface (FPGA-TN-02102)
- CrossLinkPlus Hardware Checklist (FPGA-TN-02105)
- CrossLinkPlus sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN02109)
- CrossLinkPlus sysI/O Usage Guide (FPGA-TN-02108)
- CrossLinkPlus Memory Usage Guide (FPGA-TN-02110)
- Power Management and Calculation for CrossLinkPlus Devices (FPGA-TN-02111)
- CrossLinkPlus I2C Hardened IP Usage Guide (FPGA-TN-02112)
- Advanced CrossLinkPlus I2C Hardened IP Reference Guide (FPGA-TN-02135)
- Minimizing System Interruption During Configuration Using TransFR Technology (TN1087)
- Programming Tools User Guide

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.2, June 2023

Section	Change Summary

All	• Updated document titled from *CrossLinkPlus Programming and Configuration Usage Guide* to *CrossLinkPlus Programming and Configuration User Guide*.
	• Added below sections:
	  • Appendix A. CrossLink SSPI SRAM Configuration Flow
	  • Appendix B. CrossLink Slave I2C SRAM Configuration Flow
	  • Appendix C. CrossLink Slave I2C SRAM Configuration Flow

Technical Support Assistance	Added Lattice FAQ website link.

Revision 1.1, October 2020

Section	Change Summary
CrossLink Plus Features	Removed *Dual Boot*.
Definition of Terms	• Updated definition of Dummy Byte. • Added XFLASH.
Configuration Process and Flow	• General update to the Configuration Ports Default Behavior and Arbitration section. • Added ISC_ENABLE command is received to bulleted list in User Mode. • Updated statement to "A CrossLinkPlus design with every EBR pre-initialized with unique data values requires the largest amount of storage." In Bitstream/PROM Sizes. • Minor editorial change in Lock Bits • Updated guidelines in the sysCONFIG Pins, including descriptions of SPI_SS and CSN.
Configuration Mode	• Updated statement in Master SPI Configuration Mode to "…when power is applied or the CRESET_B pin HIGH to LOW to HIGH transition (without receiving an Activation Key)…." • Updated Figure 5.1. Slave SPI Configuration Mode and Figure 5.2. I2C Configuration Logic.
Software Selectable Options	Updated TRACEID, MY_ASSP, and ONE_TIME_PROGRAM_SRAM
Device Wake-up Sequence	Minor update in wake-up signal *GSRN*.

Revision 1.0, September 2019

Section	Change Summary
All	Production release.

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