I2CFIFO Module

User Guide

FPGA-IPUG-02064-1.5

July 2024

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
I^2C	Inter-Integrated Circuit
LMMI	Lattice Memory Mapped Interface

1. Introduction

The I2CFIFO Module provides industry standard two-pin communication interface that conforms to V2.1 of the I²C bus specification and is compliant with V1.0 of the MIPI I3C specification for legacy I²C devices. It can be configured as either Master or Slave port. In Master mode, it supports configurable data transfer rate and performs arbitration detection to allow it to operate in multi-master systems. It supports clock stretching in both Master and Slave mode with enable/disable capability. It supports both 7 bits and 10 bits addressing in Slave mode with configurable Slave address. It supports general call address detection in both Master and Slave modes. It provides interrupt logic for easy communication with the host. It also provides configurable digital delay at SDA output for reliably generating start/stop condition, as the specification recommended. In addition, FIFOs is used for storing more than one byte of data for transmit and/or receive to efficiently support the I²C sensor applications.

This design is implemented in Verilog. It can be targeted to Lattice FPGA devices built on the Lattice Nexus™ platform and implemented using the Lattice Radiant Software Place and Route tool integrated with the Synplify Pro® synthesis tool.

1.1. Features

Key features of the I2CFIFO Module include:

- Configurable Master and Slave I²C modes
- Programmable 7-bit and 10-bit addressing
- Multi-master arbitration
- Clock stretching
- Standard-Mode, Fast-Mode, and Fast-Mode Plus
- General call
- Two data FIFOs with configurable sizes; one for transmit and one for receive
- 50 ns analog delay
- FPGA sleep wake-up
- Hard-connection and programmable I/O connection
- Programmable to a mode compliant with I3C requirements on legacy I²C Slave devices
  - Fast-Mode and Fast-Mode Plus
  - Slave only mode
  - Disabled clock stretching
  - 50 ns SCL and SDA glitch filter
  - Programmable 7-bit address
- Configuration register initialization

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals

2. Functional Description

2.1. Overview

The I2CFIFO Module supports two operational modes:

- Register Mode and
- FIFO Mode

The Register Mode is the original I²C Controller. A host in the FPGA fabric controls all the data transfers on the I²C bus by issuing commands for each transfer and using polling to determine the status of each transfer. The FIFO Mode is the enhancement to the existing I²C Controller. It allows the host to provide a large amount of data for transfer and allows the I²C Controller to control most of the link layer activities. The host is interrupted only when the entire transaction is done. This *fire and forget* approach frees up the host to other tasks while the I²C Controller is handling the data transaction.

In both modes, the registers that control the overall I²C Controller behavior must be initialized in order for the IP to function correctly. These registers include, but are not limited to, the control register and the clock pre-scale registers.

A top-level block diagram of the I2CFIFO Module is shown in Figure 2.1. The signals represented in dashed lines are optional, their availability is based on user-selected attributes. Please refer to Table 2.1 for more information.

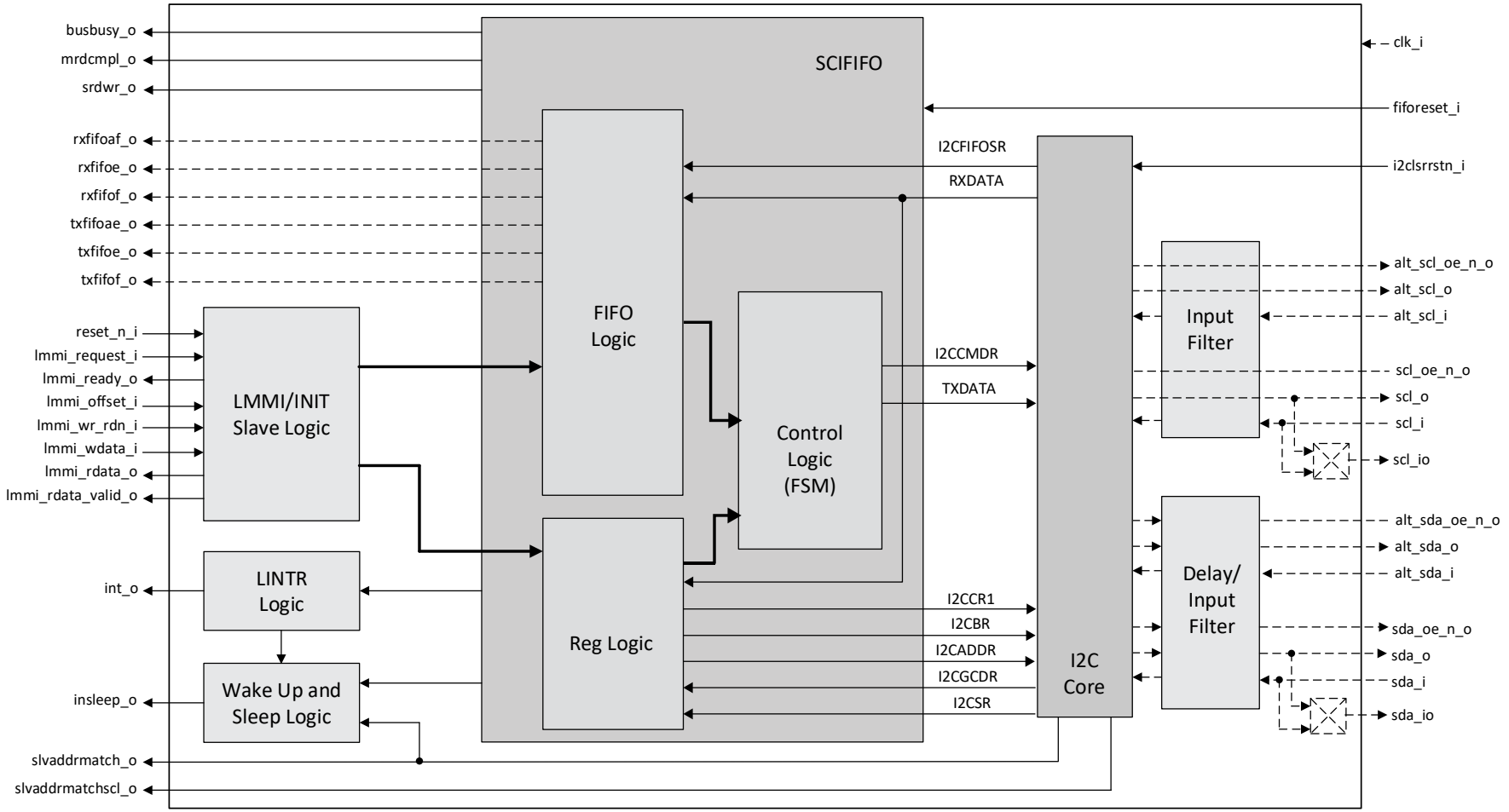


Figure 2.1. I2CFIFO Top Level Block Diagram

2.2. Signal Description

Table 2.1 lists the top-level input and output signals for the I2CFIFO Module.

Table 2.1. I2CFIFO Module Ports

Port Name	Direction	Description
Clock and Reset		
clk_i	Input	System clock input.
reset_n_i	Input	Resets LMMI state machine to prevent lock up if wait states are implemented.
i2clsrrstn_i	Input	Active low LSR reset that comes from CIB. This reset only resets the I^2C core and does not reset the configuration registers. When asserted, the internal FSM in the I^2C core is reset to idle state, all status flag is cleared, and the I^2C bus is released. The assertion of this signal stops the on-going I2C transaction and may cause an incomplete transaction on the I^2C bus.
fiforeset_i	Input	The reset signal, when asserted, synchronously resets the FIFOs (I2CTXFIFO and I2CRXFIFO) and transmits/receives byte counters (I2CFIFOTXCNT and I2CFIFORXCNT). The associated FIFO flags are cleared as well. The assertion of this signal does not affect the ongoing I^2C transaction, which continues until the byte transaction is completed.
I^2C Interface (with I/O Buffers)[1]		
scl_io	In/Out	I^2C Serial Clock Input/Output to I/O
sda_io	In/Out	I^2C Serial Data Input/Output to I/O
I^2C Interface (without I/O Buffers)[2]		
scl_i	Input	I^2C Serial Clock Input from Fabric
scl_o	Output	I^2C Serial Clock Output to Fabric
scl_oe_n_o	Output	I^2C Serial Clock Output Enable to Fabric
sda_i	Output	I^2C Serial Data Input from Fabric
sda_o	Output	I^2C Serial Data Output to Fabric
sda_oe_n_o	Output	I^2C Serial Data Output Enable to Fabric
Alternative I^2C Interface[*3]		
alt_scl_i	Input	Alternative I^2C Serial Clock Input from dedicated I/O connection
alt_scl_o	Output	Alternative I^2C Serial Clock Output to dedicated I/O connection
alt_scl_oe_n_o	Output	Alternative I^2C Serial Clock Output Enable to dedicated I/O connection
alt_sda_i	Output	Alternative I^2C Serial Data Input from dedicated I/O connection
alt_sda_o	Output	Alternative I^2C Serial Data Output to dedicated I/O connection
alt_sda_oe_n_o	Output	Alternative I^2C Serial Data Output Enable to dedicated I/O connection
LMMI Interface		
lmmi_wdata_i[7:0]	Input	The data input array *lmmi_wdata* is used to write register and FIFO binary data and commands.
lmmi_wr_rdn_i	Input	The write enable input *wr_rdn* indicates whether the current LMMI cycle is a READ or WRITE cycle. The signal is negated during READ cycles, and is asserted during WRITE cycles.
lmmi_offset_i[5:0]	Input	The address input array *lmmi_offset* is used to pass a binary address for LMMI Addressable Registers.
lmmi_request_i	Input	The strobe input *lmmi_request*, when asserted, indicates that the LMMI Slave component is selected. An LMMI Slave responds to other LMMI signals only when the *lmmi_request* is asserted.
lmmi_ready_o	Output	Indicates if the IP is ready to have a transaction on a register/block
lmmi_rdata_o[7:0]	Output	The data output array *lmmi_rdata* is used to readback register and FIFO binary data and status.

Port Name	Direction	Description
lmmi_rdata_valid_o	Output	Indicates if valid data is available on *lmmi_rdata*
LINTR Interface		
int_o	Output	Interrupt signal. I2CFIFO has an interrupt, which needs to be serviced. Stays High as long as the cause for the enabled interrupt is not addressed and the interrupt itself is not cleared in the end.
General		
busbusy_o	Output	Indicates that there is communication on the I^2C bus. This bit is triggered even when this I^2C is not involved in the communication.
insleep_o	Output	This output informs you when the switch between clocks (fabric clock to sleep clock and vice versa) is completed. An assertion of this signal signifies that the I2CFIFO is running off sleep_clk and is ready for transactions during sleep. A deassertion of this signal signifies that the I2CFIFO is successfully switched between sleep_clk to fabric clock and is ready for transactions. This signal stays asserted or deasserted throughout the entirety of the I2CFIFO's current state (that is not a pulse).
mrdcmpl_o	Output	The Master Read Complete signal. A transaction is considered complete when 1) the specified number of data bytes from the slave are received in the RX FIFO; or 2) the Master terminates the read transaction before the specified number of data bytes are received.
slvaddrmatch_o	Output	Indicates that the I^2C Slave Address is matched for this communication. Resets on Restart and Stop.
slvaddrmatchscl_o	Output	An active high output signal to fabric that indicates that the slave address of this I^2C IP is called (matching slave address) through the I^2C bus by another I^2C master.
srdwr_o	Output	Slave read/write signal. A *1* indicates a slave transmitting (external master receiving). A *0* means slave receiving (external master transmitting).
FIFO[4]		
rxfifoaf_o	Output	RXFIFO almost full status signal, indicating user-defined almost full threshold value is reached.
rxfifoe_o	Output	RXFIFO is empty status signal. It can be used as an active low FIFO Data Ready Signal.
rxfifof_o	Output	RXFIFO is full status signal.
txfifoae_o	Output	TXFIFO almost empty status signal, indicating user-defined almost empty threshold value is reached.
txfifoe_o	Output	RXFIFO is empty status signal. It can be used as an active low FIFO Data Ready Signal.
txfifof_o	Output	TXFIFO is full status signal.

Notes:

1. The signals under I^2C Interface (with I/O Buffers) group are available when the *Include I/O Buffers* attribute is checked.
2. The signals under the I^2C Interface (without I/O Buffers) group are available when the *Include I/O Buffers* and the *Use Dedicated Pins* attributes are unchecked.
3. The signals under the Alternative I^2C Interface group are available when the *Include I/O Buffers* attribute is unchecked and the *Use Dedicated Pins* attribute is checked.
4. The signals under the FIFO group are available when the *Enable FIFO Mode* attribute is checked.

2.3. Attribute Summary

The I2CFIFO Module is initialized through configuration bitstream. INIT bus is used to initialize the addressable registers in the IP. The addressable registers that require initialization at device configuration are Control, Pre-Scale, Slave Address, Interrupt Control, and FIFO Threshold.

In User Mode, the following configuration sequence should be kept in order for the IP to work properly:

- Registers I2CNONUSRCR1 and I2CCR1 (Control register) must be configured first to enable the IP, to select the mode of operation, and to set other features as described in the Register Description section.
- Following registers are to be configured next before data transaction, but they do not need to be in a specific order. They are I2CCR2, I2CBR (I2CBRLSB and I2CBRMSB), I2CSLVADDR, I2CINTCR/I2CFIFOINTCR, and I2CFIFOTHRESHOLD. The FIFO Threshold register is optional since not every application requires almost empty/full thresholds.
- When the above registers are configured to the user-defined values, data transaction can begin by providing data to the I2CTXFIFO in FIFO Mode, or by providing data to I2CTXDR followed by I2CCMDR in Register Mode. The other registers, such as I2CSR or I2CRXFIFO, can be read when interrupt occurs or when the FIFO flags indicate appropriate states.

Table 2.2 provides the list of user-configurable parameters for the I2CFIFO Module. These parameter settings are specified using Module/IP Block Wizard in Lattice Radiant Software.

Table 2.2. Attribute Summary

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
Use Dedicated Pins	Checked, Unchecked	Unchecked	Include I/O Buffers is Checked
General Call Enable	Checked, Unchecked	Unchecked	—
Include I/O Buffers	Checked, Unchecked	Checked	—
SDA Input Delay (ns)	0, 50	0	—
SDA Output Delay (ns)	0, 50, 75, 100, 150, 200, 300, 350	300	—
Actual SDA Output Delay	Calculated	300	SDA Output Delay (ns)
Master Clock Rate			
System Clock Frequency (MHz)	10–250	50	—
Desired Frequency (kHz)	40, 100, 400, 1000	100	—
Prescaler	Calculated	124	System Clock Frequency (MHz), Desired Frequency (kHz)
Actual Frequency (kHz)	Calculated	100	System Clock Frequency (MHz), Prescaler
FIFO Mode			
Enable FIFO Mode	Checked, Unchecked	Unchecked	—
CLK Stretch Enable	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
RxFIFO Almost Full	1–31	30	Enable FIFO Mode is Checked
TxFIFO Almost Empty	1–15	3	Enable FIFO Mode is Checked
Sleep Clock Enable	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
Addressing			
I2C Addressing mode	7-bit, 10-bit	7-bit	—
LSB Select	Register, HW Tie	HW Tie	—
Address	1–31,	—	—
PMU Wake Options			
Address Match	Checked, Unchecked	Unchecked	—
RxFIFO Almost Full	Checked, Unchecked	Unchecked	—
FIFO Master Read Complete	Checked, Unchecked	Unchecked	—

Attribute	Selectable Values	Default	Dependency on Other Attributes
Non-FIFO Interrupts			
Arbitration Lost	Checked, Unchecked	Unchecked	Enable FIFO Mode is Unchecked
Tx/Rx Ready	Checked, Unchecked	Unchecked	Enable FIFO Mode is Unchecked
Overrun or NACK	Checked, Unchecked	Unchecked	Enable FIFO Mode is Unchecked
General Call IRQ Enable	Checked, Unchecked	Unchecked	Enable FIFO Mode is Unchecked
FIFO Interrupts			
General Call IRQ Enable	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
Receive NACK	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
Master Read Complete	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
Arbitration Lost	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
TxFIFO Sync Error	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
TxFIFO Overflow	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked
RxFIFO Overflow	Checked, Unchecked	Unchecked	Enable FIFO Mode is Checked

2.4. Register Description

2.4.1. Overview

Table 2.3. List of Configuration or Status Registers in I2CFIFO Module

Offset/Address (Hex)	Name	Description	Usage	Register Width	INIT Access	LMMI Access
00	I2CNONUSRCR1	I^2C Non-User Control Register 1	Configuration	8	R/W	R/MW
02	I2CCR1	I^2C Control Register 1	Configuration	8	R/W	R/W
04	I2CCR2	I^2C Control Register 2	Configuration	8	R/W	R/W
06	I2CBRLSB	I^2C Clock Prescale register, LSB	Configuration	8	R/W	R/W
08	I2CBRMSB	I^2C Clock Prescale register, MSB	Configuration	8	R/W	R/W
0A	I2CSLVADDR_LSB	I^2C Slave Address Register, LSB	Configuration	8/10	R/W	R/W
0B	I2CSLVADDR_MSB	I^2C Slave Address Register, MSB	Configuration	—	—	—
0C	I2CINTCR/ I2CFIFOINTCR	I^2C Reg Mode Interrupt Control Register/I^2C FIFO Mode Interrupt Control Register	Configuration	8/10	R/W	R/W
0E	I2CFIFOTHRESHOLD	I^2C FIFO Threshold Register	Configuration	10	R/W	R/W
10	I2CCMDR	I^2C Command Register	Interactive	8	R/W	R/W
12	I2CTXDR/I2CTXFIFO	I^2C Transmitting Data Register/I^2C Transmit Data FIFO	Interactive	8/10	W*	W*
14	I2CRXDR/I2CRXFIFO	I^2C Receiving Data Register/I^2C Receive Data FIFO	Interactive	8/10	R*	R*
16	I2CGCDR	I^2C General Call Information Register	Interactive	8	R	R
18	I2CSR/I2CFIFOSR	I^2C Reg Mode Status Register/I^2C FIFO Mode Status Register	Interactive	8/10	R	R
1A	I2CINTSR/I2CFIFOINTSR	I^2C Reg Mode Interrupt Status Register/I^2C FIFO Mode Interrupt Status Register	Interactive	8/10	R	R
1C	I2CFIFOSMSR	I2CFIFO State Machine Status Register	Interactive	10	R	R
1E	I2CFIFOTXCNT	I^2C TXFIFO byte Counter	Interactive	10	R	R
20	I2CFIFORXCNT	I^2C RXFIFO byte Counter	Interactive	10	R	R
22	I2CINTFR / I2CFIFOINTFR	I^2C Reg Mode Interrupt Force Register/I^2C FIFO Mode Interrupt Force Register	Interactive	8/10	R/W	R/W
24	I2CNONUSRTEST	I^2C Non-User Test Mode Register	Interactive	8	R/W	R/MW

2.4.2. I²C Control Register 1 (I2CCR1)

I2CCR1 can be read or written through LMMI and INIT. A write operation through LMMI or INIT causes the I²C core reset.

Table 2.4. I2CCR1 Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	I2CEN	R/W	R/W	I²C System Enable Bit – Enables the I²C core functions. If I2CEN is cleared, I²C is disabled and forced into idle state, status bits in I2CSR/I2CFIFOSR register are reset. 0 – I²C disabled 1 – I²C enabled	0
6	GCEN	R/W	R/W	Generic call Response Enable Bit - Enables the generic call response in Slave Mode. 0 – Disabled 1 – Enabled	0
5	RSVD	N/A	N/A	Reserved	0
4	FIFO_MODE	R/W	R/W	I²C Mode Select - Choose between using FIFO or Register 0 – Register Mode (default) 1 – FIFO Mode	0
3:2	SDA_DEL_SEL[1]	R/W	R/W	SDA Output Delay Selection – These two bits select the output delay (in Number of clk cycle. The Base Delay is set by MSB of the I2CBRMSB) 2'b00 : NDelay = 0 2'b01 : NDelay = 1 * Nbase_delay + 3 ; (when Nbase_delay = 0, NDelay = 1) 2'b10 : NDelay = 2 * Nbase_delay + 3 ; (when Nbase_delay = 0, NDelay = 1) 2'b11 : NDelay = 4 * Nbase_delay + 3 ; (when Nbase_delay = 0, NDelay = 1)	00
1	CKSDIS/RSVD	N/A	N/A	FIFO Mode Clock Stretching Disable Option (this bit is used in FIFO Mode only; refer to i2ccmdr[2] for reg mode) — Disables clock stretching for both master and slave mode. Then, overflow error flag must be monitored. 0 – Enabled 1 – Disabled	0
0	SLP_CLK_EN	N/A	N/A	Sleep Clock Enable – Enables sleep clock to control fabric interface to continue I²C master FIFO operations during sleep. 0 – Disabled 1 – Enabled	0

Note:

1. When using a slow clock, SDA delay could be too large which may cause SDA glitch to happen. Set 2'b00 : NDelay = 0 to reduce the SDA delay to remove the glitch.

2.4.3. Control Register 2 (I2CCR2)

I2CCR1 can be read or written through LMMI and INIT.

Table 2.5. I2CCR2 Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	INTCLREN	R/W	R/W	Auto Interrupt Clear Enable – Enables the interrupt flag auto clear when the Interrupt Status Registers (I2CINTSR/I2CFIFOINTSR) are read. 0 – Disabled 1 – Enabled	0
6	SLVADDR_HARD_TIE	R/W	R/W	Slave Address Hard Tie Disable – Disables use of ADDR_LSB_TIE[1:0] as the lower 2 bits of the I^2C's slave address and allows full register to be Slave Address. 0 – Address using ADDR_LSB_TIE[1:0] 1 – Address using I2CSLVADDR value only	0
5:3	RSVD	N/A	N/A	Reserved	000
2	MRDCMPL_WKUP	R/W	R/W	Master Read Complete Device Wake-Up Enable – Enables I^2C Master Read Complete Flag for Device Wake-Up. Only available in Master Mode. 0 – Disabled 1 – Enabled	0
1	RXFIFO_AF_WKUP	R/W	R/W	RXFIFO Almost Full Device Wake-Up Enable – Enables I^2C RXFIFO Almost Full Flag for Device Wake-Up. Only available in Master Mode. 0 – Disabled 1 – Enabled	0
0	SLVADDR_WKUP	R/W	R/W	Slave Address Match Device Wake-Up Enable – Enables I^2C Slave Address Matching for Device Wake-Up. 0 – Disabled 1 – Enabled	0

2.4.4. I²C Command Register (I2CCMDR)

I2CCMDR can be read or written through LMMI in Register Mode. RBUFDIS is always at default value (0) for FIFO Mode. CKSDIS value is applicable in both the Register Mode and the FIFO Mode.

Table 2.6. I2CCMDR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	STA	N/A	R/W	Generate (Repeated) start Condition when combine with WR bit (bit 4) for master mode once the TXDR is ready.	0
6	STO	N/A	R/W	Generate STOP Condition (Exclusive with STA bit) for master mode	0
5	RD	N/A	R/W	Read from Slave for master mode	0
4	WR	N/A	R/W	Write to Slave for master mode	0
3	ACK	N/A	R/W	Acknowledge Option - When receive, ACK transmission selection for both master and slave mode 0 – Send ACK 1 – Send NACK	0
2	CKSDIS	N/A	R/W	Clock Stretching Disable Option - Disable the clock stretching if desired by the user for both master and slave mode. Then overflow error flag must be monitored. 0 – Clock Stretching is enabled 1 – Clock Stretching is disabled	0
1	RBUFDIS	N/A	R/W	Read Command With Buffer Disabled – Read from Slave in master mode with the double buffering disabled for easier control over single byte data communication scenario. 0 – Read with buffer is enabled as default 1 – Read with buffer is disabled	0
0	RSVD	N/A	N/A	Reserved	0

2.4.5. I²C Clock Pre-Scale Register (I2CBR)

I2CBR can be read or written through LMMI or INIT. Two Write or Read operations are required to access the I2CBR at different addresses. One address is for I2CBRLSB [7:0] and second address for I2CBRMSB [7:0]. A Write operation through LMMI or INIT to either I2CBRLSB or I2CBRMSB causes the I²C core reset.

Bits arrangement for I2CBRLSB is shown below.

Table 2.7. I2CBRLSB Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:0	I2CBR	R/W	R/W	Clock Divider FSCL = FSOURCE / (4 * (NI2CBR[9:0] + 1))	00000000

Bits arrangement for I2CBRMSB is shown below.

Table 2.8. I2CBRMSB Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:4	NBASEDELAY	R/W	R/W	Nbase_delay[3:0]	0000
3:2	RSVD	N/A	N/A	Reserved	00
1:0	I2CBR	R/W	R/W	Clock Divider I2CBR[9:8]	00

2.4.6. I²C Status Register (I2CSR)/I2CFIFO Status Register (I2CFIFOSR)

This address is shared by both Register Mode and FIFO Mode. However, the definition of each status bit is different for each mode. These registers can only be read through LMMI.

2.4.6.1. I2CSR Register Description

Table 2.9. I2CSR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	TIP	R	R	Transmitting In Progress – This bit indicates that current data byte is being transferred for both master and slave mode Note that the TIP flag suffers half SCL cycle latency right after the start condition because of the signal synchronization. Also note that this bit could be high after configuration wake-up and before the first valid I²C transfer start (when BUSY is low), and it is not indicating byte in transfer, but an invalid indicator. 0 – Byte transfer completed. 1 – Byte transfer in progress.	0
6	BUSY	R	R	Bus busy – This bit indicates the bus is involved in a transaction. This is set at start condition and cleared at stop. Therefore, only when this bit is high, should all other status bits be treated as valid indicators for a valid transfer.	0
5	RARC	R	R	Received Acknowledge – This flag represents acknowledge response from the addressed slave during master write or from receiving master during master read. 1 – No acknowledge received 0 – Acknowledge received	0
4	SRW	R	R	Slave RW: 1 – Master receiving / Slave transmitting 0 – Master transmitting / Slave receiving	0
3	ARBL	R	R	Arbitration Lost – This bit goes high if the master has lost its arbitration in Master mode, it causes an interrupt to system host if set in I2CINTCR. 1 – Arbitration Lost 0 – Normal	0
2	TRRDY	R	R	Transmitter or Receiver Ready Bit – This flag indicates that a Transmit Register ready to receive data or Receiver Register is ready for read depend on the mode (master or slave) and SRW bit. It causes an interrupt to system host if set in I2CINTCR. 1 – Transmitter or Receiver is ready 0 – Transmitter or Receiver is not ready	0
1	TROE	R	R	Transmitter/Receiver Overrun or NACK Received Bit – This flag indicates that a Transmit or Receive Overrun Errors happened depend on the mode (master or slave) and SRW bit, or a no-acknowledges response is received after transmitting a byte. If RARC bit is high, it is a NACK bit; otherwise, it is an Overrun bit. It causes an interrupt to system host if set in I2CINTCR. 1 – Transmitter or Receiver Overrun or No-Acknowledge Received for Transmitting 0 – Transmitter or Receiver Normal or Acknowledge Received for Transmitting	0

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
0	HGC	R	R	Hardware General Call Received - This flag indicates that a hardware general call is received from the slave port. It causes an interrupt to system host if set in I2CINTCR. 1 – Hardware General Call Received in Slave Mode 0 – NO Hardware General Call Received in Slave Mode	0

Note: A high in I2CSR [3:0] registers cause an interrupt to system host if the corresponding interrupt control registers (I2CINTCR [3:0]) are enabled.

2.4.6.2. I2CFIFOSR Register Description

Table 2.10. I2CFIFOSR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9	ADM	R	R	Slave Address Matched - Indicates that this I^2C's slave address has matched with an address sent by an external master. This status stays active for entire transmission.	0
8	BUSY	R	R	Bus busy – This bit indicates the bus is involved in a transaction. This is set at start condition and cleared at stop. Therefore, only when this bit is high, should all other status bits be treated as valid indicators for a valid transfer.	0
7	SRW	R	R	Slave RW: 1 – Master receiving / Slave transmitting 0 – Master transmitting / Slave receiving	0
6	HGC	R	R	Hardware General Call Received – This flag indicate that a hardware general call is received from the slave port. It causes an interrupt to system host if set in I2CINTCR. 1 – Hardware General Call Received in Slave Mode 0 – NO Hardware General Call Received in Slave Mode	0
5	RNACK	R	R	Received NACK - This flag represents acknowledge response from the addressed slave during master write. 1 – No acknowledge (NACK) is received; FIFO state machine issues an STOP and go to idle state. 0 – Acknowledge received	0
4	MRDCMPL	R	R	Master Read Complete – This is only valid for Master Read mode. 0 – Transaction is not completed 1 – Transaction is completed. In Master read mode, it means 1) the number of bytes read equals to the expected number, 2) Master terminates the read earlier but there is data in the RX FIFO.	0
3	ARBL	R	R	Arbitration Lost – This bit goes high if the master has lost its arbitration in Master mode 1 – Arbitration Lost, FIFO state machine goes to idle state. 0 – Normal	0
2	TXSERR	R	R	TX FIFO synchronization error – This happens when there are back-to-back commands in the FIFO. 0 – No synchronization error 1 – Synchronization error. The previous command is overwritten and continued with the next data entry in the FIFO.	0
1	TXUNDERF	R	R	TX FIFO underflow – Indicates an error condition, mutually exclusive with clock stretching function 0 – Not underflow 1 – FIFO underflow; data is not valid	0

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
0	RXOVERF	R	R	RX FIFO overflow – indicates an error condition, mutually exclusive with clock stretching function 0 – Not overflow 1 – FIFO overflow, data is not valid	0

Note: A high in any bit of this register causes an interrupt to the system host if the corresponding interrupt control registers (I2CFIFOINTCR) are enabled. MRDCMPL has a dedicated interrupt signal to the fabric. The rest of the status shares a common interrupt to the fabric.

2.4.7. I²C Transmitting Data Register (I2CTXDR)/Transmitting FIFO (I2CTXFIFO)

This address is shared by both Register Mode and FIFO Mode. During Register Mode, it is a 1-byte register, during FIFO Mode, it is 10-bit x 32 byte FIFO.

2.4.7.1. I2CTXDR Description

Table 2.11. I2CTXDR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:1	TXDATA[7:1]	N/A	W	Next byte to transmit through I²C	0000000
0	TXDATA[0]/R_W	N/A	W	In case of a data transfer, this bit represents the data's LSB. In case of a slave address, transfer this bit represents the RW bit 1 – Reading from Slave 0 – Writing to Slave	0

2.4.7.2. I2CTXFIFO Description

The I2CTXFIFO is Write only. However, a Read to this location during FIFO Mode causes the I2CTXFIFO to be reset (reset the pointers). The 2 MSB bits are the command bits, while the 8 LSBs are for data or Slave address. The 8-bit data can be interpreted differently depending on the value of bit 9. The CMD bit and the RSTAEN/LTXBYTE bit are meaningful and used when the IP is in Master Mode.

Bits [7:5] can be used as part of the RXBYTE value if the FIFO size extends beyond 32 bytes. The range of bits [4:0] is 0 to 31, with a *0* indicates receiving 1 byte, a *1* receiving 2 bytes, and a *31*receiving 32 bytes, and so on. Therefore, an I²C Read must receive at least 1 byte.

In the Master Mode, if you want to abort current transaction, the TXFIFO must be reset by issuing a Read to TXFIFO or using the FIFO_RST signal. When TXFIFO is reset while the State Machine is in Transmit Mode, it issues a STOP after the current byte is transmitted. When TXFIFO is reset and the State Machine is in Receive Mode, it issues a NACK+STOP. This is to make sure the I²C bus is gracefully released.

Table 2.12. I2CTXFIFO Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:8	CMD/FLAGs	N/A	W	Two command bits to direction the I²C state machine. *CMD, RSTAEN* 10 – Bits [4:0] of this byte is the number of bytes to be received (in Master mode). Following data transaction should be sent using a STOP then a START. 11 – Bits [4:0] of this byte is the number of bytes to be received (in Master mode). Following data transaction should be sent using a START/ReSTART. The 1st data byte should always has RSTAEN bit set to 1. *CMD, LTXBYTE* 00 – Bits [7:0] of this byte are data bits. If this is the last data byte in the TXFIFO, then depending on the CKSDIS bit, Master Write either goes into clock stretching (CKSDIS=0), or TXFIFO underflows (CKSDIS=1). 01 – Bits [7:0] of this byte are data bytes. If this is the last data byte in TXFIFO, this indicates the last byte to	00

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
				be transferred and a STOP is issued. If this is not the last byte in TXFIFO, then this bit is ignored.	
7	RSVD/DATA	N/A	W	Not used when CMD =1, bit 7 of the data byte when CMD =0	0
6	RSVD/DATA	N/A	W	Not used when CMD =1, bit 6 of the data byte when CMD =0	0
5	RSVD/DATA	N/A	W	Not used when CMD =1, bit 5 of the data byte when CMD =0	0
4	RXBYTE/DATA	N/A	W	Bit 4 of RXBYTE value when CMD =1, bit 4 of the data byte when CMD = 0	0
3	RXBYTE/DATA	N/A	W	Bit 3 of RXBYTE value when CMD =1, bit 3 of the data byte when CMD = 0	0
2	RXBYTE/DATA	N/A	W	Bit 2 of RXBYTE value when CMD =1, bit 2 of the data byte when CMD = 0	0
1	RXBYTE/DATA	N/A	W	Bit 1 of RXBYTE value when CMD =1, bit 1 of the data byte when CMD = 0	0
0	RXBYTE/DATA	N/A	W	Bit 0 of RXBYTE value when CMD =1, bit 0 of the data byte when CMD = 0	0

2.4.8. Receiving Data Register (I2CRXDR)/Receiving FIFO (I2CRXFIFO)

This address is shared by both Register Mode and FIFO Mode. During Register Mode, it is a 1-byte register, during FIFO Mode, it is 10bit x 32 byte FIFO.

2.4.8.1. I2CRXDR Description

Table 2.13. I2CRXDR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:0	RXDATA	N/A	R	Received Data	00000000

2.4.8.2. I2CRXFIFO Description

The I2CRXFIFO is Read only. However, a Write to this location during FIFO Mode causes the I2CRXFIFO to be reset (reset the pointers). The two MSB bits are the command bits, while the eight LSBs are for data.

Table 2.14. I2CRXFIFO Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9	RSVD	N/A	N/A	Reserved	0
8	DFIRST	N/A	R	Last Byte of Data 0 – Normal data 1 – First byte received after a Start or a ReStart is detected	0
7:0	DATA	N/A	R	Data received	00000000

2.4.9. I²C General Call Information Register (I2CGCDR)

This register contains information for the general call when I²C port is used as a Slave. If D0 of I2CGCDR is *ZERO*, this byte is the general command (H'00 is illegal). If D0 is *ONE*, as a *hardware general call*, D7:D1 is the address of the hardware Master devices, such as a keyboard, scanner, and so on.

Once a general call is received and the GCEN bit inside the I2CCR1 is set, an interrupt is sent out to the system host, and the status bits that associated with HCG are set in Status Registers and Interrupt Status Registers.

Table 2.15. I2CGCDR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:0	GCDATA	—	—	Received General Call Data	00000000

2.4.10. I²C Slave Address (I2CSLVADDR)

This address is shared by both Register Mode and FIFO Mode. It can be read or written through system data bus. Any change upon this register causes the I²C core reset. Depending on the setting in I2CCR2[6], the address in this register is either the full address or the MSB of the Slave address. If it is the MSB, the LSB is determined by hardware ties of ADDR_LSB_TIE[1:0]. If the I2CSLVADDR register in Hard Tied Mode is ZERO (8'H00), then a default value of 8'HF8 is taken in order to avoid conflict with reserved addresses of I²C specification. If the I2CSLVADDR register without Hard Tied Mode is ZERO (10'H000), then a default value of 10'H060 is taken in order to avoid conflict with reserved addresses of I²C specification.

Table 2.16. I2CSLVADDR Register with 7 Bit Addressing and Hard Tied LSB

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:5	RSVD	N/A	N/A	Reserved	00000
4:0	7BITADDRMSB	R/W	R/W	MSB of I²C 7 Bit Slave Address	00000

Table 2.17. I2CSLVADDR Register with 10 Bit Addressing and Hard Tied LSB

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:8	RSVD	N/A	N/A	Reserved	00
7:0	10BITADDRMSB	R/W	R/W	MSB of I²C 10 Bit Slave Address	00000000

Table 2.18. I2CSLVADDR Register with 7 Bit Addressing and without Hard Tied LSB

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:7	RSVD	N/A	N/A	Reserved	000
6:0	7BITADDR	R/W	R/W	I²C 7 Bit Slave Address	0000000

Table 2.19. I2CSLVADDR Register with 10 Bit Addressing and without Hard Tied LSB

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:0	10BITADDR	R/W	R/W	10 Bit I²C Slave Addressing	0000000000

2.4.11. I²C Interrupt Control Register (I2CINTCR)/I2CFIFO Interrupt Control Register (I2CFIFOINTCR)

This address is shared by both Register Mode and FIFO Mode. The register can be read or written through LMMI and INIT.

2.4.11.1. I2CINTCR Description

Table 2.20. I2CINTCR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	RSVD	N/A	N/A	Reserved	0
6	RSVD	N/A	N/A	Reserved	0
5	RSVD	N/A	N/A	Reserved	0
4	RSVD	R/W	R/W	Reserved	0
3	ARBL_IE	R/W	R/W	Arbitration Lost Interrupt Enable – Enable arbitration Lost Interrupt 0 – Disabled 1 – Enabled	0
2	TRRDY_IE	R/W	R/W	Transmit/Receive Register Ready Interrupt Enable – Enable TRRDY interrupt 0 – Disabled 1 – Enabled	0
1	TROE_IE	R/W	R/W	Transmit/Receive Register Overrun Interrupt Enable – Enable TROE interrupt 0 – Disabled 1 – Enabled	0
0	HGC_IE	R/W	R/W	General Call Interrupt Enable – Enable General Call interrupt 0 – Disabled 1 – Enabled	0

2.4.11.2. I2CFIFOINTCR Description

Table 2.21. I2CFIFOINTCR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9	RSVD	N/A	N/A	Reserved	0
8	RSVD	N/A	N/A	Reserved	0
7	RSVD	N/A	N/A	Reserved	0
6	HGC_IE	R/W	R/W	General Call Interrupt Enable 0 – Disabled 1 – Enabled	0
5	RNACK_IE	R/W	R/W	Receive NACK Interrupt Enable 0 – Disabled 1 – Enabled	0
4	MRDCMPL_IE	R/W	R/W	Master Read Complete Enable 0 – Disabled 1 – Enabled	0
3	ARBL_IE	R/W	R/W	Arbitration Lost Interrupt Enable - Enable arbitration Lost Interrupt 0 – Disabled 1 – Enabled	0
2	TXSERR_IE	R/W	R/W	TX FIFO Synchronization error Interrupt Enable 0 – Disabled 1 – Enabled	0

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
1	TXUNDERF_IE	R/W	R/W	TXFIFO Underflow interrupt enable 0 – Disabled 1 – Enabled	0
0	RXOVERF_IE	R/W	R/W	RXFIFO overflow interrupt enable 0 – Disabled 1 – Enabled	0

2.4.12. I²C Interrupt Force Register (I2CINTFR)/I2CFIFO Interrupt Force Register (I2CFIFOINTFR)

This address is shared by both Register Mode and FIFO Mode. The register can be read or written through LMMI.

2.4.13. I2CINTFR Description

Table 2.22. I2CINTFR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	RSVD	N/A	N/A	Reserved	0
6	RSVD	N/A	N/A	Reserved	0
5	RSVD	N/A	N/A	Reserved	0
4	RSVD	R/W	R/W	Reserved	0
3	ARBL_INTFRC	R/W	R/W	Arbitration Lost Force Interrupt – Force arbitration Lost Interrupt 0 – Disabled 1 – Enabled	0
2	TRRDY_INTFRC	R/W	R/W	Transmit/Receive Register Ready Force Interrupt – Force TRRDY interrupt 0 – Disabled 1 – Enabled	0
1	TROE_INTFRC	R/W	R/W	Transmit/Receive Register Overrun Force Interrupt – Force TROE interrupt 0 – Disabled 1 – Enabled	0
0	HGC_INTFRC	R/W	R/W	General Call Force Interrupt – Force General Call interrupt 0 – Disabled 1 – Enabled	0

2.4.13.1. I2CFIFOINTFR Description

Table 2.23. I2CFIFOINTFR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9	RSVD	N/A	N/A	Reserved	0
8	RSVD	N/A	N/A	Reserved	0
7	RSVD	N/A	N/A	Reserved	0
6	HGC_INTFRC	R/W	R/W	General Call Force Interrupt 0 – Disabled 1 – Enabled	0
5	RNACK_INTFRC	R/W	R/W	Receive NACK Force Interrupt 0 – Disabled 1 – Enabled	0
4	MRDCMPL_INTFRC	R/W	R/W	Master Read Complete Force Interrupt 0 – Disabled 1 – Enabled	0
3	ARBL_INTFRC	R/W	R/W	Arbitration Lost Force Interrupt - Force arbitration Lost Interrupt 0 - Disabled 1 - Enabled	0
2	TXSERR_INTFRC	R/W	R/W	TX FIFO Synchronization error Force Interrupt 0 – Disabled 1 – Enabled	0
1	TXUNDERF_INTFRC	R/W	R/W	TXFIFO Underflow Force interrupt 0 – Disabled 1 – Enabled	0
0	RXOVERF_INTFRC	R/W	R/W	RXFIFO overflow Force interrupt 0 – Disabled 1 – Enabled	0

2.4.14. I²C Interrupt Status Register (I2CINTSR)/I2CFIFO Interrupt Status Register (I2CFIFOINTSR)

This address is shared by both Register Mode and FIFO Mode. The register can be read through LMMI.

2.4.14.1. I2CINTSR Description

An LMMI Write to this register with a particular bit set causes the corresponding interrupt request flags cleared. If bit [7] of I2CCR2 is set, reading of the register causes all IRQ flag from this IP cleared.

Table 2.24. I2CINTSR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7	RSVD	N/A	N/A	Reserved	0
6	RSVD	N/A	N/A	Reserved	0
5	RSVD	N/A	N/A	Reserved	0
4	RSVD	N/A	N/A	Reserved	0
3	ARBL_IRQ	R	R	Arbitration Lost Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
2	TRRDY_IRQ	R	R	Transmit/Receive Register Ready Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
1	TROE_IRQ	R	R	Transmit/Receive Register Overrun Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
0	HGC_IRQ	R	R	General Call Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0

2.4.14.2. I2CFIFOINTSR Description

An LMMI Write to this register with a particular bit set causes the corresponding interrupt request flags cleared. If bit[7] of I2CCR2 is set, reading of the register causes all IRQ flag from this IP cleared.

Table 2.25. I2CFIFOINTSR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:7	RSVD	N/A	N/A	Reserved	000
6	HGC_IRQ	R	R	General Call Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
5	RNACK_IRQ	R	R	NACK Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
4	MRDCMPL_IRQ	R	R	Master Read Completion Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
3	ARBL_IRQ	R	R	Arbitration Lost Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
2	TXSERR_IRQ	R	R	TXFIFO Synchronization Error Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0
1	TXUNDERF_IRQ	R	R	TXFIFO Underflow Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
0	RXOVERF_IRQ	R	R	RXFIFO Overflow Interrupt Request Flag 0 – No Interrupt Request 1 – Interrupt Request Pending	0

2.4.15. I²C FIFO Threshold Register (I2CFIFOTHRESHOLD)

This register stores the FIFO threshold values. This register can be read or written and is used in FIFO Mode.

Table 2.26. I2CFIFOTHRESHOLD Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:5	RXFIFO_AF_VAL	R/W	R/W	5-bit Almost Full value for the RX FIFO	00000
4:0	TXFIFO_AE_VAL	R/W	R/W	5-bit Almost Empty value for the TX FIFO	00000

2.4.16. I2CFIFO State Machine Status Register (I2CFIFOSMSR)

This is a read only register and is for FIFO Mode debugging purpose. It shows the current state of the FIFO State Machine. Depending on the implementation, this register can be split into two registers, one for TX State Machine and the other for RX State Machine. In general, FIFO State Machine goes back to idle when transactions are done. FIFO State Machine cannot be asynchronously reset because complete transactions on I²C bus have to be guaranteed to follow the I²C spec.

Table 2.27. I2CFIFOSMSR Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
9:5	RSVD	N/A	N/A	Reserved	00000
4:0	STATE_DATA	R*	R	State Machine Status Data	00000

2.4.17. I2CFIFO TX Byte Counter (I2CFIFOTXCNT)

This is a read only register. It stores the current counts of data bytes transmitted onto the I²C port. The number of bytes is accumulative until the counter is cleared. A write to this register or assertion of FIFO_RST signal causes the counter to be cleared.

Table 2.28. I2CFIFOTXCNT Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:0	TX_BYTE_CNT	R*	R	The number of data bytes transmitted to the I²C port	00000000

2.4.18. I2CFIFO RX Byte Counter (I2CFIFORXCNT)

This is a read only register. It stores the current counts of data bytes that have been presented to the RXFIFO. The number of bytes is accumulative until the counter is cleared. A write to this register or assertion of FIFO_RST signal causes the counter to be cleared.

Table 2.29. I2CFIFORXCNT Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:0	RX_BYTE_CNT	R*	R	The number of data bytes received at the RX FIFO	00000000

2.4.19. I²C Non-User Control Register 1 (I2CNONUSRCR1)

This is a protected Non-User register that controls several muxes in the design. It must be set by the INIT interface for the I²C to run correctly. It can be used via LMMI when in manufacturing test mode.

Table 2.30. I2CNONUSRCR1 Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:4	RSVD	N/A	N/A	Reserved	0000
3	SDA_OUT_DLY_EN	R/W	R/MW	Enables 50ns Analog SDA Output Delay 0 – Disabled 1 – Enabled	0
2	SDA_IN_DLY_EN	R/W	R/MW	Enables 50ns Analog SDA Input Delay 0 – Disabled 1 – Enabled	0
1	ALT_IO_EN	R/W	R/MW	Enables Alternate SCL and SDA Path to Hard I/O 0 – Fabric SCL and SDA 1 – Hard I/O SCL and SDA	0
0	FILTER_DIS	R/W	R/MW	Disables SCL and SDA Input Glitch Filter 0 – Filter Enabled 1 – No Filter	0

2.4.20. I²C Non-User Test Mode Register (I2CNONUSRTEST)

This is a protected Non-User register that enables and controls a number of test features in the design. This register should NOT be set in INIT mode, and should only be used via LMMI in manufacturing test mode.

Table 2.31. I2CNONUSRTEST Register Details

Bit(s)	Label	INIT R/W	LMMI R/W	Description	Default
7:4	RSVD	N/A	N/A	Reserved	0000
3:1	SOFT_TRIM_VALUE	R/W	R/MW	Soft Trim Value – Capacitance trim value for 50ns Filter and 50ns Delay. Default on power up is 3'b000, after a clock cycle this value with take current hard trim value.	000
0	SOFT_TRIM_EN	N/A	N/A	Soft Trim Enable - Enables soft trimming of the capacitance of the 50 ns Filter and 50 ns Delay. 0 – Disabled (Hard Trim Path Used) 1 – Enabled	0

2.5. FIFO Mode Data Transaction

Below are a few examples of data transaction in FIFO Mode. The FIFO status of transmitting FIFO and receiving FIFO are available to the fabric for the host to monitor all the time. It is assumed that the control register and some other necessary registers are configured before the data transaction can happen. Details of configuration sequence are shown in Figure 2.1. The definition of the TXFIFO/RXFIFO byte is defined in the I2CFIFOSR Register Description and the I2CTXFIFO Description sections.

2.5.1. I²C Master Write (Master-Transmitter)

The host in the FPGA fabric initiates a WRITE on the I²C bus by providing data to the TXFIFO. I²C controller interprets the data in the FIFO and issues commands to carry out the I²C sequences. The host provides a command byte, a Slave address byte, and data to be transmitted. In normal operation, a Slave ACKs the Master after receiving each byte. If a NACK is received, an interrupt is sent to the host. The host can decide to stop the transaction by clearing the FIFO, or continue until all the data is transferred.

Table 2.32. Mode Master Write TXFIFO Contents

TXFIFO									
CMD	RSTA/LTXBYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0 = no read							
0	0	Slave Addr + W							
0	0	Data 0							
0	1	Data 1							

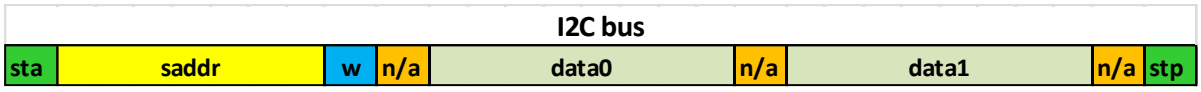


Figure 2.2. Master Mode Write I²C Data Diagram

2.5.2. I²C Master Read (Master – Receiver)

When a Restart is required, the host provides a minimum of a command byte and a Slave address byte, as shown in this case. The host can read from the RXFIFO anytime when the RXFIFO is not empty. When the last byte of data is received, the host is informed by a status signal from the IP to the fabric.

Table 2.33. Master Mode Read TXFIFO Contents

TXFIFO									
CMD	RSTA/ LTXBYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0 = no read							
0	0	Slave Addr + W							
0	0	Data 0/ Sub-Address (such as. Sub-Address from I²C Slave Memory)							
1	1	1							
0	0	Slave Addr + R							

Table 2.34. Master Mode Read RXFIFO Contents

RXFIFO									
RSVD	DFIRST	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	Data 0 (First Byte Received)							
0	0	Data 1							

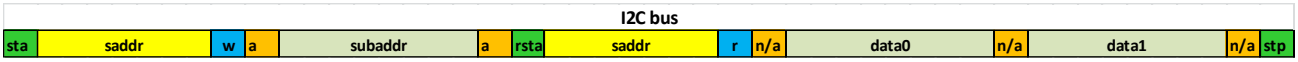


Figure 2.3. Master Mode Read I²C Data Diagram

2.5.3. Slave Write (Slave – Receiver)

The host is informed that data is available in the RXFIFO. If RXFIFO is full while the external Master continues to send data, the I²C Controller issues a NACK or carry out clock stretching depending on the CKSDIS bit is set or not.

Table 2.35. Slave Mode Write RXFIFO Contents

RXFIFO									
RSVD	DFIRST	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	Data 0 (First Byte Received)							
0	0	Data 1							
0	0	Data 2							
0	0	Data 3							

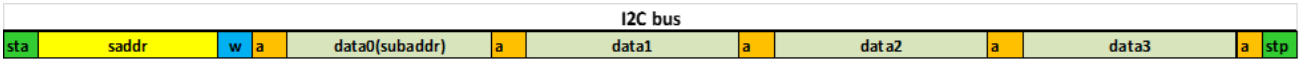


Figure 2.4. Slave Mode Write I²C Data Diagram

2.5.4. I²C Slave Read (Slave – Transmitter)

The host is informed that data is required by an external I²C Master through the Read command. Host provides data to the TXFIFO. If there is no data in the TXFIFO, the I²C Controller issues a NACK or carry out clock stretching depending on the CKSDIS bit is set or not. It is recommended the host clears the TXFIFO first before dumping data into the FIFO.

Table 2.36. Slave Mode Read RXFIFO Contents

RXFIFO									
RSVD	DFIRST	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	Data 0 (Sub-Address / Read Command)							

Table 2.37. Slave Mode Read TXFIFO Contents

TXFIFO									
CMD	RSTA/LTXBYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	Data 0							
0	0	Data 1							
0	0	Data 2							

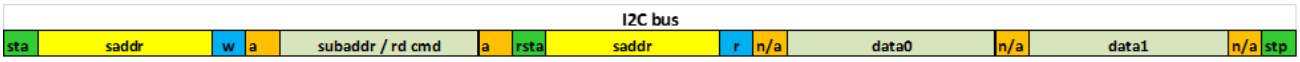


Figure 2.5. Slave Mode Read I²C Data Diagram

2.6. Timing Specifications

This chapter contains operational timing diagrams applicable to the I2CFIFO Module.

2.6.1. LMMI Write Operation

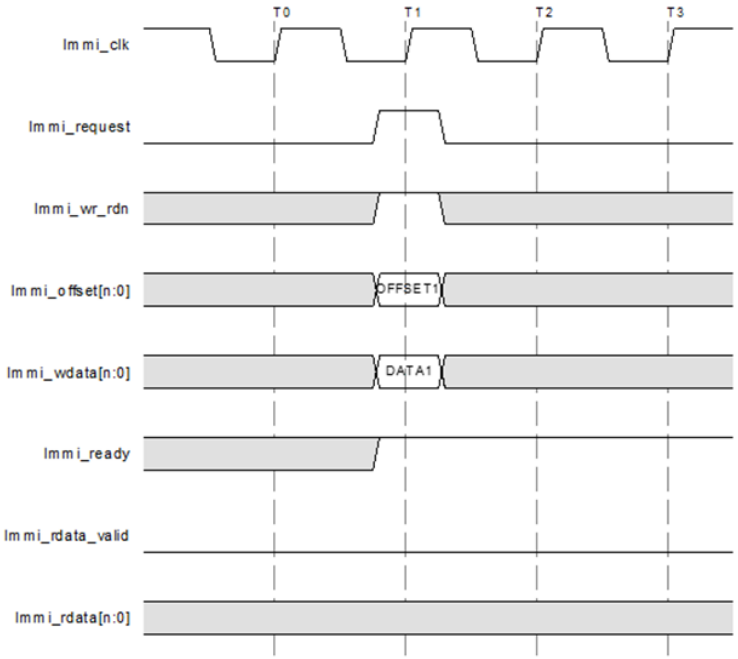


Figure 2.6. LMMI Write Operation

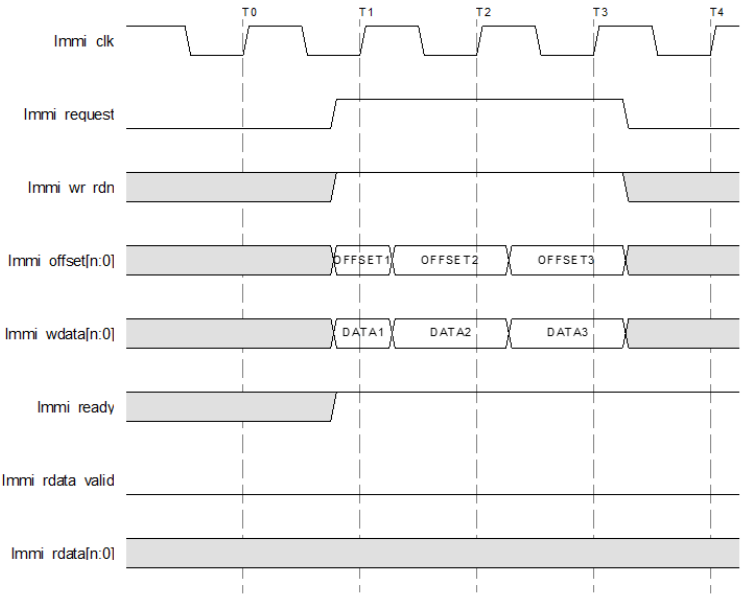


Figure 2.7. LMMI Burst Write Operation

2.6.2. LMMI Read Operation

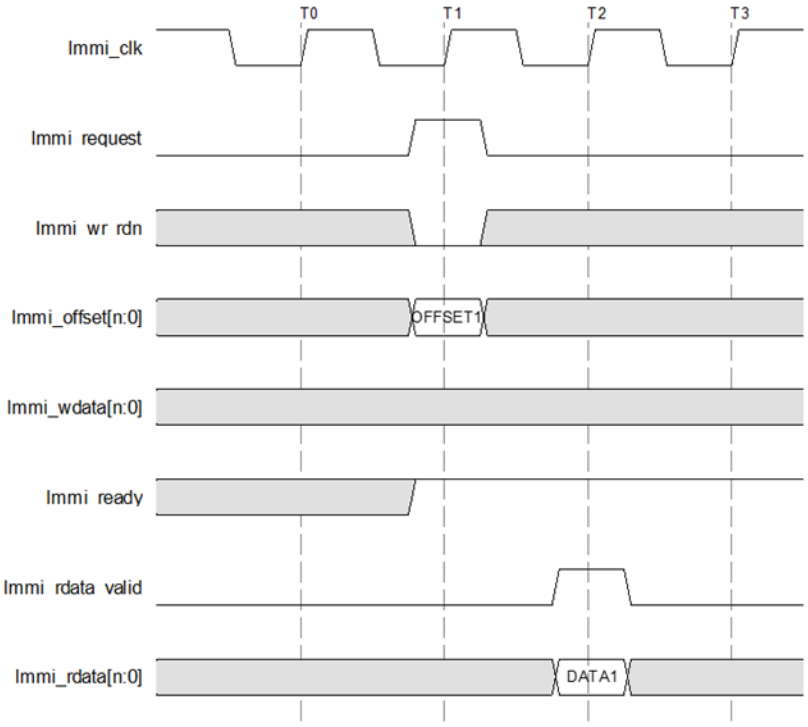


Figure 2.8. LMMI Read Operation

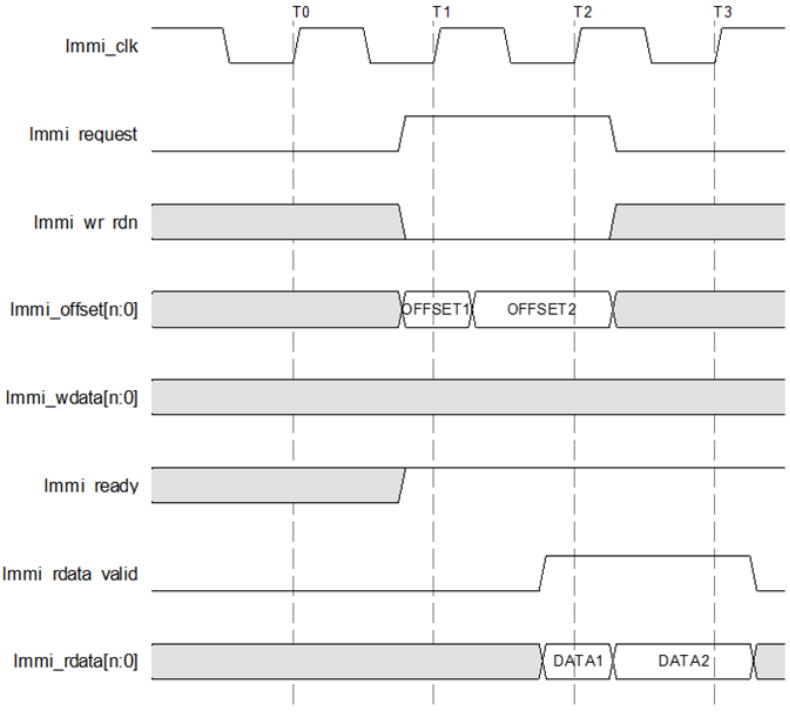


Figure 2.9. LMMI Burst Read Operation

2.7. I²C Transactions with LMMI Register Status

2.7.1. Master I²C Write

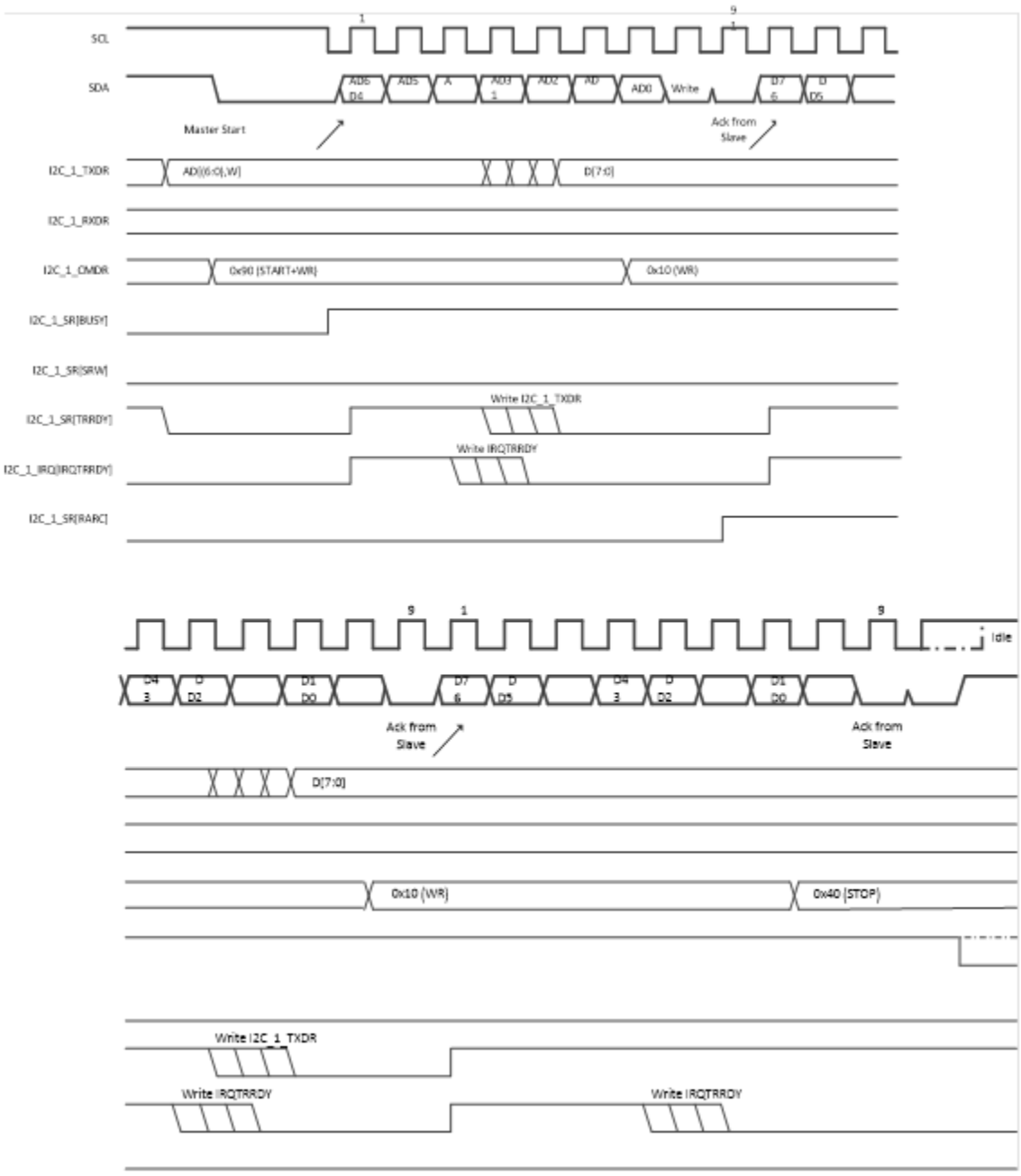
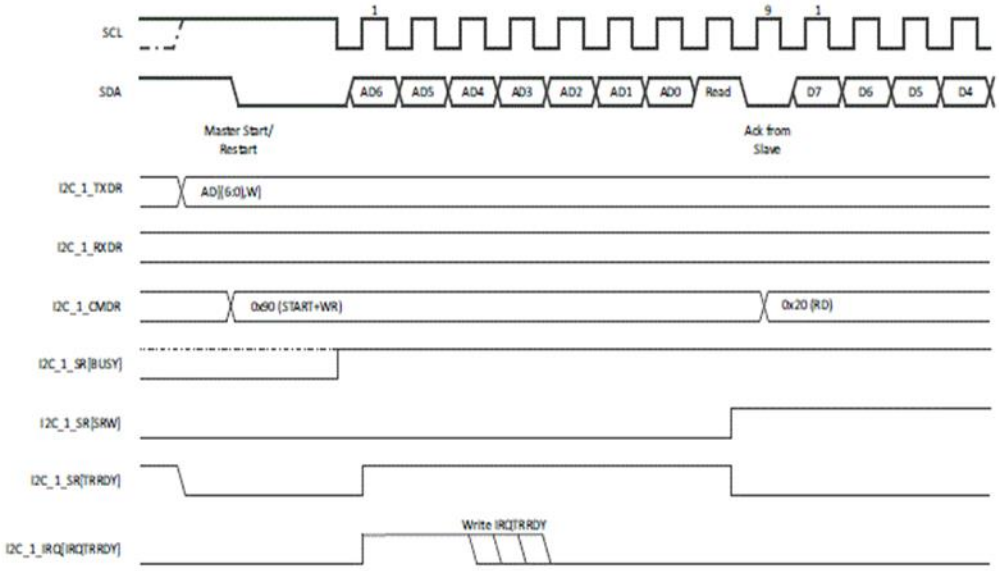


Figure 2.10. Master I²C Write with Register Status

2.7.2. Master I²C Read



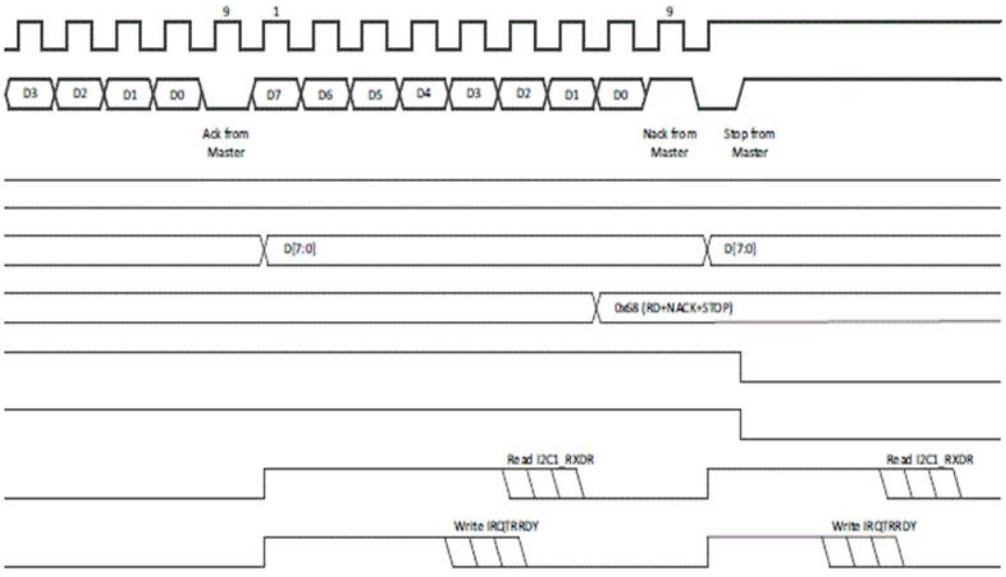


Figure 2.11. Master I²C Read with Register Status

2.7.3. Slave I²C Write

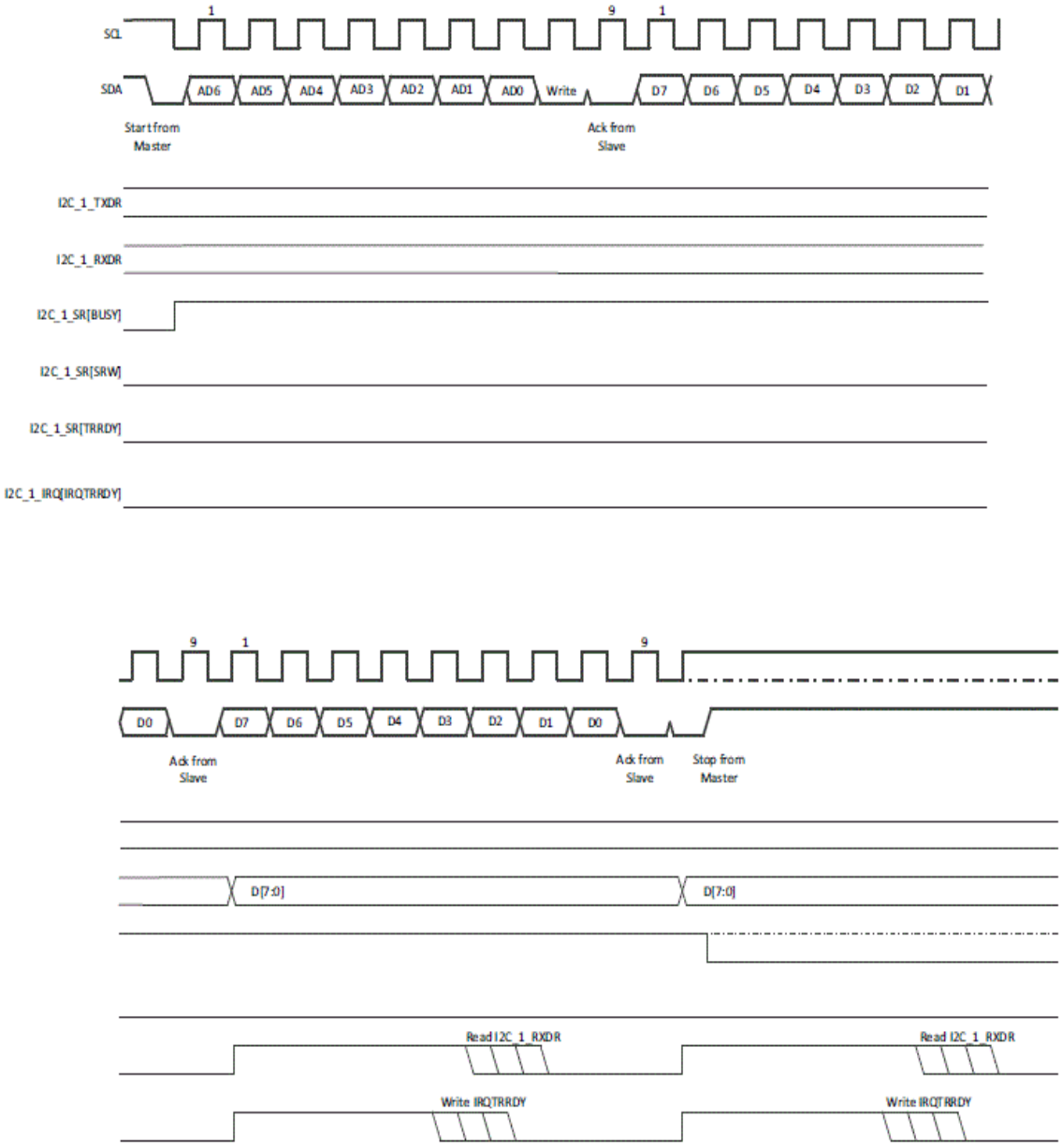


Figure 2.12. Slave I²C Write with Register Status

2.7.4. Slave I²C Read

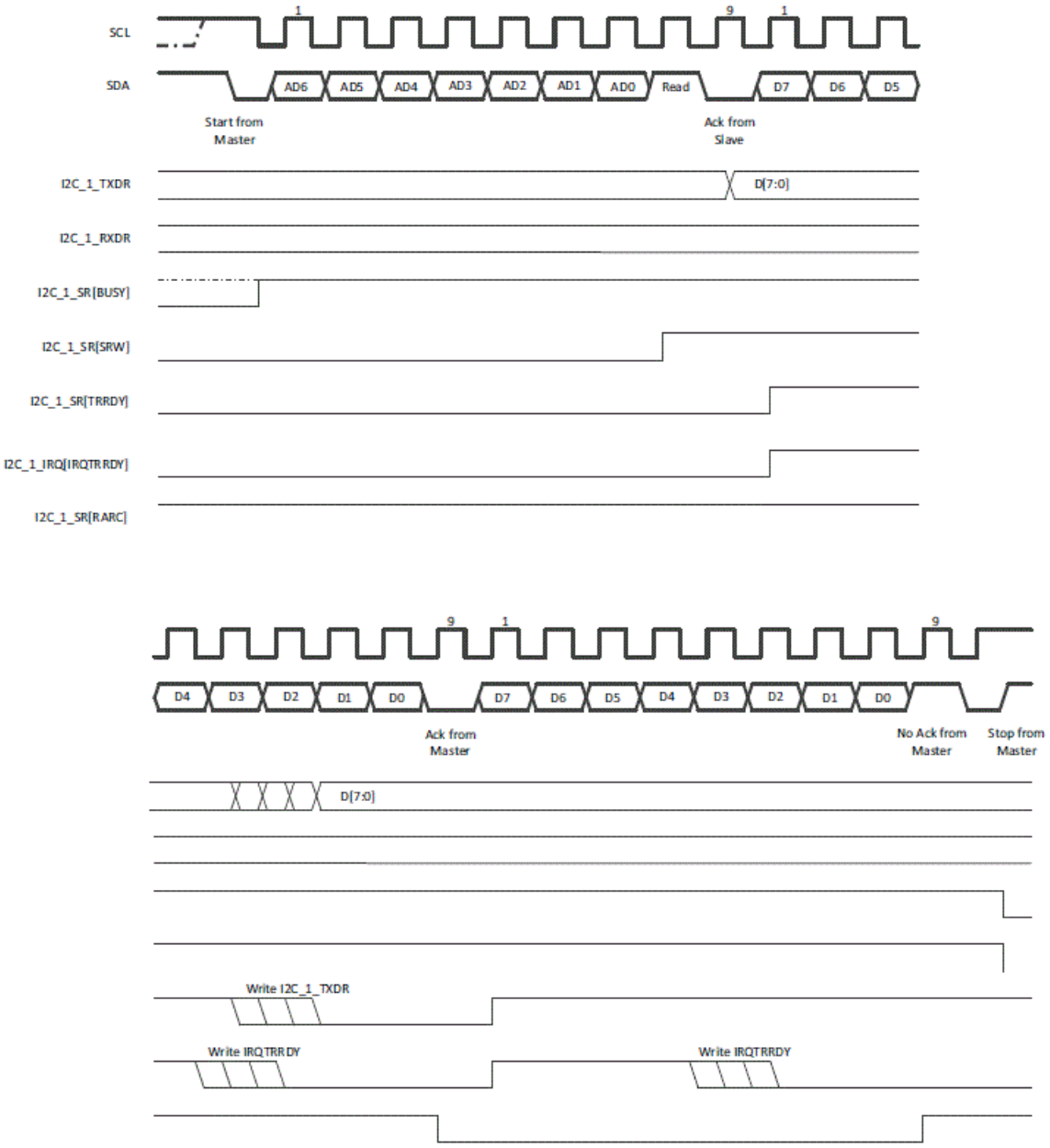


Figure 2.13. Slave I²C Read with Register Status

3. Generation, Simulation, and Validation

This chapter provides information on how to generate and synthesize the I2CFIFO Module using Lattice Radiant Software, as well as on how to run simulation. For more on Lattice Radiant software, refer to the Lattice Radiant Software 2.1 User Guide.

3.1. Licensing the IP

No license is required for this module.

3.2. Generating and Synthesizing the IP

Lattice Radiant Software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate the I2CFIFO Module in Lattice Radiant Software:

1. In the **Module/IP Block Wizard**, create a new Lattice Radiant Software project for the I2CFIFO Module.
2. In the dialog box of the **Module/IP Block Wizard** window, configure the I2CFIFO Module according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.2.

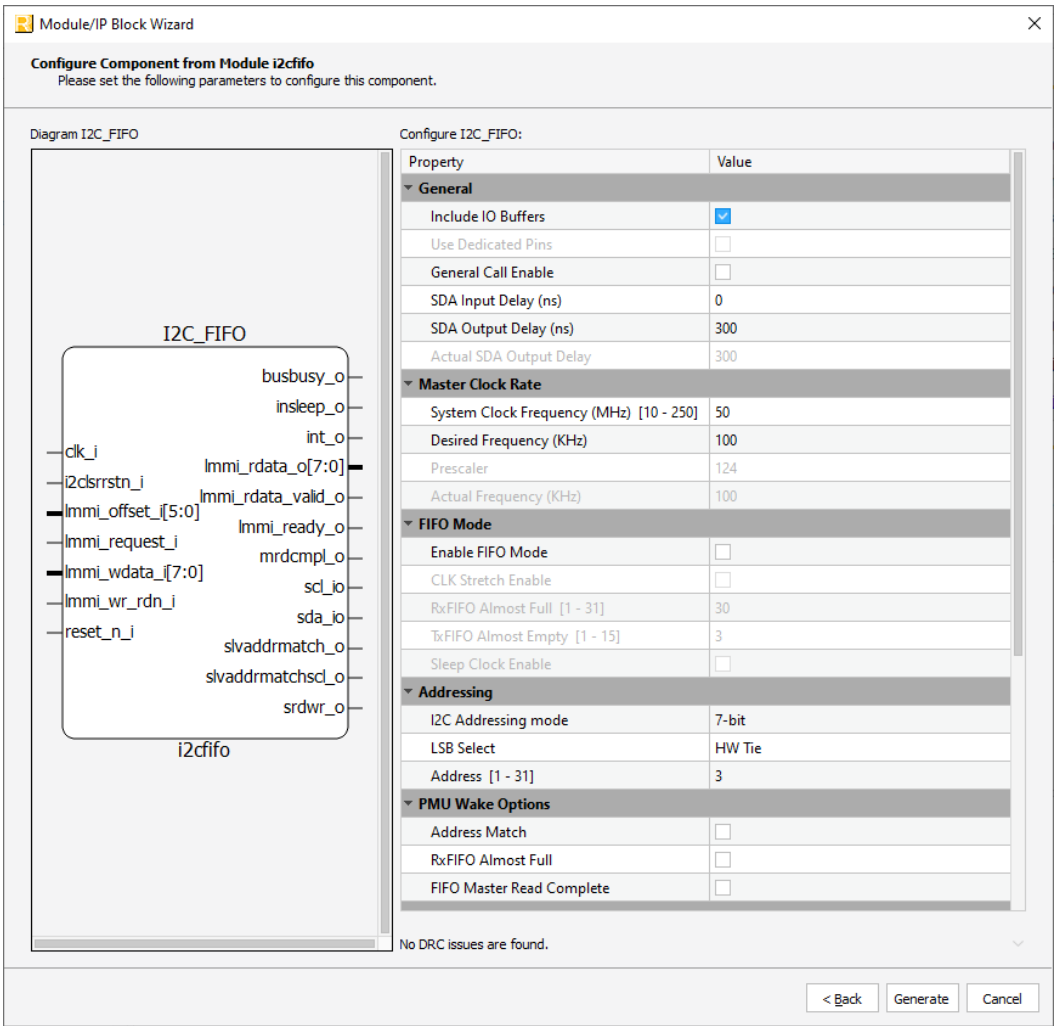


Figure 3.1. Configure Block of I2CFIFO Module

3. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.2.

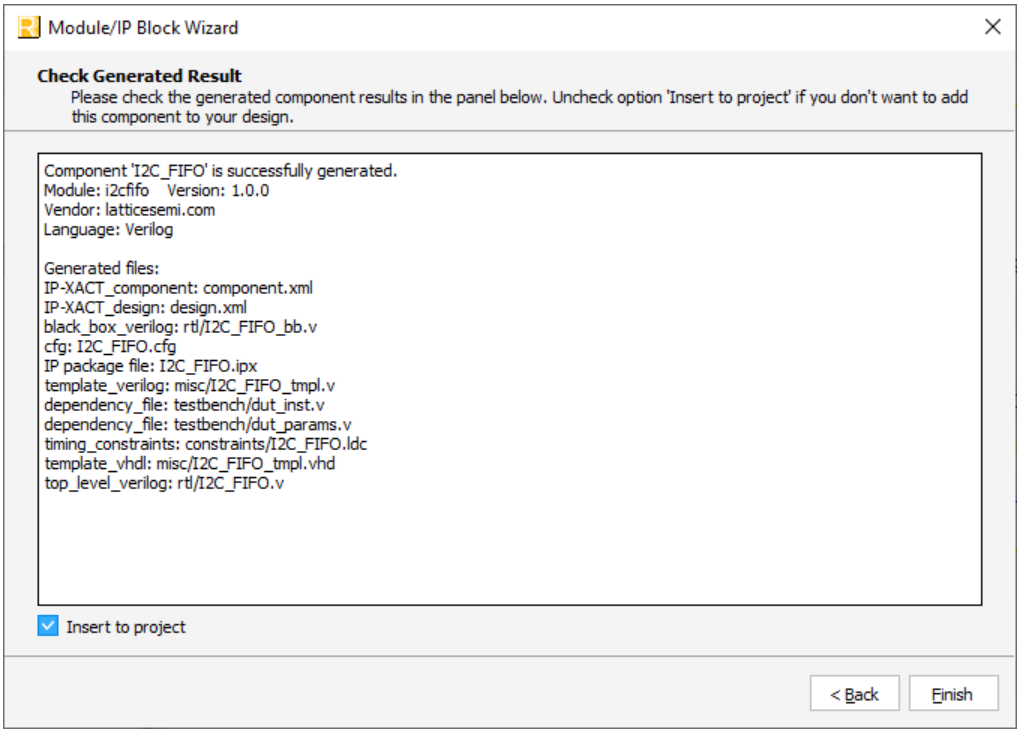


Figure 3.2. Check Generating Result

4. Click **Finish** to generate the Verilog file.
5. Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located on the top left corner of the screen, as shown in Figure 3.3.

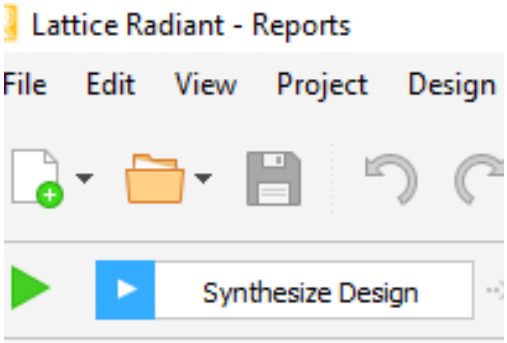


Figure 3.3. Synthesizing Design

3.3. Running the Functional Simulation

To run Verilog simulation:

1. Using the Lattice Radiant Software tcl console, go to the newly created *testbench* directory and run the command *source createDefines.tcl* to generate Verilog defines file.
2. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4

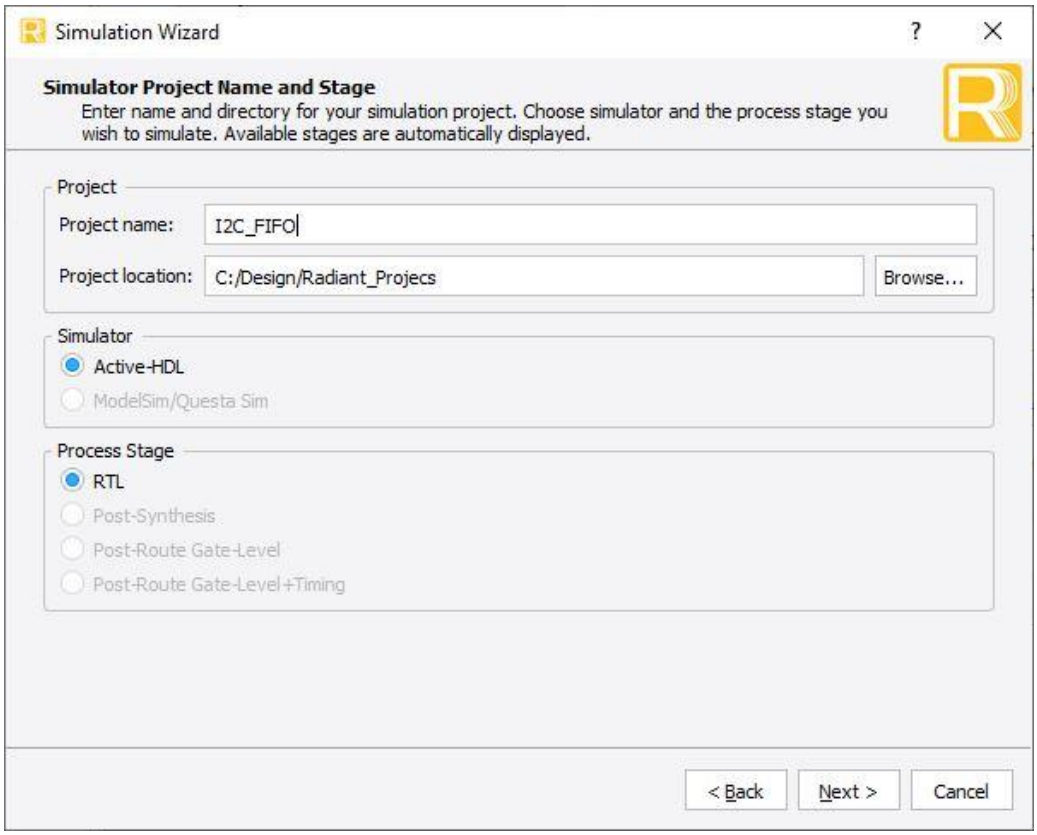


Figure 3.4. Simulation Wizard

3. Double-click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

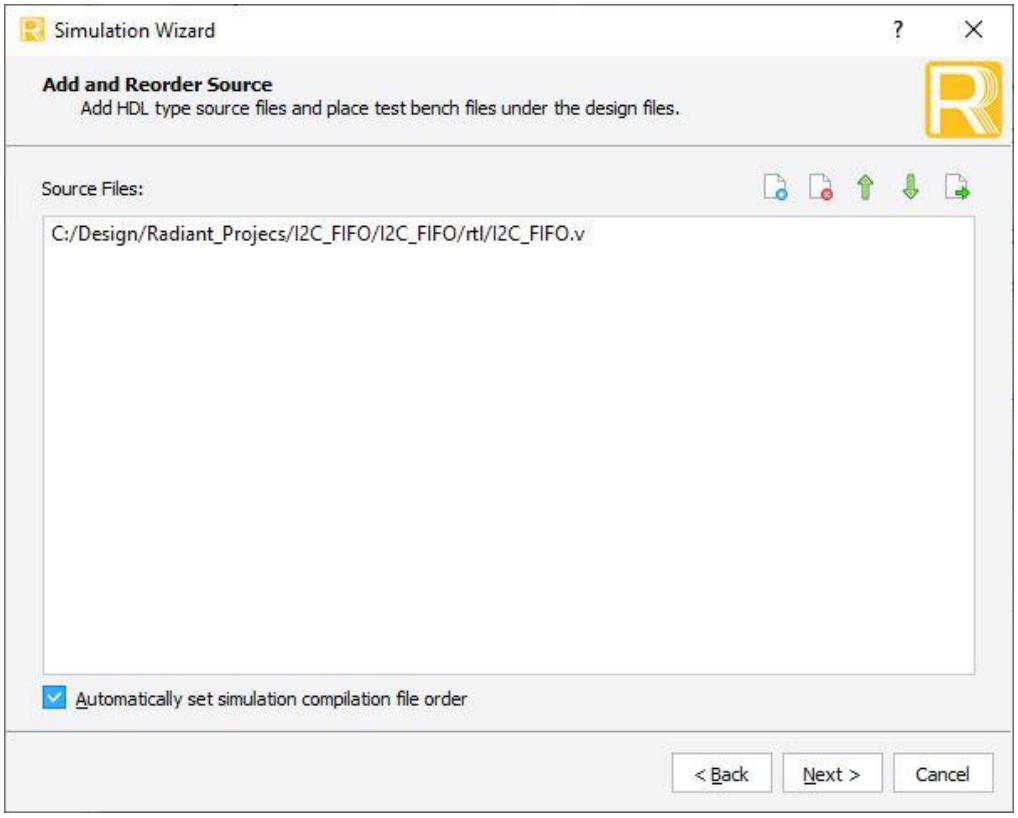


Figure 3.5. Adding and Reordering Source

4. Add *tb_top.v* file from *testbench* directory.
5. Click **Next** to run the simulation.

3.4. Hardware Evaluation

There is no restriction on the hardware evaluation for this module.

References

- Lattice Nexus Platform web page
- Lattice Radiant Software web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Document Revision 1.5, Lattice Radiant SW Version 2024.1, July 2024

Section	Change Summary
All	Updated the document title from *I2CFIFO Module - Lattice Radiant Software* to *I2CFIFO Module*.
Disclaimers	Updated boilerplate.
Functional Description	Added a note for *SDA_DEL_SEL* label in Table 2.4. I2CCR1 Register Details.
References	Updated this section.
Technical Support Assistance	Added *Lattice Answer Database* information.

Document Revision 1.4, Lattice Radiant SW Version 3.0, June 2021

Section	Change Summary
Introduction	• Replaced specific product names with Lattice FPGA devices built on the Lattice Nexus platform or Lattice Nexus devices. • Removed Quick Facts section.
References	Updated this section.

Document Revision 1.3, Lattice Radiant SW Version 2.0, June 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add Certus-NX as supported FPGA family and LFD2NX-40 as targeted device.
References	Updated this section.

Document Revision 1.2, Lattice Radiant SW Version 2.0, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.

Document Revision 1.1, Lattice Radiant SW Version 2.0, November 2019

Section	Change Summary
Acronyms in This Document	Added this section.
Introduction	Updated Table 1.1. Quick Facts.
Functional Description	• Updated Figure 2.1. I2CFIFO Top Level Block Diagram. • Improved description of I2C signals in Table 2.1. I2CFIFO Module Ports. • Updated General attribute group in Table 2.2. Attribute Summary.
References	Removed reference to the FPGA device web page and the JEDEC website.
All	Minor editorial changes

Document Revision 1.0, Lattice Radiant SW Version 2.0, October 2019

Section	Change Summary
All	Initial release

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