AHB-Lite to APB Bridge Module

IP Version: 1.2.0

User Guide

FPGA-IPUG-02053-1.4

December 2025

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CDC	Clock Domain Crossing
EBR	Embedded Block RAM
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
I/F	Interface
IP	Intellectual Property
LUT	Look-Up Table
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor AHB-Lite to APB Bridge Module provides an interface between the high-speed AHB-Lite and the low power APB. In many applications, the AHB-Lite system runs on a higher frequency clock with the APB system. This module has an optional clock crossing bridge, which can be enabled during IP configuration.

The design is implemented in Verilog HDL. The IP can be configured based on Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported Devices	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
MachXO2™	Lattice Propel™ Builder software	Lattice Diamond® software
MachXO3™	Lattice Propel Builder software	Lattice Diamond software
MachXO3D™	Lattice Propel Builder software	Lattice Diamond software
Mach™-NX	Lattice Propel Builder software	Lattice Diamond software
MachXO4™	Lattice Propel Builder software	Lattice Radiant™ software
MachXO5™-NX	Lattice Propel Builder software	Lattice Radiant software
CrossLink™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus-N2	Lattice Propel Builder software	Lattice Radiant software
CertusPro™-NX	Lattice Propel Builder software	Lattice Radiant software
Lattice Avant™	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the AHB-Lite to APB Bridge Module include:

- Compliance with AMBA 3 AHB-Lite Protocol v1.0 and AMBA 3 APB Protocol v1.0
- Data Bus width of up to 32 bits [8, 16, 32]
- Address width of up to 32-bits [11,12,...,32]
- Support of optional clock domain crossing bridge
- Registered output

1.2. Licensing the IP

The AHB-Lite to APB Bridge Module is provided at no additional cost with the Lattice Radiant software.

2. Functional Description

2.1. Overview

The Lattice Semiconductor AHB-Lite to APB Bridge Module is used for interfacing one AHB-Lite manager and one APB completer. When interfacing to multiple APB completers, this IP should be used together with an APB interconnect. The read and write transfers on the AHB-Lite are converted into equivalent transfers on the APB. In a single clock application, the bridge adds two wait states for both read and write access because of the output register in both the AHB-Lite side and the APB side. When the optional clock domain crossing bridge is enabled, the bridge is added in the APB side. The expected APB transfer size is the same as the write data bus width or the read data bus width (DATA_WIDTH).

2.2. Interface Description

Figure 2.1 shows the interface diagram of the AHB-Lite to APB Bridge Module. The diagram shows all the available ports for the IP core.

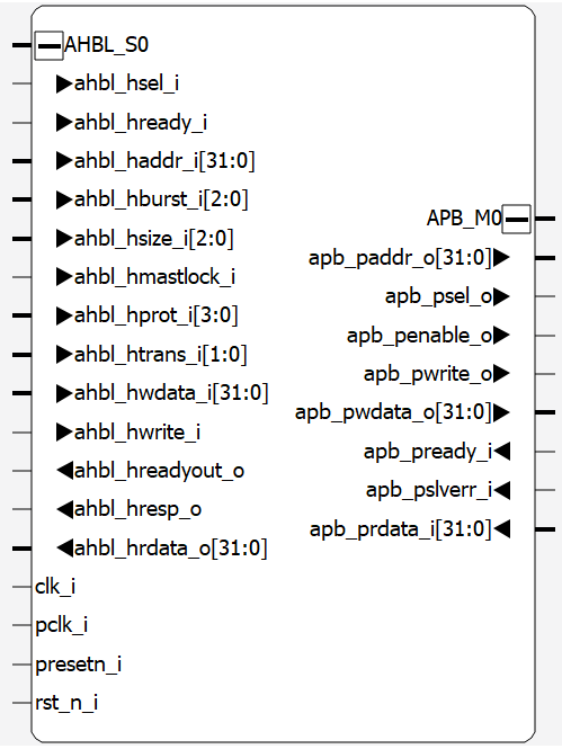

Figure 2.1. AHB-Lite to APB Bridge Module Interface Diagram

Table 2.1. AHB-Lite to APB Bridge Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
clk_i	In	1	Clock input for AHB-Lite I/F If the APB Clock Enable attribute is unchecked, this signal also clocks the APB I/F.
pclk_i	In	1	Clock input for APB I/F This is only present when the APB Clock Enable attribute is checked.
rst_n_i	In	1	Asynchronous active LOW reset input for AHB-Lite I/F Reset negation should be synchronous to clk_i. If the APB Clock Enable attribute is unchecked, this signal also resets APB I/F.
presetn_i	In	1	Asynchronous active LOW reset input for APB I/F Reset negation should be synchronous to pclk_i.
AHB-Lite Manager Interface (AHBL_S0)			
ahbl_hsel_slv_i	In	1	Subordinate select
ahbl_haddr_slv_i	In	*ADDR_WIDTH*	Adddress
ahbl_hburst_slv_i	In	3	Burst type (SINGLE, INCR, INCR4/8/16) This signal is unused; all transactions are treated as SINGLE.
ahbl_hsize_slv_i	In	3	Transfer size (8/16/32). The size of ahbl_hsize_slv_i should match the DATA_WIDTH size.
ahbl_hmastlock_slv_i	In	1	Current transfer is part of a locked transfer. This signal is unused.
ahbl_hprot_slv_i	In	4	Protection control This signal is unused.
ahbl_htrans_slv_i	In	2	Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ)
ahbl_hwdata_slv_i	In	*DATA_WIDTH*	Write data bus
ahbl_hwrite_slv_i	In	1	This indicates access direction: Write = 1, Read = 0.
ahbl_hready_slv_i	In	1	This indicates transfer completion.
ahbl_hready_slv_o	Out	1	This indicates transfer completion. This signal is driven low by the subordinate to extend the transfer.
ahbl_hresp_slv_o	Out	1	Subordinate response (OKAY/ERROR)
ahbl_hrdata_slv_o	Out	*DATA_WIDTH*	Read data bus
APB Completer Interface (APB_M0)			
apb_psel_o	Out	1	Select signal This indicates that the completer device is selected and that a data transfer is required.
apb_paddr_o	Out	*ADDR_WIDTH*	Address signal
apb_pwdata_o	Out	*DATA_WIDTH*	Write data signal
apb_pwrite_o	Out	1	Direction signal Write = 1, Read = 0
apb_penable_o	Out	1	Enable signal This indicates that the second and subsequent cycles of an APB transfer.
apb_pready_i	In	1	Ready signal This indicates transfer completion. The completer uses this signal to extend an APB transfer.

Pin Name	Direction	Width (Bits)	Description
apb_pslverr_i	In	1	Error signal This indicates a transfer failure. In case APB Completer does not have this signal, it should be tied to 1'b0.
apb_prdata_i	In	*DATA_WIDTH*	Read data signal

2.3. Attributes

Table 2.2 provides the list of user-configurable attributes for the AHB-Lite to APB Bridge Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.2.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Address Width(bits) (ADDR_WIDTH)	11–32	32	—
Data Bus Width(bits) (DATA_WIDTH)	8, 16, 32	32	—
APB Clock Enable	Checked, Unchecked	Unchecked	—

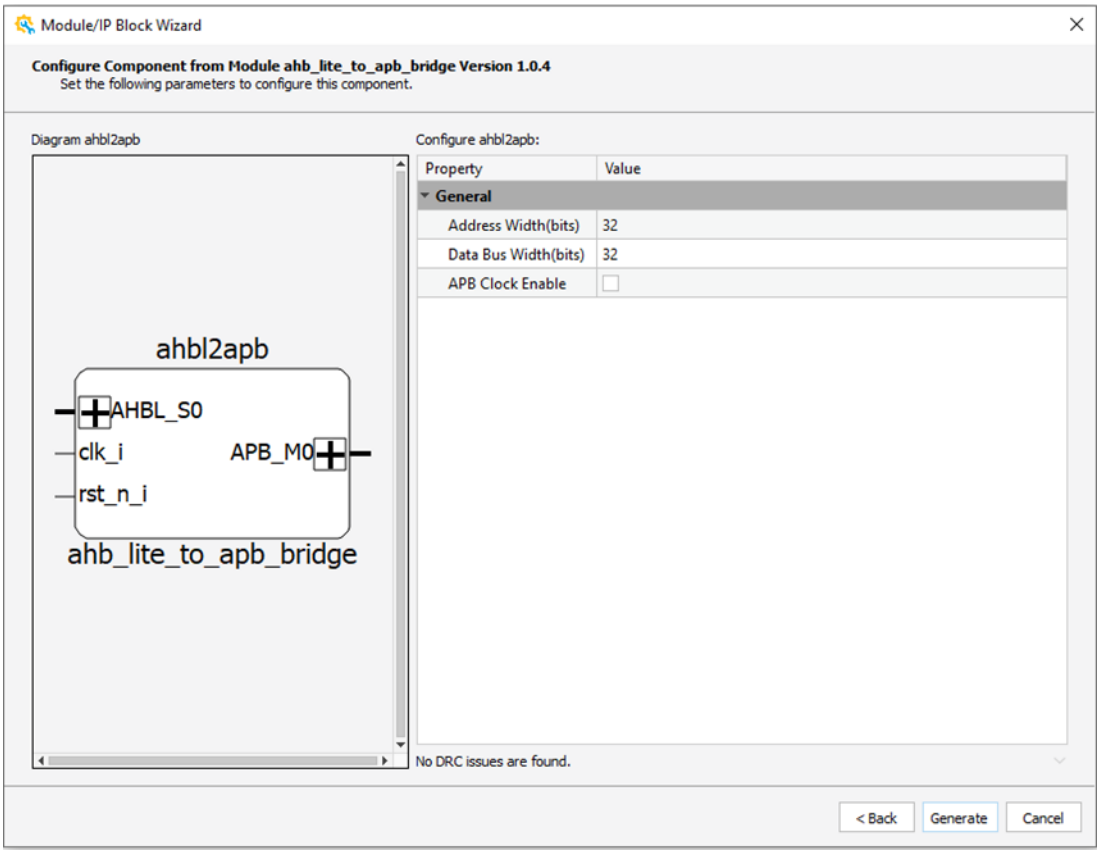

Figure 2.2. AHB-Lite to APB Bridge Module Configuration User Interface

Table 2.3. Attributes Description

Attribute	Description
Address Width(bits)	Specifies the bit width of address bus signals.
Data Bus Width(bits)	Specifies the bit with of ahbl_hwdata_slv_i and ahbl_hrdata_slv_o signals.
APB Clock Enable	Enables pclk_i and presetn_i signals as well as the clock domain crossing (CDC) logic generation. When enabled, the CDC logic is added in the APB side. Unchecked: pclk_i and presetn_i signals and CDC logic are generated Checked: pclk_i and presetn_i signals and CDC logic are generated

Appendix A. Resource Utilization

The following tables show the resource utilization of the AHB-Lite to APB Bridge Module for different Lattice FPGA devices using the Lattice Radiant software with Synplify Pro as the synthesis tool.

Table A.1. Resource Utilization Using the LAV-AT-X70ES-1LFG1156I Device

Target Device	Address Width (bit)	Data Bus Width (bit)	APB Clock Enable	Clock Fmax (MHz)	Registers	LUTs	EBRs
LAV-AT-X70ES-1LFG1156I	32	32	False	250	148	416	0
			True	250	269	496	0
LAV-AT-X70ES-1LFG1156I	22	32	False	250	128	416	0
			True	250	239	446	0
LAV-AT-X70ES-1LFG1156I	32	8	False	250	97	219	0
			True	250	164	268	0
LAV-AT-X70ES-1LFG1156I	11	8	False	250	55	171	0
			True	250	101	178	0
LAV-AT-X70ES-1LFG1156I	32	16	False	250	116	306	0
			True	250	205	336	0
LAV-AT-X70ES-1LFG1156I	22	16	False	250	96	256	0
			True	250	175	326	0

Table A.2. Resource Utilization Using the LFCPNX-100-8LFG672I Device

Target Device	Address Width (bit)	Data Bus Width (bit)	APB Clock Enable	Clock Fmax (MHz)	Registers	LUTs	EBRs
LFCPNX-100-8LFG672I	32	32	False	200	148	416	0
			True	200	269	446	0
LFCPNX-100-8LFG672I	22	32	False	200	128	413	0
			True	200	239	440	0
LFCPNX-100-8LFG672I	32	8	False	200	97	222	0
			True	200	164	258	0
LFCPNX-100-8LFG672I	11	8	False	200	55	157	0
			True	200	101	172	0
LFCPNX-100-8LFG672I	32	16	False	200	116	280	0
			True	200	205	309	0
LFCPNX-100-8LFG672I	22	16	False	200	96	271	0
			True	200	175	308	0

References

- AHB-Lite to APB Bridge Module Release Notes (FPGA-RN-02074)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- CrossLink-NX web page
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- Mach-NX web page
- MachXO2 web page
- MachXO3 web page
- MachXO3D web page
- MachXO4 web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Avant Platform web page
- AHB-Lite to APB Bridge Module web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.4, IP v1.2.0, December 2025

Section	Change Summary
All	• Renamed document from *AHB-Lite to APB Bridge Module - Lattice Propel Builder* to *AHB-Lite to APB Bridge Module*. • Added a note on IP version in the *Revision History* section.
Acronyms in This Document	Updated list of acronyms.
Introduction	• Added Certus-N2, MachXO4, and MachXO5-NX in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. • Added the Licensing the IP section.
Resource Utilization	Added this section.
References	Updated references.

Revision 1.3, November 2023

Section	Change Summary
All	Updated instances of *master/slave* to *manager/subordinate* for the AHB standard and *requestor/completer* for the APB standard.
Disclaimers	Updated this section.
Inclusive Language	Added this section.
Introduction	Added CertusPro-NX and Lattice Avant in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Functional Description	• Updated the description in section 2.1 Overview. • Updated the ahbl_hsize_slv_i pin transfer size and its description in Table 2.1.
Technical Support Assistance	Added link to the Lattice Answer Database.

Revision 1.2, May 2021

Section	Change Summary
Introduction	Updated Table 1.1 to add MachXO2 and MachXO3 as supported FPGA family.
References	Updated content to add reference for MachXO2 and MachXO3.

Revision 1.1, November 2020

Section	Change Summary
Introduction	Added Table 1.1.
Functional Description	Updated Figure 2.2.
References	Updated content to remove reference links for Lattice Propel and Lattice Diamond user guide; and to add reference links for Mach-NX, CrossLink-NX and Certus-NX web page.

Revision 1.0, May 2020

Section	Change Summary
All	Initial release

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