MachXO3D sysI/O User Guide

Technical Note

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASCII	American Standard Code for Information Interchange
BLVDS	Bus Low-Voltage Differential Signaling
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
HDL	Hardware Description Language
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVDS	Low Voltage Differential Signaling
LVPECL	Low-voltage positive/pseudo emitter–coupled logic
LVTTL	Low voltage TTL
MIPI	Mobile Industry Processor Interface
MLVDS	Multi-Point Low Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PIC	Programmable I/O Cell
PIO	Programmable Input/Output
PLD	Programmable Logic Device
VHDL	VHSIC Hardware Description Language

1. Introduction

The MachXO3D™ programmable logic device (PLD) family sysI/O™ buffers are designed to meet the needs of flexible I/O standards in today's fast-paced design world. The supported I/O standards range from single-ended I/O standards to differential I/O standards so that you can easily interface your designs to standard buses, memory devices, video applications and emerging standards. This technical note provides a description of the supported I/O standards and the banking scheme for the MachXO3D PLD family. The sysI/O architecture and the software usage are also discussed to provide a better understanding of the I/O functionality and placement rules.

2. sysI/O Buffer Overview

The basic building block of the MachXO3D sysI/O is the Programmable I/O Cell (PIC) block. There are three types of PIC blocks in the MachXO3D device architecture. These include the basic PIC block, the receiving PIC block with gearing, and the transmitting PIC block with gearing. The PIC blocks with gearing are used for video and high-speed applications. The PIC blocks with gearing have a built-in control module for word alignment. The details of the gearing PIC block can be found in Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065).

A common feature of all four types of PIC blocks is that each PIC block consists of four programmable I/O (PIOs). Each PIO includes a sysI/O buffer and an I/O logic block. A simplified sysI/O block diagram is shown in Figure 2.1. The I/O logic block consists of an input block, an output block, and a tri-state block. These blocks have registers, input delay cells, and the necessary control logic to support various operational modes. The sysI/O buffer determines the compliance to the supported I/O standards. It also supports features such as hysteresis to meet common design needs. The I/O logic block and the sysI/O buffer are designed with a minimal use of die area; providing easy bus interfacing, and pin out efficiency.

Two adjacent PIOs can form a pair of complementary output drivers. In addition, PIOA and PIOB of the PIC block form the primary pair of the buffer, while PIOC and PIOD form the alternate pair of the buffer. The primary pairs have additional capability that is not available on the alternate pair. The sysI/O buffers of the PIC block are equivalent when implemented as the single-ended I/O standards.

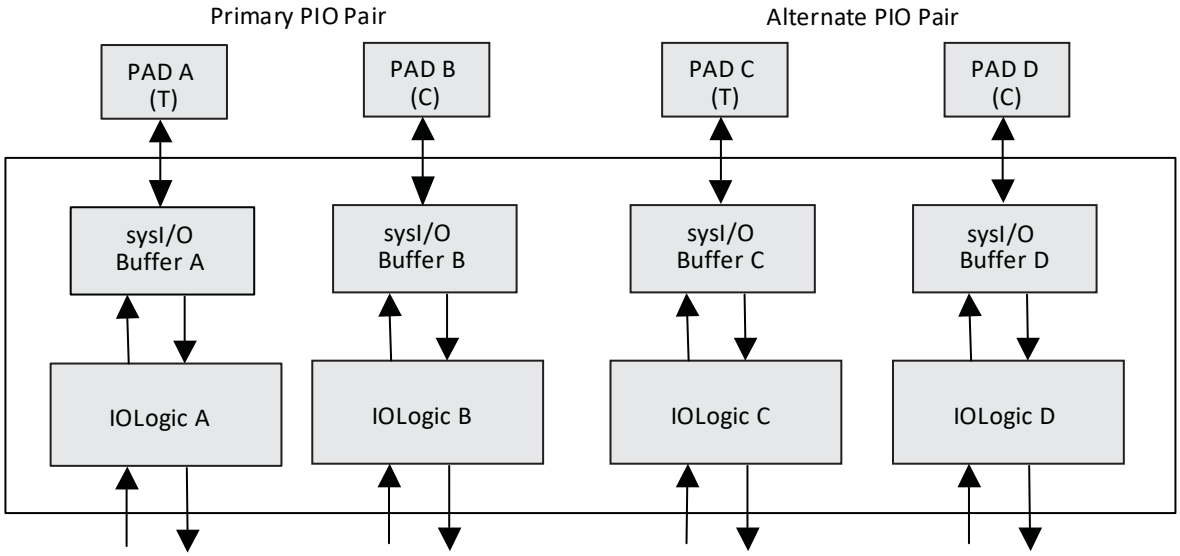


Figure 2.1. PIC Block Diagram

3. Supported sysI/O Standards

The MachXO3D sysI/O buffer supports both single-ended and differential standards. The internally ratioed standards support individually configurable drive strength and bus maintenance circuits, weak pull-up, weak pull-down, or bus keeper.

All banks of the MachXO3D devices support true differential inputs, and emulated differential outputs using external resistors and the complementary LVCMOS outputs. The true-LVDS differential outputs and LVDS input termination are supported in specific banks as described in the sysI/O Banking Scheme section of this document.

Table 3.1. Supported Input Standards

Input Standard	V_{REF} (Nominal)	V_{CCIO}[1] (Nominal)
Single Ended Interfaces		
LVTTL33	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	—
LVCMOS15	—	—
LVCMOS12	—	—
I3C33	—	—
I3C18	—	—
I3C12	—	—
Differential Interfaces		
LVDS25	—	—
LVPECL33	—	—
MLVDS25	—	—
BLVDS25	—	—
LVTTL33D	—	—
MIPI[2]	—	—

Notes:
1. If not specified, refer to mixed voltage support in Table 7.1.
2. This interface can be emulated with external resistors.

Table 3.2. Supported Output Standards

Output Standard	Drive (mA)	V_{CCIO} (Nominal)
Single-ended Interfaces		
LVTTL33	4, 8, 12, 16	3.3
LVCMOS33	4, 8, 12, 16	3.3
LVCMOS25	4, 8, 12	2.5
LVCMOS18	4, 8, 12	1.8
LVCMOS15	4, 8	1.5
LVCMOS12	2, 6	1.2
I3C33	4	3.3
I3C18	4	1.8
I3C12	2	1.2
Differential Interfaces		
LVDS25	3.5	2.5, 3.3
LVDS25E	8	2.5
LVPECL33E	16	3.3
MLVDS25E	16	2.5
BLVDS25E	16	2.5
LVTTL33 Differential	4, 8, 12, 16	3.3
LVCMOS33 Differential	4, 8, 12, 16	3.3
LVCMOS25 Differential	4, 8, 12	2.5
MIPI*	2	2.5

***Note**: This interface can be emulated with external resistors. Refer to MIPI D-PHY Interface IP (FPGA-RD-02040) for information on support for MIPI Input and Output.

4. sysI/O Banking Scheme

The MachXO3D devices have six I/O banks each, with one I/O bank on each of the top, bottom, and right sides, and three banks on the left side.

The MachXO3D devices support true LVDS differential outputs through the primary pairs on the top bank (Bank 0). These devices also support 100 Ω differential input termination on every I/O pair on the bottom I/O bank. In Bank 3, four I/O pairs can support I3C dynamic pull up capability.

The arrangements of the I/O banks are shown in Figure 4.1. Each of the I/O pins on all MachXO3D PLDs has a clamp feature which can be disabled or enabled. This clamp is similar to the PCI clamp, but it is not PCI compliant. When the CLAMP DIODE is ON, careful design considerations must be followed. For more information, refer to Appendix D.

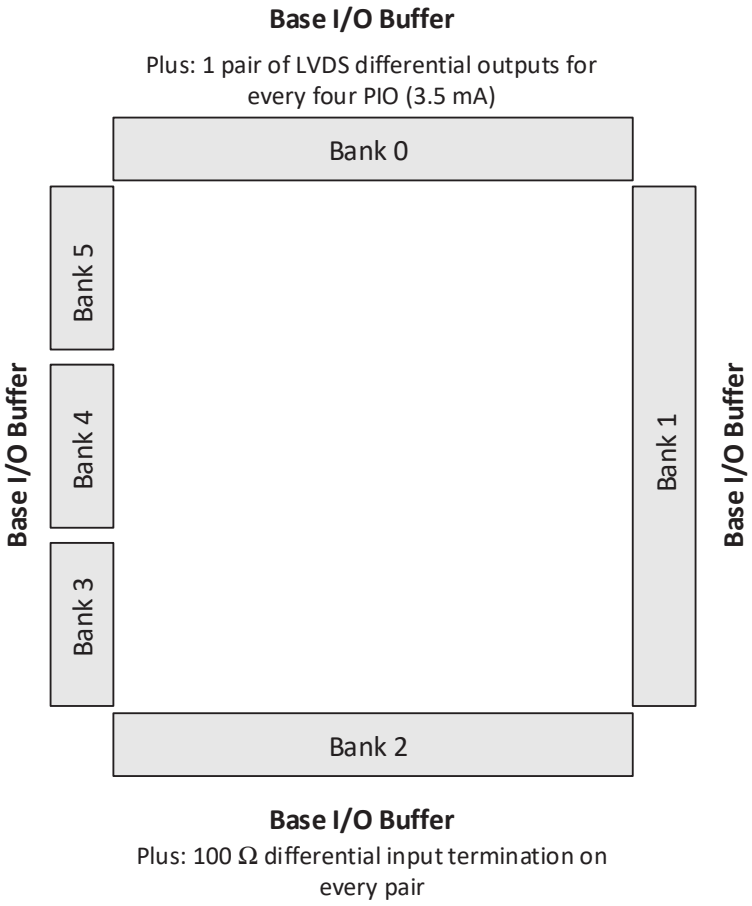


Figure 4.1. MachXO3D I/O Banking Arrangement

5. sysI/O Standards Supported by I/O Banks

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 5.1 and Table 5.2 summarize the I/O standards supported on various sides of the MachXO3D device.

Table 5.1. Single-Ended I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVTTL33	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes
I3C33	No	No	Yes (Bank 3 Only)	No
I3C18	No	No	Yes (Bank 3 Only)	No
I3C12	No	No	Yes (Bank 3 Only)	No

Table 5.2. Differential I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVDS output	Yes[1]	—	—	—
LVPECL33E[2]	Yes	Yes	Yes	Yes
MLVDS25E[2]	Yes	Yes	Yes	Yes
BLVDS25E[2]	Yes	Yes	Yes	Yes
LVDS25E[2]	Yes	Yes	Yes	Yes
LVTTL33D output	Yes	Yes	Yes	Yes
LVCMOS33D output	Yes	Yes	Yes	Yes
LVCMOS25D output	Yes	Yes	Yes	Yes
LVDS input	Yes	Yes	Yes	Yes
LVPECL33 input	Yes	Yes	Yes	Yes
MLVDS25 input	Yes	Yes	Yes	Yes
BLVDS25 input	Yes	Yes	Yes	Yes
LVTTL33D input	Yes	Yes	Yes	Yes
LVCMOS33D input	Yes	Yes	Yes	Yes
LVCMOS25D input	Yes	Yes	Yes	Yes
MIPI	Yes	Yes	Yes	Yes

Notes:
1. True LVDS output is supported at the top bank.
2. Emulated output standards are denoted with a trailing *E* in the name of the standard.

6. Power Supply Requirements

The MachXO3D device family has a simplified power supply scheme for sysI/O buffers. The core power V_{CC} and the bank power V_{CCIO} are the two main power supplies. A MachXO3D device can be powered and operated with a single power supply by connecting V_{CC} and V_{CCIO} to nominal voltages of 1.2 V. The JTAG programming pins are powered by V_{CCIO} in bank 0 where the JTAG pins reside. All the user sysI/O have a weak pull-down after power-up is complete and before the device configuration is done.

7. V_{CCIO} Requirement for I/O Standards

Each I/O bank of a MachXO3D device has a separate V_{CCIO} supply pin that can be connected to 1.2 V, 1.5 V, 1.8 V, 2.5 V or 3.3 V. This voltage is used to power the output I/O standard and source the drive strength for the output. In addition to this, V_{CCIO} also powers the ratioed input buffers such as LVTTL and LVCMOS. This ensures that the threshold of the input buffers is tracking the V_{CCIO} voltage level.

Input buffer set up to be a 1.2 V ratioed input can be used on bank set to any V_{CCIO}. This is possible because the MachXO3D sysI/O buffer has two ratioed input buffers connected to V_{CCIO} and V_{CC} in parallel.

Table 7.1. Mixed Voltage Support for LVCMOS and LVTTL I/O Types[8]

V_{CCIO}	Inputs						Outputs					
	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	—	Yes	Yes[6]	—	—	—	—	Yes	—	—	—	—
1.5 V	—	Yes[1]	Yes	Yes[6]	Yes[6]	Yes[6]	—	—	Yes	—	—	—
1.8 V	—	Yes[1]	Yes[5]	Yes	Yes[6]	Yes[6]	—	—	—	Yes	—	—
2.5 V	Yes[1, 9]	Yes[1, 10]	Yes[2, 5, 7]	Yes[3, 5, 7]	Yes	Yes[6]	Yes[11]	Yes[11]	—	—	Yes	—
3.3 V	Yes[1, 9]	Yes[1, 10]	Yes[2, 5, 7]	Yes[3, 5, 7]	Yes[4, 5, 7]	Yes	Yes[11]	Yes[11]	—	—	—	Yes

Notes:

1. Leakage occurs if bus hold or weak pull-up is turned on.
2. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS15R25 or LVCMOS15R33 with the referenced input buffer.
3. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS18R25 or LVCMOS18R33 with the referenced input buffer.
4. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS25R33 with the referenced input buffer.
5. Under-drive condition when using the ratioed input buffer and the input standard voltage is below V_{CCIO}
   a. Under-drive causes higher DC current when the I/O is at logic high. It is recommended to use Power Calculator to estimate the power consumption under such condition.
   b. Hysteresis is not supported. In the Diamond™ software, HYSTERESIS must be set to NA.
   c. CLAMP is not supported. In the Diamond software, CLAMP must be set to OFF.
   d. I/O termination is not supported. In the Diamond software, PULLMODE must be set to NONE.
6. Over-drive condition when using the ratioed input buffer and the input standard voltage is above V_{CCIO}.
   a. Hysteresis is not supported. In the Diamond software, HYSTERESIS must be set to NA.
   b. CLAMP is not supported. In the Diamond software, CLAMP must be set to OFF.
   c. I/O termination is not supported. In the Diamond software, PULLMODE must be set to NONE.
7. Ratioed input buffer in under-drive conditions is preferred over referenced input buffer due to lower power requirement for the ratioed input buffer.
8. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.
9. This input standard can be supported using the I/O types LVCMOS10R25 or LVCMOS10R33 with the referenced input buffer.
10. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS12R25 or LVCMOS12R33 with the referenced input buffer.
11. This output standard is supported as a Bidirectional open-drain buffer only. I/O termination is not supported. In the Diamond software, OPENDRAIN must be set to ON, PULLMODE must be set to NONE, and CLAMP must be set to OFF.

For differential input standards, certain mixed voltage support is allowed in the architecture as shown in Table 7.2.

Table 7.2. Mixed Voltage Support for Differential Input Standards

V_{CCIO}	Differential Inputs		
	LVDS LVPECL33 MLVDS25 BLVDS25	**LVTTL33D LVCMOS33D**	**LVCMOS25D**
1.2 V	—	—	—
1.5 V	—	—	—
1.8 V	—	—	—
2.5 V	Yes	—	Yes
3.3 V	Yes	Yes	Yes

8. Input Reference Voltage

To support mixed voltage I/O using the referenced input buffer, each I/O bank supports one reference voltage (VREF). Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as reference voltage input.

9. sysI/O Buffer Configuration

Each sysI/O buffer pair is made of two PIO buffers. PIO A and B pads form the primary pair, and PIO C and D pads form the alternate pair. Pads A and C of the pair are considered the true pad, while pads B and D are considered the comp pad. The true pad is associated with the positive side of the differential signal, while the comp pad is associated with the negative side of the differential signal.

All the PIO support bus maintenance circuitry to allow a weak pull-up, or a weak pulldown, or a weak bus keeper. The LVDS sysI/O buffer pairs have additional LVDS output drivers in the primary PIO and are available on the top side of the device. The bottom sysI/O buffer pairs have additional 100 Ω termination resistors between the *true* and *comp* pads.

9.1. LVCMOS Buffer Configurations

The LVCMOS buffers can be configured in a variety of modes to support common circuit design needs.

9.1.1. Bus Maintenance Circuit

Each pad has a weak pull-up, weak pull-down, and weak bus-keeper capability. These are selected with ON and OFF programmability. The pull-up and pull-down settings offer a fixed characteristic, which is useful in creating wired logic such as wired ORs. The bus-keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. Input leakage can be minimized by turning off the bus maintenance circuitry. However, it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer. The bus maintenance circuit is available for single-ended ratioed I/O standards.

9.1.2. Programmable Drive Strength

All single-ended drivers have programmable drive strength. This option can be set for each I/O independently. The drive strengths available for each I/O standard can be found in Table 10.2. The MachXO3D programmable drive architecture is guaranteed with minimum drive strength for each drive setting. The V/I curves in the data sheet provide details of output driving capability versus the output load. This information, together with the current per bank and the package thermal limit current, should be taken into consideration when selecting the drive strength.

9.1.3. Input Hysteresis

VIH is the trip point for a low-to-high transition and VIL is the trip point for a high-to-low transition, hysteresis voltage is the difference between VIH and VIL. Hysteresis is used to prevent several quick successive changes if the input signal contains some noise, for example. The noise could mean that you cross the trip point more than just once, which causes a glitch in the system.

All ratioed input receivers, except LVCMOS12, support input hysteresis. The input hysteresis for the LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15 have two settings for flexibility. The ratioed input receivers have no input hysteresis when they are operated in under-drive or over-drive input conditions as shown in Table 10.1.

9.1.4. Programmable Slew Rate

The single-ended output buffer for each device I/O pin has programmable output slew rate control that can be configured for either low noise (SLEWRATE=SLOW) or high speed (SLEWRATE=FAST) performance. Each I/O pin has an individual slew rate control. This slew rate control affects both the rising edge and the falling edges. The rise and fall ramp rates for each I/O standard can be found in the device IBIS file for a given I/O configuration.

9.1.5. Tri-state and Open Drain Control

Each single-ended output driver has a separate tri-state control in addition to the global tri-state control for the device. The single-ended output drivers also support open drain operation on each I/O independently. The open drain output is typically pulled up externally and only the sink current specification is maintained.

9.2. Differential Buffer Configurations

The sysI/O buffer pair supports differential input standards. The top and bottom edges support some additional functions over those supported by the base sysI/O buffer pairs.

9.2.1. Differential Receivers

All the sysI/O buffer pairs support differential input on all edges of the device. When a sysI/O buffer pair is configured as differential receiver, the input hysteresis and the bus maintenance capabilities are disabled for the buffer.

9.2.2. On-Chip Input Termination

The MachXO3D device supports on-chip 100 Ω (nominal) input differential termination on the bottom edge. The termination is available on all input PIO pairs of the bottom edge and is programmable.

9.2.3. Emulated Differential Outputs

All sysI/O buffer pairs support complementary outputs as described above. This feature can be used to drive complementary LVCMOS signals. It can also be used together with off-chip resistor networks for emulating the differential output standards such as LVPECL, MLVDS, MIPI, and BLVDS differential standards. When a sysI/O buffer pair is configured as differential transmitter, the bus maintenance and open drain capabilities are disabled. All single-ended sysI/O buffers pairs in the MachXO3D family can support emulated differential output standards.

9.3. True Differential Output and Output Drive

MachXO3D devices support true differential output drivers on the top edge of these devices. These true differential outputs are only available on the primary PIO pairs. The output driver has a fixed common mode of 1.2 V and a programmable drive current of 3.5 mA. The bank VCCIO for true differential output can be 2.5 V or 3.3 V.

9.4. I3C I/O Support

MachXO3D devices support the dynamic pull up capability to meet I3C spec. The target speed is 400 kHz, the maximum is 1 MHz for I2C, and the maximum is 12.5 MHz for I3C. Only four pairs in Bank 3 can support this feature.

10. Software sysI/O Attributes

The sysI/O attributes or primitives must be used in the Lattice development software to control the functions and capabilities of the sysI/O buffers. sysI/O attributes or primitives can be specified in the HDL source code, in the Lattice Diamond Spreadsheet View interface, or in the ASCII preference file (.lpf) file directly. Appendix A, Appendix B, and Appendix C list examples of using such attributes in different environments. This section describes each of these attributes in detail.

10.1.HDL Attributes

All the attributes discussed in this section, except two, can be used in the HDL source code to direct the sysI/O buffer functionality.

10.1.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The VCCIO required to set these I/O standards are embedded in the attribute names. The BANK VCCIO attribute is used to specify allowed VCCIO combinations for each I/O type. Table 10.1 shows the valid I/O types for the MachXO3D family.

Table 10.1. Supported I/O Types

sysI/O Signaling Standard	IO_TYPE
LVDS 2.5 V	LVDS25
Emulated LVDS 2.5 V[1]	LVDS25E
Bus LVDS 2.5 V	BLVDS25
Emulated Bus LVDS 2.5 V[1]	BLVDS25E
MLVDS 2.5 V	MLVDS25
Emulated MLVDS 2.5 V[1]	MLVDS25E
LVPECL 3.3 V	LVPECL33
Emulated LVPECL 3.3 V[1]	LVPECL33E
LVTTL 3.3 V	LVTTL33
LVTTL 3.3 V differential[2]	LVTTL33D
LVCMOS 3.3 V	LVCMOS33
LVCMOS 3.3 V differential[2]	LVCMOS33D
LVCMOS 2.5 V (default)	LVCMOS25
LVCMOS 2.5 V differential[2]	LVCMOS25D
LVCMOS 2.5 V in 3.3 V VCCIO bank[3]	LVCMOS25R33
LVCMOS 1.8 V	LVCMOS18
LVCMOS 1.8 V in 3.3 V VCCIO bank[3]	LVCMOS18R33
LVCMOS 1.8 V in 2.5 V VCCIO bank[3]	LVCMOS18R25
LVCMOS 1.5 V	LVCMOS15
LVCMOS 1.5 V in 3.3 V VCCIO bank[3]	LVCMOS15R33
LVTTL 3.3 V	LVTTL33
LVCMOS 1.5 V in 2.5 V VCCIO bank[3]	LVCMOS15R25
LVCMOS 1.2 V	LVCMOS12
LVCMOS 1.2 V in 3.3 V VCCIO bank[4]	LVCMOS12R33
LVCMOS 1.2 V in 2.5 V VCCIO bank[4]	LVCMOS12R25
LVCMOS 1.0 V in 3.3 V VCCIO bank[4]	LVCMOS10R33
LVCMOS 1.0 V in 2.5 V VCCIO bank[4]	LVCMOS10R25
MIPI	MIPI
I3C with 3.3V VCCIO	I3C33

sysI/O Signaling Standard	IO_TYPE
I3C with 1.8V VCCIO	I3C18
I3C with 1.2V VCCIO	I3C12

Notes:
1. These differential output standards are emulated by using a complementary LVCMOS driver pair together with an external resistor pack.
2. These differential standards are implemented by using a complementary LVCMOS driver pair.
3. These are input only and require VREF to be set to certain value to allow the specified I/O types to be used.
4. These are input or bidirectional only and require VREF to be set to certain value to allow the specified I/O types to be used.

10.1.2. DRIVE

The DRIVE strength attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used. Table 10.2 shows the supported drive strength for the single-ended I/O types under designated I/O standards.

Table 10.2. Output Drive Capability for Ratioed sysI/O Standards

Drive Strength (mA)	I/O Type								
	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33	I3C33	I3C18	I3C12	LVTTL33
2	YES	—	—	—	—	—	—	YES	—
4	—	YES	YES	YES	YES	YES	YES	—	YES
6	YES	—	—	—	—	—	—	—	—
8	—	YES	YES	YES	YES	—	—	—	YES
12	—	—	YES	YES	YES	—	—	—	YES
16	—	—	—	—	YES	—	—	—	YES

10.1.3. DIFFDRIVE

The DIFFDRIVE strength attribute is available for the true LVDS output standard. All true LVDS differential drivers on the top edge is set to 3.5 mA setting. This is not programmable on the MachXO3D device.

- Values: 3.5
- Default: 3.5

10.1.4. PULLMODE

The PULLMODE option can be enabled or disabled independently for each I/O. When you select OPENDRAIN=ON, the PULLMODE for the output standard is default to NONE. When you select the I/O type as I3C, the PULLMODE for the output standard is forced to be I3C for the dynamic control capability.

- Values: UP, DOWN, NONE, KEEPER, I3C
- Default: DOWN for LVTTL, and LVCMOS, I3C for I3C33/I3C18/I3C12; all others NONE

10.1.5. CLAMP

The CLAMP option can be enabled or disabled independently for each I/O. The settings are available on the bottom edge. All other I/O have ON or OFF settings for this attribute.

- Values: OFF, ON
  - Default value of the CLAMP for output: OFF
  - Default value of the CLAMP for input: ON if V_{CCIO} is the same or higher than the I/O standard.
  - Default value of the CLAMP for input: OFF if V_{CCIO} is less than the I/O standard.

When the CLAMP DIODE is ON, careful design considerations must be followed. For more information, see Appendix D.

10.1.6. HYSTERESIS

The ratioed input buffers have two input hysteresis settings. The HYSTERESIS option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards, except for the LVCMOS12 inputs. The LVCMOS12 inputs do not support HYSTERESIS.

The LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, and LVCMOS10R25 input types do not support HYSTERESIS. The HYSTERESIS option for each of the input pins can be set independently when it is supported for the I/O type.

- Values: SMALL, LARGE, NA
- Default: SMALL

10.1.7. VREF

The VREF option is enabled for referenced LVCMOS input buffers. The referenced LVCMOS input buffers are specified by choosing the I/O type as LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25. The default value of NA applies for all I/O types that do not use a VREF signal.

The VREF defaults to external VREF pin for the single-ended LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25 inputs. You may enter a VREF_NAME value in the “VREF Location(s)” pop-up window of the Spreadsheet View of the Diamond software. In doing so, the software presents the VREF_NAME as an available value in the VREF column of the Port Assignments tab of the Diamond Spreadsheet View. A pin location specified by the VREF_NAME value is used as the VREF driver for that I/O bank. VREF_NAME is only necessary if you want to specify a pin to be used as an external VREF pin. Otherwise, the software automatically assigns a pin for the VREF signal.

There is only one VREF pin needed per I/O bank and only one VREF driver can be used in each I/O bank. This attribute can be set in the software interface or in the ASCII preference file.

- Values: OFF, VREF_NAME
- Software Default: NA
- Hardware Default (Erased): OFF

10.1.8. OPENDRAIN

The OPENDRAIN option is available for all LVTTL and LVCMOS output and bidirectional I/O standards. Each sysI/O can be assigned independently to be open drain, except I3C I/O type. When the OPENDRAIN attribute is used, the PULLMODE must be NONE and the CLAMP must be OFF.

- Values: OFF, ON
- Default: OFF

10.1.9. SLEWRATE

Each I/O pin has an individual slew rate control. This allows the designer to specify slew rate control on a pin-by-pin basis for outputs and bidirectional I/O pins. This is not a valid attribute for inputs or true differential outputs.

- Values: FAST, SLOW, NA
- Default: FAST

10.1.10. DIFFRESISTOR

The bottom side I/O pins support on-chip differential input termination resistors. The termination resistor is available for both the primary pair and the alternate pair of a sysI/O. The values supported are zero (OFF) or 100 Ω.

- Values: OFF, 100
- Default: OFF

10.1.11. DIN/DOUT

The DIN/DOUT option is available for each I/O and can be configured independently. An input register is used for the input if the DIN attribute is assigned. Similarly, the software assigns an output register when the DOUT attribute is specified. By default, the software automatically assigns DIN or DOUT to input or output registers if possible.

10.1.12. LOC

This attribute specifies the site location for the component after the mapping process. When attached to multiple components, it indicates that these blocks are to be mapped together in the specified site. It specifies the PIC site for the pad when it is assigned to a pad. The LOC attribute can be attached to components that end up on an I/O cell, clocks, and internal flip-flops, but it should not be attached to combinational logic that end up on a logic cell. Doing so could cause failure in generating a locate preference. The LOC attribute overrides register ordering.

10.1.13. Bank VCCIO

This attribute is necessary to verify the valid I/O types for a bank, to determine which input buffer to use, and to set the correct drive strength for the applicable I/O types. Since the I/O bank information is not required at the HDL level, this attribute is available through either the Diamond software's Spreadsheet View or in the ASCII preference file.

- Values: AUTO, 3.3, 2.5, 1.8, 1.5, 1.2
- Default: AUTO

10.2.sysI/O Primitives

There are many sysI/O primitives in the software library. A few are selected to be discussed in this section because some sysI/O capabilities can only be utilized through instantiating the primitives in the HDL source code.

10.2.1. Tri-State All (TSALL)

The MachXO3D device supports the TSALL function that is used to enable or disable the tri-state control to all the output buffers. You can choose to assign any general purpose I/O pin to control the TSALL function since there is no dedicated TSALL pin. The TSALL primitive must be instantiated in the source code in order to enable the TSALL function. The input of the primitive can be assigned to an input pin or to an internal signal.

A value of TSALL=1 tri-states all outputs but the outputs are under individual OE control when TSALL=0.

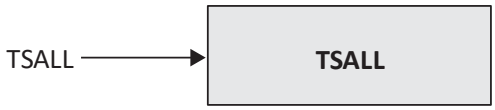


Figure 10.1. TSALL Primitive

10.2.2. Fixed Data Delay (DELAYE)

This primitive supports up to 32 steps of static delay for all sysI/O buffers in all banks of a MachXO3D device. Although you can choose USER_DEFINED mode to set input delay, this primitive is primarily used by pre-defined source synchronous interfaces as described in Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065).

Figure 10.2. DELAYE Primitive and Associated Attributes

Table 10.3. Output Drive Capability for Ratioed sysI/O Standards

Attribute	Description	Value	Software Default
DEL_MODE	Fixed delay value depending on interface or user-defined delay values	SCLK_ZEROHOLD ECLK_ALIGNED ECLK_CENTERED SCLK_ALIGNED SCLK_CENTERED USER_DEFINED	USER_DEFINED
DEL_VALUE	User-defined value	DELAY0…DELAY31	DELAY0

10.2.3. Dynamic Data Delay (DELAYD)

This primitive supports dynamic delay for the sysI/O buffers in the bottom bank (Bank 2) of the MachXO3D device only. The 5-bit inputs can be controlled by user logic to modify the delay during the device operation.

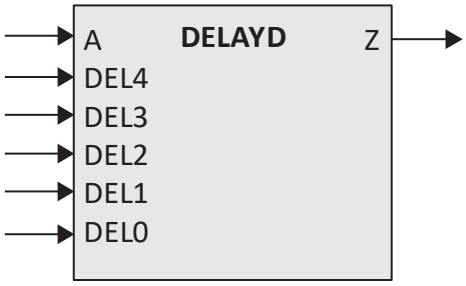


Figure 10.3. DELAYD Primitive

11. Design Consideration and Usage

This section summarizes the MachXO3D designs rules and considerations that have been discussed in detail in previous sections. Table 11.1 lists the miscellaneous I/O features on each side of a MachXO3D device.

11.1.sysI/O Buffer Features Common to All MachXO3D Devices

- All banks support true differential inputs.
- All banks support emulated differential outputs using external resistors and complementary LVCMOS outputs. Emulated differential output buffers are supported on both primary and alternate pairs.
- All banks have programmable I/O clamps.
- All banks support weak pull-up, pull-down, and bus-keeper (bus hold latch) settings on each I/O independently.
- V_{CCIO} voltage levels, together with the selected I/O types, determine the characteristics of an I/O, such as the pull mode, hysteresis, clamp behavior, and drive strength, supported in a bank. Each bank can support 1.2 V inputs regardless of the V_{CCIO} setting of the bank.
- Each bank supports one V_{CCIO} signal.

11.2.sysI/O Buffer Rules

- Only Bank 0 (top side) supports true differential output buffers with programmable drive strengths. Only the primary pair supports true differential output buffers.
- Only Bank 2 (bottom side) supports internal 100 Ω differential input terminations.
- Only four pairs of I/O in Bank 3 can support I3C dynamic pull up capability.

Table 11.1. Miscellaneous I/O Features on Each Device Edge

Feature	Top	Bottom	Left	Right
100 Ω Differential Resister	—	Yes	—	—
Hot Socket	Yes	Yes	Yes	Yes
Clamp[2]	Yes	Yes	Yes	Yes
Weak Pull-up[2]	Yes	Yes	Yes	Yes
Weak Pull-down[1]	Yes	Yes	Yes	Yes
Bus Keeper[2]	Yes	Yes	Yes	Yes
Input Hysteresis[2]	Yes	Yes	Yes	Yes
Slew Rate Control	Yes	Yes	Yes	Yes
Open Drain	Yes	Yes	Yes	Yes
Dynamic pull up control	—	—	Yes (Bank 3 only)	—

Notes:

1. Software default setting
2. I/O characteristic under special conditions:
   a. HYSTERESIS option is not available for LVCMOS12.
   b. HYSTERESIS option and BUS KEEPER option are not available for referenced input standards.
   c. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.
   d. HYSTERESIS and the bus maintenance capabilities are disabled for differential receivers.

Appendix A. sysI/O HDL Attributes

The sysI/O attributes can be used directly in the HDL source codes. This section provides a list of sysI/O attributes supported by the MachXO3D PLD family. The correct syntax and examples for the Synplify® synthesis tool is provided here for reference.

A.1. Attributes in VHDL Language

This section lists syntax and examples for the sysI/O attributes in VHDL.

Syntax

Table A.1. VHDL Attribute Syntax

Attribute	Syntax
IO_TYPE	attribute IO_TYPE: string; attribute IO_TYPE of *Pinname*: signal is *"IO_TYPE Value";*
DRIVE	attribute DRIVE: string; attribute DRIVE of *Pinname:* signal is *"Drive Value";*
DIFFDRIVE	attribute DIFFDRIVE: string; attribute DIFFDRIVE of *Pinname:* signal is *"Diffdrive Value";*
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of *Pinname:* signal is *"Diffresistor Value";*
CLAMP	attribute CLAMP: string; attribute CLAMP of *Pinname:* signal is *"Clamp Value";*
HYSTERESIS	attribute HYSTERESIS: string; attribute HYSTERESIS of *Pinname:* signal is *"Hysteresis Value";*
VREF	NA
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of *Pinname:* signal is *"Pullmode Value";*
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of *Pinname:* signal is *"OpenDrain Value";*
SLOWSLEW	attribute SLOWSLEW: string; attribute SLOWSLEW of *Pinname:* signal is *"Slewrate Value";*
DIN	attribute DIN: string; attribute DIN of *Pinname*: signal is " ";*
DOUT	attribute DOUT: string; attribute DOUT of *Pinname:* signal is " ";*
LOC	attribute LOC: string; attribute LOC of *Pinname:* signal is "pin_locations";
BANK VCCIO	NA

Examples

IO_TYPE

```
--***Attribute Declaration*** ATTRIBUTE IO_TYPE: string;
--***IO_TYPE assignment for I/O Pin***
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portD: SIGNAL IS "LVDS25";
```

DRIVE

```
--***Attribute Declaration***
ATTRIBUTE DRIVE: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE DRIVE OF portB: SIGNAL IS “8”;
```

DIFFDRIVE

```
--***Attribute Declaration***
ATTRIBUTE DIFFDRIVE: string;
--*** DIFFDRIVE assignment for I/O Pin***
ATTRIBUTE DIFFDRIVE OF portD: SIGNAL IS “2.0”;
```

DIFFRESISTOR

```
--***Attribute Declaration***
ATTRIBUTE DIFFRESISTOR: string;
--*** DIFFRESISTOR assignment for I/O Pin***
ATTRIBUTE DIFFRESISTOR OF portD: SIGNAL IS "100";
```

CLAMP

```
--***Attribute Declaration***
ATTRIBUTE CLAMP: string;
--*** CLAMP assignment for I/O Pin***
ATTRIBUTE CLAMP OF portA: SIGNAL IS “PCI33”;
```

HYSTERESIS

```
--***Attribute Declaration***
ATTRIBUTE HYSTERESIS: string;
--*** HYSTERESIS assignment for Input Pin***
ATTRIBUTE HYSTERESIS OF portA: SIGNAL IS " LARGE ";
```

PULLMODE

```
--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS “DOWN”;
ATTRIBUTE PULLMODE OF portB: SIGNAL IS “UP”;
```

OPENDRAIN

```
--***Attribute Declaration***
ATTRIBUTE OPENDRAIN: string;
--***Open Drain assignment for I/O Pin***
ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS “ON”;
```

SLEWRATE

```
--***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--*** SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS “FAST”;
```

DIN/DOUT

```
--***Attribute Declaration***
ATTRIBUTE din : string; ATTRIBUTE dout : string;
--*** din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS “TRUE “;
ATTRIBUTE dout OF output_vector: SIGNAL IS “TRUE “;
```

LOC

```
--***Attribute Declaration***
ATTRIBUTE LOC : string;
--*** LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS “E3,B3,C3 “;
```

A.2. Attribute in Verilog Language

This section lists syntax and examples for the sysI/O Attributes in Verilog.

Syntax

Table A.2. Verilog Attribute Syntax

Attribute	Syntax
IO_TYPE	PinType PinName /* synthesis IO_Type=”IO_Type Value”*/;
DRIVE	PinType PinName /* synthesis DRIVE=”Drive Value”*/;
DIFFDRIVE	PinType PinName /* synthesis DIFFDRIVE =” DIFFDRIVE Value”*/;
DIFFRESISTOR	PinType PinName /* synthesis DIFFRESISTOR =” DIFFRESISTOR Value”*/;
CLAMP	PinType PinName /* synthesis CLAMP =” Clamp Value”*/;
HYSTERESIS	PinType PinName /*synthesis HYSTERESIS = “Hysteresis Value” */;
VREF	N/A
PULLMODE	PinType PinName /* synthesis PULLMODE=”Pullmode Value”*/;
OPENDRAIN	PinType PinName /* synthesis OPENDRAIN =”OpenDrain Value”*/;
SLOWSLEW	PinType PinName /* synthesis SLEWRATE=”Slewrate Value”*/;
DIN	PinType PinName /* synthesis DIN= “value” */;
DOUT	PinType PinName /* synthesis DOUT= “value” */;
LOC	PinType PinName /* synthesis LOC=”pin_locations “*/;
Bank VCCIO	N/A

Examples

//IO_TYPE, PULLMODE, SLEWRATE and DRIVE assignment

```
output portB /*synthesis IO_TYPE=”LVCMOS33”
PULLMODE =”UP” SLEWRATE =”FAST” DRIVE =”20”*/;
output portC /*synthesis IO_TYPE=”LVDS25” */;
```

//DIFFDRIVE

```
output portD /* synthesis IO_TYPE="LVDS25" DIFFDRIVE="2.0"*/;
```

//DIFFRESISTOR

```
output [4:0] portA /* synthesis IO_TYPE="LVDS25" DIFFRESISTOR ="100"*/;
```

//CLAMP

```
output portA /*synthesis IO_TYPE=”LVCMOS33” CLAMP =”ON” */;
```

//HYSTERESIS

```
input mypin /* synthesis HYSTERESIS = “LARGE” */;
```

//OPENDRAIN

```
output portA /*synthesis OPENDRAIN =”ON”*/;
```

// DIN Place the flip-flops near the load input

```
input load /* synthesis din=”” TRUE */;
```

// DOUT Place the flip-flops near the outload output

```
output outload /* synthesis dout=”TRUE” */;
```

//LOC pin location

```
input [2:0] DATA0 /* synthesis loc=”E3,B1,F3”*/;
```

//LOC Register pin location

```
reg data_in_ch1_buf_reg3 /* synthesis loc=”R10C16” */;
```

//LOC Vectored internal bus

```
reg [3:0] data_in_ch1_reg /*synthesis loc =”R10C16,R10C15,R10C14,R10C9” */;
```

Appendix B. sysI/O Attributes Using the Spreadsheet View

The sysI/O buffer attributes can be assigned using the Spreadsheet View available in the Diamond design tool. The attributes that are not available as HDL attributes, such as Bank V_{CCIO}, are available in the Spreadsheet View interface.

The Port Assignment tab lists all the ports in a design and all the available sysI/O attributes as preferences. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when a particular IO_TYPE is chosen, the columns for the DRIVE, PULLMODE, SLEWRATE and other attributes list the valid combinations for that IO_TYPE. Pin locations can be locked using the Pin column of the Port Assignment tab. Right-clicking on a cell lists all the available pin locations. The Spreadsheet View can run a DRC check to check for incorrect sysI/O attribute assignments.

All the preferences assigned using the Spreadsheet View are written into the logical preference file (.lpf).

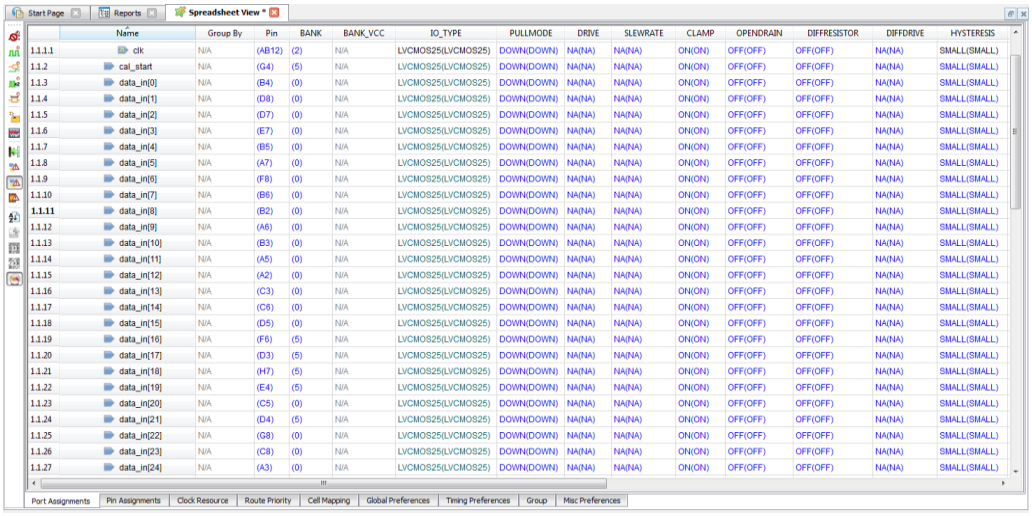


Figure B.1. Port Assignment Tab of Spreadsheet View

B.1. Bank V_{CCIO} Setting in Spreadsheet View

Bank V_{CCIO} is editable in the Global Preference tab of the Spreadsheet View. You can choose the value of the Bank V_{CCIO} to determine the value of the V_{CCIO} of a specific bank.

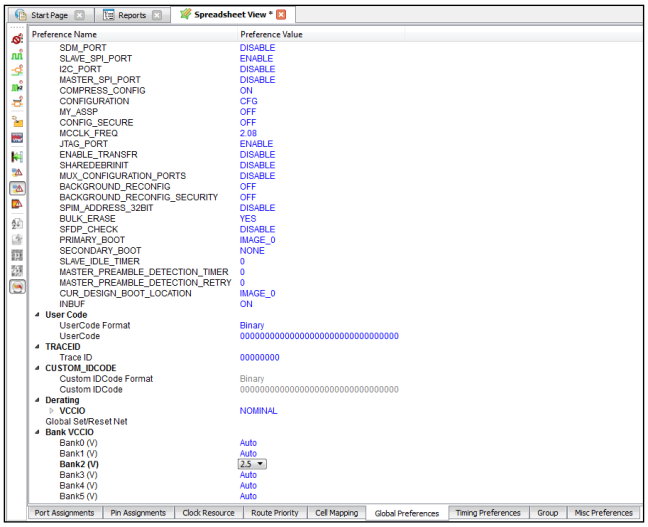


Figure B.2. Bank V_{CCIO} in Global Preference Tab

Appendix C. sysI/O Attributes Using Preference File (ASCII File)

You can enter sysI/O attributes directly in the preference (.lpf) file as sysI/O buffer preferences. The LPF file is a post-synthesis FPGA constraint file that stores logical preferences that have been created or modified in the Spreadsheet View or directly in a text editor. It also contains logical preferences originating in the HDL source. Modifying the Spreadsheet View in the Diamond software can automatically update the content of the LPF file and the reverse is also true. The settings in the Spreadsheet View are reflected in the preference file once they are saved. Details of the supported preferences and their corresponding syntax can be found in the Diamond Help System.

Appendix D. Issue: GPIO Input Prevents Powering Down the FPGA

For ZC/HC devices where the design involves V_{CC} and bank V_{CCIOx} voltages that are the same, either 3.3 V or 2.5 V, and they are connected together, careful design consideration must be followed. This is to avoid the FPGA not fully powering down and operating in an undefined state.

Note: Chip failures can occur when the datasheet input current limits are exceeded.

D.1. GPIO Input Current Leakage Pathway

The FPGA is powered on, with the bitstream program input CLAMPs on.
While the FPGA powers down, the external circuit continues to drive input pins.
As the FPGA V_{CC} and V_{CCIOx} voltage drops, the GPIO input pins allow external devices to drive reverse current into the FPGA through the on-CLAMPs ,and this current appears at the V_{CCIOx} pins which are connected to V_{CC} and keeping the V_{CC} voltage high enough for the input CLAMPs to remain active.

Other devices besides the FPGA, can be connected to the V_{CC} rail, with each device drawing current from the FPGA. As a result, the FPGA can pass enough reverse current to cause internal burnouts or failures to occur quickly or gradually, depending on the overcurrent of each pin and the number of pins involved.

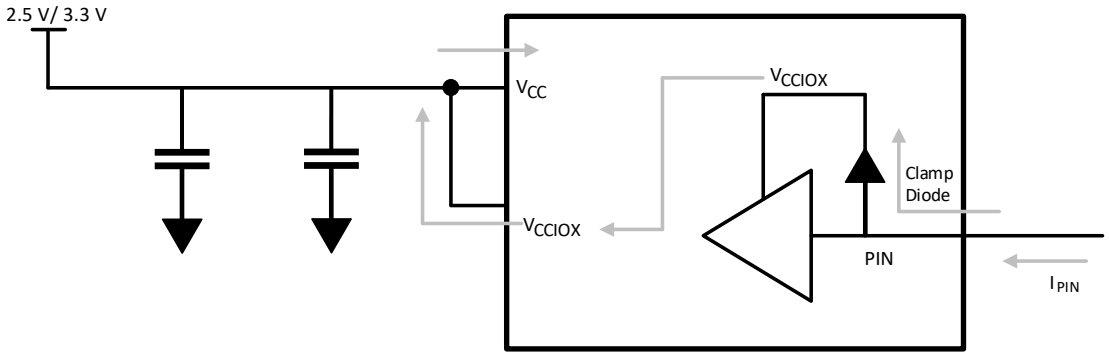


Figure D.1. Potential Current Path for Powered Down FPGA with Driven Input

D.2. Workarounds

Workaround 1

Turn off any external devices connected to the FPGA that are operating ≥ 2.5 V at the same time as FPGA.

Workaround 2

Configure the Lattice Diamond software to keep GPIO CLAMPs OFF in the bitstream when CLAMPs are not required.

Workaround 3

- Ensure that external circuits do not exceed the datasheet I/O pad current limits for banks operating at 2.5 V or higher.
- In each bank, the current should not exceed n × 8 mA. Where n represents the number of I/O pads in between two consecutive power pins. See below scenarios.
  - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – V_{CCIO}
  - GND – I/O_1 – I/O_2 – I/O_x – GND
  - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – GND
- The I/O groupings can be found in the pin tables generated by the Lattice Diamond software.

Example: Limit the pin current by connecting a series resistor to an FPGA GPIO input.

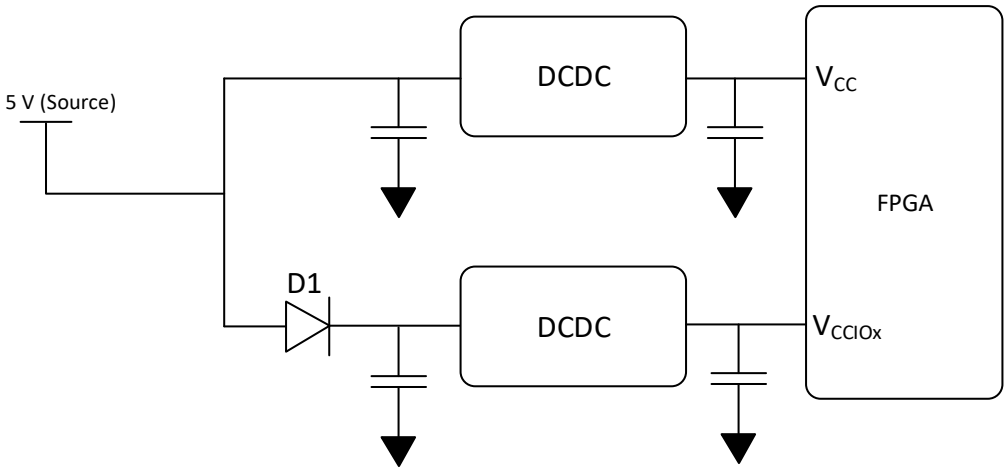
Most non-high-speed designs work well with a 200 Ω to 1 kΩ series resistor.

$$Math: R \times C \times 2\,Tau = Trise\ /\ Tfall$$

$$200\ \Omega\ series\ resistor\ at\ GPIO\ input \times 10\,pF\ etch\ and\ pin\ capacitance \times 2\,Tau = 4ns\ Trise\ /\ Tfall$$

Workaround 4

For V_{CCIO}, use a separate voltage regulator with a diode (D1) connecting the voltage source to the input.



References

For more information refer to:

- Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065)
- MachXO3D web page
- MIPI D-PHY Interface IP (FPGA-RD-02040)
- Lattice Diamond FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.3, July 2025

Section	Change Summary
Software sysI/O Attributes	• In the DRIVE section, changed *Table 10.2 shows the supported drive strength for the single-ended I/O types under designated VCCIO conditions* to *Table 10.2 shows the supported drive strength for single-ended I/O types under designated I/O standards.* • In Table 10.2. Output Drive Capability for Ratioed sysI/O Standards: changed 16 mA drive strength support of LVCMOS25 from *YES* to —.

Revision 1.2, February 2025

Section	Change Summary
All	Minor editorial fixes.
Disclaimers	Updated section contents.
Abbreviations in This Document	• Replace *Acronyms* with *Abbreviations*. • Reworked section contents.
sysI/O Banking Scheme	Added the statement, w*hen the CLAMP DIODE is ON, careful design considerations must be followed; for more information see Appendix D*.

Software sysI/O Attributes	• Reworked Clamp section.
	• Updated the section structure of sysI/O Primitives from *10.1.14* to *10.2*. This is a general description that covers previous 10.1.15, 10.1.16 and 10.1.17.
	  • Updated the section structure of Tri-State All (TSALL) from *10.1.15* to *10.2.1*.
	  • Updated the section structure of Fixed Data Delay (DELAYE) from *10.1.16* to *10.2.2*.
	  • Updated the section structure of Dynamic Data Delay (DELAYD) from *10.1.17* to *10.2.3*.

Appendix D	Added this section.

Revision 1.1, August 2023

Section	Change Summary
Input Reference Voltage	Removed the statement, *The input reference voltage can also be generated internally from the VREF generator. Again, there is one VREF generator per bank and its programmable settings include OFF, 45% of VCCIO, 50% of VCCIO, and 55% of VCCIO. Programming of the internal VREF generator and the external VREF pin cannot be set at the same time for a particular bank because there is only one VREF bus per bank*.
Software sysI/O Attributes – VREF sub section	• Removed the statement, *in additional to the I45, I50 and I55 values.* • Replaced the statement, *or internal VREF driver* with *needed.* • Removed the period after the word *bank.* • Replaced the word, *only* with *and only.* • Removed the statement, *settings chosen from I45, I50, I55 or VREF1_LOAD.* • Removed the statement, *I45, I50, I55.*
References	Added this section.

Revision 1.0, July 2021

Section	Change Summary
Software sysI/O Attributes	Changed *VCCIO* to *Drive Strength (mA)* in Table 10.2.

Revision 0.90, May 2019

Section	Change Summary
All	First preliminary release.

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