MIPI D-PHY Bandwidth Matrix and Implementation

Technical Note

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CMOS	Complementary Metal-Oxide Semiconductor
CSI	Camera Serial Interface
DE	Data Enable
DMT	Display Monitor Timing
DSI	Display Serial Interface
EAV	End of Active Video
FHD	Full High Definition
FPGA	Field-Programmable Gate Array
HD	High Definition
HS	High Speed; Horizontal Sync
I/O	Input/Output
LP	Low Power
MIPI	Mobile Industry Processor Interface
PIO	Programmable Input/Output
RB	Reduced Blanking
SAV	Start of Active Video
UHD	Ultra High Definition
VS	Vertical Sync

1. Introduction

As we move from the world of standard-definition to the high-definition and ultra-high-definition, the common parallel interfaces are difficult to expand, require many interconnects and consume relatively large amounts of power. Emerging packet-based serial interfaces, such as MIPI CSI-2 and DSI address many of the shortcomings of the parallel interfaces, while also introducing system complexity.

Understanding the mathematics behind the parallel and serial interface bandwidth estimation can prevent a lot of problems when choosing an FPGA device with the right number of data lanes supporting the required data transfer rate. This document describes in detail the methods of calculating the bandwidth and data rate of the image sensor's output of the RGB, YUV, or RAW data over a single or multi-lane MIPI CSI-2 and DSI interface. The same calculation method can be applied to other video interfaces such as FPD-Link, HiSPI, and HDMI.

Some Lattice FPGA devices can support the MIPI D-PHY interface by implementing it through a Soft D-PHY, a Hardened D-PHY or both. Hardened D-PHYs are dedicated MIPI D-PHY blocks embedded within the FPGA. Soft D-PHYs are implemented through the Programmable I/Os on the high-speed banks of the FPGA. Only Lattice CrossLink™, CrossLinkPlus™, and CrossLink-NX (only LIFCL-17 and LIFCL-40) devices have Hardened D-PHY blocks. This document focuses on the Soft D-PHY support of the various Lattice FPGA devices.

Figure 1.1 shows a conceptual model of the CMOS Sensor Bridge Design. On the left, a CMOS sensor transfers image data to the FPGA through 1 to 4 serial data lanes; the FPGA sensor bridge merges the image data from multiple lanes and converts them into parallel data; on the right, the image data are sent out over the parallel bus in standard video format. Based on the known video format information, we can calculate the required bandwidth. Because the FPGA does not buffer the video frames, the peak transfer rate of CMOS sensor input must meet the bandwidth requirement of the output. With this presumption, we can estimate the maximum data rate and bit clock frequency of the CMOS sensor interface.

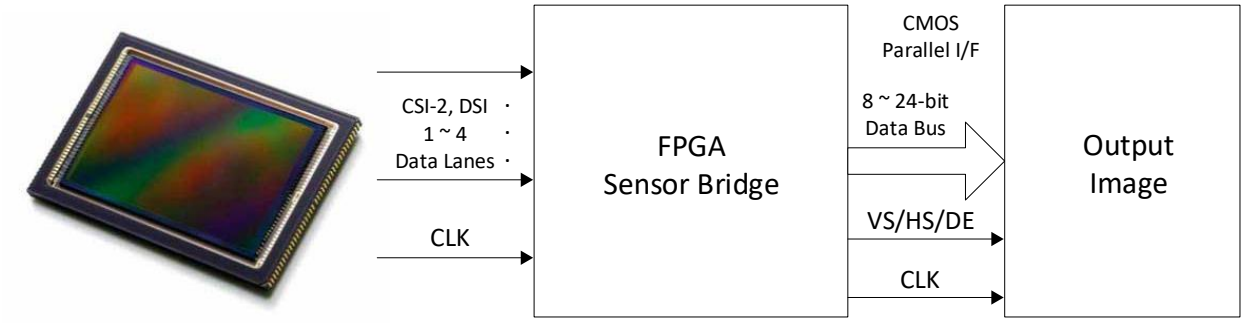

Figure 1.1. CMOS Sensor Bridge Model

2. Video Format

To estimate the data transfer rate, we need to understand the format of the video data transferred over the sensor bridge. Video is composed of a series of still images. Each still image is composed of individual lines of pixel data. Figure 2.1 illustrates a conceptual interlaced video frame. The progressive video frame is similar to it except for only one field per frame.

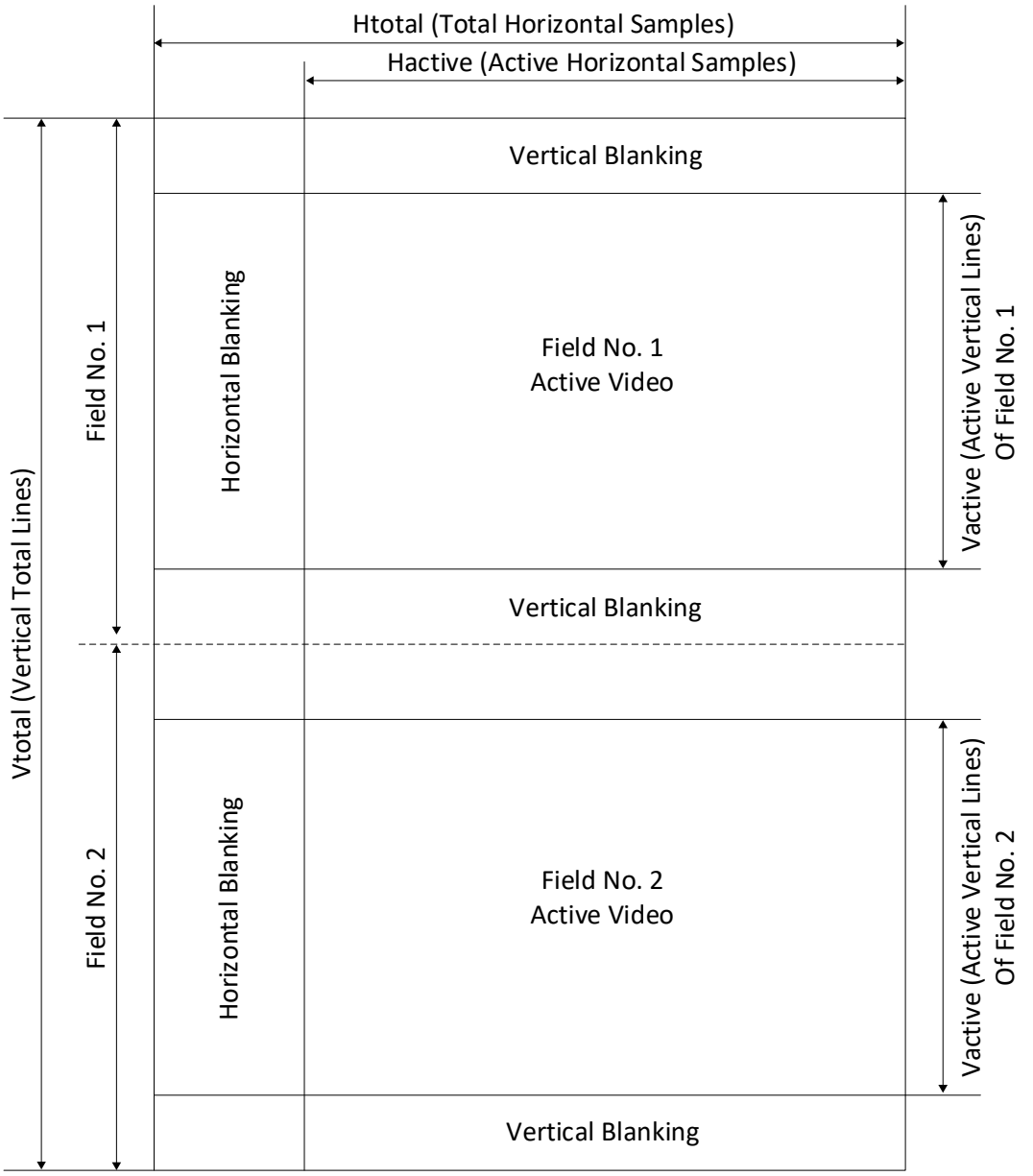

Figure 2.1. Interlaced Mode Video Frame Format

For digital video, either a separate Horizontal Sync (HS), Vertical Sync (VS) and Data Enable (DE) signals are used to synchronize the video data transfer, or a special sequence embedded into the video data stream indicating the Start of Active Video (SAV) or End of Active Video (EAV). For MIPI CSI-2, two-packets structures are defined for Low Level Protocol layer: Long packets to carry payload data, and the Short Packets for Frame Synchronization (that is Frame Start and Frame End) and Line Synchronization (that is Line Start and Line End).

There are many characteristics of the video streams such as frame rate, interlaced vs progressive, aspect ratio, stereoscopic, color space, and color depth. We will review the major parameters that will be used in the calculation of the data transfer rate in the later sections of the document.

2.1. Video Resolution and Pixel Clock

The video resolution is quoted as Width × Height, with the unit in pixels: for example, 1920 × 1080 means the horizontal width is 1920 pixels and the vertical height is 1080 lines. Figure 2.2 shows the chart of the common display resolutions.

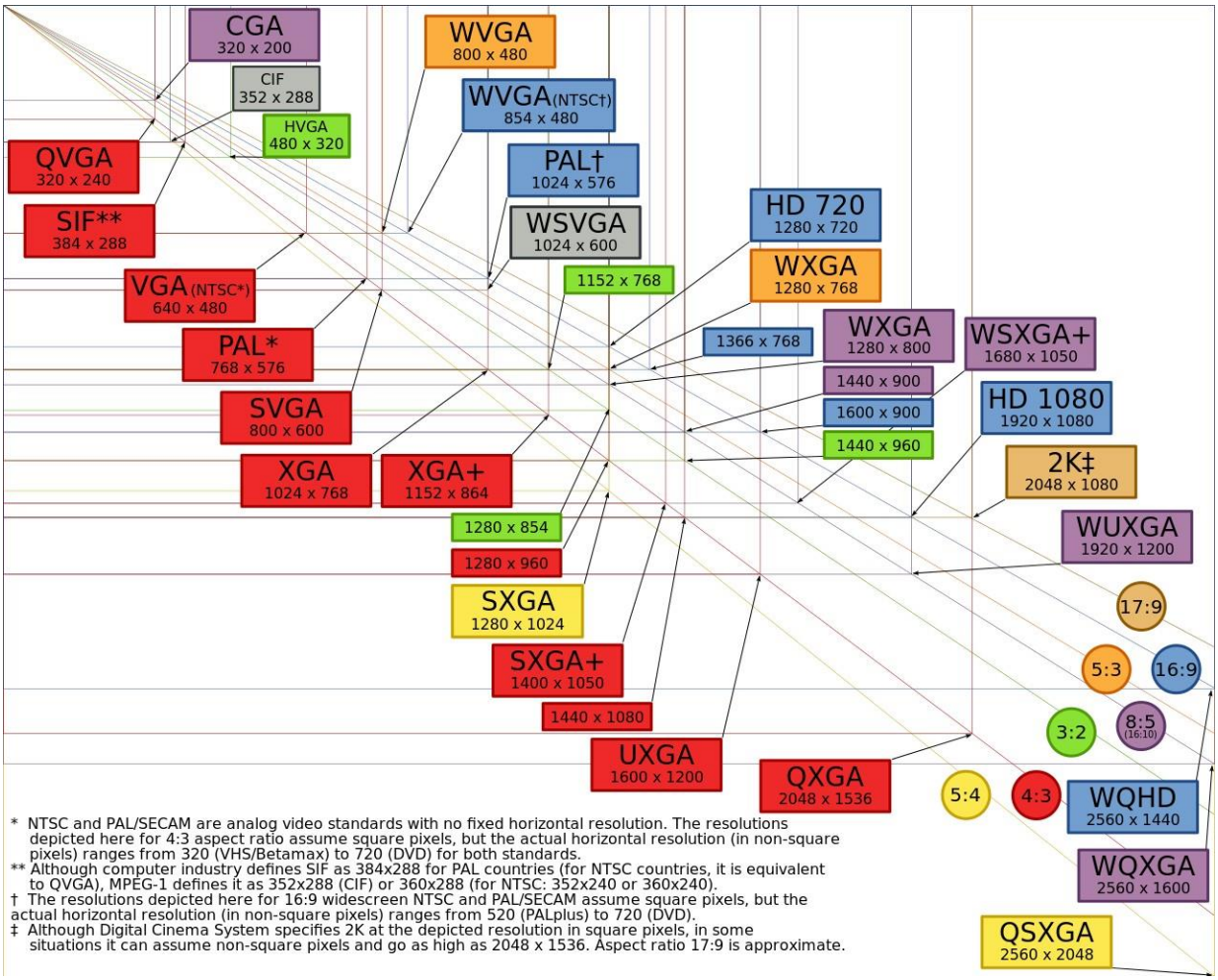

Figure 2.2. Most Common Display Resolutions

Source: https://en.wikipedia.org/wiki/File:Vector_Video_Standards4.svg

There are two major types of video format standards: SMPTE/CEA defines video standards for the Television and broadcast; VESA Display Monitor Timing (DMT) standard defines the video standards for the computer monitors. Table 2.1 lists the most common video resolutions. Among them, we choose HD (1280 × 720p), FHD (1920 × 1080p) and UHD (3840 × 2160p) as examples to calculate the bandwidth and data rate in the later sections.

Table 2.1. Common Video Format

		Hactive	Vactive	Htotal	Vtotal	Refresh Rate (Hz)	Pixel Freq (MHz)
Television Video Format							
EDTV	640x480p @ 59.94 Hz	640	480	800	525	59.94	25.175
	720x480p @ 59.94 Hz	720	480	858	525	59.94	27
	720x576p @ 50 Hz	720	576	864	625	50	27
HDTV	1280x720p @ 60 Hz	1280	720	1650	750	60	74.25
Full HD	1920x1080i @ 60 Hz	1920	1080	2200	1125	60	74.25
	1920x1080p @ 60 Hz	1920	1080	2200	1125	60	148.5
UHDTV	3840x2160p @ 60 Hz	3840	2160	4400	2250	60	594
	4096x2160p @ 60 Hz	4096	2160	4400	2250	60	594
Computer Monitor Format							
XGA	1024x768p @ 60 Hz	1024	768	1344	806	60	65
WXGA	1280x800p @ 60 Hz	1280	800	1680	831	59.81	83.5
WXGA+	1440x900p @ 60 Hz	1440	900	1904	934	59.887	106.5
HD	1366x768p @ 60 Hz	1366	768	1792	798	59.79	85.5
HD+	1600x900p @ 60 Hz (RB*)	1600	900	1800	1000	60	108
WUXGA	1920x1200p @ 60 Hz (RB*)	1920	1200	2080	1235	59.95	154
WQXGA	2560x1600p @ 60 Hz (RB*)	2560	1600	2720	1646	59.97	268.5

***Note**: RB – reduced blanking

Some of the image sensors can output the standard video formats by cropping or binning the pixels, while others may output non-standard resolutions. The important thing is to obtain the information of the Total Horizontal Samples, Total Vertical Lines, and frame Refresh Rate. This document discusses how to calculate the bandwidth based on the above information.

2.2. Color Depth

Color depth, also known as bit depth, can be either referred to as bits-per-pixel (bpp) which specifies the number of bits used for a single pixel, or referred to as bits-per-component (bpc) which specifies the number of bits used to represent each color component of a single pixel. Deep color supports 30/36/48-bit for three RGB colors. In this document, the term Pixel Size is equivalent to the color depth in bits-per-pixel. For example, the pixel size of a 30-bit deep color RGB is defined as 30 bits per pixel, or 10 bits per color component.

3. MIPI CSI-2/DSI Interfaces

MIPI Camera Serial Interface 2 (CSI-2) and Display serial Interface (DSI) are two of the serial interface protocols based on the MIPI D-PHY physical interface. MIPI D-PHY supports unidirectional HS (High Speed) mode and Bidirectional LP (Low Power) mode.

The following figures show the MIPI CSI-2/DSI implementation through Programmable I/Os of some Lattice FPGA devices. Figure 3.1 shows the block diagram of the Unidirectional Receive HS Mode and Bidirectional LP Mode interface. Figure 3.2 shows the block diagram of the Unidirectional Receiver HS Mode Only interface. Figure 3.1 and Figure 3.2 do not apply to CrossLink, CrossLinkPlus, CrossLink-NX, Certus™-NX, and CertusPro™-NX as these devices use Programmable I/Os that can be configured as MIPI D-DPHY input buffers without any need for external components.

Figure 3.3 shows the block diagram of the Unidirectional Transmit HS Mode and Bidirectional LP Mode interface. Figure 3.4 shows the block diagram of the Unidirectional Transmit HS Mode Only interface. Figure 3.3 and Figure 3.4 do not apply to CrossLink and CrossLinkPlus as their programmable I/Os can only be configured as MIPI D-PHY receivers. Figure 3.3 and Figure 3.4 also do not apply to CrossLink-NX, Certus-NX and CertusPro-NX since these devices use Programmable I/Os that can be configured as MIPI D-DPHY output buffers without any need for external components.

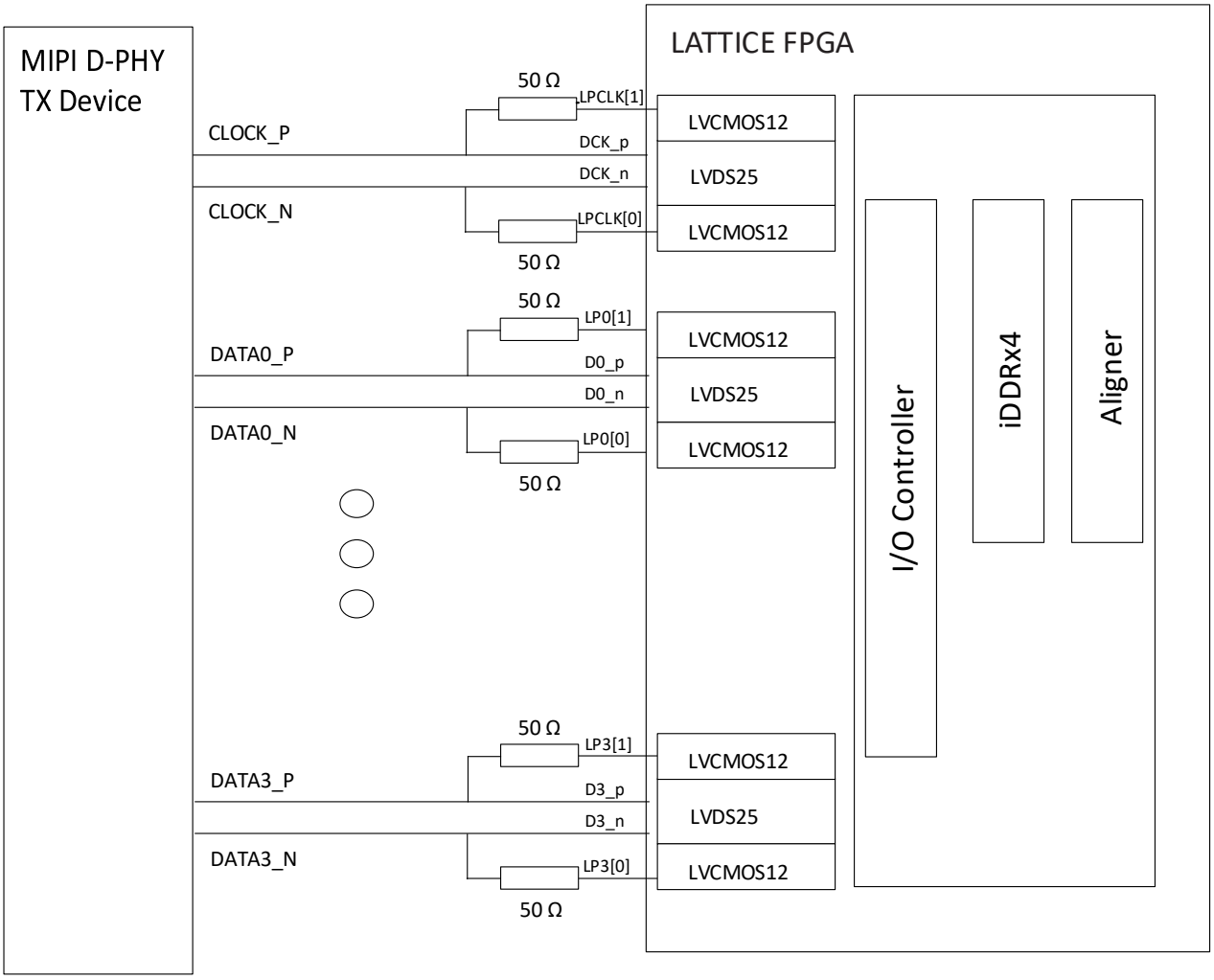

Figure 3.1. Unidirectional Receive HS Mode and Bidirectional LP Mode Interface Implementation

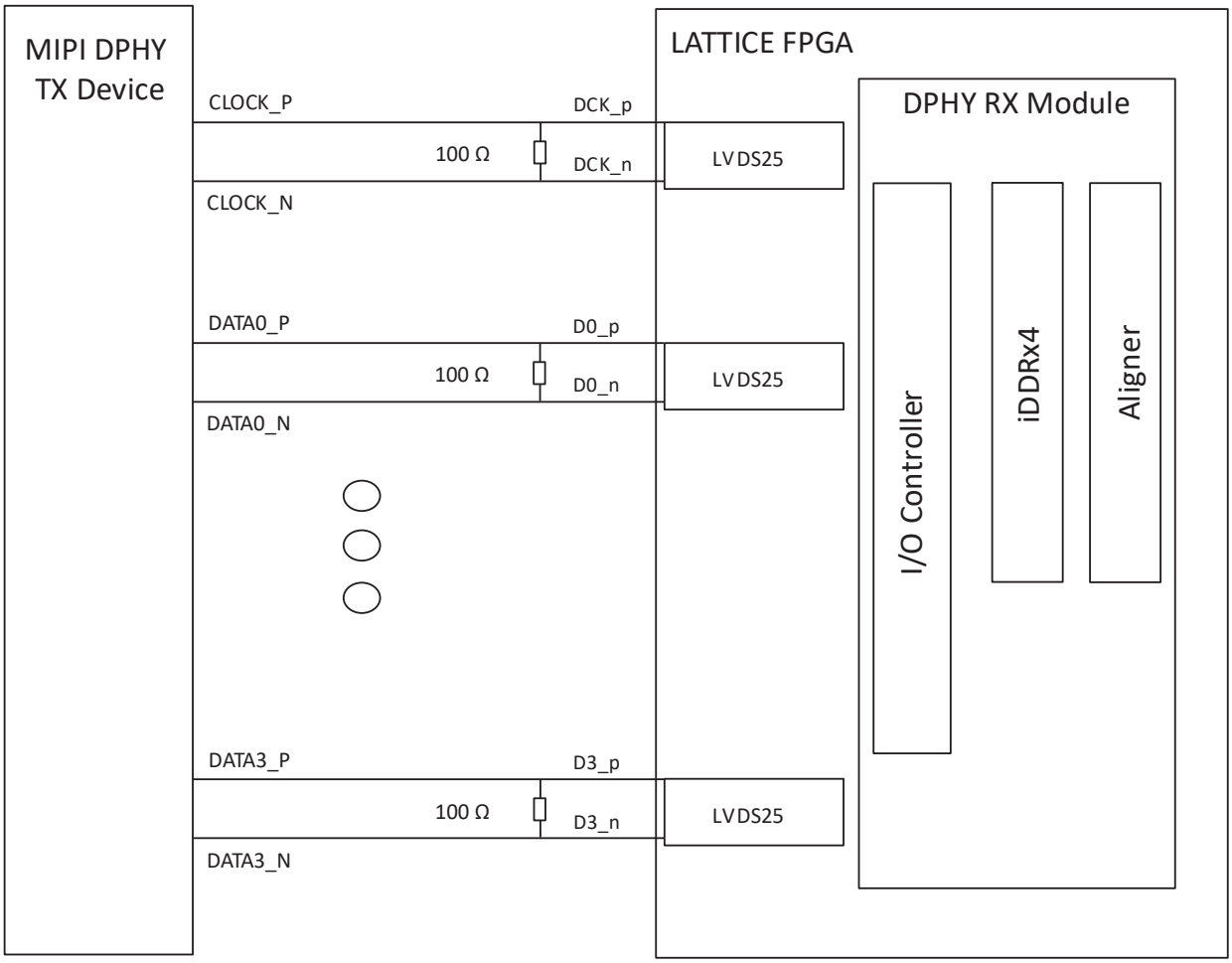

Figure 3.2. Unidirectional Receive HS Mode Only Implementation

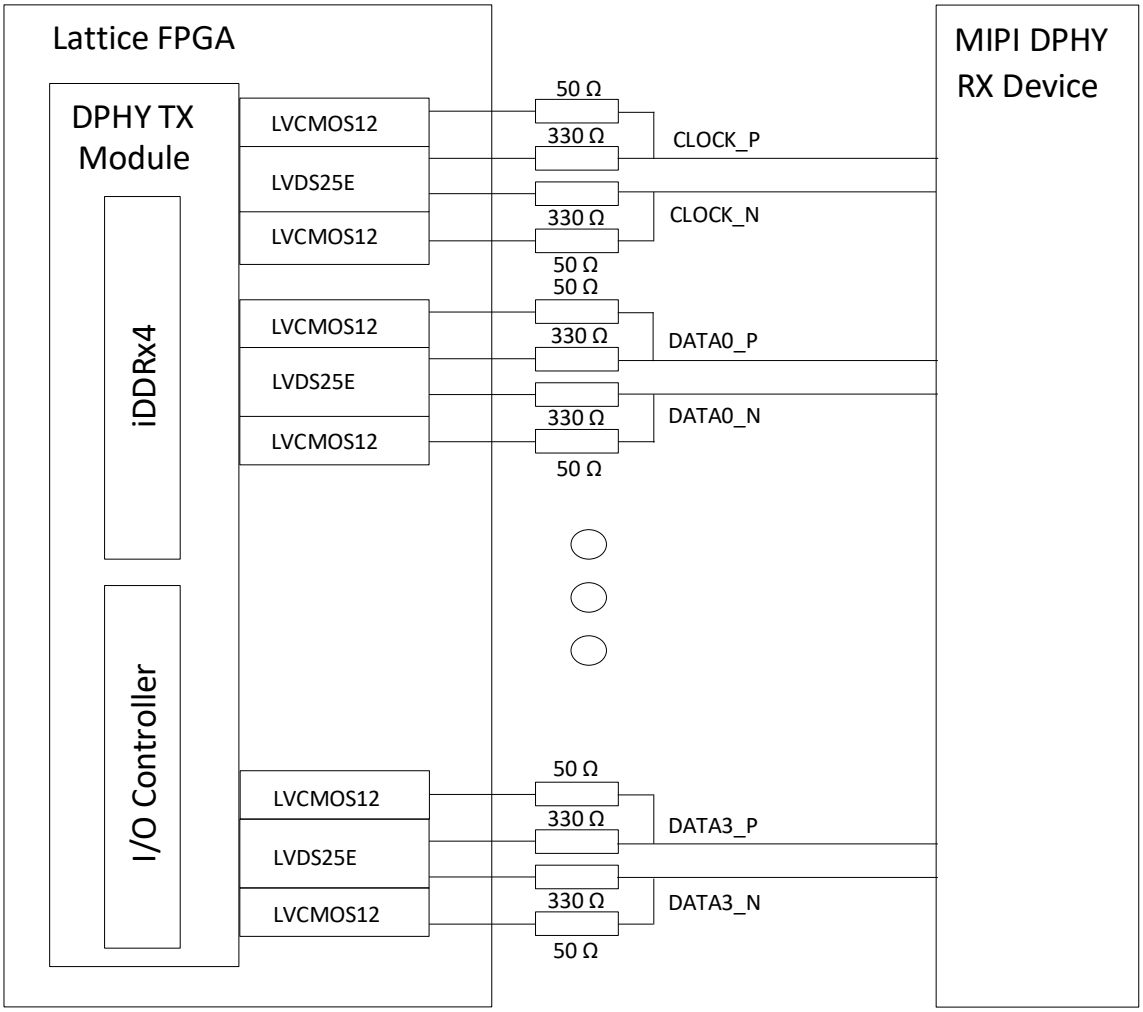

Figure 3.3. Unidirectional Transmit HS Mode and Bidirectional LP Mode Interface Implementation

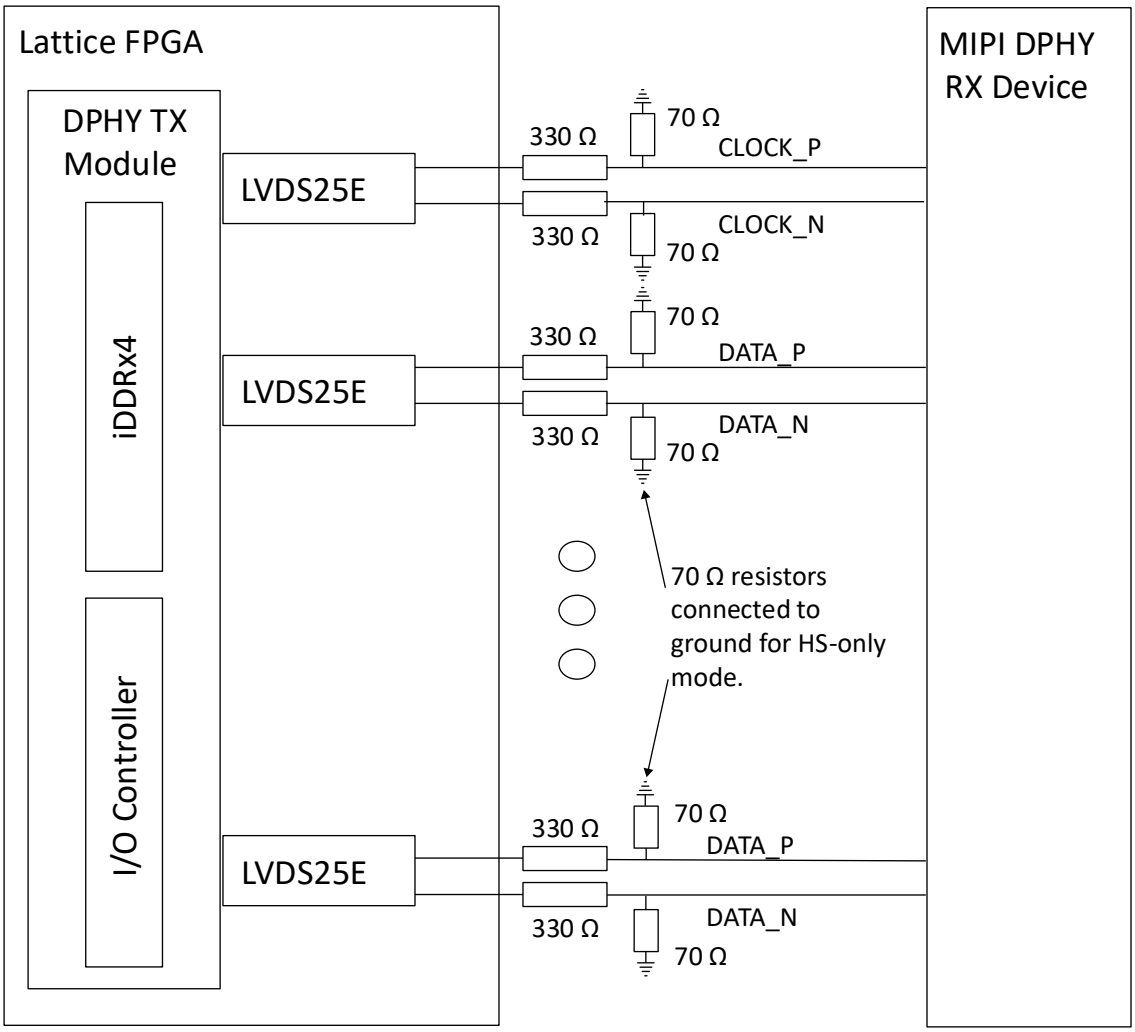

Figure 3.4. Unidirectional Transmit HS Mode Only Implementation

4. Packetizing

The MIPI CSI-2 supports YUV, RGB or RAW data with varying pixel formats from 6 to 24 bits per pixel. In the transmitter, the pixels are packed into bytes (Pixel-to-byte Packing) before sending the data to Low Level Protocol layer; in the receiver the bytes received from the Low Level Protocol layer are unpacked into pixel (Byte-to-pixel Unpacking). One CSI-2 long packet shall contain one line of image data. The total size of data within a long packet for all data types shall be a multiple of eight bits (byte). Figure 4.1 shows an example of packing four 10-bit pixel data, or RAW10, into five bytes to look like 8-bit data format.

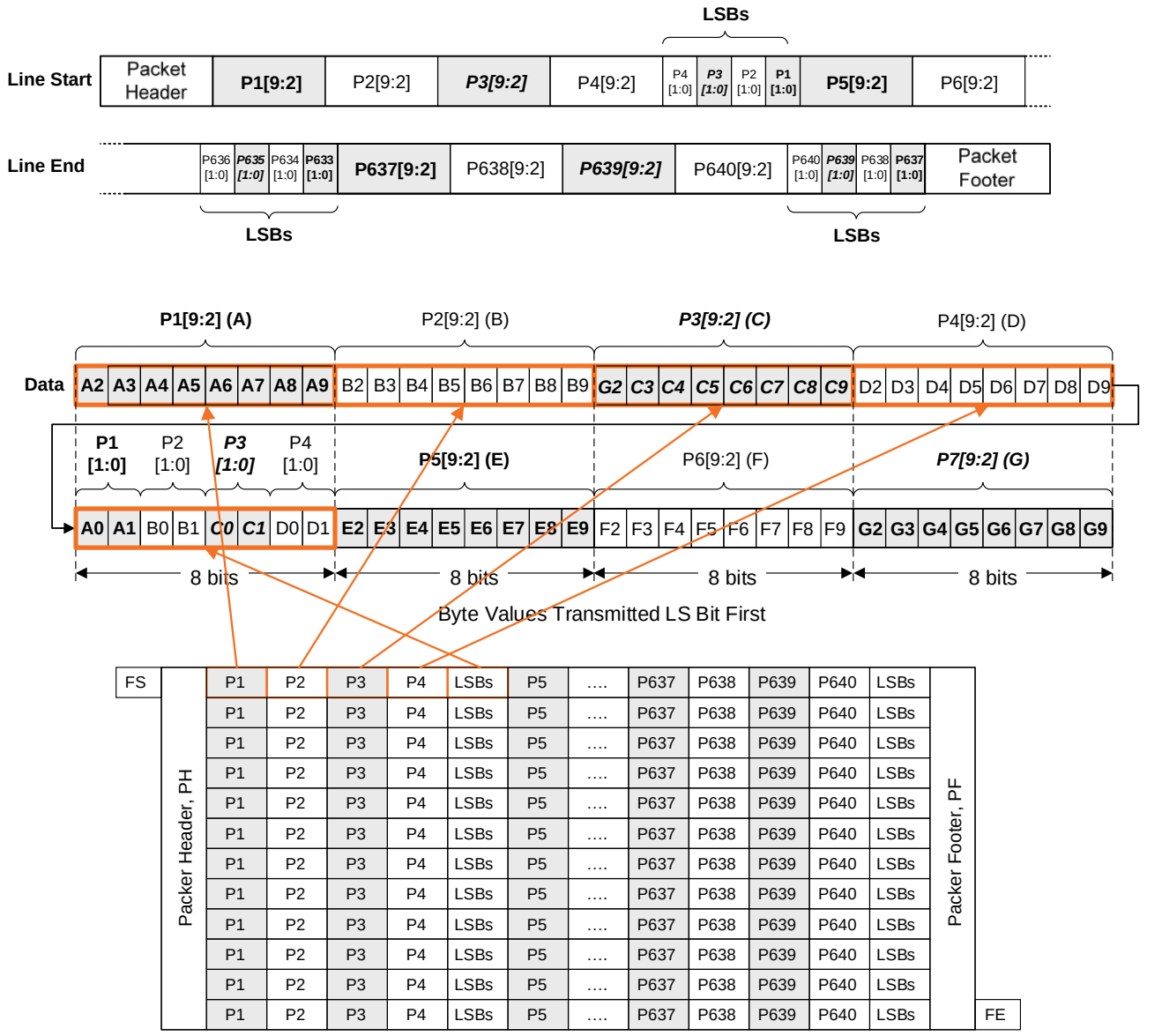

Figure 4.1. An Example of RAW10 Transmissions on CSI-2 Bus

Table 4.1 specifies the packet size constraints for the supported data formats. The length of each packet must be a multiple of the values in the table. For simplicity, all data format examples are single lane configurations.

Table 4.1. CSI-2 Packet Size Constraints

Data Format	Odd/Even Lines	Pixels	Bytes	Bits
YUV420 8-bit	Odd	2	2	16
	Even	2	4	32
YUV420 10-bit	Odd	4	5	40
	Even	4	10	80
YUV422 8-bit	—	2	4	32
YUV422 10-bit	—	2	5	40
RGB888	—	1	3	24
RGB666	—	4	9	72
RGB565	—	1	2	16
RGB555	—	1	2	16
RGB444	—	1	2	16
RAW6	—	4	3	24
RAW7	—	8	7	56
RAW8	—	1	1	8
RAW10	—	4	5	40
RAW12	—	2	3	24
RAW14	—	4	7	56
RAW16	—	1	2	16
RAW20	—	2	5	40

Note: RGB555 and RGB444 data should be made to look like RGB565 data by inserting padding bits to the LSBs of each color component.

4.1. xMulti-lane

MIPI CSI-2 is lane-scalable. Applications requiring more bandwidth than that provided by one data lane, or those trying to avoid high clock rates, can expand the data path to two, three, or four lanes wide and obtain approximately linear increases in peak bus bandwidth.

5. Bandwidth and Data Rate

This section provides the definitions of terms used in a video performance and summarizes the process of calculating the bandwidth and data transfer rate. The terms used and their descriptions are as follows:

- **Pixel Clock** – the time base in MHz at which individual pixels are transmitted.
- **Bandwidth** – the capacity required in Mb/s of a given system to pass a specific frequency.
- **Data Rate** – the data flow throughput in bits per second of the transport layer.

5.1. Bandwidth and Data Rate Calculation

5.1.1. Pixel Clock

If the video format is standard, the pixel clock frequency can be obtained from the SMPTE/CEA or VESA standards. You can also calculate the pixel clock frequency using the following equation:

Pixel Clock Frequency = Total Horizontal Samples × Total Vertical Lines × Refresh Rate

The Total Horizontal Samples and Total Vertical Lines include blanking period. The Refresh Rate may be referred to as Frame Rate or Vertical Frequency

5.1.2. Total Data Rate or Bandwidth

The bandwidth of a given video format is simply a product of the Pixel Clock Frequency and Pixel Size in bits. The total data rate of the CMOS sensor interface must match the bandwidth.

Total Data Rate (Bandwidth) = Pixel Clock Frequency × Pixel Size (in bits)

5.1.3. Data Rate per Lane

The per-lane data rate (Line Rate) is the total data rate (bandwidth) divided by the number of lanes. CSI-2 can support up to four data lanes.

Data Rate per Lane = Total Data Rate (Bandwidth) ÷ Number of Data Lane

5.1.4. Bit Clock

Because the MIPI data lane is a Double Data Rate interface, the CSI-2 Bit Clock frequency is one half of the Data Rate per Lane.

Bit Clock Frequency = Data Rate per Lane ÷ 2

5.2. Examples

5.2.1. Example 1: 1920x1080p@60Hz, RAW10, 2-lane

Total Horizontal Samples = 2200, Total Vertical Lines = 1125

Pixel Clock Frequency = 2200 × 1125 × 60 = 148.5 MHz

Bandwidth (Total Data Rate) = 148.5 MHz × 10-bit = 1.485 Gb/s

Line Rate (Data Rate per Lane) = 1.485 Gb/s ÷ 2-lane = 742.5 Mb/s

MIPI Bit Clock Frequency = 742.5 ÷ 2 = 371.25 MHz

5.2.2. Example 2: 3840x2160@30Hz, RAW8, 4-lane

Total Horizontal Samples = 4400, Total Vertical Lines = 2250

Pixel Clock Frequency = 4400 × 2250 × 30 = 297 MHz

Bandwidth (Total Data Rate) = 297 MHz × 8-bit = 2.376 Gb/s

Line Rate (Data Rate per Lane) = 2.376 Gb/s ÷ 4-lane = 594 Mb/s

MIPI Bit Block Frequency = 594 ÷ 2 = 297 MHz

6. Device Selection

This section summarizes the Lattice FPGA device families that support MIPI interface with and without external components as described in the MIPI CSI-2/DSI Interfaces section.

6.1. Hardware Features

Table 6.1 and Table 6.2 highlight the features of MIPI D-PHY hardware implementation using the Lattice MachXO2™, MachXO3L™, MachXO3LF™, MachXO3D™, LatticeECP3™, ECP5™, ECP5-5G™, Crosslink, CrossLinkPlus, CrossLink-NX, Certus-NX, and CertusPro-NX device families. For more details on MIPI D-PHY Receiver and Transmitter resource utilization and design performance for some of the FPGA devices, refer to the MIPI D-PHY Reference Design (FPGA-RD-02040).

Table 6.1. MIPI D-PHY Rx/Tx Implementation Hardware Comparison for MachXO2, MachXO3L, MachXO3LF, MachXO3D, LatticeECP3, ECP5, ECP5-5G, CrossLink, and CrossLinkPlus Device Families

		MachXO2, MachXO3L, MachXO3LF, and MachXO3D (Soft)	LatticeECP3 (Soft)	ECP5 and ECP5-5G (Soft)	CrossLink and CrossLinkPlus[3] (Soft)	CrossLink and CrossLinkPlus[3] (Hardened)
MIPI D-PHY Rx Implementations	HS Mode	• LVDS25 • VCCIO = 2.5 V or 3.3 V • Internal 100 Ω differential termination	• LVDS25 • VCCIO = 2.5 V or 3.3 V • Internal 100 Ω differential termination	• LVDS25 • VCCIO = 2.5 V or 3.3 V • Internal 100 Ω differential termination. • Or use IMIPI primitive (C/D pair)	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination	
	LP Mode	• LVCMOS12 • VCCIO = 1.2 V	• LVCMOS12 • VCCIO = 1.2 V	• LVCMOS12 • VCCIO = 1.2 V Or use IMIPI primitive (C/D pair)		
MIPI D-PHY Tx Implementations	HS Mode	• LVDS25E	• LVDS25E or LVCMOS33D[2]	• LVDS25E or LVCMOS33D[2]	N/A	• Use CSI-2/DSI D-PHY Tx IP Core • Internal 100 Ω differential termination
	LP Mode	• LVCMOS12 • VCCIO = 1.2 V	• LVCMOS12 • VCCIO = 1.2 V	• LVCMOS12 • VCCIO = 1.2 V	N/A	
DDR Gearing Ratio		X4	X2	X2	X8 or X16	X8 or X16
Number of D-PHY	Rx	Up to two Rx D-PHYs; Bank 2 only.	Up to two Rx D-PHYs. Only two clock divider primitives, one on Bank 2 or Bank 3 (right), one on Bank 6 or Bank 7 (left).	Up to four Rx D-PHYs (left and right sides); Four dedicated Clock Divider (CLKDVI) available.	Limited by PIO pairs and clock dividers available in Bank 1 and Bank 2 only	Up to 2 D-PHY Rx
	Tx	Tx D-PHY max limited by PIO A/B pairs; Bank 0 only.	Tx D-PHY maximum limited by PIO pairs available in Bank 2, Bank 3, Bank 6, and Bank 7 if CLKDIV is shared on each side. If Tx D-PHY on side, can only have Rx D-PHY on the other.	Tx D-PHY maximum limited by PIO pairs, available in the left and right banks.	N/A	Up to 2 D-PHY Tx

	MachXO2, MachXO3L, MachXO3LF, and MachXO3D (Soft)	LatticeECP3 (Soft)	ECP5 and ECP5-5G (Soft)	CrossLink and CrossLinkPlus[3] (Soft)	CrossLink and CrossLinkPlus[3] (Hardened)
Number of Lanes	Depends on the number of PIO A/B pairs available	Depends on the number of PIO pairs available	Depends on the number of PIO pairs available	Depends on the number of PIO pairs available	4 lanes max per Hardened D-PHY
Rx Performance[1]	523 Mb/s	467 Mb/s	467 Mb/s	1.2 Gb/s	1.5 Gb/s
Tx Performance[1]	728 Mb/s	698 Mb/s	800 Mb/s	N/A	1.5 Gb/s

Notes:

1. Rx Performance and Tx Performance values are calculated from the data sheet External Timing Table using IDDRX2/X4/X8 and ODDRX2/X4/X8 with data and clock centered aligned. The maximum data rate each family device can achieve is compliant with MIPI Alliance Specification (v1.1). This is ±0.15 UI setup/hold window on the receiver at ≤1 Gb/s and ±0.15 UI skew window on the transmitter at ≤1 Gb/s. See the MIPI Data Rate Calculation section for the calculations based on current data sheet. It is still practical to reach performance higher than the specified data rate. Refer to the tSU/tHD Valid Window at Higher Data Rate and Tskew Window at Higher Data Rate sections for details.
2. If LVCMOS33D is used instead of LVDS25E, external resistors shown in Figure 3.3 and Figure 3.4 should be adjusted to 400 Ω to modulate common mode voltage level.
3. CrossLink and CrossLinkPlus have a maximum of two Hardened MIPI blocks on the top side of the chip (depending on package), and has dedicated I/Os associated with Hardened blocks. The Hardened MIPI D-PHY receiver interface can support line rates up to 1.5 Gb/s while the Soft D-PHY receiver interface can support line rates up to 1.2 Gb/s. Only the Hardened D-PHY can be configured as a MIPI D-PHY transmitter capable of line rates up to 1.5 Gb/s. Refer to CrossLink High-Speed I/O MIPI D-PHY and DDR interfaces (FPGA-TN-02012) for details.

Table 6.2. MIPI D-PHY Rx/Tx Implementation Hardware Comparison for CrossLink-NX, CrossLink-NX-33, CrossLinkU-NX, Certus-NX, and CertusPro-NX Device Families

		CrossLink-NX (Soft)	CrossLink-NX (Hardened)	CrossLink-NX-33 and CrossLinkU-NX (Soft)	Certus-NX (Soft)	CertusPro-NX (Soft)
MIPI D-PHY Rx Implementations	HS Mode	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination		• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination
	LP Mode					
MIPI D-PHY Tx Implementations	HS Mode	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination		• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination	• Use CSI-2/DSI D-PHY Rx IP Core • Internal 100 Ω differential termination
	LP Mode					
DDR Gearing Ratio		X8 or X16	X8 or X16	X8 or X16	X8 or X16	X8 or X16
Number of D-PHY	Rx	Limited by PIO pairs and clock dividers available in Banks 3, 4 & 5.	Up to 2 D-PHY Rx	Limited by PIO pairs and clock dividers available in Banks 2, 3 & 4.	Limited by PIO pairs and clock dividers available in Banks 3, 4 & 5.	Limited by PIO pairs and clock dividers available in Banks 3, 4 & 5.
	Tx	Limited by PIO pairs and clock dividers available in Banks 3, 4 & 5.	Up to 2 D-PHY Tx	Limited by PIO pairs and clock dividers available in Banks 2, 3 & 4.	Limited by PIO pairs and clock dividers available in Banks 3, 4 & 5.	Limited by PIO pairs and clock dividers available in Banks 3, 4 & 5.
Number of Lanes		Depends on the number of PIO pairs available	4 lanes max	Depends on the number of PIO pairs available	Depends on the number of PIO pairs available	Depends on the number of PIO pairs available
RX Performance*		1.5 Gb/s	2.5 Gb/s	1.25 Gb/s	1.5 Gb/s	1.5 Gb/s
TX Performance*		1.5 Gb/s	2.5 Gb/s	1.25 Gb/s	1.5 Gb/s	1.5 Gb/s

***Note**: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7. MIPI Data Rate Calculation

This section shows the calculations of the maximum data rate that can be achieved on Lattice FPGA products through the Programmable I/Os. The values are based on data sheet specification of DDRX2/X4/X8/X16 with clock and data center-aligned.

The MIPI Alliance Specification for D-PHY versions 1.1 and 1.2 have the same setup, hold and skew timing requirements for line rates up to 1.5 Gb/s. Refer to the following details:

- ±0.15 UI setup/hold window on the receiver at ≤ 1.0 Gb/s and ±0.15 UI skew window on the transmitter at ≤ 1.0 Gb/s.
- ±0.20 UI setup/hold window on the receiver at 1.0 Gb/s to 1.5 Gb/s and ±0.20 UI skew window on the transmitter at 1.0 Gb/s to 1.5 Gb/s.

This section also provides the method of calculating the window if higher data rate is desired. The window for higher data rate does not meet the MIPI Alliance Specification but can still be practical in your implementation. Check the latest data sheet on the maximum data rate each Lattice FPGA device family can achieve.

7.1. FPGA Receiver Interface

7.1.1. MachXO2, MachXO3L/LF, and MachXO3D

Maximum MIPI compliance data rate calculation for MachXO2, MachXO3L/LF, and MachXO3D device families:

- Max (0.233, 0.287) = 0.15 × UI
- UI = 0.287/0.15 = 1.913 ns
- Max Data Rate = 1/UI = 1/1.913 = 523 Mb/s (at 0.15 UI)

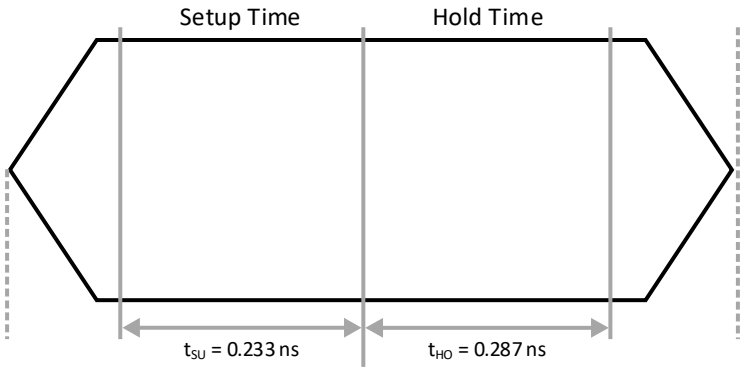

Figure 7.1. MachXO2, MachXO3L/LF, and MachXO3D Maximum Data Rate

Table 7.1. MachXO2 Data Sheet Rev. 3.3 at 756 Mb/s

Generic DDRX4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered									
Parameter	Description	Device	–6		–5		–4		Unit
			Min	Max	Min	Max	Min	Max	
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mb/s
f_{DDRX4}	DDRX2 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz

7.1.2. LatticeECP3

Maximum MIPI compliance data rate calculation for LatticeECP3 device family:

- Max (0.321, 0.321) = 0.15 × UI
- UI = 0.321/0.15 = 2.14 ns
- Max Data Rate = 1/UI = 1/2.14 = 467 Mb/s (at 0.15 UI)

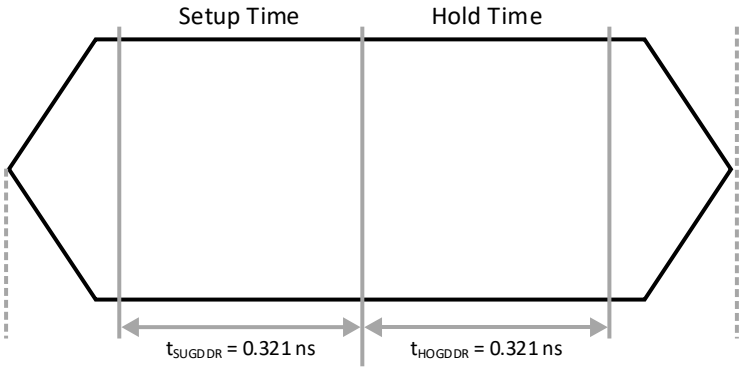

Figure 7.2. LatticeECP3 Maximum Data Rate

Table 7.2. LatticeECP3 Data Sheet Rev. 2.8EA at 800 Mb/s

Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock Input									
Left and Right Sides									
Parameter	**Description**	**Device**	**–8**		**–7**		**–6**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{SUGDDR}	Data Setup Before CLK	ECP3-150EA	321	—	403	—	471	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-150EA	321	—	403	—	471	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	405	—	325	—	280	MHz
t_{SUGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	321	—	403	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-70EA/95EA	321	—	403	—	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	405	—	325	—	250	MHz
t_{SUGDDR}	Data Setup Before CLK	ECP3-35EA	335	—	425	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-35EA	335	—	425	—	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	405	—	325	—	250	MHz
t_{SUGDDR}	Data Setup Before CLK	ECP3-17EA	335	—	425	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-17EA	335	—	425	—	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	405	—	325	—	250	MHz

7.1.3. ECP5/ECP5-5G

Maximum MIPI compliance data rate calculation for ECP5/ECP-5G device family:

- Max (0.321, 0.321) = 0.15 × UI
- UI = 0.321/0.15 = 2.14 ns
- Max Data Rate = 1/UI = 1/2.14 = 467 Mb/s (at 0.15 UI)

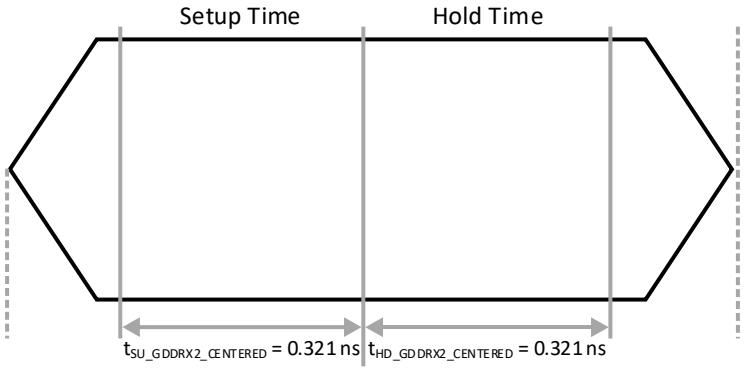

Figure 7.3. ECP5/ECP5-5G Maximum Data Rate

Table 7.3. ECP5/ECP5-5G Data Sheet Rev. 1.9 at 800 Mb/s

Generic DDRX2 Inputs with Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right Sides Only									
Parameter	**Description**	**Device**	**–8**		**–7**		**–6**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{SU\_GDDRX2\_CENTERED}$	Data Setup before CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$t_{HD\_GDDRX2\_CENTERED}$	Data Hold after CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$f_{DATA\_GDDRX2\_CENTERED}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_CENTERED}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz

7.1.4. CrossLink Soft D-PHY

Maximum MIPI compliance data rate calculation for CrossLink device family:

- 1200 Mb/s at V_{IDTH} = 140 mv, V_{IDTL} = -140 mv
- 900 Mb/s at V_{IDTH} = 140 mv, V_{IDTL} = -140 mv
- 600 Mb/s at V_{IDTH} = 70 mv, V_{IDTL} = -70 mv

Table 7.4. CrossLink Data Sheet Rev. 2.1

General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
Parameter	**Description**	**Conditions**	**–6**		**Unit**
			Min	**Max**	
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	—	UI
		600 Mb/s < Data Rate ≤ 900 Mb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	—	UI
		Data Rate ≤ 600 Mb/s & V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	—	UI
$t_{HD\_GDDRX\_MP}$	Input Data Hold After CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	—	UI
		600 Mb/s < Data Rate ≤ 900 Mb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	—	UI
		Data Rate ≤ 600 Mb/s & V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	—	UI
$f_{MAX\_GDDRX\_MP}$	Frequency for ECLK	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

7.1.5. CrossLink-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for CrossLink-NX device family:

- Max (0.133, 0.133) = 0.20 × UI
- UI = 0.133/0.20 = 0.665 ns
- Max Data Rate = 1/UI = 1/0.665 = 1.5 Gb/s (at 0.20 UI)

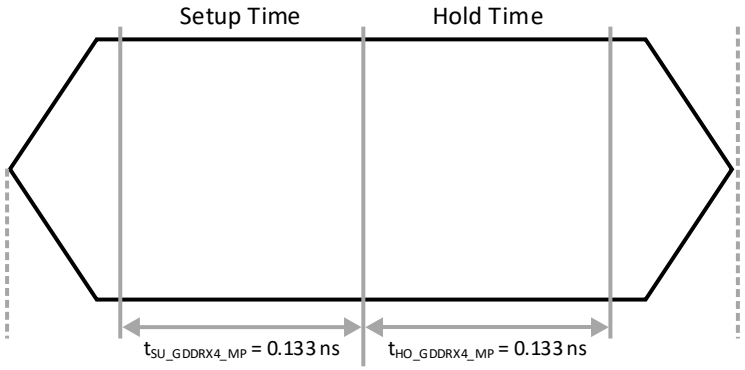

Figure 7.4. CrossLink-NX Soft D-PHY Maximum Data Rate

Table 7.5. CrossLink-NX Data Sheet Rev. 1.9

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input									
Parameter	**Description**	**Device**	**-9**		**-8**		**-7**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.1.6. Certus-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for Certus-NX device family:

- Max (0.133, 0.133) = 0.20 × UI
- UI = 0.133/0.20 = 0.665 ns
- Max Data Rate = 1/UI = 1/0.665 = 1.5 Gb/s (at 0.20 UI)

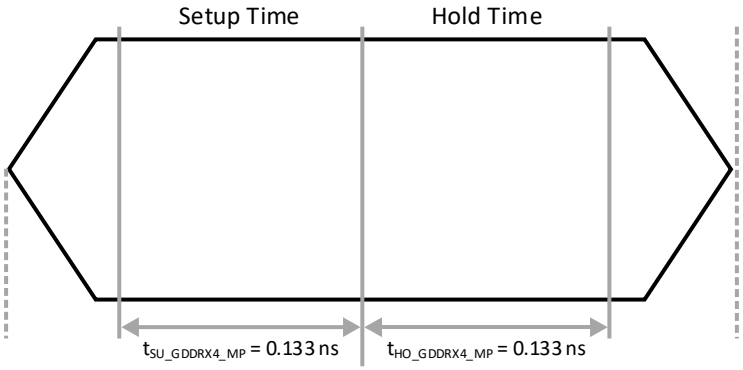

Figure 7.5. Certus-NX Soft D-PHY Maximum Data Rate

Table 7.6. Certus-NX Data Sheet Rev. 1.7

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input									
Parameter	Description	Device	-9		-8		-7		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.1.7. CertusPro-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for CertusPro-NX device family:

- Max (0.133, 0.133) = 0.20 × UI
- UI = 0.133/0.20 = 0.665 ns
- Max Data Rate = 1/UI = 1/0.665 = 1.5 Gb/s (at 0.20 UI)

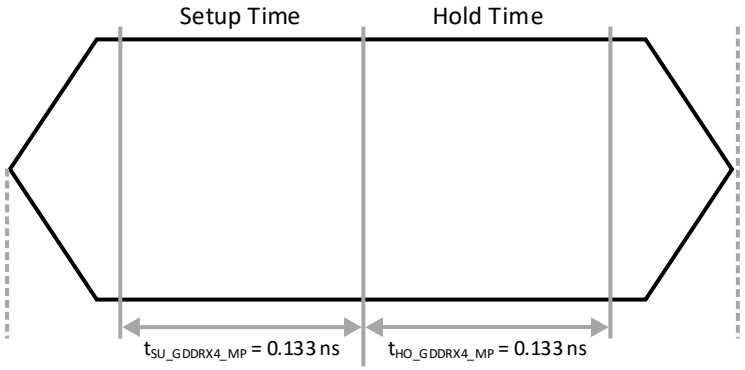

Figure 7.6. CertusPro-NX Soft D-PHY Maximum Data Rate

Table 7.7. CertusPro-NX Data Sheet Rev. 1.5

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input									
Parameter	**Description**	**Device**	**-9**		**-8**		**-7**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.1.8. CrossLink-NX-33 and CrossLinkU-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for CrossLink-NX-33 and CrossLinkU-NX device families:

- Max (0.167, 0.167) = 0.20 × UI
- UI = 0.167/0.20 = 0.835 ns
- Max Data Rate = 1/UI = 1/0.835 = 1.2 Gb/s (at 0.20 UI)

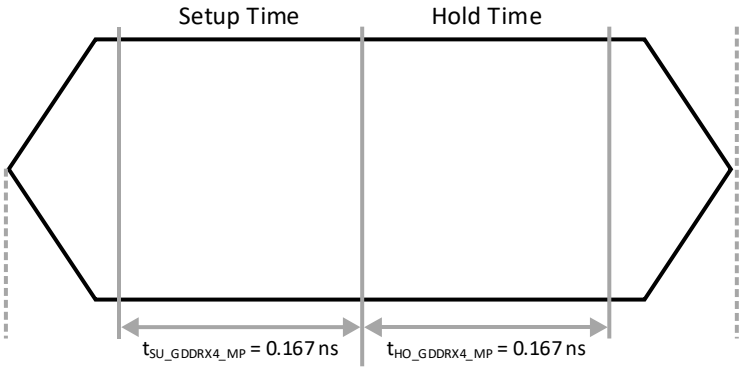

Figure 7.7. CrossLink-NX-33 and CrossLinkU-NX Soft D-PHY Maximum Data Rate

Table 7.8. CrossLink-NX-33 and CrossLinkU-NX Data Sheet Rev. 0.92

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input							
Parameter	Description	Device	-8		-7		Unit
			Min	Max	Min	Max	
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	All Devices	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	All Devices	0.167	—	0.193	—	ns

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.1.9. t_{SU}/t_{HD} Valid Window at Higher Data Rate

For data rates higher than specified above, the t_{SU}/t_{HD} window may exceed the 0.15 UI or 0.20 UI specified in the MIPI Alliance Specification.

To calculate the window, the following equation can be used:

t_{SU}/t_{HD} Window = max(t_{SU}/t_{HD}) / (1 / Data Rate)

For 800 Mb/s, 1 / Data Rate = 1.25 ns.

The maximum data rate each device can support on the receiver is limited to the data rate supported with IDDRX2/X4/X8 with center-aligned data. This is summarized in Table 7.9.

Table 7.9. t_{SU}/t_{HD} Window for Higher Data Rate

Device Family	Soft D-PHY Max Data Rate	t_{SU}/t_{HD} Window
MachXO2	756 Mb/s	0.217 UI
MachXO3L/LF and MachXO3D	900 Mb/s	0.285 UI
LatticeECP3	800 Mb/s	0.257 UI
ECP5	800 Mb/s	0.257 UI
ECP5-5G	800 Mb/s	0.257 UI
CrossLink	1200 Mbps at V_{IDTH} =140 mv, V_{IDTL} = –140 mv	0.20 UI
CrossLink-NX	1500 Mb/s	0.20 UI
Certus-NX	1500 Mb/s	0.20 UI
CertusPro-NX	1500 Mb/s	0.20 UI
CrossLink-NX-33 and CrossLinkU-NX	1200 Mb/s	0.20 UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.2. FPGA Transmitter Interface

7.2.1. MachXO2, MachXO3L/LF, and MachXO3D

Maximum MIPI compliance data rate calculation for MachXO2, MachXO3L/LF, and MachXO3D device families:

- 0.206 = 0.15 × UI
- UI = 0.206/0.15 = 1.373 ns
- Max Data Rate = 1/UI = 1/1.373 = 728 Mb/s (at 0.15 UI)

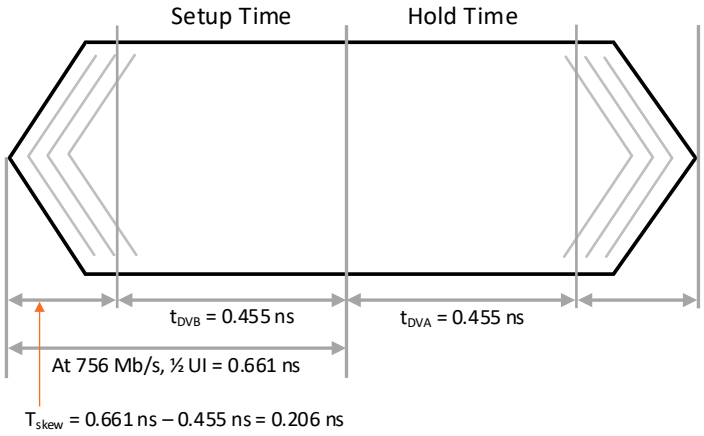

Figure 7.8. MachXO2 Maximum Data Rate

Table 7.10. MachXO2 Data Sheet Rev. 3.3 at 756 Mb/s

Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4TX.ECLK.Centered									
Parameter	Description	Device	–6		–5		–4		Unit
			Min	Max	Min	Max	Min	Max	
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Hold After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mb/s
f_{DDRX4}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	Mhz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	Mhz

7.2.2. LatticeECP3

Maximum MIPI compliance data rate calculation for LatticeECP3 device family:

- 0.215 = 0.15 × UI
- UI = 0.215/0.15 = 1.433 ns
- Max Data Rate = 1/UI = 1/1.433 = 698 Mb/s (at 0.15 UI)

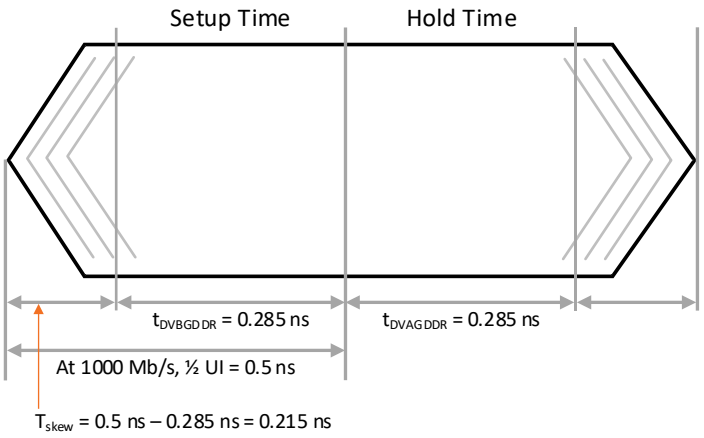

Figure 7.9. LatticeECP3 Maximum Data Rate

Table 7.11. LatticeECP3 Data Sheet Rev.2.8EA at 1000 Mb/s

Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)									
Left and Right Sides									
Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
$t_{DVBGDDR}$	Data Valid Before CLK	All ECP3EA Devices	285	—	370	—	431	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	All ECP3EA Devices	285	—	370	—	432	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz

7.2.3. ECP5/ECP5-5G

Maximum MIPI compliance data rate calculation for ECP5/ECP5-5G device family:

- 0.183 = 0.15 × UI
- UI = 0.183/0.15 = 1.22 ns
- Max Data Rate = 1/UI = 1/1.22 = ~800 Mb/s (at 0.15 UI)

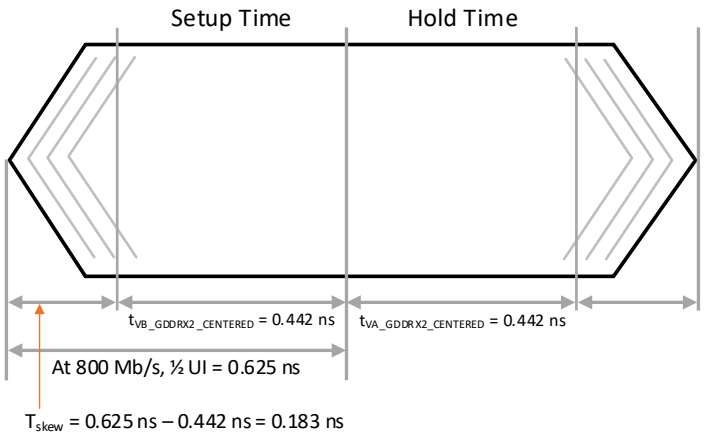

Figure 7.10. ECP5/ECP5-5G Maximum Data Rate

Table 7.12. ECP5/ECP5-5G Data Sheet Rev. 1.9 at 800 Mb/s

Generic DDRX2 Outputs with Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right Sides Only									
Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
$t_{VB\_GDDRX2\_CENTERED}$	Data Output Valid Before CLK Output	All Devices	0.442	—	0.56	—	0.676	—	ns + ½ UI
$t_{VA\_GDDRX2\_CENTERED}$	Data Output Valid After CLK Output	All Devices	—	0.442	—	0.56	—	0.676	ns + ½ UI
$f_{DATA\_GDDRX2\_CENTERED}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_CENTERED}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz

7.2.4. CrossLink-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for CrossLink-NX device family:

- 1500 Mb/s

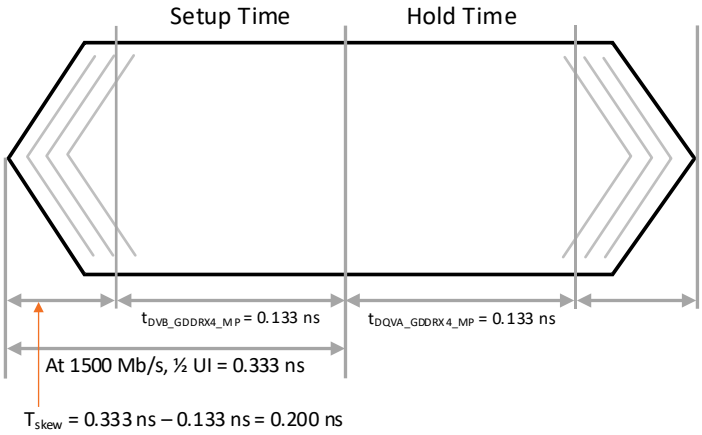

Figure 7.11. CrossLink-NX Soft D-PHY Maximum Data Rate

Table 7.13. CrossLink-NX Data Sheet Rev. 1.9

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input									
Parameter	**Description**	**Device**	**-9**		**-8**		**-7**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.2.5. Certus-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for Certus-NX device family:

- 1500 Mb/s

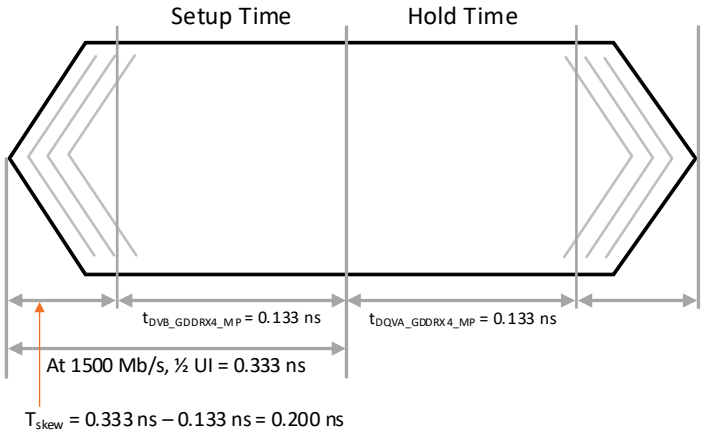

Figure 7.12. Certus-NX Soft D-PHY Maximum Data Rate

Table 7.14. Certus-NX Data Sheet Rev. 1.7

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input									
Parameter	**Description**	**Device**	**-9**		**-8**		**-7**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.2.6. CertusPro-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for CertusPro-NX device family:

- 1500 Mb/s

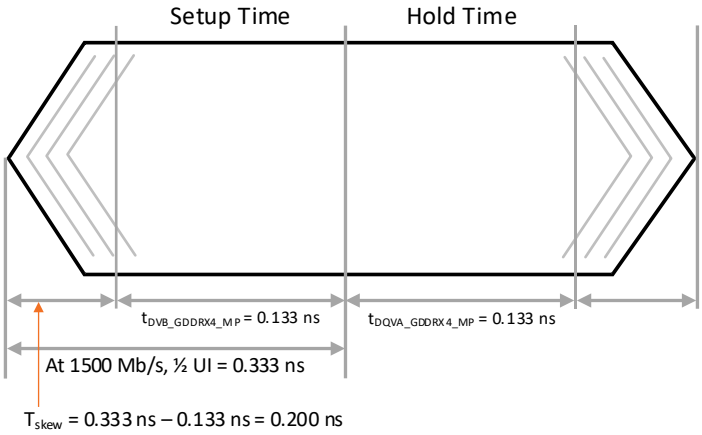

Figure 7.13. CertusPro-NX Soft D-PHY Maximum Data Rate

Table 7.15. CertusPro-NX Data Sheet Rev. 1.5

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input									
Parameter	**Description**	**Device**	**-9**		**-8**		**-7**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	All Devices	0.133	—	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.2.7. CrossLink-NX-33 and CrossLinkU-NX Soft D-PHY

Maximum MIPI compliance data rate calculation for CrossLink-NX-33 and CrossLinkU-NX device families:

- 1200 Mb/s

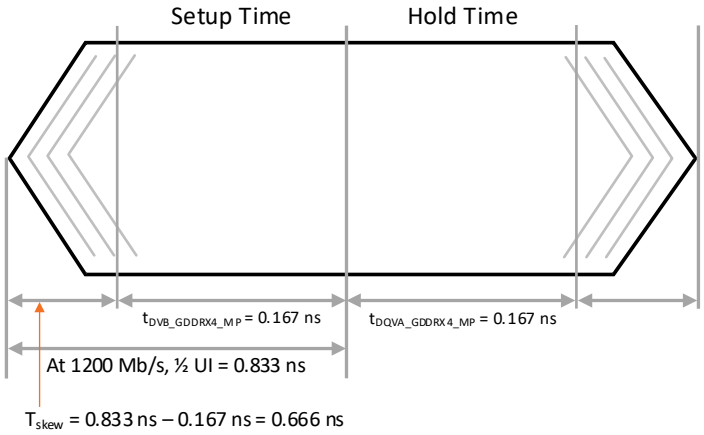

Figure 7.14. CrossLink-NX-33 and CrossLinkU-33 Soft D-PHY Maximum Data Rate

Table 7.16. CrossLink-NX-33 and CrossLinkU-NX Data Sheet Rev. 0.92

Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input							
Parameter	**Description**	**Device**	**-8**		**-7**		**Unit**
			Min	**Max**	**Min**	**Max**	
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	All Devices	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	All Devices	0.167	—	0.193	—	ns
		All Devices	0.20	—	0.20	—	UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.2.8. T_{skew} Window at Higher Data Rate

For data rates higher than specified above, the tskew window may exceed the 0.15 UI or 0.20 UI specified in the MIPI Alliance Specification.

To calculate the window, the following equation can be used:

½ UI = ½ × (1 / Data Rate)

T_{skew} Window = (½ UI – min (tDVA, tDVB)/UI)

For 800 Mb/s, 1 / Data Rate = 1.25 ns.

The maximum data rate each device can support on the transmitter is limited to the data rate supported with ODDRX2/X4/X8 with center-aligned data. This can be summarized in Table 7.17.

Table 7.17. T_{skew} Window for Higher Data Rate

Device Family	Soft D-PHY Max Data Rate	T_{skew} Window
MachXO2	756 Mb/s	0.155 UI
MachXO3L/LF and MachXO3D	900 Mb/s	0.185 UI
LatticeECP3	800 Mb/s	0.172 UI
ECP5	800 Mb/s	≤ 0.150 UI
ECP5-5G	800 Mb/s	≤ 0.150 UI
CrossLink-NX	1500 Mb/s	0.20 UI
Certus-NX	1500 Mb/s	0.20 UI
CertusPro-NX	1500 Mb/s	0.20 UI
CrossLink-NX-33 and CrossLinkU-NX	1200 Mb/s	0.20 UI

Note: Maximum line rate is package/speed grade dependent. See respective data sheets for details.

7.3. MIPI D-PHY Lane Number Selection Matrix Table

Table 7.18 lists some example video formats and the number of MIPI data lanes and line rates needed to support these various video formats. This matrix table selected three common resolutions and the major color depths as examples. The lane number and line rate for other video formats can be calculated using the equations listed in the Bandwidth and Data Rate section.

Table 7.18. MIPI D-PHY Interface Lane Number and Line Rate Selection Example Matrix Table

Resolution	Frame Rate	Pixel Clock	Color Depth	Total Data Rate	Number of Lane = 1		Number of Lanes = 2		Number of Lanes = 3	
					Line Rate	D-PHY Clock	Line Rate	D-PHY Clock	Line Rate	D-PHY Clock
	Hz	MHz	Bits	Mb/s	Mb/s	MHz	Mb/s	MHz	Mb/s	MHz
HD 1280x720p (1650x750)*	60	74.25	8	594.0	594.00	297.00	297.00	148.50	148.50	74.25
			10	742.5	742.50	371.25	371.25	185.625	185.625	92.8125
			12	891.0	891.00	445.50	445.50	222.75	222.75	111.375
			18	1336.5	1336.50	668.25	668.25	334.125	334.125	167.0625
			24	1782.0	1782.00	891.00	891.00	445.50	445.50	222.75
	120	148.5	8	1188.0	1188.00	594.00	594.00	297.00	297.00	148.50
			10	1485.0	1485.00	742.50	742.50	371.25	371.25	185.625
			12	1782.0	1782.00	891.00	891.00	445.50	445.50	222.75
			18	2673.0	2673.00	1336.50	1336.50	668.25	668.25	334.125
			24	3564.0	3564.00	1782.00	1782.00	891.00	891.00	445.50
	240	297	8	2376.0	2376.00	1188.00	1188.00	594.00	594.00	297.00
			10	2970.0	2970.00	1485.00	1485.00	742.50	742.50	371.25
			12	3564.0	3564.00	1782.00	1782.00	891.00	891.00	445.50
			18	5346.0	5346.00	2673.00	2673.00	1336.50	1336.50	668.25
			24	7128.0	7128.00	3564.00	3564.00	1782.00	1782.00	891.00
FHD 1920x1080p (2200x1125)*	60	148.5	8	1188.0	1188.00	594.00	594.00	297.00	297.00	148.50
			10	1485.0	1485.00	742.50	742.50	371.25	371.25	185.625
			12	1782.0	1782.00	891.00	891.00	445.50	445.50	222.75
			18	2673.0	2673.00	1336.50	1336.50	668.25	668.25	334.125
			24	3564.0	3564.00	1782.00	1782.00	891.00	891.00	445.50
	120	297	8	2376.0	2376.00	1188.00	1188.00	594.00	594.00	297.00
			10	2970.0	2970.00	1485.00	1485.00	742.50	742.50	371.25
			12	3564.0	3564.00	1782.00	1782.00	891.00	891.00	445.50
			18	5346.0	5346.00	2673.00	2673.00	1336.50	1336.50	668.25
			24	7128.0	7128.00	3564.00	3564.00	1782.00	1782.00	891.00

Resolution	Frame Rate	Pixel Clock	Color Depth	Total Data Rate	Number of Lane = 1		Number of Lanes = 2		Number of Lanes = 3	
					Line Rate	D-PHY Clock	Line Rate	D-PHY Clock	Line Rate	D-PHY Clock
	Hz	MHz	Bits	Mb/s	Mb/s	MHz	Mb/s	MHz	Mb/s	MHz
UHD 3840x2160p (4400x2250)*	30	297	8	2376.0	2376.00	1188.00	1188.00	594.00	594.00	297.00
			10	2970.0	2970.00	1485.00	1485.00	742.50	742.50	371.25
			12	3564.0	3564.00	1782.00	1782.00	891.00	891.00	445.50
			18	5346.0	5346.00	2673.00	2673.00	1336.50	1336.50	668.25
			24	7128.0	7128.00	3564.00	3564.00	1782.00	1782.00	891.00
	60	594	8	4752.0	4752.00	2376.00	2376.00	1188.00	1188.00	594.00
			10	5940.0	5940.00	2970.00	2970.00	1485.00	1485.00	742.50
			12	7128.0	7128.00	3564.00	3564.00	1782.00	1782.00	891.00
			18	10692.0	10692.00	5346.00	5346.00	2673.00	2673.00	1336.50
			24	14256.0	14256.00	7128.00	7128.00	3564.00	3564.00	1782.00

***Note**: Standard blanking times per CEA-861 Specification.

References

- MIPI D-PHY Reference Design (FPGA-RD-02040)
- CrossLink High-Speed I/O MIPI D-PHY and DDR interfaces (FPGA-TN-02012)
- MachXO2 web page
- MachXO3 web page
- MachXO3D web page
- Lattice ECP3 web page
- ECP5/ECP5-5G web page
- CrossLink web page
- CrossLink-NX web page
- CrossLinkPlus web page
- Certus-NX web page
- CertusPro-NX web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 1.3, May 2024

Section	Change Summary
All	Made editorial fixes.
Disclaimers	Updated boilerplate.
Inclusive Language	Added boilerplate.

Abbreviations in This Document	• Replaced the word *acronyms* to *abbreviations*.
	• Added the following abbreviations:
	  • *Complementary Metal-Oxide Semiconductor (CMOS)*
	  • *Full High Definition (FHD)*
	  • *High Definition (HD)*
	  • *Input/Output (IO)*
	  • *Programmable Input/Output (PIO)*
	  • *Reduced Blanking (RB)*
	  • *Ultra High Definition (UHD)*

Introduction	Added a paragraph on *Soft D-PHY* and *Hardened D-PHY*.
Video Format	Added a table note on *RB* for Table 2.1. Common Video Format.

MIPI CSI-2/DSI Interfaces	• Updated the following items in the paragraphs of this section:
	  • Removed the following sentences:
	  • A sentence on the *application of CMOS sensor bridge*.
	  • A *Note* regarding Figure 3.1 and Figure 3.2.
	  • A reference to the *MIPI D-PHY Interface IP (RD1182)* document.
	  • Added additional descriptions to Figure 3.1, Figure 3.2., Figure 3.3, and Figure 3.4.

Device Selection	• Added details for *CrossLinkPlus*, *CrossLink-NX*, *Certus-NX* and *CertusPro-NX* devices into this section. • Replaced MIPI D-PHY Interface IP (RD1182) with MIPI D-PHY Reference Design (FPGA-RD-02040). • Updated *Notes 2* and *3* for Table 6.1. MIPI D-PHY Rx/Tx Implementation Hardware Comparison for MachXO2, MachXO3L, MachXO3LF, MachXO3D, LatticeECP3, ECP5, ECP5-5G, CrossLink, and CrossLinkPlus Device Families. • Added Table 6.2. MIPI D-PHY Rx/Tx Implementation Hardware Comparison for CrossLink-NX, CrossLink-NX-33, CrossLinkU-NX, Certus-NX, and CertusPro-NX Device Families.

MIPI Data Rate Calculation	• Updated the following items in the paragraphs of the 7. MIPI Data Rate Calculation section:
	  • Added *Programmable I/Os* and *DDRX16*.
	  • Updated the descriptions to *MIPI Alliance Specification for D-PHY*.
	• Updated Figure 7.1 – Figure 7.3 and Figure 7.8 – Figure 7.10.
	• Added Table 7.1 – Table 7.4 and Table 7.10 – Table 7.12.
	• Added table headers for Table 7.1 – Table 7.4 and Table 7.10 – Table 7.12.
	• Updated the *CrossLink Data Sheet Revision* from *1.5* to *2.1* in section 7.1.4. CrossLink Soft D-PHY.
	• Added the following sections and updated the heading numbers of remaining sections accordingly:
	  • 7.1.5. CrossLink-NX Soft D-PHY – 7.1.8. CrossLink-NX-33 and CrossLinkU-NX Soft D-PHY.
	  • 7.2.4. CrossLink-NX Soft D-PHY – 7.2.7. CrossLink-NX-33 and CrossLinkU-NX Soft D-PHY.
	• Updated the following items for sections 7.1.9. tSU/tHD Valid Window at Higher Data Rate and 7.2.8. Tskew Window at Higher Data Rate:
	  • Added the phrase: *or 0.20 UI*.

Section	Change Summary
	• Added information on CrossLink-NX, Certus-NX, CertusPro-NX, CrossLink-NX-33, and CrossLinkU-NX device families. • Added a table note on *maximum line rate*. • Updated Table 7.9. tSU/tHD Window for Higher Data Rate and Table 7.17. Tskew Window for Higher Data Rate. • Updated the paragraph of section 7.3. MIPI D-PHY Lane Number Selection Matrix Table. • Updated Table 7.18. MIPI D-PHY Interface Lane Number and Line Rate Selection Example Matrix Table.
References	• Removed MIPI D-PHY Interface IP (RD1182) from the list of references. • Added the following references: • MIPI D-PHY Reference Design (FPGA-RD-02040) • CrossLink High-Speed I/O MIPI D-PHY and DDR interfaces (FPGA-TN-02012) • MachXO2 web page • MachXO3 web page • MachXO3D web page • Lattice ECP3 web page • ECP5/ECP5-5G web page • CrossLink web page • CrossLink-NX web page • CrossLinkPlus web page • Certus-NX web page • CertusPro-NX web page • Lattice Insights web page
Technical Support Assistance	• Renamed this section from *Technical Support* to *Technical Support Assistance*. • Added *Lattice Answer Database* technical support.

Revision 1.2, May 2019

Section	Change Summary
—	Added Disclaimers section.
Device Selection	Updated Table 6.1. MIPI D-PHY RX/TX Implementation Hardware Comparison. • Specified Soft and hard implementations. • Added CrossLink (Hard) column. • Updated footnotes.
—	Changed instances of *MachXO3L* to *MachXO3L/LF and MachXO3D*.

Revision 1.1, March 2019

Section	Change Summary
All	Changed document title to MIPI D-PHY Bandwidth Matrix and Implementation.
Device Selection	Updated Table 6.1. MIPI D-PHY RX/TX Implementation Hardware Comparison. • Added IMIPI information for ECP5/ECP5-5G. • Updated information in the Number of Lanes row.
Back cover	Updated template.

Revision 1.0, November 2018

Section	Change Summary

All	Initial release.
	Note: Contents of this technical note were migrated from FPGA-UG-02041 (previously UG110). Publication of FPGA-UG-02041 user guide will be discontinued.
	
	Below are the changes from the previous FPGA-UG-02041 release (version 1.1).
	• Updated Table 6.1. MIPI D-PHY RX/TX Implementation Hardware Comparison.
	  • Changed the RX Performance value for CrossLink.
	  • Changed the TX Performance value for ECP5/ECP5-5G.
	• Corrected statement in MIPI Data Rate Calculation section to “The window for higher data rate does not meet MIPI Alliance Specification, but can still be practical in the user’s implementation.”
	• Corrected value in Figure 7.5. MachXO2 Maximum Data Rate to Tskew = 0.661 - 0.455 = 0.206.
	• Updated the ECP5/ECP5-5G section.
	  • Corrected value from 820 to 800 in Max Data Rate = 1/UI = 1/1.22 = ~800 Mbps (at 0.15 UI).
	  • In Figure 7.7. ECP5/ECP5-5G Maximum Data Rate, changed tSU_GDDRX2_centered to tVB_GDDRX2_centered and tHD_GDDRX2_centered to tVA_GDDRX2_centered.
	• Changed header value in Table 7.3. MIPI D-PHY Interface Lane Number and Line Rate Selection Example Matrix Table to CrossLink (900 Mbps for RX and 1250 Mbps for TX I/O)

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