SPI Slave to PWM Generation – iCE40 UltraPlus

Reference Design

FPGA-RD-02049 Version 1.0

September 2018

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CPOL	Positive clock polarity
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
LED	Light Emitting Diode
PWM	Pulse-width modulation
SPI	Serial Peripheral Interface

1. Introduction

Pulse-width modulation (PWM) uses a rectangular pulse wave whose pulse width is modulated resulting in the variation of the average value of the waveform. Every PWM signal is a continuous succession of high and low pulses. The length of each pulse is defined by the desired duty cycle and frequency.

In mobile phones and other consumer electronic products, the Light Emitting Diode (LED) is increasingly being used as a display backlight. PWM offers an ideal solution for LED controllers as the dimming intensity of the LED can be controlled by changing duty cycle and frequency of the pulse.

This design provides a bridge between a microprocessor and a PWM generator. The SPI slave interface is used to receive data from an external SPI master. The data are used to set the frequency and duty cycle of the PWM.

A typical application of this design includes interfacing a SPI compliant on-board microprocessor and a LED device. This design can also be used as a reference to generate PWM for analog dimming.

2. Reference Design Overview

2.1. Block Diagram

Figure 2.1 shows the block diagram of the SPI Slave to PWM Generation reference design.

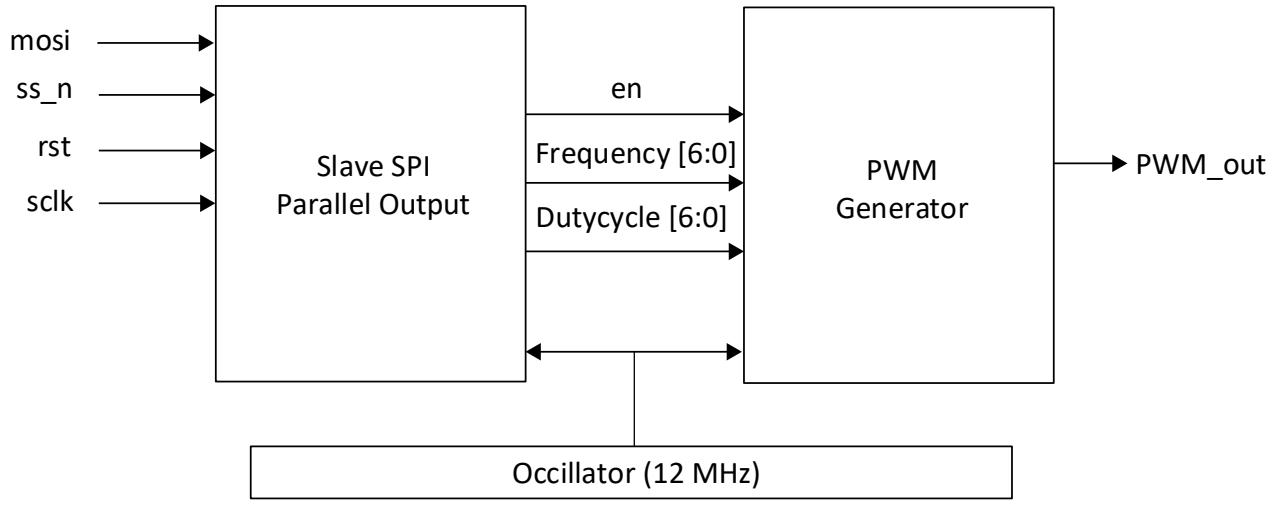

Figure 2.1. Top-Level Block Diagram

2.2. Features

This design provides a bridge between the microprocessor and PWM generator via a SPI slave interface. The features include:

- Programmable frequency varying from 1 kHz to 100 kHz with 1 kHz increment
- Programmable duty cycle varying from 1% to 100% with 1% increment
- Internal oscillator to generate 12 MHz clock signal

3. Functional Description

In this SPI to PWM module there are two major blocks. The SPI Slave Parallel Output and Pulse-Width Modulator modules.

The SPI Slave Parallel Output module is used to capture the SPI input from an external SPI Master. In this case, the FPGA acts as a Slave SPI and receives the frequency and duty cycle of the PWM signals.

The PWM Generator module calculates the frequency and duty cycle counts relative to the system clock at 12 MHz. The module generates 120 frequency counts and 60 duty cycle counts when the input frequency and duty cycle are 100 kHz and 50%, respectively. This determines how much counts the pulse is high and low in a period.

Table 3.1 provides examples of binary representations of frequencies and their corresponding duty cycles.

Table 3.1. Frequency and Duty Cycle

Frequency [6:0]		Duty Cycle [6:0]	
25 kHz	7'b0011001	75%	7'b1001011
50 kHz	7'b0110010	25%	7'b0011001
75 kHz	7'b1001011	50%	7'b0110010
100 kHz	7'b1100100	90%	7'b1011010

In addition, internal oscillator is set to 12 MHz output, which is used to provide the system clock of the two major blocks.

Table 3.2 lists the I/O ports of the design.

Table 3.2. Pin Descriptions

Signal	Width	Type	Description
SPI Interface			
sclk	1	Input	Serial clock
mosi	1	Input	Serial data in
miso	1	Output	Serial data out
ss_n	1	Input	Slave select
PWM Generator Interface			
PWM_out	PWM_out	PWM_out	PWM_out
Reset	Reset	Reset	Reset

4. Design Description

The design has two (2) major blocks as shown in Figure 2.1. These modules include logic for SPI Slave and Pulse Width Modulator (PWM). The SPI slave sclk operates at 3 MHz and positive clock polarity (CPOL). It converts serial data to parallel. The PWM is running at 12 MHz system clock and receives data from SPI Slave and calculates counts for frequency and duty cycle relative to the system clock.

5. SPI Command Format

An external Master SPI needs to send the 8-bit duty-cycle data followed by the 8-bit frequency data. The least significant bit is not used and is discarded in the design.

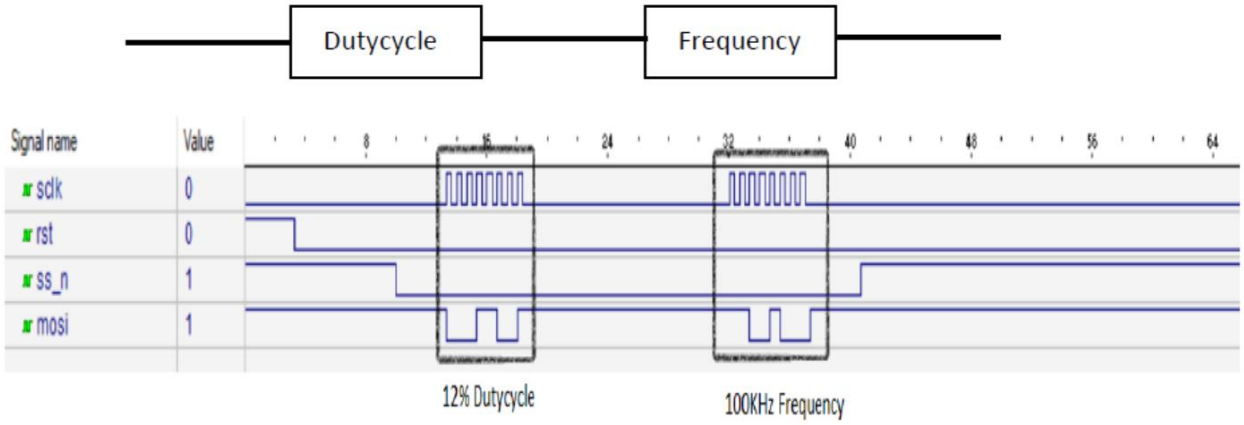

Figure 5.1. SPI Command Format

6. HDL Simulation and Verification

The SPI slave based PWM controller design is simulated using a standard SPI master model.

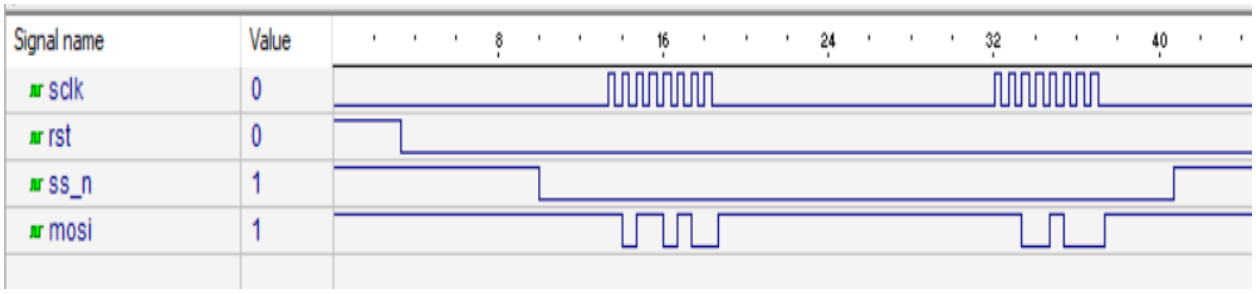

Figure 6.1. Emulated Master SPI (Aardvark) Data Transmission

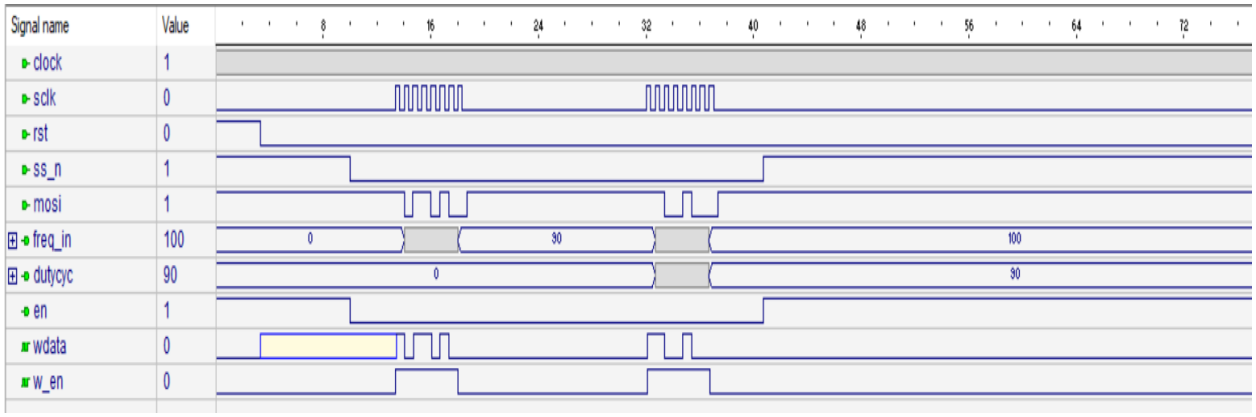

Figure 6.2. Slave SPI Parallel Output (100 kHz Frequency, 90% Duty-Cycle)

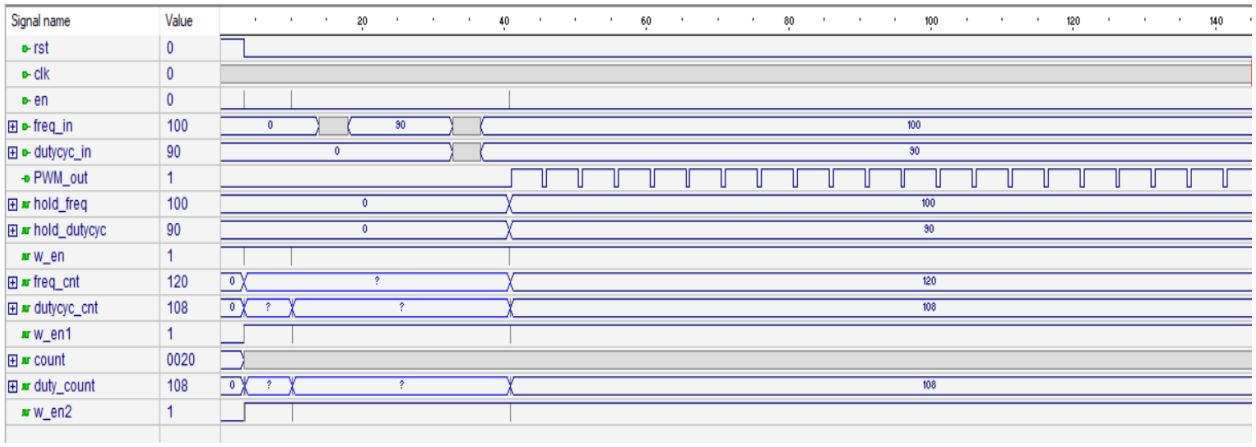

Figure 6.3. PWM Generator

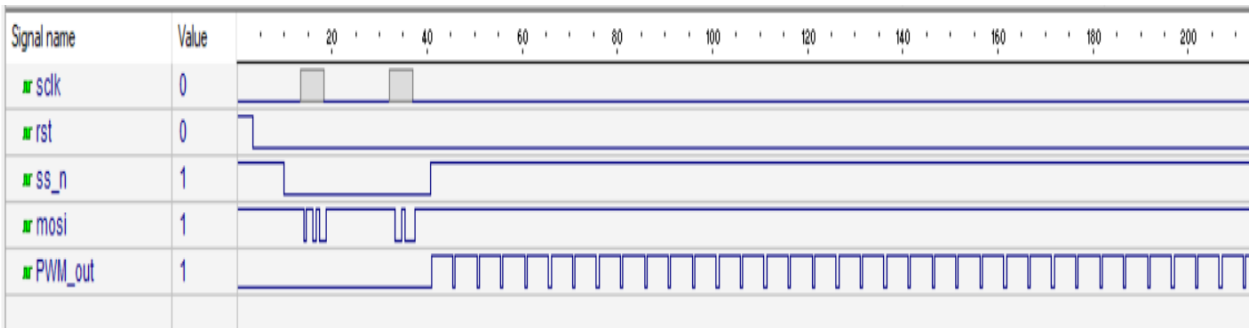

Figure 6.4. SPI to PWM 100 kHz frequency and 90% Duty-Cycle

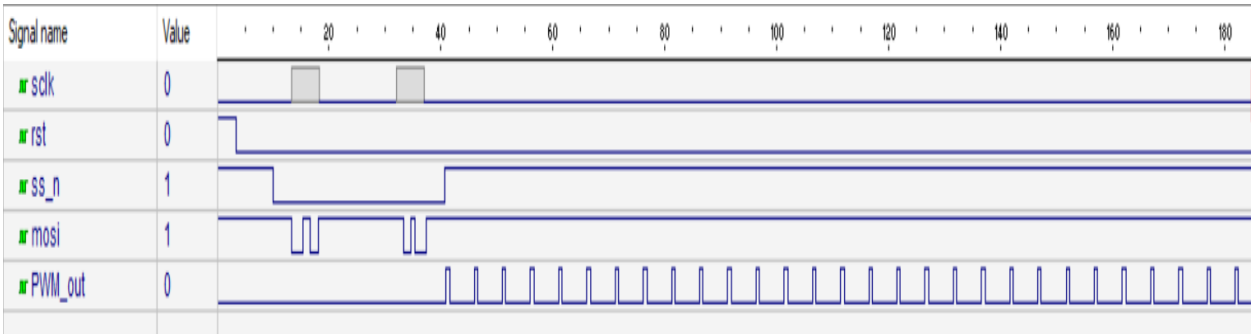

Figure 6.5. 100 kHz frequency and 25% duty-cycle

7. Implementation

This design is implemented in Verilog. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

Table 7.1. Performance and Resource Utilization*

Family	Language	Utilization	Operating Frequency	I/O
iCE40UP5K	Verilog	2124	12 MHz	5

***Note**: Performance and utilization characteristics are generated iCE40UP5k, with Radiant™ 1.0 design software.

References

- iCE40 UltraPlus FPGA
- iCE40 UltraPlus Development Kits and Boards

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, September 2018

Section	Change Summary
All	Initial release.

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