Lattice Radiant Software 1.0 Service Pack 1 Release Notes

Welcome to Lattice Radiant™ software, the new and complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs). Radiant software offers leading-edge design and implementation tools optimized for cost-sensitive and low-power Lattice FPGA architectures.

Radiant software is available for both the Windows and Linux operating systems, and provides key features to make designing for Lattice Semiconductor programmable devices easier than ever, and improves your time to market. Some of the key benefits include:

- **Design Exploration:** Explores design alternatives with Implementations and Strategies.
- **Ease-of-Use Features:** Introduces next generation and simple user interface, with intuitive message filtering, and cross-probing for effective debugging.
- **Improved Design Flow:** Utilizes standard Synopsys Design Constraints SDC format for constraint flow, integrates Timing Analysis for rapid timing closure, and provides Tcl scripting support for automation.

Lattice Semiconductor offers a rich variety of information sources, including a Help system, PDF user manuals, tutorials, and online discussions. The easiest way to access any of them is through Radiant software online Help.

You can also find extensive information about Radiant software and its capabilities, tools, and workflow on the Lattice Semiconductor website at: www.latticesemi.com.

Service Pack 1 Updates

- **If users uses the LVDSE IO type in their design, please re-compile with this service pack.**
- **If CCU2 primitives are indicated in the Area Report of the LSE synthesis report file, there is a chance of getting an incorrect synthesis result from carry chain optimizations. It is advised to re-compile the design using this service pack to avoid a simulation and/or hardware operation failure. This fix is applicable for LSE only.**
- **Fixed several other key customer defects resolving instability relating to map, place and route in the timing engine.**

Key Features in Radiant software

- **Standardized Timing and Physical Constraints utilizing the popular SDC format to help you easily apply constraints to your designs.**
- **Unified Static Timing Analysis from Synthesis to Place & Route to accelerate design timing closure.**
- **Enhanced IP Security Flow and Ecosystem to allow efficient distribution of Soft IP's and to improve 3rd Party Soft IP security.**
- **New and Simplified GUI design with option of light or dark color theme.**
- **Simplified and Efficient Design Flows and Tools to improve Ease-of-Use.**

Device Support

The following device family is supported in Radiant software.

Device Family	Free License
iCE40 UltraPlus	Yes

Help Resources

Available information resources for the Radiant software include the following:

- User Guides
  - Lattice Radiant Software User Guide
    This document provides an overview of the Radiant software features.
  - Reveal Troubleshooting Guide for Lattice Radiant Software
    This document provides Reveal restrictions on Radiant software.
- Online Help
  - Lattice Radiant Software Online Help: Start Lattice Radiant software and select "Getting Started" icon under Information Center.

- Lattice Radiant Software 1.0 Help (PDF version)
  This is a PDF version for the Radiant software Online Help.

- Tutorial
  - Lattice Radiant Software Tutorial
    This document provides a tutorial for Radiant software.

- Installation
  - Lattice Radiant Software 1.0 Installation Guide for Windows
    This document provides installation instructions for Windows OS.
  - Lattice Radiant Software 1.0 Installation Guide for Linux
    This document provides installation instructions for Linux OS.

- Lattice website
  - General Information: General information on Radiant software can be found on the Lattice Web site:
    http://www.latticesemi.com/latticeradiant

Help for Lattice Diamond users

If you are a current Lattice Diamond software user, a tool and documentation exist that will help you quickly understand Radiant software features and concepts.

- Import Diamond project – This tool allows you to quickly and easily import your Diamond software project into Radiant software. For more information, refer to Radiant software online Help **User Guides > Managing Projects > Importing Lattice Diamond Projects**.

- Lattice Radiant Software Guide for Lattice Diamond Users
  This document provides information to help Lattice Diamond users quickly grasp the features and concepts of Radiant software, as well as understand the differences between Radiant and Diamond software.

Help for migrating iCEcube2 designs to Radiant software

The following reference documents will help you migrate your iCEcube2 designs to Radiant software.

- Migrating iCEcube2 iCE40 UltraPlus Designs to Lattice Radiant Software
  This document provides information to help iCEcube2 users migrate iCE40 UltraPlus designs into Radiant software.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel Pentium or Pentium-compatible PC
- 64-bit OS:
  - Windows 7, Windows 8 and 8.1, or Windows 10
  - Red Hat Enterprise Linux 6.6 or 7
- Approximately 2 GB free disk space
- Computer Memory Requirement: 2 GB Minimum, 3GB Recommended
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Microsoft Internet Explorer 8 or higher (required for Aldec Active-HDL Lattice Edition simulator)
- Acrobat Reader 5.0 or later

Support for Third-Party Synthesis and Simulator Tools

In addition to the Synopsys Synplify Pro® for Lattice and Aldec Active-HDL™ Lattice Edition tools included with Radiant software suite, the following 3rd-Party Synthesis and Simulator tools are supported by Radiant software:

- **Synthesis Tools**
  - Synopsys Synplify Pro FPGA synthesis software
    (contact Lattice Technical Support for supported version)
- **Simulator Tools**
  - Aldec Active-HDL v10.4 or later
  - Aldec Riviera-PRO™ v2016.02 or later
  - Mentor Questa® Sim v10.4g or later
    v10.6b or later

Known Issues

The following are known Issues and workarounds for the Radiant software 1.0 release.

Radiant software Main Window

Radiant software Main Window stops working on Windows 10 when Dell Backup and Recovery software is installed.

When Dell Backup and Recovery software is installed, it conflicts with Radiant software, and may cause it to stop working.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-2303
Workaround: Uninstall Dell Backup and recovery software

Lattice Synthesis Engine (LSE)

The DSP implementation feature using DSP blocks or LUT implementation may not work when the HDL attributes are specified on wires of the multiplier output registers.

If you specified attribute “synthesis syn_multstyle = "block_mult | logic” on the wires of the multiplier output registers, the attributes may not work.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-1653
Workaround: Use one of the following solutions:

1. Set the option globally via the LSE Strategy option “DSP style = DSP or Logic”.
2. Set the HDL attribute “synthesis syn_multstyle = "block_mult | logic" on the multiplier instance.

LOC attribute does not work when assignment values are not specified completely for registered bus.

For example,

```
reg     [3:0]     A_reg /* synthesis  LOC = "R8C7D" */
```

Register A_reg is 4 bits wide but user specifies only 1 location value R8C7D. LSE ignores this attribute since it is incomplete.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-2767
Workaround: Use “ldc_set_location” constraint in .pdc file to set location constraints for registers

The *syn_useioff* attribute does not work for LSE.

This attribute controls selective register to be pack into I/O pad cell based on timing requirements. LSE "Use IO Registers" Strategy option is set to Auto to use IO registers whenever applicable. Those IO register inferences cannot be individually prevented by the user HDL attribute “syn_useioff = 0”.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-3382
Workarounds (2 options):

1. Use the global option "Use IO Registers = False" in Strategy Manager if the design permits, in which LSE will not pack any register into I/O pad cell unless instantiated.
2. Use Synplify Pro for Lattice synthesis tool

Synplify Pro for Lattice Synthesis

For designs with multiple assignments to same parameter, Synplify Pro synthesis will pick up the first assignment without any warning message. Users may get unexpected results.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-2077
Workaround: Remove any unused assignments and keep the ones with the expected value.

LOC attribute does not work for locating registers for Synplify Pro synthesis.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-2767
Workaround: Use “ldc_set_location” constraint in .pdc file to set location constraints for registers

Floorplan View

When using the left mouse button to zoom while objects are selected, the selected objects will be lost.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-3231
Workaround: If there are objects selected, zoom using the wheel mouse button or keys Ctrl + and Ctrl – keys. .

Timing Constraint Editor

It is not possible to drag and drop objects from RTL view into the Timing Constraint Editor while in Detach mode on certain computers.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-2728
Workaround: If you run into this issue, use “Attach” mode to drag and drop objects from RTL view into the Timing Constraint Editor.

Place & Route (PAR)

Some designs may encounter long run times.

Versions affected: 1.0
Devices affected: All
DNG-3007
Workaround: Turn off the Place & Route Design Strategy “Path-based Placement” option.

Timing Analysis

If there are overlapping set_clock_uncertainty constraints, the most constraining one will be honored by the Timing engine.

Here is an example of the issue:

```
set_clock_uncertainty 1.33 -from [get_clocks myclk1] -to [get_clocks myclk2] -setup

set_clock_uncertainty 3.0 [get_clocks myclk2] -setup
```

In the case above, 3.0 will be applied as the constraint.

Versions affected: 1.0
Devices affected: All
Bug number: DNG-2761
Workaround: None. This limitation will be reviewed and addressed in future version.

Programmer

Programmer software may not work properly if you open two or more Radiant software projects at the same time.

When two Radiant software projects are opened at the same time with only one using the imported .xcf file, the Programmer software may not operate properly. Clicking on the Programmer icon for the first

project opens the .xcf file. If you subsequently click on the programmer icon of the second project, the Programmer will close the first .xcf file and open the second. The second .xcf file will be empty and Programmer will show an error message.

Versions affected: 1.0
Devices affected: All
DNG-2915
Workaround: If you need two Radiant software projects opened at the same time, close the first Radiant software project before clicking on the programmer icon of the second project.

Contacting Technical Support

FAQs

The first place to look. The Answer Database on the Lattice Semiconductor Web site provides solutions to questions that many of our customers have already asked. Lattice Applications Engineers are continuously adding to the Database.

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

For Local Support

Contact your nearest Lattice Sales Office.