SGMII and Gb Ethernet PCS IP

IP Version: v1.7.1

User Guide

FPGA-IPUG-02077-2.0

December 2024

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CDR	Clock Data Recovery
CSR	Control and Status Register
CTC	Clock Tolerance Compensation
DDR	Double Data Rate
FIFO	First In First Out
FSM	Finite State Machine
GDDR	Generic Double Data Rate
GMII	Gigabit Media Independent Interface
GPLL	Generic Phase-Locked Loop
GUI	Graphical User Interface
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Controllers
MII	Media Independent Interface
MDIO	Management Data Input/Output
PCS	Physical Coding Sublayer
PHY	Physical Layer Devices
PLL	Phase-Locked Loop
QFN	Quad Flat No-Leads
RTL	Register Transfer Language
SERDES	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
TSMAC	Tri-Speed MAC
WLCSP	Wafer-Level Chip Scale Packaging

1. Introduction

The Serial Gigabit Media Independent Interface (SGMII) connects the Ethernet Media Access Controllers (MACs) and Physical Layer Devices (PHYs). This intellectual property (IP) core may be used in bridging applications and/or PHY implementations. It is widely used as an interface for a discrete Ethernet PHY chip.

1.1. Quick Facts

The following table shows the summary of the SGMII IP.

Table 1.1. Summary of the SGMII and Gb Ethernet PCS IP

IP Requirements	Supported FPGA Families	Lattice Avant™, Certus™-N2, MachXO5™-NX[1], CrossLink™-NX[1, 2], CertusPro™-NX[1], and Certus™-NX[1] Notes: 1. All Nexus™ (NX) devices require speed grade 9. 2. This IP is not supported on CrossLink-NX devices with the 72 WLCSP and 72 QFN packages.
	IP Changes	For a list of changes to the IP, refer to the SGMII and Gb Ethernet PCS IP Release Notes (FPGA-RN-02035).
Resource Utilization	Targeted Devices	LAV-AT-X70, LAV-AT-G70, LAV-AT-E70, LAV-AT-E30, LFMXO5-25, LFMXO5-55T, LFMXO5-100T, LIFCL-40, LIFCL-17, LFCPNX-100, LFD2NX-40, LFD2NX-28, LFD2NX-17, LN2-CT-20
	Supported User Interface	(G)MII
	Resources	See Table A.1. Resource Utilization.
Design Tool Support	Lattice Implementation	IP core v1.0.0 – Lattice Radiant™ software 2.1 IP core v1.1.0 – Lattice Radiant software 2.2 and Lattice Propel™ Builder software 2.0 IP core v1.2.0 – Lattice Radiant software 3.0 and Lattice Propel Builder software 2.0 IP core v.1.4.0 – Lattice Radiant software 3.2 IP core v1.5.2 – Lattice Radiant software 2023.2 IP core v1.6.2 – Lattice Radiant software 2024.1 IP core v1.7.1 – Lattice Radiant software 2024.2 or later
	Synthesis	Synopsys® Synplify Pro for Lattice.
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. IP Support Summary

The following table provides IP support information on the SGMII Gb Ethernet PCS IP core.

Table 1.2. SGMII Gb Ethernet PCS IP Core Support Readiness

Device Family	Radiant Timing Model	Hardware Validated
Lattice Avant	Preliminary	Yes
Certus-N2	Preliminary	No
MachXO5-NX, CrossLink-NX, CertusPro-NX, and Certus-NX	Final	Yes

1.3. Features

The following lists the key features of the SGMII IP:

- Physical Coding Sublayer (PCS) functions of the Cisco SGMII Specification, Revision 1.8
- PCS functions for IEEE 802.3z (1000BASE-X)
- Dynamic selection of SGMII/1000BASE-X PCS operation
- Support for MAC or PHY mode for SGMII auto-negotiation
- Support for (G)MII data rates of 1 Gbps, 10 Mbps, and 100 Mbps
- Easy Connect option for seamless integration with the Lattice Semiconductor Tri-Speed MAC (TSMAC) IP core
- Management Interface Port for control and maintenance

1.4. Conventions

1.4.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.4.2. Signal Names

Signal names that end with:

- _*n* are active low signals (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

1.4.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The SGMII/Gb Ethernet PCS IP core converts GMII frames into 8-bit code groups in both transmit and receive directions and performs auto-negotiation with a link partner as described in the Cisco SGMII and IEEE 802.3z specifications. The SGMII IP is a connection bus for MACs and PHYs and is often used in bridging applications and/or PHY implementations. It is widely used as an interface for a discrete Ethernet PHY chip.

The following figure shows the top-level block diagram of the SGMII IP core.

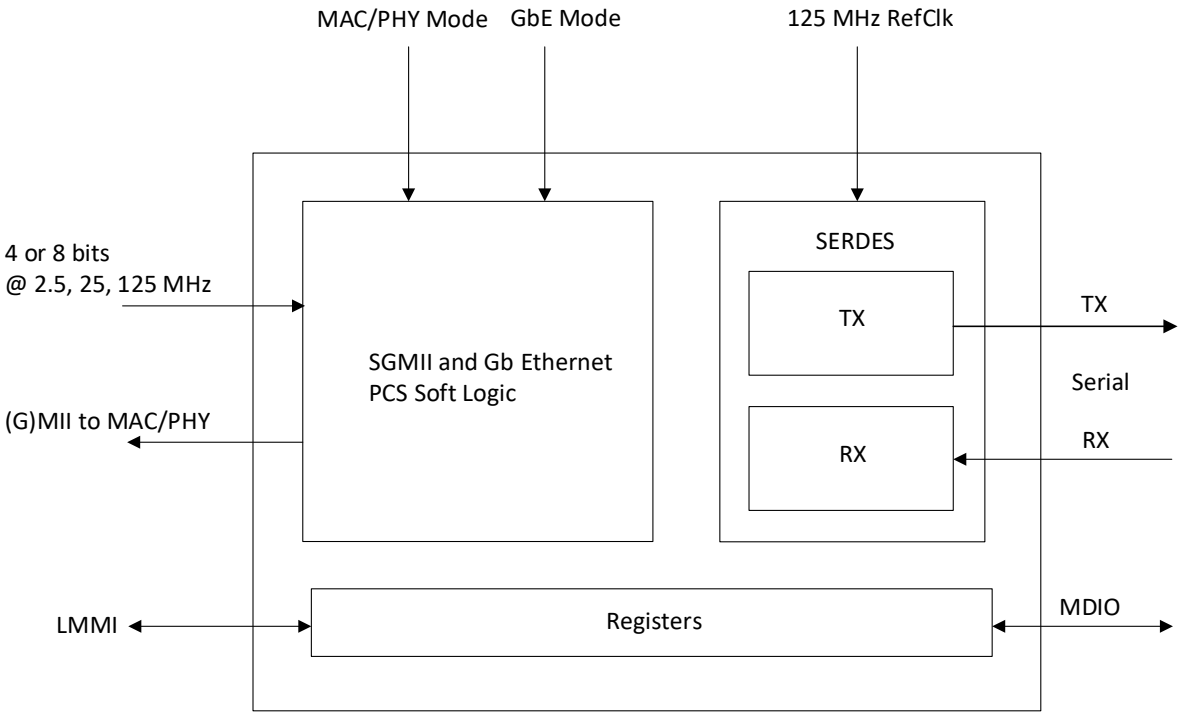

Figure 2.1. SGMII/Gb Ethernet PCS IP Top-Level Block Diagram

2.2. Signal Description

Table 2.1. SGMII IP Core Signal Description

Port Name	I/O	Width	Description
Clock and Reset			
tx_clk_mii_i	In	1	Transmit MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for incoming (G)MII transmit data. Data is sampled on the rising edge of this clock. For *TSMAC Easy Connect* option, this clock is always 125 MHz.
tx_clock_enable_source_o[1]	Out	1	Transmit Clock Enable Source – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. The signal is generated by the transmit rate adaptation block. This clock enable should be tied to the transmit section of the MAC that sends transmit Ethernet frames to the SGMII and Gb Ethernet PCS IP core. This clock enable should also be tied to the clock enable sink of the SGMII and Gb Ethernet PCS IP core. This clock enable's behavior is controlled by the setting of the operational rate pins - operational_rate_i, of the IP core. For 1 Gbps operation, the clock enable is constantly high. For 100 Mbps operation, the clock enable is high for one-out-of-ten 125 MHz clock cycles. For 10 Mbps operation, the clock enable is high for one-out-of-one-hundred 125 MHz clock cycles.[1]
tx_clock_enable_sink_i[1]	In	1	Transmit Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. When the clock enable is high and the transmit clock edge rises, (G)MII data is sampled.[1]
rx_clk_mii_i	In	1	Receive MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for outgoing (G)MII receive data. Data is launched on the rising edge of this clock. *For TSMAC Easy Connect* option, this clock is always 125 MHz.
rx_clock_enable_source_o[2]	Out	1	Receive Clock Enable Source – This signal is similar to the tx_clock_enable_source_o described above, except that it is used for the receive data path. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.
rx_clock_enable_sink_i[2]	In	1	Receive Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the receive 125 MHz clock to regulate the flow of receive (G)MII data. When the clock enable is high and the receive clock edge rises, (G)MII data is launched.
rst_n_i	In	1	Reset – Active low global reset.
cdr_refclk_i	In	1	CDR Reference Clock – 125 MHz user-provided CDR reference clock input. Note that this signal is only available for non-Avant devices and *if Enable Port: CDR Reference clock* is enabled. This input clock should be coming from Generic PLL of the device.
clk_125m_pll_i	In	1	125 MHz PLL Clock – 125 MHz clock input. Note that this signal is only available if *Use External PLL* is enabled in the GUI. The *Use External PLL* option is not available for Avant devices.
clk_625m_pll_i	In	1	625 MHz PLL Clock – 625 MHz clock input. Note that this signal is only available if *Use External PLL* is enabled in the GUI. The *Use External PLL* option is not available for Avant devices.
clk_625m_90_pll_i	In	1	90-degree Phase Shift 625 MHz PLL Clock – 625 MHz clock input with 90-degree phase shift. Note that this signal is only available if *Use External PLL* is enabled in the GUI. The *Use External PLL* option is not available for Avant devices.
pll_refclk_i	In	1	PLL Reference Clock – 250 MHz clock input for Avant devices and 125 MHz clock input for non-Avant devices. Data is sampled on the rising edge of this clock. Note that this signal is only available if *Use External PLL* is disabled in the GUI.

Port Name	I/O	Width	Description
clk_125m_pll_o	Out	1	125 MHz PLL primary output clock – Note that this signal is only available if Enable Port: CDR Reference clock is enabled in GUI or if *Use External PLL* is disabled in the GUI. The *Use External PLL* option is not available for Avant devices.
usr_clk_o	Out	1	User Clock – 125 MHz clock from ECLKDIV output. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.
clk_gddr_o	Out	1	DDR Clock – assumes an LVDS buffer.
lmmi_clk_i	In	1	LMMI clock—The typical recommended frequency is 125 MHz, depending on the fabric clock.
mdc_i	In	1	Management Data Clock – Clock source for the serial management interface. The IEEE 802.3 specification (clause 22) dictates that the maximum frequency for this clock is 2.5 MHz. Note that this signal is only present when the IP core Register Access is in *MDIO* option.
eclk_oddr_o	Out	1	Edge Clock—625 MHz clock from DDR output. It is a CDR clock. This clock signal is for CDR debug purpose. Note: This signal is only available for Avant devices.
sclk_oddr_o	Out	1	Primary System Clock—125 MHz clock from DDR output. It is a divided CDR clock. This clock signal is for CDR debug purpose. Note: This signal is only available for Avant devices.
GMII			
tx_d_i	In	8	Transmit Data – Incoming (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of tx_d_i are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of tx_d_i are valid. For the *TSMAC Easy Connect* mode all 8 bits of tx_d_i are valid for all (G)MII data rates (1 Gbps, 10 Mbps, 100 Mbps).
tx_en_i	In	1	Transmit Enable – Active high signal; asserts when incoming data is valid.
tx_er_i	In	1	Transmit Error – Active high signal used to denote transmission errors and carrier extension on incoming (G)MII data port.
rx_d_o	Out	8	Receive Data – Outgoing (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of rx_d_o are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of rx_d_o is valid. For the *TSMAC Easy Connect* mode, all 8 bits of rx_d_o is valid for all (G)MII data rates (1 Gbps, 10 Mbps, 100 Mbps).
rx_dv_o	Out	1	Receive Data Valid – Active high signal, asserts when outgoing data is valid.
rx_er_o	Out	1	Receive Error—Active high signal used to denote transmission errors and carrier extension on outgoing (G)MII data port.
col_o	Out	1	Collision Detect—Active high signal, asserts when tx_en_i and rx_dv_o is active at the same time.
crs_o	Out	1	Carrier Sense Detect – Active high signal, asserts when rx_dv_o is high.
Management			
mr_adv_ability_i[3]	In	16	Advertised Ability—Configuration status transmitted by PCS during auto-negotiation process. This signal must not change during auto-negotiation.
mr_an_enable_i[3]	In	1	Auto-Negotiation Enable—Active high signal that enables auto-negotiation state machine to function. This signal must not change during auto-negotiation.
mr_main_reset_i[3]	In	1	Main Reset—Active high signal that forces all PCS state machines to reset.
mr_restart_an_i[3]	In	1	Auto-Negotiation Restart—Active high signal that forces auto-negotiation process to restart.
mr_an_complete_o	Out	1	Auto-Negotiation Complete—Active high signal that indicates that the auto-negotiation process is completed.

Port Name	I/O	Width	Description
mr_lp_adv_ability_o	Out	16	Link Partner Advertised Ability—Configuration status received from partner PCS entity during the auto-negotiation process. The bit definitions are the same as described above for the mr_adv_ability_i port.
mr_page_rx_o	Out	1	Auto-Negotiation Page Received—Active high signal that asserts while the auto-negotiation state machine is in the *Complete_Acknowledge* state.
force_isolate_i[3]	In	1	Force PCS Isolate—Active high signal that isolates the PCS. When asserted, the RX direction forces the (G)MII port to all zeros, regardless of the condition of the incoming 1.25 Gbps serial data stream. In the TX direction, the condition of the incoming (G)MII port is ignored. The TX PCS behaves as though the (G)MII TX input port was forced to all zeros. Note, however, that the isolate function does not produce any electrical isolation – such as tri-stating of the (G)MII RX outputs of the IP core. When the signal is de-asserted (low), the PCS isolation functions are deactivated. The use of this signal is optional. If the user chooses not to use the isolate function, then this signal should be tied low.
force_loopback_i[3]	In	1	Force PCS Loopback—Active high signal that activates the PCS loopback function. When asserted, the 10-bit code-group output of the transmit state machine is looped back to the 10-bit code-group input of the receive state machine. When de-asserted, the loopback function is deactivated. The use of this signal is optional. If the user chooses not to use the loopback function, then this signal should be tied low.
force_unidir_i[3]	In	1	Force PCS Unidirectional Mode—Active high signal that activates the PCS unidirectional mode. When asserted, the transmit state machine path between the TX (G)MII input and the TX 10-bit code-group output remain operational, regardless of what happens on the RX data path. (Normally RX loss of sync, invalid code-group reception, auto-negotiation restarts can force the transmit state machine to temporarily ignore inputs from the TX (G)MII port). When de-asserted, the unidirectional mode is deactivated. The use of this signal is optional. If the user chooses not to use the unidirectional function, then this signal should be tied low.
an_link_ok_o	Out	1	Auto-Negotiation Link Status OK—Active high signal that indicates that the link is ok. The signal is driven by the auto-negotiation state machine. When auto-negotiation is enabled, the signal asserts when the state machine is in the LINK_OK state. If auto-negotiation is disabled, the signal asserts when the state machine is in the AN_DISABLE_LINK_OK state (see IEEE 802.3 figure 37-6). This signal is intended to be used to produce the Link Status signal as required by IEEE 802.3, Status Register 1, Bit D2 (see IEEE 802.3 paragraph 22.2.4.2.13).
Serial Interface			
ser_tx_o	Out	1	Serial Transmit Data—DDR data. Assumes an LVDS buffer.
ser_rx_i	In	1	Serial Receive Data—DDR data. Assumes an LVDS buffer.
MDIO			
mdio_io	In/ Out	1	Management Data Input/Output—Bi-directional signal used to read/write management registers. Note that this signal is only present when the IP core Register Access is in *MDIO* option.
port_id_i	In	5	Port Identification Address—Used to define the binary address of this management node. The value used here corresponds to the PHY-ADD portion of the management frame format (specified in IEEE 802.3, clause 22). Note that this signal is only present when the IP core Register Access is in *MDIO* option.
LMMI			
lmmi_resetn_i	In	1	LMMI active low reset.
lmmi_request_i	In	1	Starts transaction.
lmmi_wr_rdn_i	In	1	Write = 1’b1, Read = 1’b0.

Port Name	I/O	Width	Description
lmmi_offset_i	In	6	Register offset, starting at offset 0.
lmmi_wdata_i	In	16	Output data bus.
lmmi_rdata_o	Out	16	Input data bus.
lmmi_rdata_valid_o	Out	1	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	Out	1	IP is ready to receive a new transaction. This is always asserted (tied to 1'b1).
Miscellaneous			
sgmii_mode_i	In	1	SGMII Mode—Controls the behavior of the auto-negotiation process when the core is operating in SGMII mode. 0 = operates as MAC-side entity, 1 = operates as PHY-side entity.
gbe_mode_i	In	1	Gigabit Ethernet Mode—Controls the PCS function of the core. 0 = operates as SGMII PCS, 1 = operates as Gigabit Ethernet PCS (1000BASE-X)
operational_rate_i	In	2	Operational Rate—When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 = 1 Gbps Rate 01 = 100 Mbps Rate 00 = 10 Mbps Rate Note: In Gigabit Ethernet PCS mode, the rate adaptation blocks always operate at the 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	In	1	Debug Link Timer Mode—Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes (for example, allowing simulations to run through the auto-negotiation process much faster than normal). This signal must not change during auto-negotiation.
pll_lock_i	In	1	PLL Lock—External PLL lock signal. Note that this signal is only available if *Use External PLL* is enabled in GUI.

Notes:

1. Connect tx_clock_enable_sink_i to tx_clock_enable_source_o. Relationships between TX-side signals are shown in Figure 2.3.
2. Connect rx_clock_enable_sink_i to rx_clock_enable_source_o. Relationships between RX-side signals are shown in Figure 2.4.
3. To control the AN process through these ports, you must set the Configuration Source Control Register (config_source) to 0. For more information, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.

2.3. Attribute Summary

The configurable attributes of the SGMII IP core are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog Module/IP wizard of the Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
(G)MII Interface	Classic, TSMAC	Classic	—
CTC Mode	Static, Dynamic, None	Dynamic	—
Static Low FIFO Threshold	1–1016	16	Editable when CTC Mode == Static
Static High FIFO Threshold	4–1020	32	Editable when CTC Mode == Static
Optional Ports			
Use External PLL (remove internal PLL instance)	Checked, Unchecked	Unchecked	This option is not available for Avant devices.
Enable Port: CDR Reference clock (input)	Checked, Unchecked	Unchecked	This option is not available for Avant devices.
SGMII Core Register Access	LMMI, MDIO	MDIO	—

Table 2.3. Attributes Descriptions

Attribute	Description
General	
(G)MII Interface	This attribute affects the behavior and implementation of the (G)MII port. In *Classic* mode, the (G)MII data port is 8 bits wide. All 8 bits are used for 1 Gbps operation. Only the lower 4 bits are used for 100 Mbps and 10 Mbps operation. A separate MII clock is used to synchronize the (G)MII data. The MII clock frequency varies with the (G)MII data rate: 125 MHz for 1 Gbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps. For the *TSMAC Easy Connect* mode, the (G)MII data port is 8 bits wide; and all 8 bits are used, regardless of the (G)MII data rate. A single 125 MHz clock is used to synchronize (G)MII data; and a clock enable is used to regulate the (G)MII data rate.
CTC Mode	This attribute controls the behavior of the CTC block. In dynamic mode, the CTC FIFO thresholds are automatically changed, based upon the current operational rate of the rate adaptation blocks. Optimal thresholds are internally chosen for the three data rates (1 Gbps, 10 Mbps, 100 Mbps). In static mode, the user manually chooses the CTC FIFO thresholds, and these thresholds remain fixed. This mode is used when the IP is expected to operate at only data rate (either 1 Gbps, or 10 Mbps, or 100 Mbps). In *None* mode, the CTC function is replaced by a shallow FIFO that facilitates clock domain crossing between the recovered SERDES clock and the local IP core receive-side 125 MHz clock.
Static Low FIFO Threshold	When Static CTC mode is chosen, this attribute specifies FIFO low (almost empty) threshold.
Static High FIFO Threshold	When Static CTC mode is chosen, this attribute specifies FIFO high (almost full) threshold. This attribute must be higher than the Static Low FIFO Threshold.
Optional Ports	
Use External PLL (remove internal PLL instance)	By default, there is a PLL instance inside the IP that provides clock to the CDR and GDDR block. This option allows you to remove the internal PLL instance in the IP. This option is useful if you intend to use some ports of the PLL that are not possible if it is inside the IP. User applications with multiple SGMII instance may prefer to have a common PLL instead of per IP instance. For some devices like LFMXO5, the reference clock of CDR blocks is tied to a common PLL so this option is needed when implementing with multiple SGMII instance.
Enable Port: CDR Reference clock (input)	This is related to the *Use External PLL* option above. When enabled, the internal CDR reference clock input is provided as an IP port. For LFMXO5 devices, this option should always be enabled regardless of the *Use External PLL* setting. CDR and DDR cannot share PLL clocks so you are expected to instantiate a separate PLL in the design. Note that CDR reference clock can only come from CLKOP of the PLL.
SGMII Core Register Access	This attribute controls register access in the SGMII core. In MDIO mode, SGMII core registers (Control, Status, Advertised Ability, Link Partner, Auto Negotiation Expansion, Extended Status, Configuration Source Control) are accessible to MDIO, but PCS registers, Interrupt registers and CDR registers are only accessible through the LMMI. In LMMI mode, all registers are accessible through the LMMI.

2.4. Register Description

This section provides detailed descriptions of SGMII data registers. Note that registers that are not available are highlighted in gray.

The register address map shown in Table 2.4 specifies the available IP core registers.

Table 2.4. Register Address Map

Offset	Register Name	Description
0x000	Control Register	These are five management registers specified in IEEE 802.3, Clause 37 – Control, Status, Auto Negotiation Advertisement, Link Partner Ability, Auto Negotiation Expansion, and Extended Status. The register set is accessible through the LMMI or MDIO interface.
0x001	Status Register	
0x004	Advertised Ability	
0x005	Link Partner Ability	
0x006	Auto Negotiation Expansion Register	
0x00F	Extended Status Register	

Offset	Register Name	Description
0x00E	Configuration Source Control Register	Switches between SGMII Core management ports and internal configuration registers. This register is accessible through the LMMI or MDIO interface.
0x010 – 0x01C	Reserved	Do not use.
0x020	PCS Control Register 0	PCS Debugging Control Register 0. This register is only accessible through the LMMI interface.
0x021	PCS Control Register 1	PCS Debugging Control Register 1. This register is only accessible through the LMMI interface.
0x029	PCS Status Register 9	RX, TX, and CTC FIFO Status. This register is only accessible through the LMMI interface.
0x02A	PCS Control Register 10	PCS Debugging Control Register 10. This register is only accessible through the LMMI interface.
0x02B	PCS Control Register 11	PCS Debugging Control Register 11. This register is only accessible through the LMMI interface.

The behavior of registers to write and read access is defined by its access type, which is listed in Table 2.5.

Table 2.5. Access Type Definition

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value	Ignores write access
RW	Returns register value	Updates register value
RSVD	Returns 0	Ignores write access

2.4.1. [0x000] Auto-Negotiation Control Register

Table 2.6. Control Register

Bit Field	Name	Access	Width	Description	Default
15	Reset	RW	1	1 – Reset (self-clearing) 0 – Normal operation This register is equivalent to mr_main_reset_i.	1'b0
14	Loopback	RW	1	1 – Loopback 0 – Normal operation This register is equivalent to force_loopback_i.	1'b0
13	Speed Selection[0]	RW	1	Combined with bit[6] to form 2-bit vector Speed Selection [1:0] = 11 = reserved Speed Selection [1:0] = 10 = 1 Gbps Speed Selection [1:0] = 01 = 100 Mbps Speed Selection [1:0] = 00 = 10 Mbps In GbE Mode, Speed Selection [1:0] is stuck at *10* = 1 Gbps. In SGMII Mode, the Speed Selection [1:0] bits can be written to any value.	1'b0
12	Auto Neg Enable	RW	1	1 – Enable 0 – Disable	1'b1
11	Power Down	RW	1	1 – Enable 0 – Disable This feature is not supported.	1'b0
10	Isolate	RW	1	1 – Isolate 0 – Normal operation This register is equivalent to force_isolate_i.	1'b0
9	Restart Auto Neg	RW	1	1 – Restart auto-negotiation 0 – Normal operation This register is equivalent to mr_an_restart_i.	1'b0

Bit Field	Name	Access	Width	Description	Default
8	Duplex Mode	RW	1	1 – Full Duplex 0 – Half Duplex Note that the setting of this bit has no effect on the operation of the PCS channel. The PCS channel is always a 4-wire interface with separate TX and RX datapaths.	1'b1
7	Collision Test	RW	1	1 – Enable test 0 – Normal operation This register is dependent on bit[14] or force_loopback_i. Setting this bit only takes effect when bit[14] or force_loopback_i is asserted.	1'b0
6	Speed Selection[1]	RW	1	Combined with bit [13] to form the 2-bit vector Speed Selection [1:0]	1'b1
5	Unidirectional	RW	1	1 – Loopback 0 – Normal operation This register is equivalent to force_unidir_i.	1'b0
4:0	—	RSVD	5	—	5'h00

2.4.2. [0x001] Auto-Negotiation Status Register

Table 2.7. Status Register

Bit Field	Name	Access	Width	Description	Default
15	100BASE-T4	RO	1	0 – Not supported	1'b0
14	100BASE-X Full Duplex	RO	1	0 – Not supported	1'b0
13	100BASE-X Half Duplex	RO	1	0 – Not supported	1'b0
12	10 Mbps Full Duplex	RO	1	0 – Not supported	1'b0
11	10 Mbps Half Duplex	RO	1	0 – Not supported	1'b0
10	100BASE-T2 Full Duplex	RO	1	0 – Not supported	1'b0
9	100BASE-T2 Half Duplex	RO	1	0 – Not supported	1'b0
8	Extended Status	RO	1	1 – Supported	1'b1
7	Unidirectional Capability	RO	1	1 – Supported 0 – Not supported	1'b0
6	MF Preamble Suppress	RO	1	0 – Not supported	1'b0
5	Auto Neg Complete	RO	1	1 – Complete 0 – Not complete	1'b0
4	Remote Fault	RO	1	0 – Not supported	1'b0
3	Auto Neg Ability	RO	1	1 – Supported	1'b1
2	Link Status	RO	1	1 – Link Up 0 – Link Down (Latch-on-zero, Clear-on-read)	1'b0
1	Jabber Detect	RO	1	0 – Not supported	1'b0
0	Extended Capability	RO	1	0 – Not supported	1'b0

2.4.3. [0x004] Auto-Negotiation Advertised Ability Register

Table 2.8. For PCS=GbE

Bit Field	Name	Access	Width	Description	Default
15	Next Page	RW	1	The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero to communicate that there is no more Next Page information to be sent (see Clause 37.2.4.3 of IEEE 802.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero. This feature is not supported. This bit should always be 0.	1'b0
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.	1'b1
13:12	Remote Fault	RW	2	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. 0 – No error, link OK (default) 1 – Offline 2 – Link Failure 3 – Auto-Negotiation Error	2'b00
11:9	—	RSVD	3	—	3'b000
8:7	Pause	RW	2	Pause provides a pause capability exchange mechanism. 0 – No PAUSE 1 – Asymmetric PAUSE toward link partner 2 – Symmetric PAUSE 3 – Both Symmetric PAUSE and Asymmetric PAUSE toward local device	2'b00
6	Half Duplex	RW	1	Half Duplex Capability	1'b0
5	Full Duplex	RW	1	Full Duplex Capability	1'b0
4:0	—	RSVD	5	—	5'b00000

Table 2.9. For PCS=SGMII-PHY-Side

Bit Field	Name	Access	Width	Description	Default
15	Link Status	RW	1	1 – Link Up 0 – Link Down	1'b0
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.	1'b1
13	—	RSVD	1	—	1'b0
12	Duplex Mode	RW	1	1 – Full Duplex 0 – Half Duplex	1'b0
11:10	Speed	RW	2	11 – Reserved 10 – 1 Gbps 01 – 100 Mbps 00 – 10 Mbps	2'b00
9:0	—	RO	10	Value=10'h001	10'h001

Table 2.10. For PCS=SGMII-MAC-Side

Bit Field	Name	Access	Width	Description	Default
15:0	—	RO	16	Value=16'h4001	16'h4001

2.4.4. [0x005] Auto-Negotiation Link Partner Ability

Table 2.11. For PCS=GbE

Bit Field	Name	Access	Width	Description	Default
15	Next Page	RO	1	The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero to communicate that there is no more Next Page information to be sent (see Clause 37.2.4.3 of IEEE 802.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero.	1'b0
14	Acknowledge	RO	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.	1'b0
13:12	Remote Fault	RO	2	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. 0 – No error, link OK (default) 1 – Offline 2 – Link Failure 3 – Auto-Negotiation Error	2'b00
11:9	—	RSVD	3	—	3'b000
8:7	Pause	RO	2	Pause provides a pause capability exchange mechanism. 0 – No PAUSE 1 – Asymmetric PAUSE toward link partner 2 – Symmetric PAUSE 3 – Both Symmetric PAUSE and Asymmetric PAUSE toward local device	2'b00
6	Half Duplex	RO	1	Half Duplex Capability	1'b0
5	Full Duplex	RO	1	Full Duplex Capability	1'b0
4:0	—	RSVD	5	—	5'b00000

Table 2.12. For PCS=SGMII-PHY-Side

Bit Field	Name	Access	Width	Description	Default
15	Link Status	RO	1	1 – Link Up 0 – Link Down	1'b0
14	Acknowledge	RO	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.	1'b0
13	—	RSVD	1	—	1'b0
12	Duplex Mode	RO	1	1 – Full Duplex 0 – Half Duplex	1'b0
11:10	Speed	RO	2	11 – Reserved 10 – 1 Gbps 01 – 100 Mbps 00 – 10 Mbps	2'b00
9:0	—	RO	10	Value=10'h001	10'h001

2.4.5. [0x006] Auto-Negotiation Auto Negotiation Expansion Register

Table 2.13. Auto Negotiation Expansion Register

Bit Field	Name	Access	Width	Description	Default
15:3	—	RSVD	13	—	13'h0000
2	Next Page Able	RO	1	0 – Not supported	1'b0
1	Page Received	RO	1	1 – Received 0 – Not received latch on 1, clear on read	1'b0
0	—	RSVD	1	—	1'b0

2.4.6. [0x00F] Auto-Negotiation Extended Status Register

Table 2.14. Extended Status Register

Bit Field	Name	Access	Width	Description	Default
15	1000BASE-X Full Duplex	RO	1	1 – Supported	1'b1
14	1000BASE-X Half Duplex	RO	1	0 – Not supported	1'b0
13	1000BASE-T Full Duplex	RO	1	0 – Not supported	1'b0
12	1000BASE-T Half Duplex	RO	1	0 – Not supported	1'b0
11:0	—	RSVD	12	—	12'h000

2.4.7. [0x00E] Configuration Source Control Register for Auto-Negotiation

Table 2.15. Configuration Source Control Register

Bit Field	Name	Access	Width	Description	Default
15:1	—	RSVD	15	—	15'h0000
0	config_source	RW	1	Select the Configuration Source for Auto-Negotiation. 0 – From Management Ports, mr_* ports 1 – From Auto-Negotiation Programmable Registers [0x000] – [0x00F] *Note: This method of using management ports is not validated in Avant devices.	1'b0

2.4.8. [0x020] PCS Control Register 0

Table 2.16. PCS Control Register 0

Bit Field	Name	Access	Width	Description	Default
15	enable_cgalign	RW	1	1 – Enable/restart code group alignment 0 – Disable code group alignment This bit is only valid when lsm_disable = 1. **Note**: The IP core ignores any value of this bit because lsm_eca of PCS Control Register 10 is always enabled.	1'b1
14:13	—	RSVD	2	—	2'b00
12	ge_an_enable	RW	1	Auto-negotiation enable. 1 – Enables the feature 0 – Disables the feature	1'b0
11:0	—	RSVD	12	—	12'h000

2.4.9. [0x021] PCS Control Register 1

Table 2.17. PCS Control Register 1

Bit Field	Name	Access	Width	Description	Default
15	—	RSVD	1	—	1'b0
14	sb_bypass	RW	1	This bit should always be active (1). Deactivation breaks the link. For debugging purpose only.	1'b1
13	—	RSVD	1	—	1'b0
11	enc_bypass	RW	1	This bit should always be inactive (0). Activation excludes the encoder from the TX path. For debugging purpose only.	1'b0
10	—	RSVD	1	—	1'b0
9	tx_gear_bypass	RW	1	1 – Bypass PCS TX gear box 0 – Enable PCS TX gear box This bit should always be active (1). Deactivation breaks the link.	1'b1
8	fb_loopback	RW	1	Activates RX-TX loopback. Loopback activation must be done at least 500 ns before tx_en activation and removed later than at least 500 ns after tx_en drop (or core tx-rx latency delay). This makes the transition from loopback to normal mode seamless. When this bit is enabled, You must ignore data coming out from the RX MAC.	1'b0
7	lsm_disable	RW	1	1 – Disable RX link synchronizer. When RX link synchronizer is disabled, user must manually control the word alignment through enable_cgalign bit of PCS Control Register 0. 0 – Enable RX link synchronizer When this bit is set, ls_sync_status of PCS Control Register 9 is always 1'b1. This bit is only valid when lsm_eca of PCS Control Register 10 is disabled. **Note**: The IP core ignores any value of this bit because lsm_eca of PCS Control Register 10 is always enabled.	1'b0
6	signal_detect	RW	1	1 – Force to enable/restart RX link synchronization 0 – Start of link synchronization is dependent on the Link Status (bit[2] of Status Register).	1'b0
5	rx_gear_bypass	RW	1	This bit should always be active (1). Deactivation breaks the RX link.	1'b1
4	ctc_bypass	RW	1	This bit should always be active (1). Otherwise, additional CTC is added into the RX path, which is necessary when SGMII is in the Gigabit Ethernet Mode.	1'b1
3	dec_bypass	RW	1	This bit should always be inactive (0). Otherwise, it breaks the link. For debugging purposes.	1'b0
2	wa_bypass	RW	1	This bit should always be inactive (0). Otherwise, it breaks the link. For debugging purposes.	1'b0
1:0	—	RSVD	2	—	2'b00

2.4.10. [0x029] PCS Control Register 9

Table 2.18. PCS Control Register 9

Bit Field	Name	Access	Width	Description	Default
15:11	—	RSVD	6	—	7'h00
10:7	align_status	RO	4	Word alignment status – number of bits that the input has been shifted.	4'h0
6	ls_sync_status	RO	1	Link synchronization status 1 – Link synchronization achieved. 0 – Link synchronization not yet achieved.	1'b0
5	rstb_rxf	RO	1	Receiver reset pulse.	1'b0
4	rstb_txf	RO	1	Transmitter reset pulse.	1'b0
3:0	—	RSVD	4	—	4'h0

2.4.11. [0x02A] PCS Control Register 10

Table 2.19. PCS Control Register 10

Bit Field	Name	Access	Width	Description	Default
15	lsm_eca	RW	1	Enables code group alignment regardless of *lsm_disable* and *fc_mode*. This bit should always be 1 for this IP core.	1'b1
14:13	—	RSVD	2	—	2'b00
12	wa_mode	RW	1	1 – bitslip word alignment mode. 0 – barrel shift word alignment mode. This bit should always be 0 for this IP core.	1'b0
11:10	—	RSVD	2	—	2'b00
9	fc_mode	RW	1	1 – Fiber channel link synchronization. 0 – 1000BASE-X link synchronization. This bit should always be 0 for this IP core.	1'b0
8:0	—	RSVD	9	—	9'h000

2.4.12. [0x02B] PCS Control Register 11

Table 2.20. PCS Control Register 11

Bit Field	Name	Access	Width	Description	Default
15:8	—	RSVD	8	—	8'h00
7	rst_pcs	RW	1	Reset PCS module (RX+TX).	1'b0
6	rst_pcs_rx	RW	1	Reset PCS RX sub-module.	1'b0
5	rst_pcs_tx	RW	1	Reset PCS TX sub-module.	1'b0
4:0	—	RSVD	5	—	5'h00

2.5. Module Description

The following figure shows the detailed block diagram of the SGMII/Gb Ethernet PCS IP core.

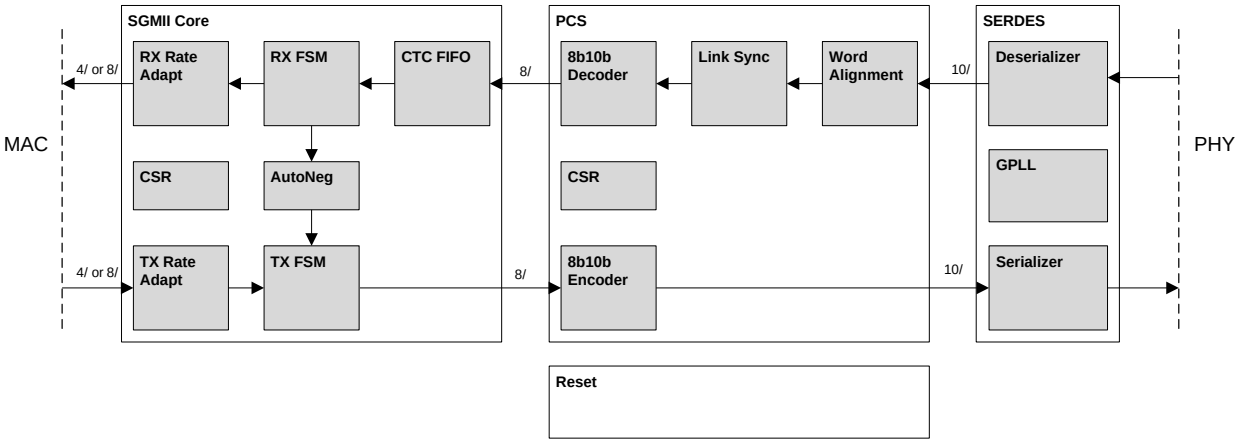

Figure 2.2. Detailed Block Diagram

2.5.1. SERDES and PCS

This block is composed of Generic DDR blocks that receives and transmits the serial data to and from the PHY. It also instantiates a Generic PLL that generates clock sources for SERDES, PCS, and SGMII core blocks.

See section 36.2 of IEEE 802.3-2018 specifications for PCS modules description.

2.5.2. Transmit SGMII Core

Transmit Rate Adaptation

This module adjusts the byte-per-byte data rate such that the output rate is always 1 Gbps. When incoming GMII data operates at 1 Gbps, there is no data rate alteration. The incoming data is 8-bits wide running at 125 MHz and the outgoing data is also 8-bits wide running at 125 MHz. When incoming GMII data operates at 100 Mbps, each incoming data byte is replicated ten times on the outgoing port. The incoming data is 4-bits wide running at 25 MHz and the outgoing data is 8-bits wide running at 125 MHz. The incoming 10 Mbps is similar except that data bytes are replicated 100 times and the incoming clock rate is 2.5 MHz.

The following figure shows the timing diagram of the signals in Transmit Rate Adaptation block. When the IP core is generated using the *TSMAC Easy Connect* option, you should use the tx_clock_enable_source_o to control the flow of incoming GMII data.

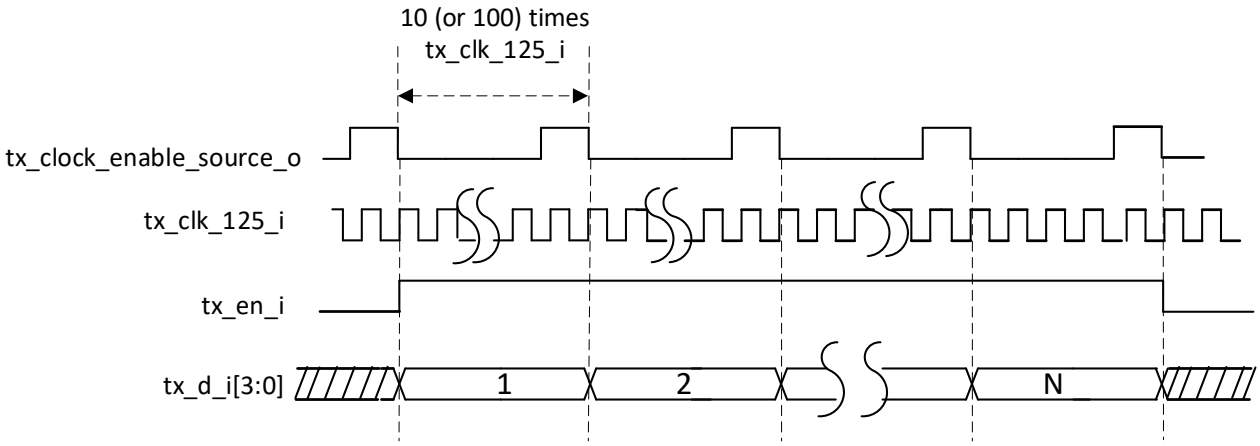

Figure 2.3. SGMII TX-Side Signals Relationship

Transmit State Machine

The transmit state machine implements transmit function described in clause 36 of the IEEE802.3 specification. The main purpose of the state machine is to convert GMII data frames into code groups. The state machine does not fully implement conversion to 10-bit code groups as specified in IEEE802.3 specification. Instead, partial conversion to 8-bit code groups is performed. A separate encoder in the PCS layer completes the full conversion to 10-bit code groups.

2.5.3. Receive SGMII Core

Soft Receive Clock Tolerance Compensation (CTC) Circuit

This block allows the receive path to compensate for slight frequency offsets between two clocks with a nominal frequency of 125 MHz. One timing source is the recovered clock from the SERDES RX physical link. The other timing source is the locally generated RX clock. If the two clock frequencies are within acceptable limits, the compensation circuit can maintain datapath integrity.

You can choose the desired CTC mode when the IP core is generated through the CTC Mode attribute.

Receive State Machine

Receive State Machine implements receive functions described in clause 36 of the IEEE802.3 specification. The main purpose of the state machine is to convert code groups into GMII data frames. The state machine in this IP does not fully implement conversion from 10-bit code groups as specified in the IEEE802.3 specification. Instead, partial conversion from 8-bit code groups is performed. A separate decoder in the PCS performs 10-bit to 8-bit code group conversions.

Receive Rate Adaptation

The function of this block is like the Transmit Rate Adaptation block, except that it operates in reverse. The incoming data rate is always 1 Gbps. The outgoing data rate is reduced by factors of 1x, 10x, or 100x for (G)MII rates of 1 Gbps, 10 Mbps, and 100 Mbps respectively.

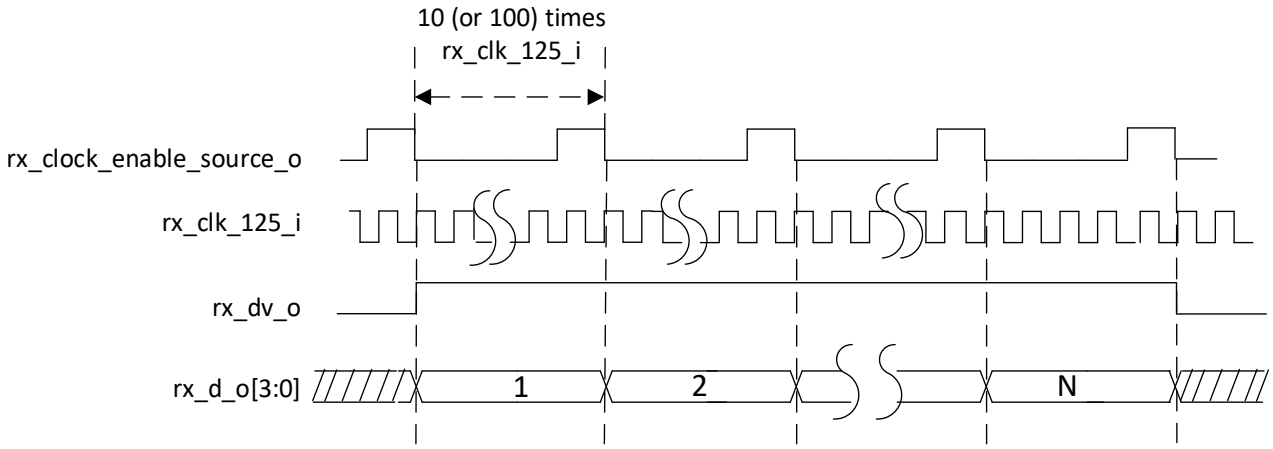

Figure 2.4. SGMII RX-Side Signals Relationship

2.5.4. Auto-Negotiation State Machine

Auto-Negotiation State Machine implements link configuration functions described in clause 37 of IEEE802.3 specification. However, Cisco SGMII specification defines several changes (summarized below). This IP operates in adherence to either specification, based on the setting of the gbe_mode_i pin (1=GBE PCS Mode Active - overrides SGMII PCS Function; 0=GBE PCS Mode Inactive - SGMII PCS Function is now active). Please refer to both specifications for detailed description of auto-negotiation operation. Main auto-negotiation functions are to test the physical link for proper operation and to circulate link configuration information between entities sitting on both sides of the link.

Here is a summary of the Cisco SGMII modifications for Auto-Negotiation:

- Decreases link timer interval from 10 msec to 1.6 msec.
- Redefines “link ability” bit assignments.
- Eliminates the need to pass link ability information from MAC to PHY.
- Adds a new condition that forces a restart on the PHY side whenever the PHY link abilities change.

For more information on Auto-Negotiation configuration, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.

2.6. Clock Network

The following figure shows the clock network of the SGMII and Gb Ethernet PCS IP core.

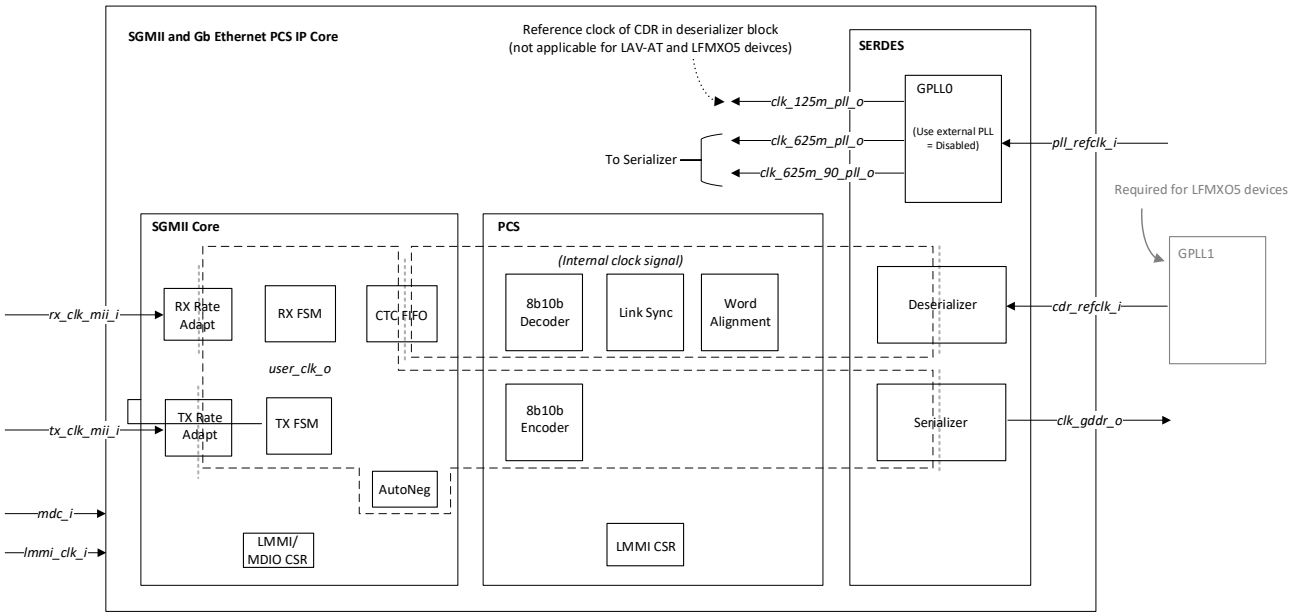

Figure 2.5. Clock Network Diagram

3. IP Generation, Simulation, and Validation

This section provides information on how to generate the SGMII IP core using the Lattice Radiant software and how to run synthesis and simulation. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

3.1. Generating the IP

The Lattice Radiant software allows you to customize and generate modules and IP cores and integrate them into the device architecture. The following section describes the procedure for generating the SGMII IP core in the Lattice Radiant software.

To generate the SGMII IP core, follow these steps:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **SGMII and Gb Ethernet PCS** under **IP, Connectivity** category. The **Module/IP Block Wizard** opens, as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

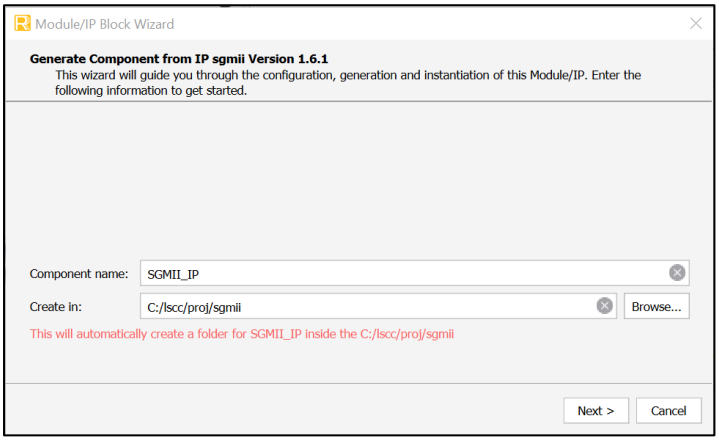

Figure 3.1. Module/IP Block Wizard

3. In the **Module/IP Block Wizard** window, customize the selected SGMII IP core. For a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

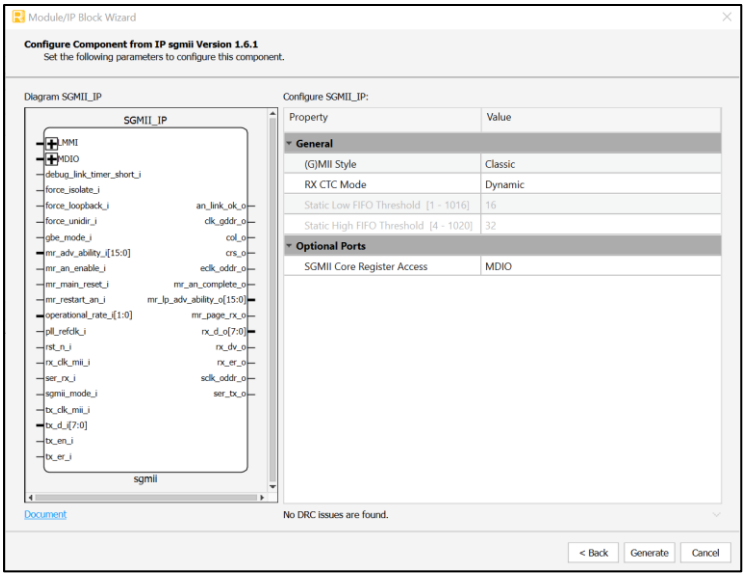

Figure 3.2. Configure User Interface of SGMII IP Core

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results, as shown in Figure 3.3.

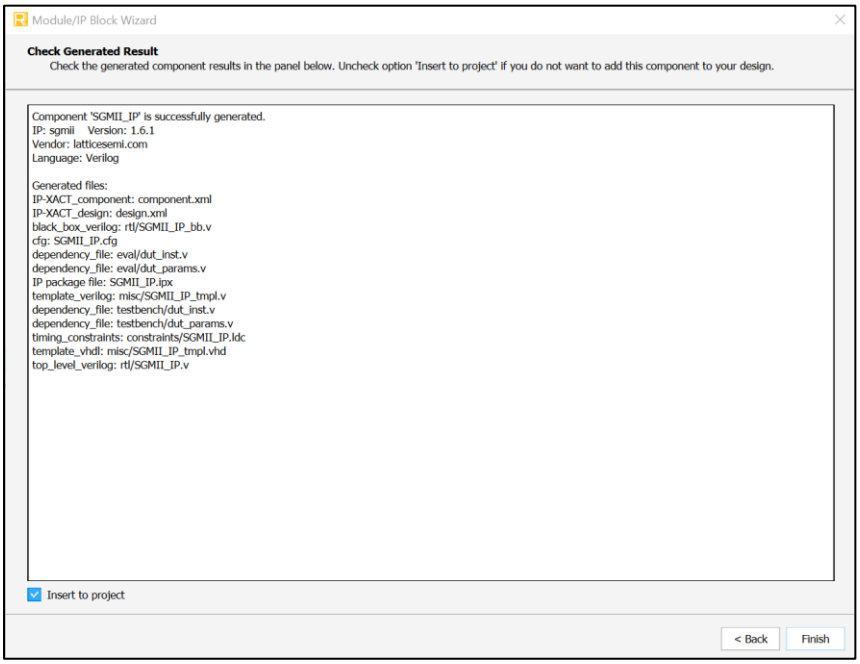

Figure 3.3. Check Generating Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated SGMII IP core package includes the black box (*<Instance Name>_bb.v*) and instance templates (*<Instance Name>_tmpl.v/vhd*) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (*<Instance Name>.v*) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an RTL example top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.
eval/eval_top.v	Top DUT file for synthesis and simulation.
eval/constraint.pdc	Post-synthesis constraint file.

3.2. Running Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run the Verilog simulation, follow these steps:

1. Add the **eval/eval_top.v** (for synthesis and simulation) and **testbench/tb_top.v** (for simulation only) as existing simulation file in the Radiant **Input Files** list to let the **Simulation Wizard** know that this is the top DUT file and top testbench file respectively.

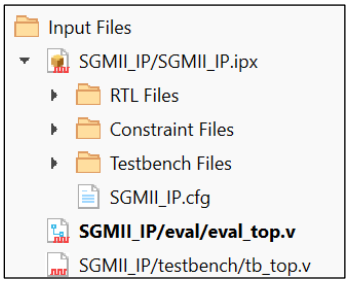

Figure 3.4. Updated Input Files List

2. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in the following figure.

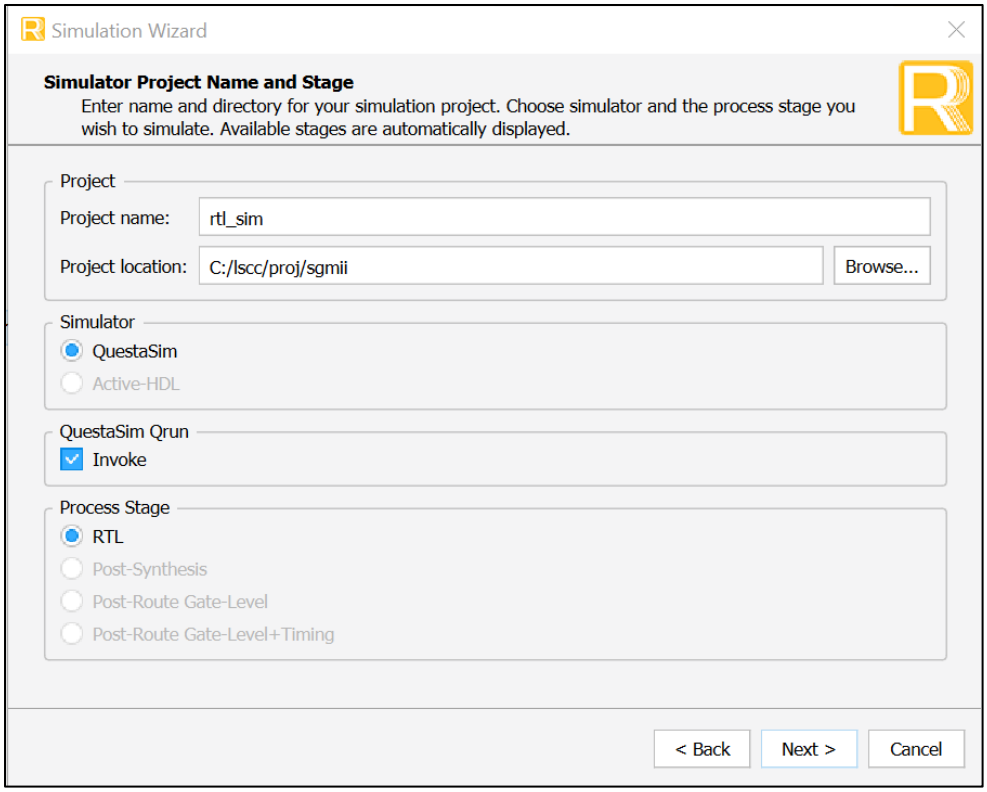

Figure 3.5. Simulation Wizard

3. Click **Next** to open the **Add and Reorder Source** window.

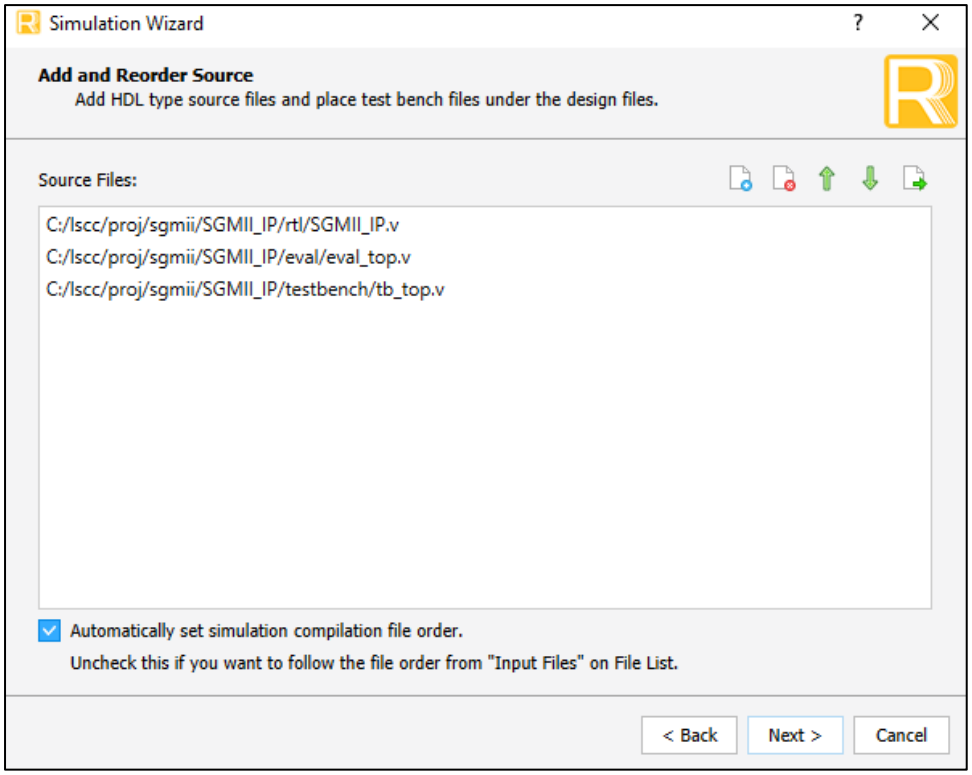

Figure 3.6. Adding and Reordering Source

4. Click **Next**. The **Parse HDL files for simulation** window is shown.

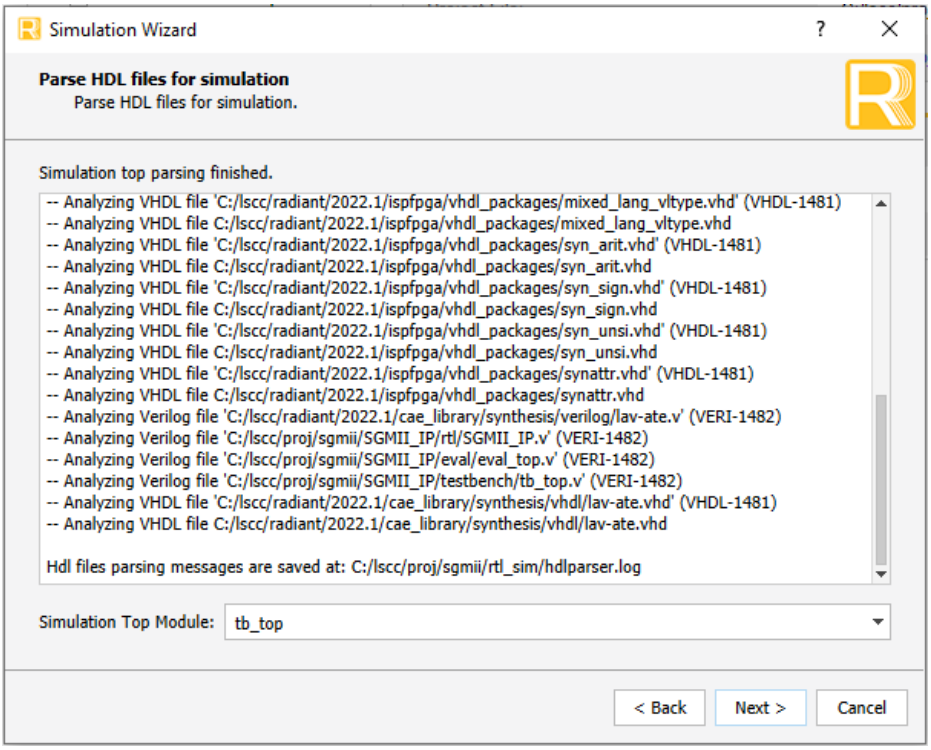

Figure 3.7. Parse HDL Files for Simulation

5. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

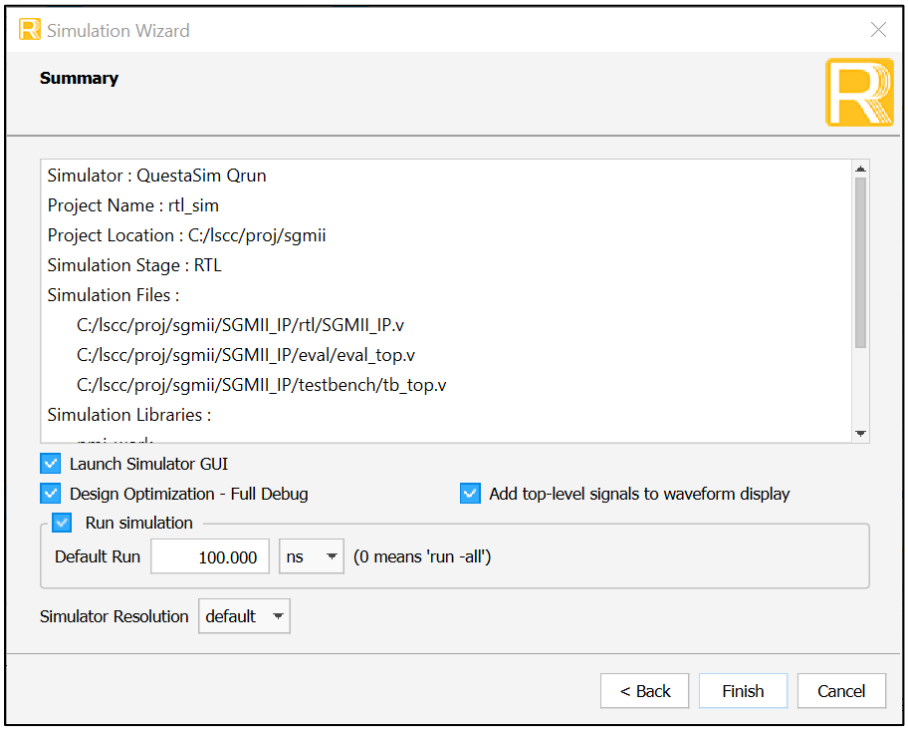

Figure 3.8. Summary

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

3.3. Constraining the IP

The *<ip_instance path>/eval/constraint.pdc* file described in Table 3.1 is generated based on the IP configuration selected by the user. The content of this file should be included to the top-level design constraint file. The timing constraints are based on the clock frequency used. The timing constraints for the IP are defined in relevant constraint files. The following example shows the IP timing constraints generated for the SGMII IP. The content of the file should be used as reference to constrain the IP only, you must modify the constraints according to system level implementation. For example, the default clock period of clk_i is 10 ns (100 MHz), if this clock is driven by 125 MHz clock in your project, the clock period of the constraint must be changed to 8 ns.

3.3.1. Constraints

To ensure proper design coverage and hardware functionality, you must include the following necessary constraints in your design for the IP project.

Table 3.2. Project Constraints

File Name	Description	Action Required
SGMII IP LDC file: ./constraint/<instance_name>.ldc	Pre-synthesis and pre-map IP constraints.	No.
SGMII IP PDC file: ./eval/constraint.pdc	Contains generated clock uncertainty constraints.	Yes – You must copy the clock uncertainty constraints listed in this file directly into your top-level PDC file.

If you select the internal clocks manually, refer to the Post-Synthesis Timing Constraints section.

For more information on how to constrain the IP, refer to the Lattice Radiant Timing Constraints Methodology Application Note (FPGA-AN-02059).

3.3.2. Post-Synthesis Timing Constraints

Internally generated clocks can only be constrained after design synthesis is done. The set_clock_group constraint for the internally generated clocks is needed. Otherwise, the place and route (PAR) timing does not close.

1. Ensure that the design synthesis is completed, as shown in the following figure.

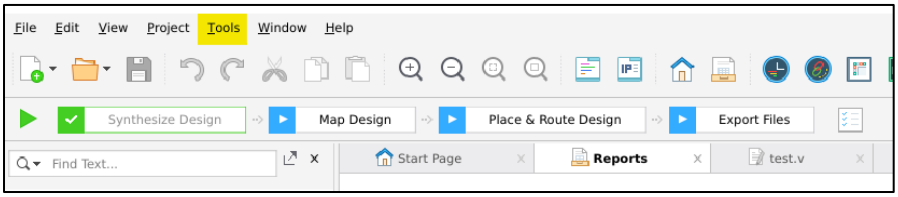

Figure 3.9. Synthesis Design

2. Go to **Tools > Post-Synthesis Timing Constraints Editor > Clock Group** to open the Object Edit window, as shown in the following figure.

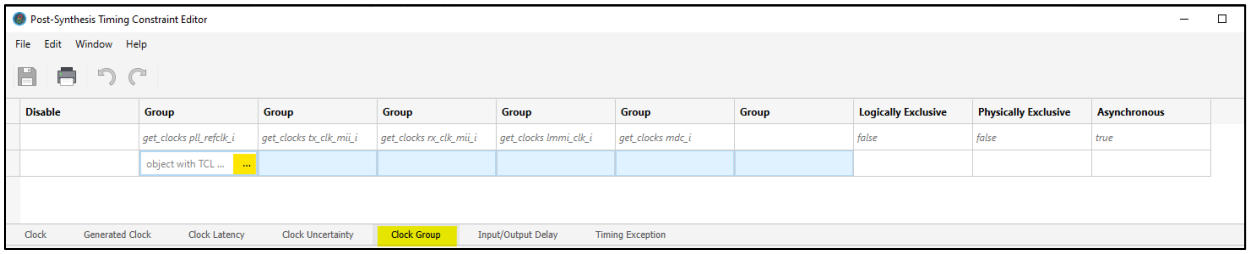

Figure 3.10. Post-Synthesis Timing Constraint Editor

3. Refer to the example in the following figure and put in all the clocks of the SGMII IP, which is under **Object Type > CLOCK** and enable the **Asynchronous** option.

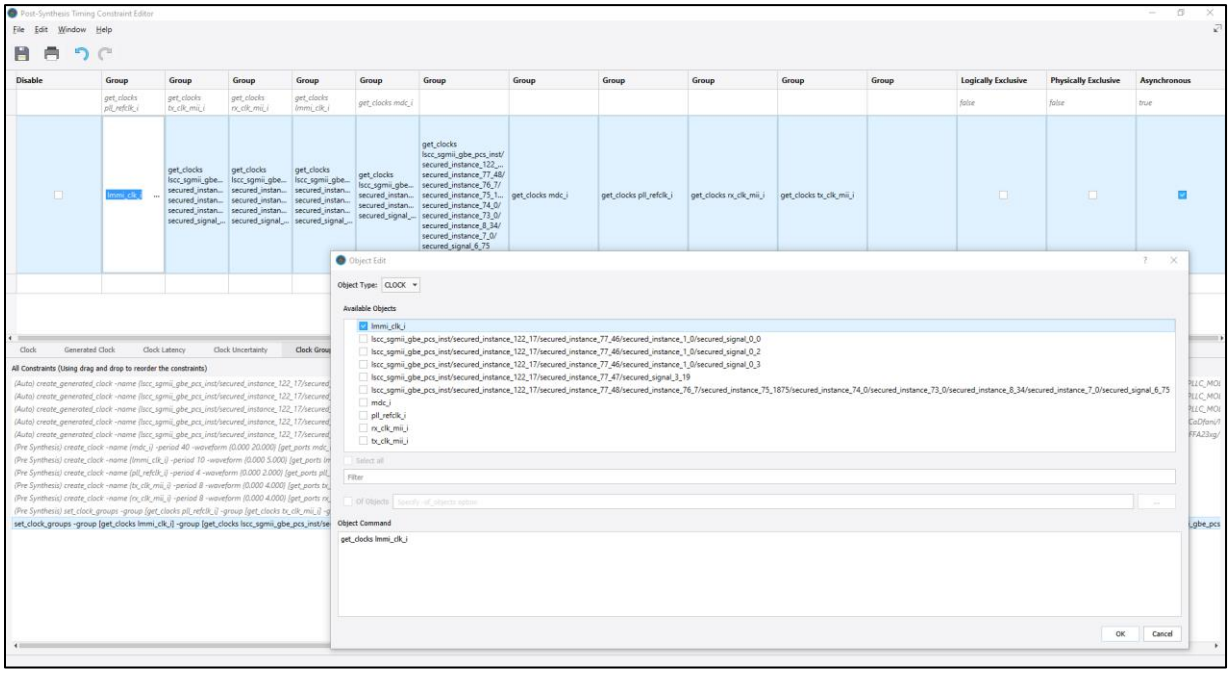

Figure 3.11. Object Edit Window

4. Save the constraints and the *.pdc* file is updated. Proceed to run the map design.

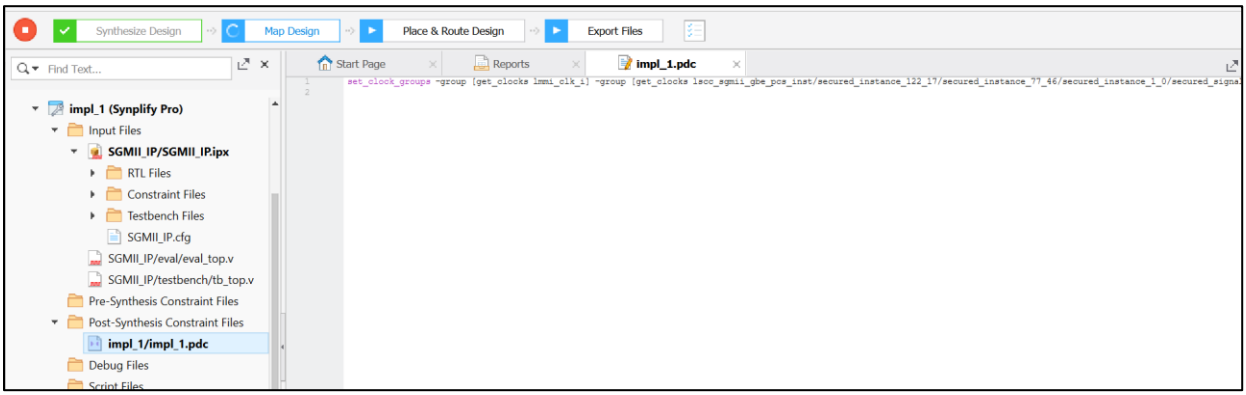

Figure 3.12. Run the Map Design

3.4. IP Evaluation

The IP core supports Lattice IP evaluation capability when used in the supported FPGA family and targeted device. This makes it possible to create versions of the IP core that operates in hardware for a limited period (approximately four hours) without requiring the purchase of an IP license. The IP evaluation capability may be enabled/disabled in the **Strategy** dialog box. It is disabled by default. To change this setting, go to **Strategies** > **Strategy1** (active strategy) > **Bitstream**.

3.5. Hardware Validation

This IP has been hardware validated for all devices.

For Avant devices, we have tested this using an in-house Lattice board with the Texas Instruments DP83867ERGZ SGMII 1000M/100M/10M Ethernet PHY Evaluation Module. For more information, refer to the DP83867ERGZ-S-EVM evaluation board web page.

3.6. Hardware Requirements (Avant Devices)

This IP has PCB requirements. The routing from the pin to the external PHY must be kept at a recommended maximum length of 4 inches using 100 ohm differential impedance with a maximum of 1 via per RX/TX signal.

The RX Eye valid window requirement is 0.6UI Eye Opening (480ps for 1.25 Gbps SGMII).

Currently, a maximum of 1 SGMII links per HPIO bank and each bank must have a PLL. Each SGMII x1 link consists of 1 LVDS TX and RX pair. For larger Avant devices, banks 3 to 11 with PLL can be used. For more information, refer to the Lattice Avant Hardware Checklist (FPGA-TN-02317).

For VCCPLL, share the DC supply with VCC and do AC isolation with an inductor.

4. Ordering Part Number

The following table lists the ordering part number (OPN) for this IP core.

Table 4.1. Ordering Part Numbers

Device Family	Part Number	
	Single Seat Annual	Multi-Site Perpetual
MachXO5-NX	GBE-SGMII-XO5-US	GBE-SGMII-XO5-UT
CrossLink-NX	GBE-SGMII-CNX-US	GBE-SGMII-CNX-UT
Certus-NX	GBE-SGMII-CTNX-US	GBE-SGMII-CTNX-UT
CertusPro-NX	GBE-SGMII-CPNX-US	GBE-SGMII-CPNX-UT
Certus-N2	GBE-SGMII-CN2-UT	GBE-SGMII-CN2-US
Avant-AT-G	GBE-SGMII-AVG-US	GBE-SGMII-AVG-UT
Avant-AT-X	GBE-SGMII-AVX-US	GBE-SGMII-AVX-UT
Avant-AT-E	GBE-SGMII-AVE-US	GBE-SGMII-AVE-UT

Appendix A. Resource Utilization

The following table lists the resource utilization for the LAV-AT-E70-1LFG676I device using the Lattice Radiant software.

Table A.1. Resource Utilization

Configuration	Slice Registers	LUTs	EBRs
Default	2,584	4,688	1

The following table lists the resource utilization for the LFCPNX-50-7ASG256I device using the Lattice Radiant software.

Table A.2. Resource Utilization

Configuration	Slice Registers	LUTs	EBRs
Default	1,691	2,167	1

For more information on the Lattice Radiant software, refer to the Lattice Design Software web page.

References

- SGMII and Gb Ethernet PCS IP Release Notes (FPGA-RN-02035)
- Lattice Radiant Timing Constraints Methodology Application Note (FPGA-AN-02059)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Solutions Boards web page
- Lattice Solutions Demonstrations web page
- Lattice Insights web page for training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.0, IP v1.7.1, December 2024

Section	Change Summary
All	Added IP version on the cover page.
Abbreviations in This Document	Added the following abbreviations: • QFN • WLCSP

Introduction	• In Table 1.1. Summary of the SGMII and Gb Ethernet PCS IP:
	  • Added IP Changes— For a list of changes to the IP, refer to the SGMII and Gb Ethernet PCS IP Release Notes (FPGA-RN-02035).
	  • Added targeted devices—LN2-CT-20ES.
	  • Updated IP version—IP core v1.0.0 – Lattice Radiant software 2.1.
	  • Updated IP version—IP core v1.1.0 – Lattice Radiant software 2.2 and Lattice Propel Builder software 2.0.
	  • Updated IP version—IP core v1.2.0 – Lattice Radiant software 3.0 and Lattice Propel Builder software 2.0.
	  • Updated IP version—IP core v.1.4.0 – Lattice Radiant software 3.2.
	  • Updated IP version—IP core v1.5.2 – Lattice Radiant software 2023.2.
	  • Updated IP version—IP core v1.6.2 – Lattice Radiant software 2024.1.
	  • Added new IP version—IP core v1.7.1 – Lattice Radiant software 2024.2 or later.
	• Added the IP Support Summary section.

Functional Description	Updated the values for Static Low FIFO Threshold and Static High FIFO Threshold attributes in Table 2.2. Attributes Table.
IP Generation, Simulation, and Validation	• Updated step 1 and Figure 3.4. Updated Input Files List in the Running Functional Simulation section. • Added the Constraints section.
Ordering Part Number	Added part numbers for Certus-N2 device family.

References	• Added the following references:
	  • SGMII and Gb Ethernet PCS IP Release Notes
	  • Lattice Solutions IP Cores web page
	  • Lattice Solutions Reference Designs web page
	  • Lattice Solutions Boards web page
	  • Lattice Solutions Demonstrations web page
	• Removed the following references:
	  • Lattice Radiant Software User Guide
	  • Lattice Propel Builder User Guide

Appendix B. Evaluation Board Support	Removed this section.

Revision 1.9, September 2024

Section	Change Summary
Abbreviations in This Document	Replaced *acronyms* with *abbreviations* in this section.
Introduction	In Table 1.1. Summary of the SGMII and Gb Ethernet PCS IP: • Added the following note: *Note: All Nexus™ (NX) devices require speed grade 9.* • Updated the targeted devices list. • Added new IP version—IP core v1.6.x – Lattice Radiant software 2024.1 or later.

Functional Description	• Updated the description for the following clock signals in Table 2.1 SGMII IP Core Signal Description:
	  • cdr_refclk_i
	  • clk_125m_pll_i

Section	Change Summary
	• clk_625m_pll_i • clk_625m_90_pll_i • pll_refclk_i • clk_125m_pll_o • Added the following signals in Table 2.1 SGMII IP Core Signal Description: • eclk_oddr_o • sclk_oddr_o • Updated the description for the following optional ports in Table 2.1. SGMII IP Core Signal Description: • Use External PLL • Enable Port: CDR reference clock • Updated the following section titles: • [0x000] Auto-Negotiation Control Register • [0x001] Auto-Negotiation Status Register • [0x004] Auto-Negotiation Advertised Ability Register • [0x005] Auto-Negotiation Link Partner Ability • [0x006] Auto-Negotiation Auto Negotiation Expansion Register • [0x00F] Auto-Negotiation Extended Status Register • [0x00E] Configuration Source Control Register for Auto-Negotiation • [0x020] PCS Control Register 0 • [0x021] PCS Control Register 1 • [0x029] PCS Control Register 9 • [0x02A] PCS Control Register 10 • [0x02B] PCS Control Register 11 • Updated the description for the *Speed Selection[0]* register in Table 2.6. Control Register. • Updated the description for the *config_source* register in Table 2.15. Configuration Source Control Register. • Added the following reference in the Auto-Negotiation State Machine section: *For more information on Auto-Negotiation configuration, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.*
IP Generation, Simulation, and Validation	• Updated the following figures in this section: • Figure 3.1. Module/IP Block Wizard • Figure 3.2. Configure User Interface of SGMII IP Core • Figure 3.3. Check Generating Result • Updated step 1 and the following figures in the Running Functional Simulation section: • Figure 3.4. Updated Input Files List • Figure 3.5. Simulation Wizard • Figure 3.8. Summary • Updated the Constraining the IP section. • Updated the Hardware Validation section. • Added the Hardware Requirements (Avant Devices) section.
Appendix A. Resource Utilization	Updated the resource utilization information.

Revision 1.8, December 2023

Section	Change Summary
Introduction	In Table 1.1. Summary of the SGMII and Gb Ethernet PCS IP: • Updated LAV-AT-500E to LAV-AT-X70, LAV-AT-G70, and LAV-AT-E70 • Added new IP version — IP core v1.5.x – Lattice Radiant software 2023.2 or later
Functional Description	In Table 2.1 SGMII IP Core Signal Description, updated the description for the LMMI clock.
Ordering Part Number	Updated the OPNs for the SGMII and Gb Ethernet PCS IP core.

Section	Change Summary
Appendix A. Resource Utilization	Updated the resource utilization information.
Appendix B. Evaluation Board Support	Updated all LAV-AT-500E references to LAV-AT-E70.
References	Added the following resource links: • Avant-G web page • Avant-X web page • Lattice Radiant Timing Constraints Methodology Application Note (FPGA-AN-02059)

Revision 1.7, August 2023

Section	Change Summary
Abbreviations in This Document	Updated this section.
Introduction	In Table 1.1. Summary of the SGMII and Gb Ethernet PCS IP: • newly added *MachXO5-NX* to Supported FPGA Families; • newly added *LFMXO5-55T* and *LFMXO5-100T* to Targeted Devices.

Functional Description	• In Table 2.2. Attributes Table, updated the Dependency on Other Attributes of the Use External PLL (remove internal PLL instance) port to *this option is only available for non-LAV-AT devices*.
	• In Table 2.4. Register Address Map:
	  • Changed the Register Name of 0x010 – 0x01C to *Reserved*;
	  • Changed the Description of 0x010 – 0x01C to *Do not use*.
	• Added the Clock Network section.

Ordering Part Number	Updated the OPNs for the SGMII and Gb Ethernet PCS IP core.
Appendix B. Evaluation Board Support **Error! Reference source not found.**	Newly added section.
References	Added links to Certus-NX web page, CertusPro-NX web page, CrossLink-NX web page, MachXO5-NX web page, Avant-E web page, and Lattice Insights for training series and learning plans.
Technical Support Assistance	Added the link to the Lattice Answer Database.

Revision 1.6, November 2022

Section	Change Summary
Introduction	Added Lattice Avant and LAV-AT-500E in Table 1.1.
Functional Descriptions	• Updated Table 2.1. SGMII IP Core Signal Description Table 2.3. Attributes Descriptions, Table 2.4. Register Address Map, Table 2.6. Control Register, Table 2.7. Status Register, Table 2.8. For PCS=GbE, Table 2.9. For PCS=SGMII-PHY-Side, Table 2.10. For PCS=SGMII-MAC-Side, Table 2.11. For PCS=GbE, Table 2.12. For PCS=SGMII-PHY-Side, Table 2.13. Auto Negotiation Expansion Register, Table 2.14. Extended Status Register, Table 2.15. Configuration Source Control Register, PCS Control Register 0, Table 2.16. PCS Control Register 0, Table 2.17. PCS Control Register 1, Table 2.18. PCS Control Register 9, Table 2.19. PCS Control Register 10, and Table 2.20. PCS Control Register 11. • Deleted Figure 2.2. SGMII TX-Side Signals Relationship and Figure 2.3. SGMII RX-Side Signals Relationship. • Added the Module Description section.
IP Generation, Simulation, and Validation	Updated IP Generation, Simulation, and Validation section.
Ordering Part Number	Added part numbers for Avant-AT-E.

Revision 1.5, July 2022

Section	Change Summary
All	Minor adjustments in formatting across the document.

Section	Change Summary
Introduction	Added LATG1 to Supported FPGA Families and LATG1-500 to Targeted Devices in Table 1.1. Summary of the SGMII and Gb Ethernet PCS IP.
Functional Descriptions	• Updated Figure 2.1. SGMII/Gb Ethernet PCS IP Top-Level Block Diagram. • Updated Table 2.1. SGMII IP Core Signal Description to remove tx_clk_125_i, rx_clk_125_i, serdes_recovered_clk_i, and soft_plol_o ports; Added MDIO ports, Serial Interface ports, and pll_lock_i port. • Updated Table 2.2. Attributes Table to add SGMII Core Register Access attribute. • Updated Table 2.3 Attributes Descriptions to add SGMII Core Register Access attribute. • Updated Table 2.4. Register Address Map to add CDR Control/Status Registers
IP Generation and Evaluation	Updated figures.

Revision 1.4, May 2022

Section	Change Summary
Introduction	Added LFMXO5-25 to Targeted Devices in Table 1.1. SGMII IP Quick Facts.
Functional Descriptions	• Added rows cdr_refclk_i, clk_125m_pll_i, clk_625m_pll_i and clk_625m_90_pll_i to Table 2.1. SGMII IP Core Signal Description. • Added Use External PLL (remove internal PLL instance) and Enable Port: CDR Reference clock (input) to Table 2.3. Attributes Descriptions.

Revision 1.3, June 2021

Section	Change Summary
All	Revised document title to SGMII and Gb Ethernet PCS IP Core.
Introduction	Updated Table 1.1. Quick Facts. • Added CertusPro-NX product family. • Added LFD2NX-17 and LFCPNX-100 devices. • Revised Lattice Implementation. • Updated reference to the Lattice Radiant Software User Guide.
IP Generation and Evaluation	• Updated reference to the Lattice Radiant Software User Guide. • Replaced *LIFCL devices* with *Lattice FPGA devices built on the Lattice Nexus platform or Lattice Nexus devices*.
Ordering Part Number	Added part numbers.
References	Updated and added references.

Revision 1.2, June 2020

Section	Change Summary
Introduction	• Updated Table 1.1 to add Certus-NX and LFD2NX-40 as targeted device. • Updated Lattice Implementation to Lattice Radiant 2.1.
Ordering Part Number	Updated devices and part numbers.
Appendix A. Resource Utilization	Updated device to LIFCL-40-9BG400I and adjusted contents of Table A.1.
All	Updated references to the Lattice Radiant Software 2.1 User Guide.

Revision 1.1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

www.latticesemi.com