OSC Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02065-1.9

July 2023

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DC	Direct Current
FPGA	Field Programmable Gate Array
LMMI	Lattice Memory Mapped Interface
LSE	Lattice Synthesis Engine
RTL	Register Transfer Level

1. Introduction

The Oscillator (OSC) module for Lattice FPGA devices built on the Lattice Nexus™ platform is designed to produce two clock signals that drive the FPGA clock tree for user-specific applications. The trimmed low frequency oscillator and trimmed high frequency oscillator are also used by the IP sub-system of the FPGA. The low frequency oscillator always run, even at sleep mode.

1.1. Features

The key features of this module are:

- Independent output enable
- Built-in divider with static control
- Dynamic on/off glitchless enable/disable
- Low DC leakage in both Stand-by Mode and in Sleep Mode
- Low frequency oscillator output is 32 kHz +/–10%
- High frequency oscillator output is 450 MHz +/–10% and is controlled by a user-configurable frequency divider.
- Maximum oscillator frequency for user application is 225 MHz
- Active current consumption of 6 uA for LF OSC and 0.3 mA for HF OSC

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals

1.2.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

OSC Module includes two accuracy oscillators, which can be individually enabled. One oscillator generates an internal 128 kHz clock used by the IP sub-system. This clock is divided by 4 for user-specific application. The other oscillator provides a clock whose maximum frequency is 450 MHz and hardened dividers allowing optional division from 2 to 256 to scale the output frequency down. The maximum frequency for user application is 450 MHz divided by 2, which is 225 MHz.

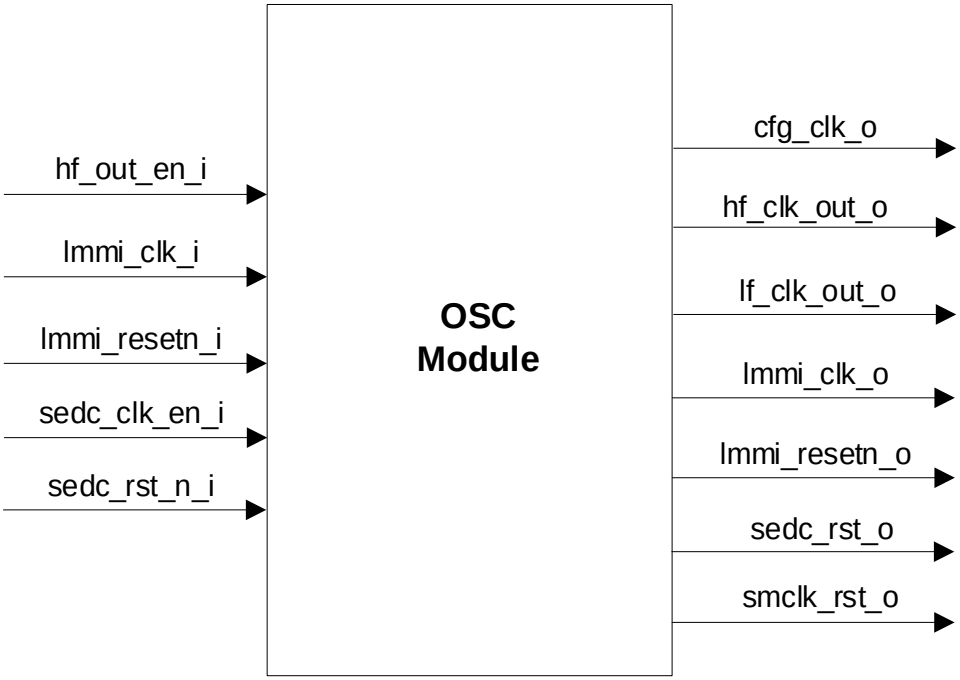

Figure 2.1. OSC Block Diagram

2.1. Signal Descriptions

Table 2.1. OSC Module Signal Description

Port Name	I/O	Width	Description
Clock ports			
hf_clk_out_o	Out	1	High frequency clock output, enabled by *HFCLK Enable* and controlled by *HFCLK Divider*.
lf_clk_out_o	Out	1	Low frequency clock output after div4:32 kHz, controlled by *LFCLK Enable*.
lmmi_clk_i	In	1	LMMI clock input, enabled by *CFGLMMICLK Enable.*
lmmi_clk_o	Out	1	LMMI clock output, enabled by *CFGLMMICLK Enable.*
cfg_clk_o	Out	1	Config clock output, enabled by *SEDCLK Enable* and not controlled by *SEDCLK Divider*. See Appendix A for more details.
Enable Ports			
hf_out_en_i	In	1	Enable port for hf_clock_out_o
hf_switch_i	In	1	Input port to control hf_clk_out_o which functions when *HFCLK Enable* == DISABLED. Available if Device is LIFCL-33U.
reboot_i	In	1	Input port to control internal clock cfg_clk_w which functions when *HFCLK Enable* == DISABLED. Available if Device is LIFCL-33U.
lmmi_resetn_i	In	1	Available if *CFGLMMICLK Enable* == ENABLED.
lmmi_resetn_o	Out	1	Available if *CFGLMMICLK Enable* == ENABLED.
sedc_clk_en_i	In	1	Available if *SEDCLK Enable* == ENABLED BY SIGNAL
Reset port			
sedc_rst_o	Out	1	Reset port for SEDC. Available if *SEDCLK Enable* == ALWAYS ENABLED or *SEDCLK Enable* == ENABLED BY SIGNAL
smclk_rst_o	Out	1	Available if CFGLMMICLK Enable == ENABLED

2.2. Attribute Summary

The configurable attributes of the OSC Module are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
HFCLK Enable	ENABLED DISABLED	ENABLED	—
HFCLK Divider	N/A	2	Uneditable.
HFCLK Frequency(MHz)	1.7578 – 225.0	225.0	Active if *HFLCK Enable* == ENABLED
LFCLK Enable	DISABLED ENABLED	ENABLED	—
LFCLK Frequency (kHz)	N/A	32	Uneditable.
SEDCLK Enable	DISABLED ALWAYS ENABLED ENABLED BY SIGNAL	DISABLED	—
SEDCLK Divider	N/A	2	Uneditable.
SEDCLK Frequency (MHz)	1.7578 – 225.0	225.0	Active if: *SEDCLK Enable* == ALWAYS ENABLED or *SEDCLK Enable* == ENABLED BY SIGNAL
CFGLMMICLK Enable	ENABLED DISABLED	DISABLED	—

Table 2.3. Attributes Descriptions

Attribute	Description
General	
HFCLK Enable	Enables the presence of hf_clk_out_o signal on the generated IP. ENABLED – Signal is available. DISABLED – Signal is unavailable.
HFCLK Divider	Displays the divider of the High Frequency Oscillator. *HFCLK Divider* == (450MHz/*HFCLK Frequency*).
HFCLK Frequency(MHz)	Specifies the HFCLK Frequency in float type, wherein, the 450 MHz oscillator is used internally by the IP sub-system. Maximum oscillator frequency for user application is 225 MHz (450 MHz divided by 2)
LFCLK Enable	Enables the presence of lf_clk_out_o signal on the generated IP. ENABLED – Signal is available. DISABLED – Signal is unavailable.
LFCLK Frequency (kHz)	Specifies the LFCLK Frequency after div4, which means that the internal LFCLK (128kHz) is divided by 4. Fixed attribute value is 32 kHz.
SEDCLK Enable	Enables the presence of sedc_clk_en_i and cfg_clk_o signal on the generated IP. ALWAYS ENABLED – sedc_clk_en_i signal is unavailable and is tied to 1'b1, cfg_clk_o signal available. ENABLED BY SIGNAL: sedc_clk_en_i and cfg_clk_o signals are available. DISABLED – sedc_clk_en_i and cfg_clk_o signals are unavailable; input signal is tied to 1'b1 and output signal is dangling.
SEDCLK Divider	Displays the frequency divider of the SEDCLK. *SEDCLK Divider* == (450MHz/ *SEDCLK Frequency*).
SEDCLK Frequency (MHz)	Specifies the SEDCLK Frequency in float type.
CFGLMMICLK Enable	Enables the presence of lmmi-related signals on the generated IP. ENABLED – Signal is available. DISABLED – Signal is unavailable.

3. IP Generation, Synthesis, and Validation

This section provides information on how to generate and synthesize this module using the Lattice Radiant software. For more on Lattice Radiant software, refer to the Lattice Radiant software user guide and relevant tutorials.

3.1. Licensing the IP

No license is required for this module.

3.2. Generating and Synthesizing the IP

The Lattice Radiant software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the OSC Module in Lattice Radiant software is described below.

To generate the OSC Module:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **OSC** under **Module, Architecture_Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

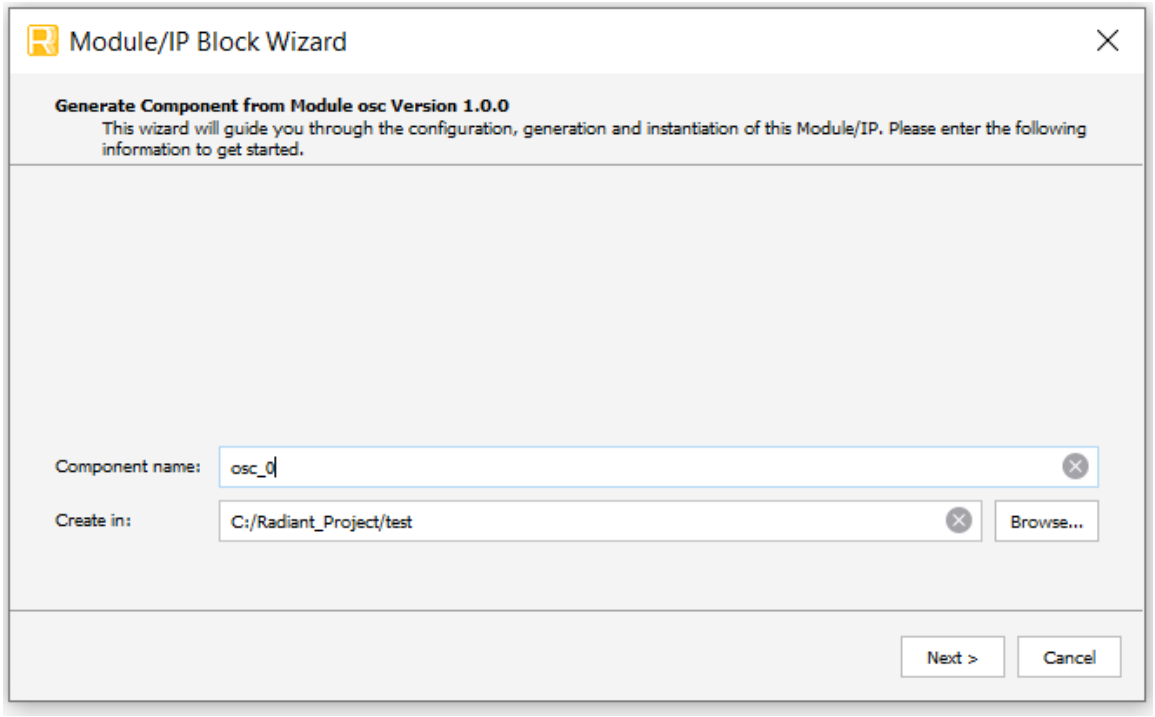

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected OSC Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

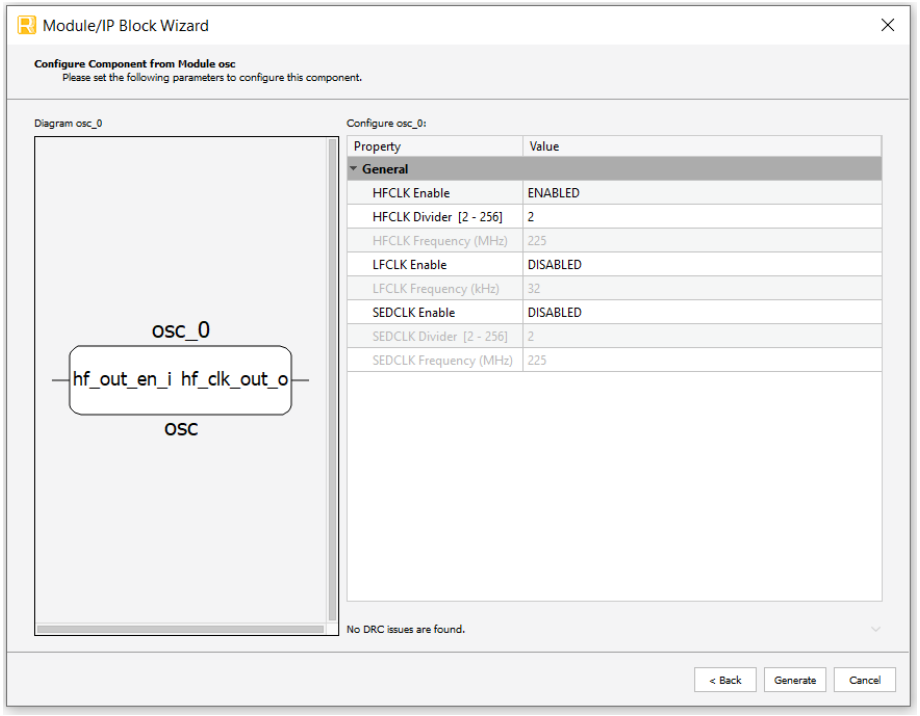

Figure 3.2. Configure User Interface of OSC Module

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

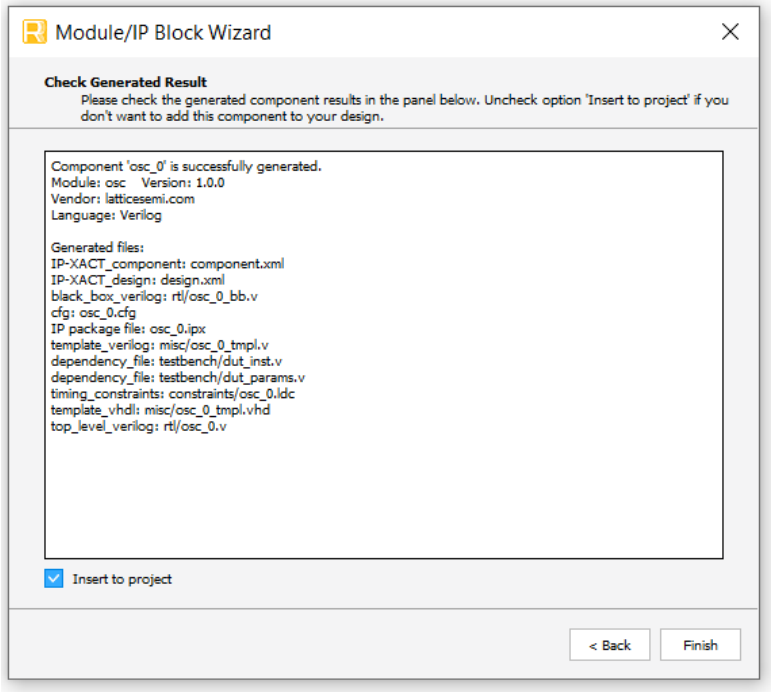

Figure 3.3. Check Generating Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields shown in Figure 3.1.

The generated OSC Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.3. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run Verilog simulation:

1. Click the  button located on the Toolbar to initiate the Simulation Wizard shown in Figure 3.4.

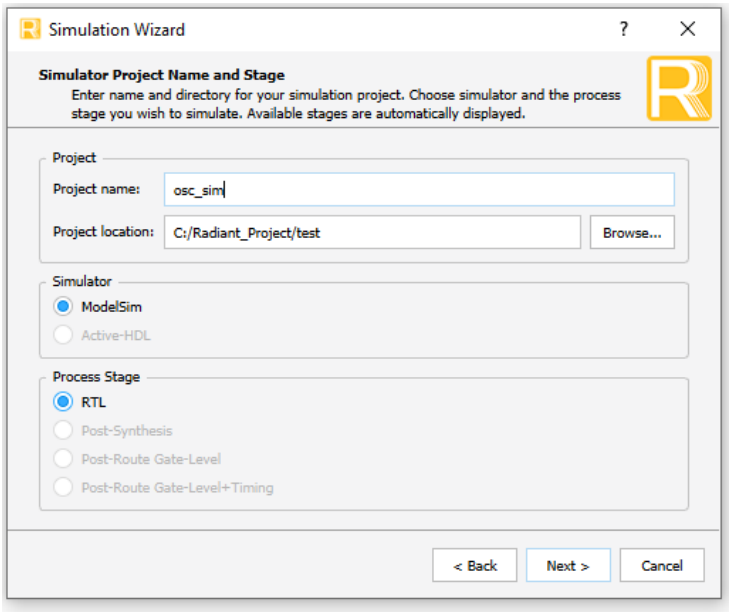

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

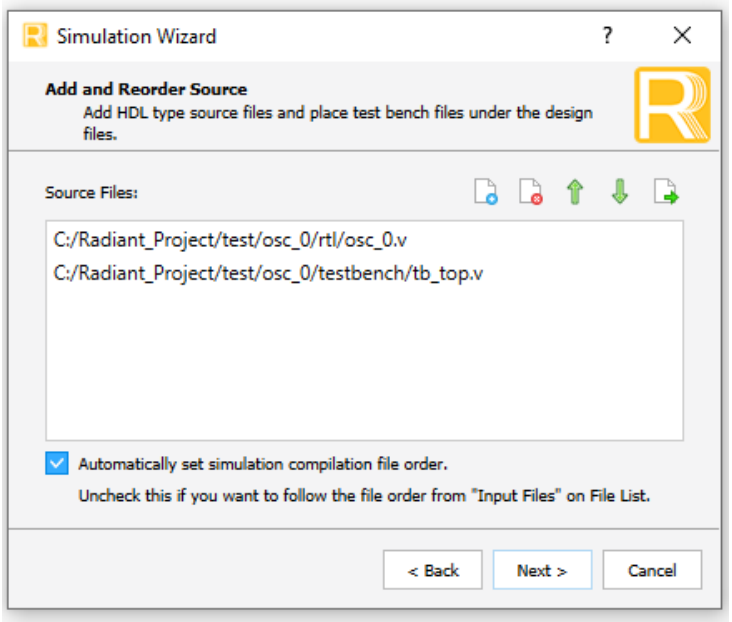

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

   Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software Suite.

   The results of the simulation in our example are provided in Figure 3.6.

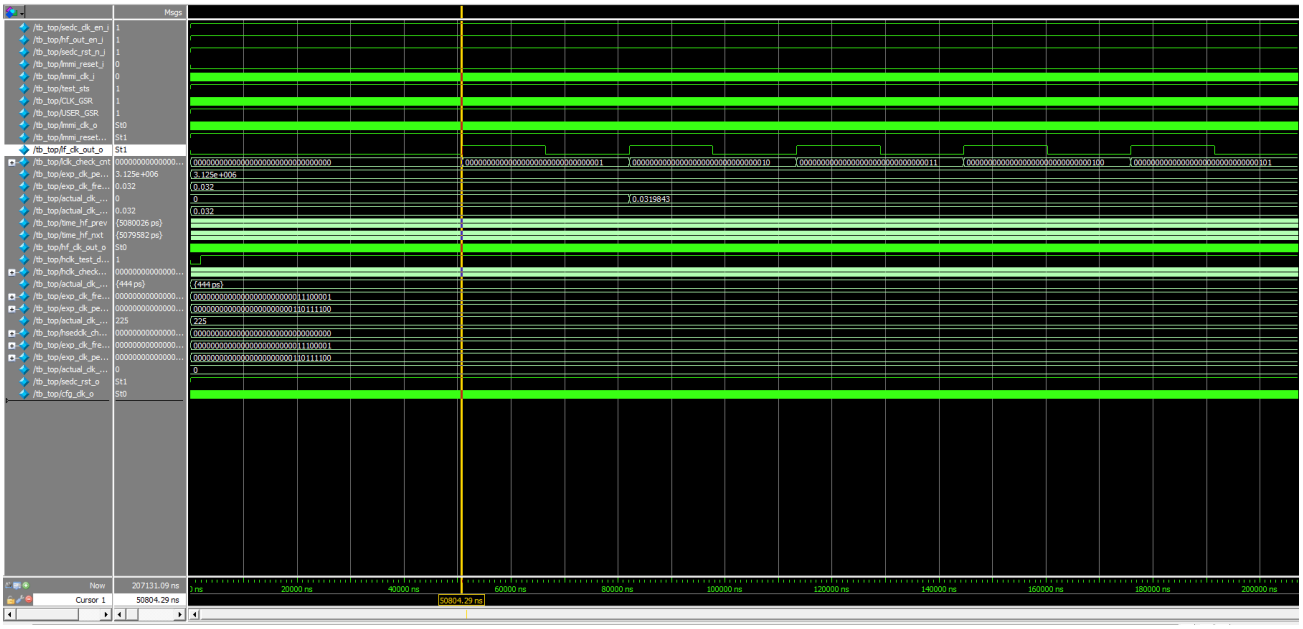

Figure 3.6. Simulation Waveform

Appendix A. Limitations

The following is a known limitation:

cfg_clk_o frequeny not changing based on *SEDCLK Divider*. Even though the SEDCLK Divider is in the OSC Module, the divider is physically located in the SEDC block. Therefore, you do not see the CFG_CLK output frequency changes according to the *SEDCLK Divider* attribute. There is no simulation model to support SEDC to run SEDC-related simulation.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

- CrossLink-NX FPGA web page
- Certus-NX FPGA web page
- CertusPro-NX FPGA web page
- MachXO5-NX FPGA web page
- Lattice Radiant Software FPGA webpage

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.9, July 2023

Section	Change Summary
Functional Description	• Replaced "lmmi_reset_i" with "lmmi_resetn_i" and added output port "smclk_rst_o" in Figure 2.1. OSC Block Diagram. • Replaced port from *lmmi_reset_i* to *lmmi_resetn_i* and added reset port *smclk_rst_o* in Table 2.1. OSC Module Signal Description. • Deleted *Available only if Family == LFMXO5* in Table 2.2. Attributes Table.
References	Added links for Crosslink™-NX, Certus™-NX, CertusPro™-NX, MachXO5™-NX devices, Lattice Radiant Software.
Technical Support Assistance	Added Lattice Frequently Asked Questions website link.

Revision 1.8, November 2022

Section	Change Summary
Functional Description	Added the ports hf_switch_i and reboot_i in Table 2.1.

Revision 1.7, November 2022

Section	Change Summary
Functional Description	Changed the default value of the attribute 'LFCLK Enable' from DISABLED to ENABLED in Table 2.2.

Revision 1.6, November 2021

Section	Change Summary
Acronyms in This Document	Added items.
Functional Description	• Added lmmi_clk_i, lmmi_clk_o, lmmi_reset_i, and lmmi_resetn_o ports to Table 2.1. OSC Module Signal Description. • Added CFGLMMICLK Enable attribute to Table 2.2. Attributes Table and Table 2.3. Attributes Descriptions.
IP Generation, Synthesis, and Validation	Updated figures in the Running the Functional Simulation section.

Revision 1.5, June 2021

Section	Change Summary
Introduction	• Updated introductory paragraph. • Removed Quick Facts section.
References	Updated this section.

Revision 1.4, December 2020

Section	Change Summary
Introduction	Added LFD2NX-17 in Table 1.1.
Functional Description	• Updated cfg_clk_o description in Signal Description. • Updated HFCLK and SEDCLK attributes in Attribute Summary.
References	Updated this section.

Revision 1.3, October 2020

Section	Change Summary
Appendix A. Limitations	Added this section.

Revision 1.2, June 2020

Section	Change Summary
Acronyms in This Document	Added this section.
Introduction	• Added Certus-NX support. • Updated Table1.1 to add LFD2NX-40 as targeted device. • Updated Lattice Implementation to Lattice Radiant 2.1.
Functional Description	• Updated Figure 2.1. • Updated SEDCLK Enable description in Table 2.2. Attributes Table.
Signal Description	Updated SEDC signal names and added output SEDC reset port.

Revision 1.1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.
Functional Description	• Updated Figure 2.1. OSC Block Diagram. • Updated Table 2.1. OSC Module Signal Description.
IP Generation, Synthesis, and Validation	Updated Figure 3.2. Configure User Interface of OSC Module.

Revision 1.0, November 2019

Section	Change Summary
All	Changed document status from Preliminary to final.
Introduction	Added *Maximum oscillator frequency for user application is 225MHz*in Features section.
IP Generation, Synthesis, and Validation	Updated Figure 3.6. Simulation Waveform.

Revision 0.80, October 2019

Section	Change Summary
All	Preliminary release.

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